*Preliminary Information*

# AMD-762™ System Controller

## Data Sheet

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# Revision History

| Date | Rev | Description |
|---|---|---|
| Dec./2001 | C | Added AMD-768 peripheral bus controller throughout as the Southbridge device for the MPX chipset. |
| June/2001 | B-1 | Package name in datasheet corrected from PBGA to CCGA. |
| June/2001 | B | Initial public release. |
| Nov./2000 | A | Initial NDA release. |

# 1 Features

**The AMD Athlon™ processor powers the next generation in computing platforms, delivering the ultimate performance for cutting-edge applications and an unprecedented computing experience.**

The AMD-760MPX™ and AMD-760MP™ chipsets are highly integrated system logic solutions that deliver enhanced performance for the AMD Athlon™ processor and other AMD Athlon processor system bus-compatible processors. The AMD-760MPX chipset consists of the AMD-762™ system controller in a 949-pin Ceramic Column Grid Array (CCGA) package and the AMD-768™ peripheral bus controller. The AMD-760MP chipset consists of the AMD-762 system controller in a CCGA package and the AMD-766™ peripheral bus controller.

The AMD-762 system controller features the AMD Athlon system bus, system memory controller, Accelerated Graphics Port (AGP) controller, and Peripheral Component Interconnect (PCI) bus controller. Figure 1 on page 5 shows a block diagram for the AMD-760MPX chipset. Figure 2 on page 6 shows a block diagram for the AMD-760MP chipset.

The AMD-762 system controller is designed with the following features:

- Two AMD Athlon processor system buses support the high-speed, split-transaction AMD Athlon system bus interface. These buses are designed to operate at 100/200-MHz or 133/266-MHz double-data rate.
- A 66/33-MHz 64/32-bit PCI 2.2-compliant bus interface supports up to seven bus masters plus the AMD-766 peripheral bus controller at 33 MHz or up to two bus masters plus the AMD-768 peripheral bus controller at 66 MHz.
- The 66-MHz AGP 2.0-compliant interface supports 1x, 2x, and 4x data transfer mode.
- High-speed memory—The AMD-762 system controller is designed to support DDR SDRAM DIMMs, operating at either 100/200-MHz or 133/266-MHz double-data rate. Note that the DDR interface speed is always locked to the front-side bus speed.

This document describes the features and operation of the AMD-762 system controller. For a description of the AMD-766 peripheral bus controller, see the *AMD-766™ Peripheral Bus Controller Data Sheet*, order# 23167. For a description of the AMD-768 peripheral bus controller, see the *AMD-768™ Peripheral Bus Controller Data Sheet*, order# 24467. Key features of the AMD-762 system controller are provided in this section.

## 1.1 AMD Athlon™ System Buses

The AMD Athlon system buses have the following features:

- High-performance point-to-point system bus topology
- Source-synchronous clocking for high-speed transfers
- 200- or 266-MHz, split-transaction AMD Athlon system bus interface
- 1.6 Gbytes/s peak data transfer rates at 100/200 MHz, 2.1 Gbytes at 133/266 MHz
- Large 64-byte (cache line) data burst transfers

## 1.2 Integrated Memory Controller

The integrated memory controller has the following features:

- The AMD-762 system controller supports the following concurrencies:
  - Processor-to-main-memory with PCI-to-main-memory
  - Processor-to-main-memory with AGP-to-main-memory
  - Processor-to-PCI with PCI-to-main-memory or AGP-to-main-memory
- Memory Error Correcting Code (ECC) support
- Supports the following DRAM:
  - Supports 64-Mbit, 128-Mbit, 256-Mbit, and 512-Mbit technology
  - 64-bit data width, plus 8-bit ECC paths
  - Flexible row and column addressing
- Supports up to 4 Gbytes of memory
- Four open pages within one CS (device selected by chip select)

- BIOS-configurable memory-timing parameters and configuration parameters
- 2.5-V memory interface operation with no external buffers or PLLs
- Concurrent DRAM writeback and read-around-write
- Burst read and write transactions
- Decoupled and burst DRAM refresh with staggered CS timing
- Provides the following refresh options:
  - Programmable refresh rate
  - CAS-before-RAS
  - Populated banks only
  - Automatic refresh of idle slots—improves bus availability for memory access by the processor or system

## 1.3 PCI Bus Controller

The PCI bus controller has the following features:

- Compliance with *PCI Local Bus Specification*, Revision 2.2.
- Supports up to seven PCI bus masters plus the AMD-766 peripheral bus controller when operating in 33-MHz-only mode, or up to two PCI bus masters and the AMD-768 peripheral bus controller when operating in 66/33-MHz PCI mode.
- 64-bit interface, compatible with 3.3-V and 5-V PCI I/O
- Synchronous PCI bus operation up to 66 MHz
- PCI-initiator peer concurrency
- Automatic processor-to-PCI burst cycle detection
- Zero wait-state PCI initiator and target burst transfers
- Enhanced PCI command optimization, such as Memory Read Line (MRL), Memory Read Multiple (MRM), and Memory-Write-and-Invalidate (MWI)

## 1.4 AGP Features

The AGP features include the following:

- Bus Features
  - Compliance with *Accelerated Graphics Port Interface Specification*, Revision 2.0
  - Synchronous 66-MHz 1x, 2x, and 4x data-transfer modes
  - Multiplexed and demultiplexed transfers
  - Up to four pipelined grants
  - Support of Sideband Address (SBA) bus
- Request Queue Features
  - Separate read-request and write-request queues
  - Reordering of high-priority requests over low-priority requests in queue
  - Simultaneous issuing of requests from both the write queue and read queue
- Graphics Address Remapping Table (GART) Features
  - Conventional (two-level) GART scheme
  - Eight-entry, fully-associative GART table cache
  - Three fully-associative GART directory caches

    One 4-entry for PCI

    One 8-entry for the processor

    One 16-entry for AGP

## 1.5 Power Management

The power management features include the following:

- Compliance support for both Advanced Configuration and Power Interface (ACPI) and Microsoft® PC 99 power management
- The AMD-762 system controller supports the following power states:
  - ACPI S1 (power on suspend) and S3 (suspend to RAM) sleep states
  - Clock throttling with the processor's STPCLK#/stop grant mechanism

Refer to Figure 1 for a block diagram of the AMD-760MPX™ chipset with an AMD-768 peripheral bus controller (66-MHz PCI). Refer to Figure 2 on page 6 for a block diagram of the AMD-760MP chipset with the AMD-766 peripheral bus controller (33-MHz PCI).

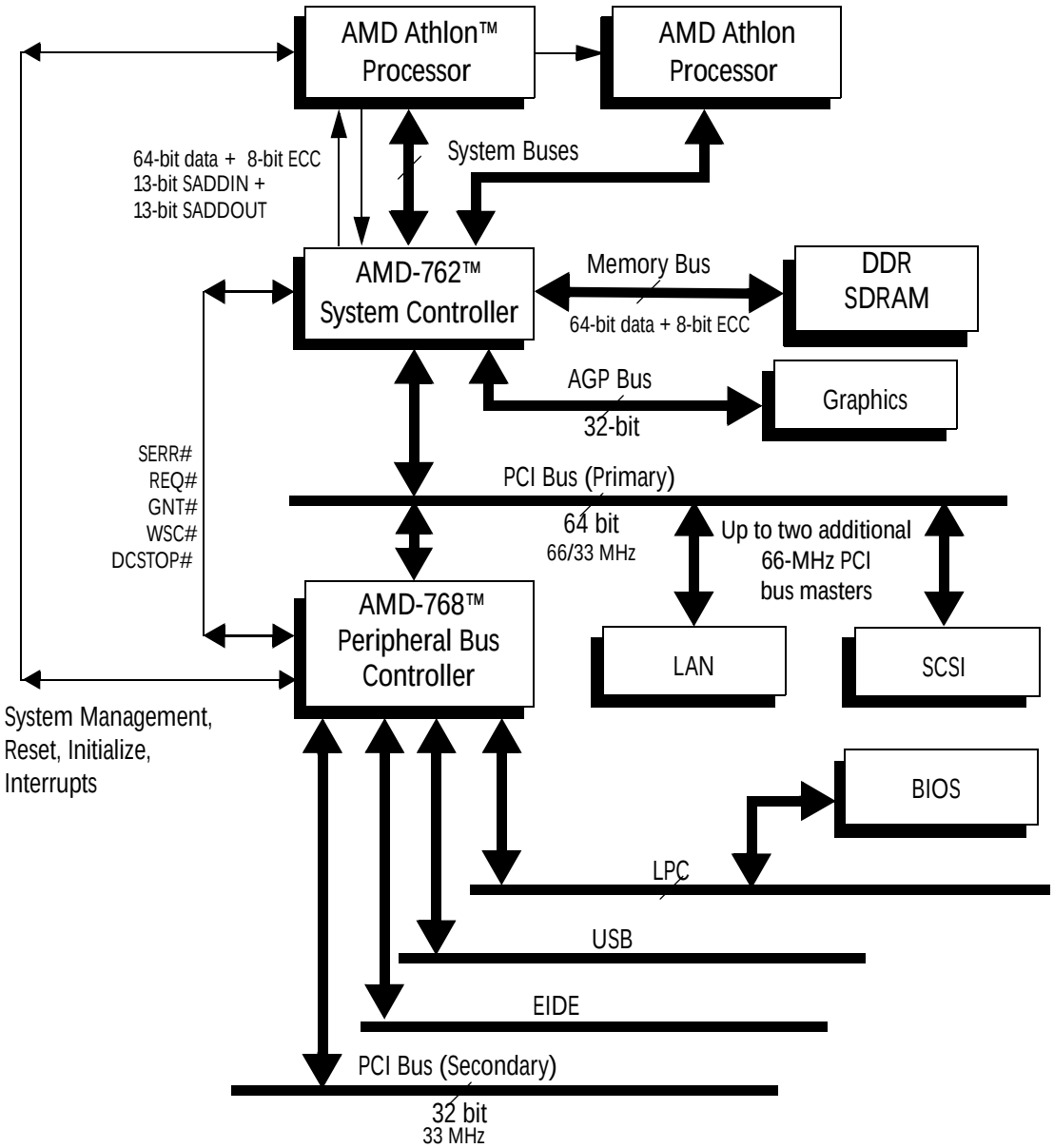



**Figure 1. AMD-760MPX™ System Block Diagram (66-MHz PCI)**

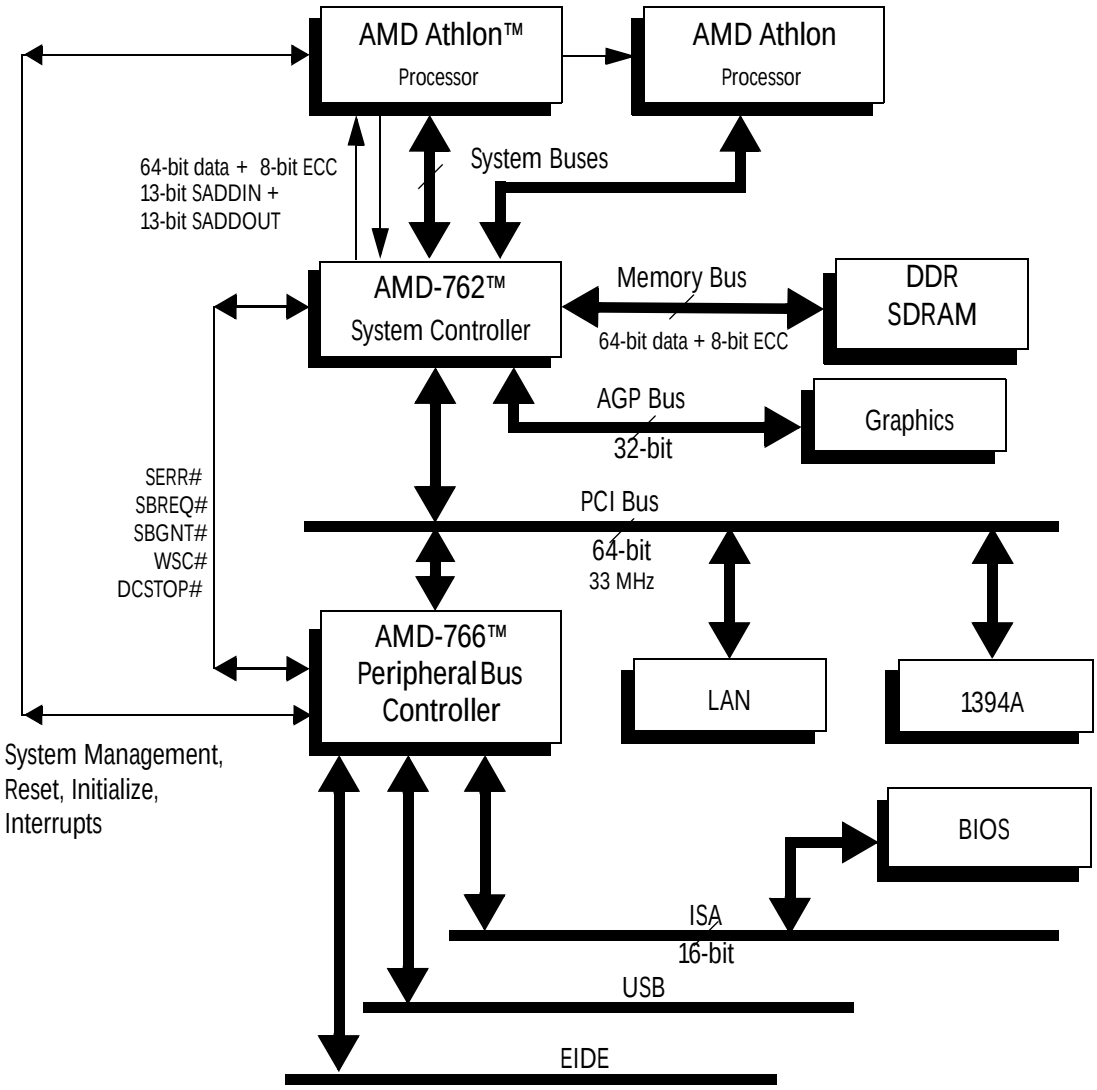



**Figure 2. AMD-760MP™ Chipset System Block Diagram (33-MHz PCI)**

# 2 Functional Operation

This section describes the functional operation of the AMD-762™ system controller.

## 2.1 Processor Interface

The two AMD Athlon processor system buses are high-performance, out-of-order, split-transaction buses, each capable of transferring one processor command and one probe response, one chip-set response and one probe request, and one data packet simultaneously. Data and command packets are transferred as packets of two, four, or eight datums on each edge of the 100-MHz or 133-MHz clock.

### 2.1.1 Out of Order, Split Transaction

The split transaction buses separate the transfer of the command and the associated data into different transactions on different buses. Data may be returned in a different order than it was requested, subject to ordering rules.

A read transaction consists of a Read command sent from the processor to the memory system over the SADDOUT bus. When the memory system is ready to return data, a ReadData command is sent to the processor over the SADDIN bus to alert the processor that data is coming and identify the associated data request. The data is sent to the processor over the SDATA bus a programmable number of clocks later. Similarly, a write transaction is sent to the chipset over the SADDOUT bus, the chipset requests the associated write data over the SADDIN bus, and the data is transferred over the SDATA bus a programmable number of clocks later. Probes and probe responses are piggybacked with the other commands on the SADDIN and SADDOUT bus.

The split transaction scheme provides a high degree of parallelism between the various buses and facilitates pipeline flow or memory requests and responses.

### 2.1.2 Point-to-Point, Source Synchronized

All of the AMD Athlon system bus signals use a terminated, point-to-point topology—that is, there is one signal connection plus termination on each end of each wire. The terminated point-to-point topology allows the use of incident wave signalling, eliminating most of the time for transmission line reflections. This feature allows high-transfer speeds while maintaining high signal integrity. All data transfer is synchronized by a clock generated at the data source. The clock and data propagate over matched length paths, minimizing skew between clock and data, and the data is sampled at the destination using this forwarded clock.

Data is sampled into a FIFO at the receiver synchronous to the forwarded clock and read out of FIFO a programmable number of processor clocks later, reducing all metastability concerns. The initialization procedure establishes the location of a common ClockN on both ends of the wire to within the system wide, clock distribution skew. A data object, transmitted from one end of the wire on ClockM, is sampled into the FIFO at the other end of the wire by ClockM forwarded with the data. It is read from the FIFO by ClockM+X that is generated in the receivers clock domain, X clocks later. X is a programmed constant that accounts for the worst case propagation delay.

A detailed description of the AMD Athlon system bus, including operations, initialization, and timing can be found in the *AMD Athlon™ System Bus Specification*, order# 21902, and the *AMD Athlon™ System Bus Design Guide*, order# 22666.

### 2.1.3 Push-Pull Compensation

The AMD-762 system controller provides push-pull driver configuration. The push-pull driver scheme implements drivers with a user-defined output impedance. This feature allows the point-to-point signals to be source terminated without any external devices, greatly simplifying layout and reducing cost. In current semiconductor technology, it is not possible to implement a transistor with a tightly controlled impedance over realistic voltage, temperature, and process parameters. For this reason, a dynamic compensation scheme is implemented. For a push-pull transmission line example, see Figure 3 on page 9.

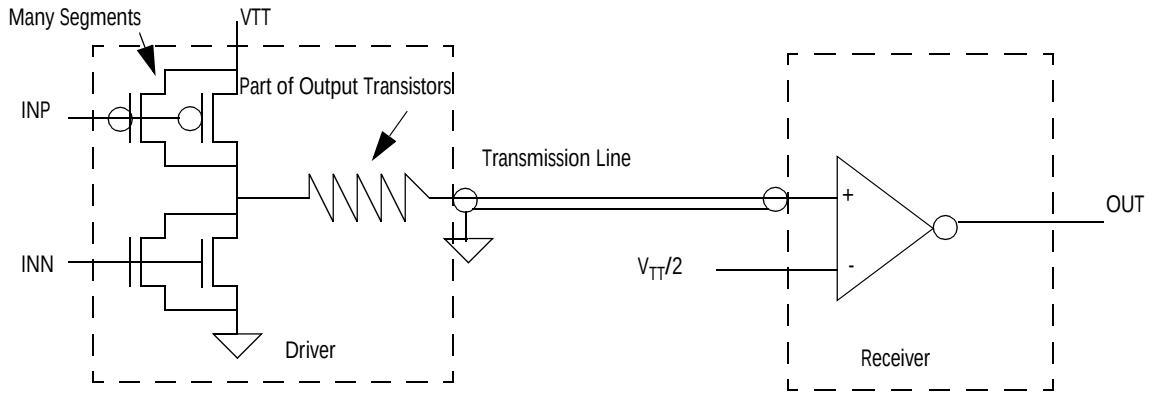



**Figure 3. Push-Pull Transmission Line Example**

The dynamic compensation scheme implements a dummy driver with characteristics exactly matching the normal driver. An external precision resistor is attached, and the voltage of the resulting voltage divider is compared to $V_{TT}/2$. The drive strength is then adjusted until a voltage near $V_{TT}/2$ is achieved. The output impedance then roughly matches the resistor value. Separate compensation is performed for the N and P transistors. The drive strength is changed in small steps when no data is being driven. Refer to Figure 4.

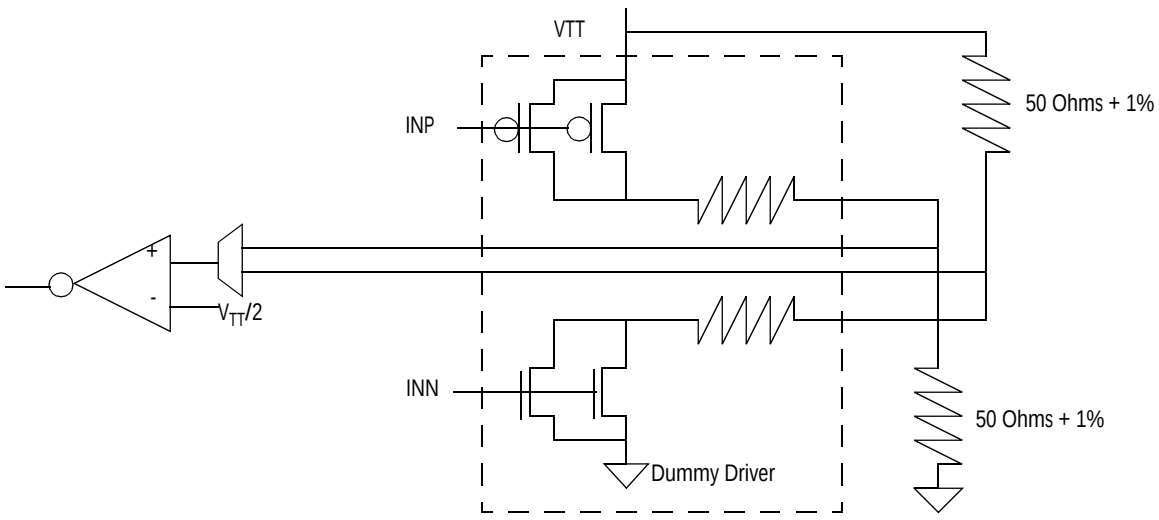



**Figure 4. Dummy Load with External Compensation Resistors**

## 2.2 Memory Interface

The AMD-762 memory controller arbitrates and optimizes incoming memory requests, handles ECC and Graphics Address Remapping Table (GART), and controls up to four double-data-rate (DDR) SDRAM DIMMs.

The AMD-762 system controller memory interface is designed to support registered DDR DIMMs. Up to four registered DIMMs can be supported by the AMD-762 system controller.

The AMD-762 system controller supports 64-Mbit, 128-Mbit, 256-Mbit, and 512-Mbit DDR devices. Device widths of x4, x8, and x16 are supported. Mixed banks are supported, meaning that a x8 DIMM can coexist with x4 and x16, etc.

Refer to Table 1 on page 11 for the total memory sizes for various registered DIMM configurations. A total of 4 Gbytes is supported.

DDR timing parameters are programmable via the AMD-762 system controller's memory controller configuration registers, allowing support of different DIMM configurations and loading. Refresh is also programmable, with support of various refresh rates as well as the ability to queue up to four outstanding refreshes. Clock pairs can also be selectively disabled to unpopulated DIMM slots via configuration register bits in the memory controller.

The memory controller supports up to four open pages in the active chip select. All pages in a chip select are closed when an access to another chip select is detected. Memory page operation can be further optimized by programming the number of idle cycles to a bank before the bank is automatically precharged.

**Table 1. Total Memory Sizes**

| Devices used on DIMM | 1 DIMM (2 Rows) x64/x72 | 2 DIMMs (2 Rows Each) x64/x72 | 3 DIMMs (2 Rows Each) x64/x72 | 4 DIMMs (2 Rows Each) x64/x72 |
|---|---|---|---|---|
| 64 Mbit (4M x 4 x 4 banks) | 256 Mbytes | 512 Mbytes | 768 Mbytes | 1 Gbytes |
| 64 Mbit (2M x 8 x 4 banks) | 128 Mbytes | 256 Mbytes | 384 Mbytes | 512 Mbytes |
| 64 MBit (1M x 16 x 4 banks) | 64 Mbytes | 128 Mbytes | 192 Mbytes | 256 Mbytes |
| 128 MBit (8M x 4 x 4 banks) | 512 Mbytes | 1 Gbytes | 1.5 Gbytes | 2 Gbytes |
| 128 MBit (4M x 8 x 4 banks) | 256 Mbytes | 512 Mbytes | 768 Mbytes | 1 Gbytes |
| 128 MBit (2M x 16 x 4 banks) | 128 Mbytes | 256 Mbytes | 384 Mbytes | 512 Mbytes |
| 256 MBit (16M x 4 x 4 banks) | 1 Gbytes | 2 Gbytes | 3 Gbytes | 4 Gbytes |
| 256 MBit (8M x 8 x 4 banks) | 512 Mbytes | 1 Gbytes | 1.5 Gbytes | 2 Gbytes |
| 256 MBit (4M x 16 x 4 banks) | 256 Mbytes | 512 Mbytes | 768 Mbytes | 1 Gbytes |
| 512 MBit (32M x 4 x 4 banks) | 2 Gbytes | 4 Gbytes | 4 Gbytes | 4 Gbytes |
| 512 MBit (16M x 8 x 4 banks) | 1 Gbytes | 2 Gbytes | 3 Gbytes | 4 Gbytes |
| 512 MBit (8M x 16 x 4 banks) | 512 Mbytes | 1 Gbytes | 1.5 Gbytes | 2 Gbytes |
| ***Note:*** *The maximum address space supported by the AMD-762 system controller is 4 Gbytes.* | | | | |

Support of four registered DIMMs is accomplished by the AMD-762 system controller's eight DDR chip-select pins (CS[7:0]#), which allow DIMMs with two chip selects as illustrated in Figure 5 on page 12. In this example, each DIMM contains two physical DRAM banks, thus two chip selects are routed to the DIMM. The AMD-762 system controller provides one differential clock pair for each registered DIMM.

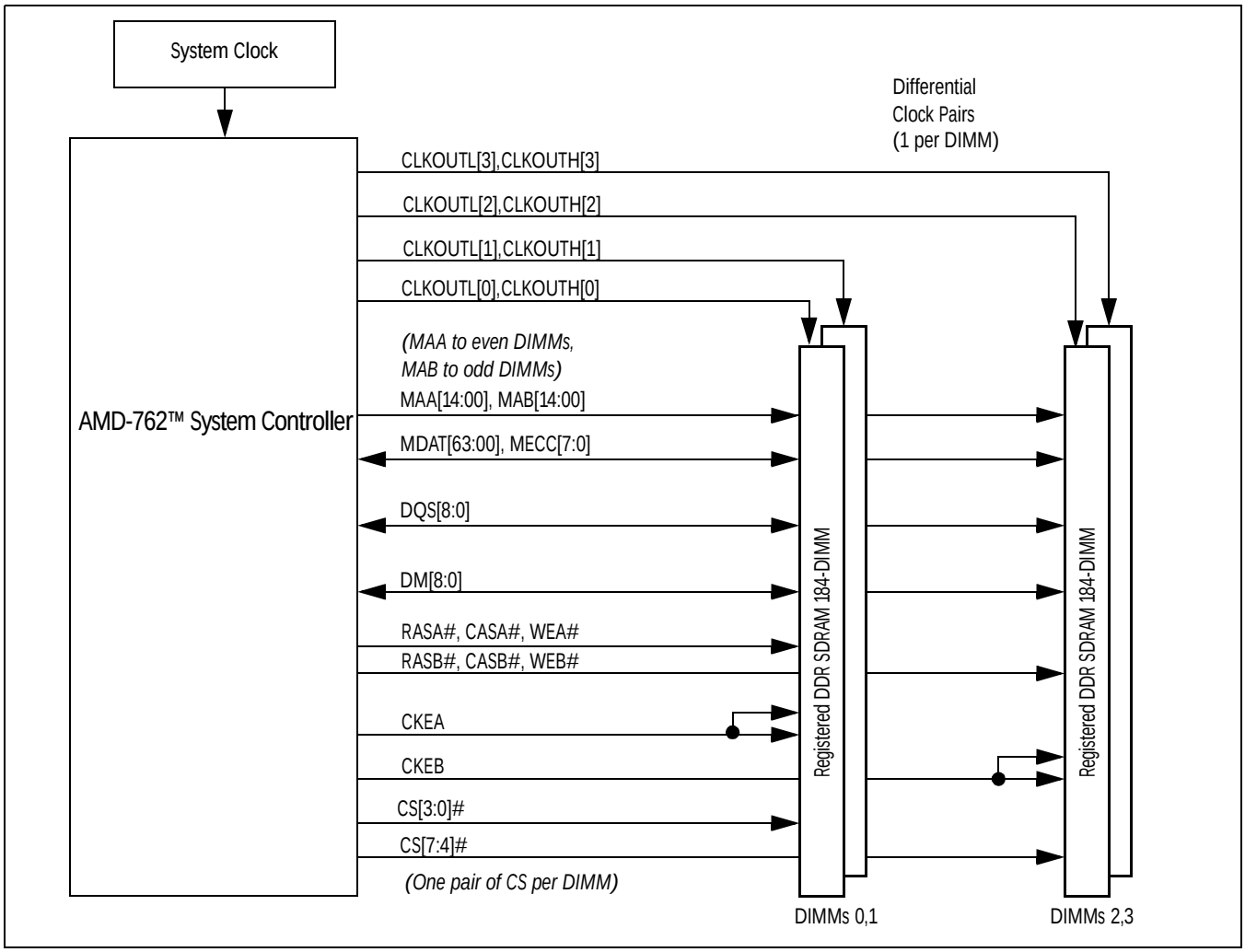



**Figure 5. AMD-762™ System Controller Connection to DDR DIMMs**

## 2.2.1 DRAM Refresh

The AMD-762 system controller keeps track of when each of CS[7:0] needs to be refreshed. Each CS is refreshed independently. Refresh is only performed on rows that are populated. A concurrent refresh cycle can be executed in parallel with other read and write requests, if there is no CS conflict and the command bus is free. Figure 6 on page 13 shows DRAM refresh timing.

Refresh rates are programmable by BIOS and can accommodate various rates at 100-MHz or 133-MHz system bus speeds.

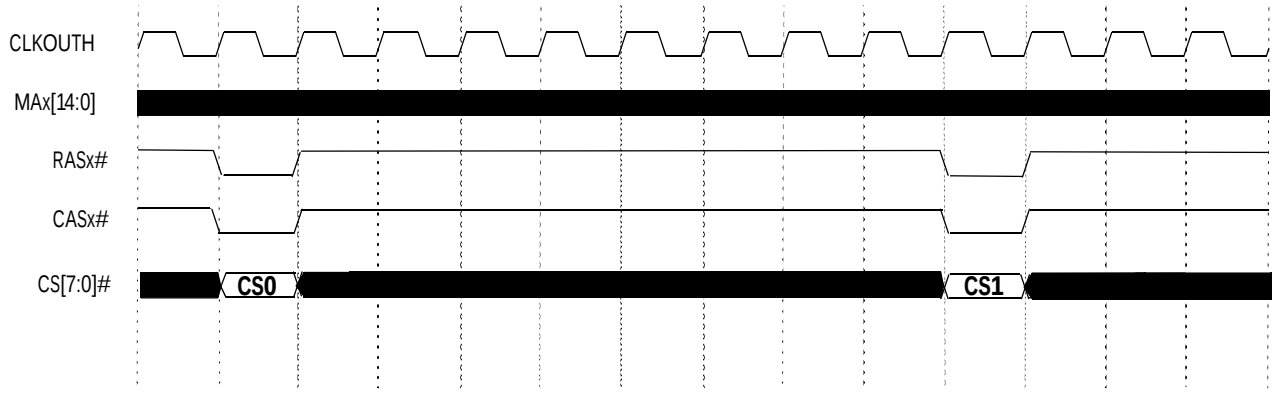



**Figure 6. DRAM Refresh Timing**

## 2.2.2 DDR Data Strobes

Unlike single data rate SDRAMs, Double Data Rate (DDR) does not latch data on the rising edge of the memory clock. Instead, DDR devices specify bidirectional data strobes (DQS pins) between the system memory controller and the DDR memories that are used to capture data. The data strobes are source-synchronous, which means that the DQS signals are driven by the device that is currently driving the data bus. The AMD-762 system controller provides one DQS pin per byte when using x8 and x16 DIMMs, or one per nibble when using x4 DIMMs. The Data Mask (DM) pins provide the additional DQS strobe function when accessing a x4 DIMM. The DM pins no longer provide a mask function when performing a write access to a x4 DIMM. Therefore, a read-modify-write cycle occurs for partial write accesses ("partial" implying an incomplete quadword of data). In the case of writes to memory, the AMD-762 system controller must drive DQS such that each edge is centered in the write-data valid window to allow the DDR DRAMs to capture the data on each edge of the strobe. For memory reads, the devices drive the DQS pins edge-aligned with the memory clock, and the AMD-762 system controller must center the DQS with the incoming data. Delaying the DQS accordingly for each byte or nibble is required. Because this timing is very tight, the AMD-762 system controller implements Programmable Delay Lines (PDLs) to accomplish this centering of DQS with the data. A separate PDL is implemented for each DQS pin.

Because the propagation delay of an individual buffer internal to the AMD-762 system controller is a function of Process, Voltage and Temperature (PVT), a mechanism is required to compensate for these three variables. As mentioned above, the delay value is known, but the number of buffers that provides this delay value is not known for a given PVT point. The calibration mechanism provides this piece of information. The mechanism used is a simple measurement of how many buffer delays are required to equal the system clock period. Because the system clock is generated by a PLL in the AMD-762 system controller that is already compensated for PVT, the system clock period is independent of PVT. Therefore, the clock period can be assumed to be a constant, and can be used to correlate the PDL values to units of time.

The calibration is automatically performed once after reset and once after self-refresh exit (before acknowledging self-refresh exit), and the resultant value is transferred to each PDL. Recalibration can be initiated via software. The AMD-762 system controller also has a mode that enables periodic autocalibration.

## 2.3 PCI Bus Controller

The AMD-762 system controller supports both 32-bit and 64-bit PCI agents on a cycle-by-cycle basis as defined by the PCI bus specification. The AMD-762 system controller asserts the REQ64# pin during reset to allow 64-bit devices to detect that the host bridge supports the full 64-bit data width. All 64-bit transactions from these bus masters are then negotiated with the PCI bus REQ64#/ACK64# protocol. The address space is still 32-bits maximum when operating with 64-bit transactions.

The AMD-762 system controller supports two PCI clock speed options as follows:

- 66/33-MHz mode that supports a 66-MHz Southbridge and two 66-MHz PCI bus slots or on-board chips. In this mode, the AMD-762 system controller provides the clocks for the Southbridge and the two optional PCI bus agents. If any of these devices are 33 MHz only (the M66EN pin is Low), then the AMD-762 system controller automatically drives 33 MHz on the PCI_66CLK[2:0] pins during reset.

- 33-MHz-only mode that always supports 33-MHz maximum PCI bus speed. In this mode, the Southbridge and all downstream PCI agents are clocked from the system clock generator's PCI clocks.

The desired PCI clocking mode is selected with the AD[15] pinstrap on the AMD-762 system controller. Refer to Chapter 7 on page 81 for details of the AMD-762 system controller's pinstrapping.

The AMD-762 system controller drives the 64-bit PCI bus synchronously with the PCI clock. For 32-bit agents, the AMD-762 system controller converts the 64-bit processor data to 32-bit PCI data and regenerates commands with minimal overhead. A processor-to-PCI posted write buffer enables the processor and PCI to operate concurrently. The AMD-762 system controller converts consecutive processor addresses to burst PCI cycles. A PCI-to-DRAM posted write buffer and a DRAM-to-PCI prefetch buffer enable concurrent PCI bus and processor-DRAM accesses during PCI-initiator transactions.

When the processor drives an I/O cycle to an address other than the AMD-762 system controller configuration register addresses, the AMD-762 system controller passes the I/O cycle to the PCI bus and responds to the CPU only after the PCI cycle completes. The AMD-762 system controller does not respond to I/O cycles driven by PCI initiators on the PCI bus. The AMD-762 system controller allows these cycles to complete on the PCI bus. A memory write is the only transaction permitted from PCI to AGP.

The PCI block can be broken up into two sub-blocks—the PCI target module and the PCI master module. The PCI target module handles cycles initiated by an external master on the PCI bus. The AMD-762 system controller responds to cycles that are directed to main memory or writes that are sent to the other PCI interface (the AGP interface). This module contains write buffers (PCI-to-memory and PCI-to-PCI), read buffers from memory, and a target sequencer that keeps track of the bus while the AMD-762 system controller is a PCI target.

The PCI master module handles processor-to-PCI bus cycles. Within a processor stream, no reordering is done.

### 2.3.1 Memory Coherency

The AMD-762 system controller assures that all data accesses remain coherent:

- All PCI/AGP accesses not in the GART range generate processor probes assuring that reads receive only the latest version of the data and that writes update only the latest version of the data. Writes are always performed in order.
- The GART range is by definition not cacheable. As a result, all PCI/AGP accesses that are in the GART range are subject to non-cacheable ordering rules—that is, they do not generate probes to the processor, writes are performed in order, and reads receive the results of all earlier writes.
- Processor accesses to addresses mapped by the GART range can either use the GART for the final address translation or map the addresses through its page tables as a non-cacheable memory type.

### 2.3.2 PCI Arbitration

The AMD-762 system controller contains arbitration logic that allocates ownership of the PCI bus among itself on behalf of the processors, the Southbridge, and other PCI initiators.

The AMD-762 supports up to seven bus grant pins and a dedicated grant pin for the Southbridge when operating in legacy mode. The request/grant pairs used depend on the system configuration supported as described in the following sections.

**Legacy Mode—Single PCI Bus Southbridge**

The legacy mode implies a standard system configuration where the PCI bus typically operates at 33 MHz with a common Southbridge such as the AMD-766 peripheral bus controller. All PCI agents connect to this PCI bus segment and their request grant pairs are connected to the AMD-762 system controller's REQ[6:0]# and GNT[6:0]# pins, while the Southbridge connects to the SBREQ#/SBGNT# pins.

The SBREQ#/SBGNT# pins are treated differently than the standard request/grant pairs as is required for legacy ISA DMA cycles. To avoid potential deadlock conditions, the AMD-762 system controller allows the SBREQ# to be asserted for extended periods of time. Bus masters using the REQ[6:0]# and GNT[6:0]# signals are preempted when another requestor

asserts its PCI request pin, but the Southbridge is allowed to complete its transactions before the SBGNT# is deasserted.

### Southbridge with an Integrated PCI-PCI Bus Bridge

A significant performance benefit of the AMD-762 system controller is the support of a 66-MHz, 64-bit PCI bus. This allows the system to support peripherals that consume much higher bandwidth, but it requires a 66-MHz Southbridge and is limited to a maximum of two additional PCI slots due to the tight 66-MHz PCI timing.

In this configuration, an AMD-768™ peripheral bus controller supports a 66-MHz PCI primary bus, and integrates a PCI to PCI bridge. The secondary bus of this bridge supports a 32-bit, 33-MHz PCI bus that supports up to seven slots that can be used for less bandwidth-intensive peripherals. In this system configuration, the Southbridge connects to the AMD-762 system controller's REQ[0]# and GNT[0]# request/grant pair, and the two optional slots on the primary bus connect to the REQ[2:1]# and GNT[2:1]# pairs. All 32-bit, 33-MHz PCI slots are arbitrated by the Southbridge and therefore connect their request/grant pairs to the Southbridge.

**Note:** Only REQ[2:0]# and GNT[2:0]# should be used when operating the primary PCI Bus at 66 MHz.

### Arbitration Priority

Access priority rotates between the Southbridge (when connected to the SBGNT# pin) and CPU/PCI bus masters (GNT[6:0]#) such that the following arbitration sequence could be seen in a busy system:

1. Southbridge (SBGNT# pin only)
2. CPU
3. Southbridge (SBGNT# pin only)
4. PCI master (one of GNT[6:0]#)
5. Repeat step 1

The SBREQ#/SBGNT# pin should be used only with a legacy Southbridge such as described in "Legacy Mode—Single PCI Bus Southbridge" on page 16.

When there are no requests for the bus, ownership can default to either processor through the AMD-762 system controller or the last PCI bus master that had bus ownership. This mode is called bus parking and is controlled by the PCI Arbitration Control register (Dev 0:F0, 0x84, bit 0).

### 2.3.3 PCI Configuration

The AMD-762 system controller uses PCI configuration mechanism #1 to select all of the options available for interaction with the processor, DRAM, and the PCI bus. This mechanism is defined in the *PCI Local Bus Specification*, Revision 2.2. All configuration functions for the AMD-762 system controller are performed by using two I/O-mapped configuration registers—IO_CNTRL (I/O address 0CF8h) and IO_DATA (I/O address 0CFCh).

These two registers are used to access all the other internal configuration registers of the AMD-762 system controller. The AMD-762 system controller decodes accesses to these two I/O addresses and handles them internally. A read to a nonexistent configuration register returns a value of FFh. Accesses to all other I/O addresses are forwarded to the PCI bus as regular I/O cycles. Read and write cycles involving the AMD-762 system controller configuration registers are only distinguished by the address and command that is sent.

The AMD-762 system controller implements the following configuration spaces:

- Device 0:Function 0 (host bridge configuration registers)
- Device 0:Function 1 (DDR I/O and PDL configuration)
- Device 1:Function 0 (PCI-PCI bridge, AGP configuration)

The Device 0:Function 1 space is disabled by default, and must be enabled by writing to a specific bit in the PCI Control register (Dev 0:F0:0x4C). The normal reserved PCI header space (0x00-0x3F) in this function returns all 1s.

### 2.3.4 PCI Parity/ECC Errors

The AMD-762 system controller indicates that an ECC error occurred on the memory bus by setting a bit in the status register and optionally asserting the PCI SERR# signal. This action results in the error being reported by the Southbridge.

The AMD-762 system controller does not check parity on the PCI bus. The status bit (Dev 0:04h, bit 31) is always 0.

### 2.3.5 PCI Accesses by an Initiator

A PCI initiator begins a memory read or write cycle by asserting FRAME# and placing the memory address on AD[31:00] (note that the AMD-762 system controller supports a maximum address space of 32 bits). The AMD-762 system controller decodes the address. If the address is within the memory region as defined by PCI Top of Memory (Dev 0:F0:0x9C), the AMD-762 system controller accepts the cycle and responds as a PCI target by asserting DEVSEL#. If the address is not within the defined memory region, the AMD-762 system controller ignores the cycle and allows it to complete on the PCI.

Read requests from PCI masters to the memory subsystem are full cache lines only. After fetching the initial cache line, the AMD-762 system controller can optionally start prefetching the next cache line. Prefetching the next cache line is preferred, because the PCI master typically reads more than one line, but can waste DRAM bandwidth if this line is thrown away.

The length of a read request is always 8 quadwords (one cache line). During writes, the AMD-762 system controller attempts to accumulate an entire cache line. If the start address is not cache aligned, the AMD-762 system controller makes single write requests until it reaches a cache-aligned address. When aligned, it makes a request every 8 quadwords. If a partial cache line write is detected, no more data is accumulated, and a request is issued to the memory subsystem.

## 2.4 Accelerated Graphics Port (AGP)

The Accelerated Graphics Port (AGP) is a point-to-point connection between a graphics adapter (AGP initiator) and the AMD-762 system controller memory controller (AGP target), which enables the adapter to store and use graphics data in main memory. This connection relieves graphics traffic from the PCI bus and greatly accelerates video performance.

The AMD-762 system controller functions as an AGP target, providing all the signals, buffers, and logic required for full compliance with the *Accelerated Graphics Port Interface Specification*, Revision 2.0.

While AGP relieves traffic on the PCI bus and frees up graphics adapter memory, the greatest impact on system performance comes from the many innovations AGP brings to data transfer operations. These improvements include the following:

- *Split Transactions*—Requests to read or write data are separate from the data transfers.
- *Pipelined Requests*—Requests can be issued contiguously and stored in the AMD-762 system controller request queue. Pipelining allows AGP to achieve high levels of concurrency with PCI and the processor.
- *Pipeline Grants*—Pipelined GNT# signals for up to four write transactions.
- *Prioritizing* (reordering)—Read and write requests can be assigned a high priority or a low priority to ensure that more urgent requests are serviced first.
- *Defined-Length Requests*—The amount of data requested is indicated in the AGP command, rather than the duration of an asserted signal, such as FRAME# in PCI.
- An 8-byte minimum data size for AGP 2x/4x transfers, which provides a more efficient method for moving the large amount of data typical in a graphics request.
- A separate, optional Sideband Address (SBA) bus that enables concurrent transmissions of requests and data transfers.
- Optional 2x/4x modes that increase the AGP graphics adapter data transfer rate.
- Freedom from the coherency requirements of PCI, which eliminates the latency resulting from cache snooping.
- Full PCI 2.2 capability, which enables the AMD-762 system controller to pass programming information from the processor to the graphics adapter.
- A Graphics Address Remapping Table (GART).

The AGP request queue is split up into two queues—one for read requests and one for write requests. Because there is a reordering FIFO in the address module, the request queues do not have to be large. The read queue is big enough to hold all outstanding read requests, which avoids stalling writes that run on the bus while the reads occur to memory.

Requests from the SBA bus are multiplexed with PIPE# requests and written to the same queues. High-priority requests are inserted in front of low-priority requests so that the request to be serviced is at the top of the queue. This reordering is done dynamically as a new request is written into the queue.

Requests from each of the queues can be read out of both the queues at the same time. The reads start fetching data from memory and the write data is sent across the AGP bus at the same time.

The AGP ordering rules specify that writes are ordered ahead of reads. Reads are serviced only when all the preceding writes have been written to memory, which is only required for low-priority requests and does not affect high-priority read requests. When a low-priority request is the next one to be serviced from the read queue, the tag of that request is compared with all valid entries in the write queue. If any entry matches, then the read request is blocked. Only after the write requests are serviced are the read requests allowed to proceed.

**AGP Request Queue.** In general, the AGP request queue services AGP requests in the order received, subject to their priority (write High, read High, write, read).

**Ordering Rules.** The request queue is subject to the following AGP ordering rules:

- High-priority write requests are processed in the order they are received.
- High-priority read requests are processed in the order they are received.
- Low-priority write requests are processed in the order they are received.
- Low-priority read requests are processed in the order they are received.
- Low-priority reads push low-priority writes, meaning that a write request is serviced before a subsequently received read request is serviced.
- Low-priority writes can pass low-priority reads, meaning that a write request can be serviced before a previously received read request.

- There are no ordering restrictions between AGP and PCI transactions on the AGP bus.
- PCI transactions on the AGP bus follow the PCI ordering rules described in the *PCI Local Bus Specification*, Revision 2.2.
- High-priority requests are re-ordered in front of low-priority requests.
- There is no ordering relationship between high-priority reads, high-priority writes, and any other transfer type, such as low-priority reads, low-priority writes, PCI reads, or PCI writes.

If a low-priority data transfer is in progress when a high-priority request is received, the data transfer completes before the high-priority request is serviced—that is, a request is not preemptable. A high-priority request supersedes a low-priority request on a request boundary only.

## 2.5 System Clocking

The AMD-762 system controller requires the following system clocks:

- SYSCLK, used for clocking the AMD Athlon system busses and the DDR DRAM interface. This clock is typically either 100 MHz or 133 MHz. This clock is also used to create the differential DDR DRAM clock outputs (CLKOUT[5:0], CLKOUT[5:0]#).
- AGPCLK, 66 MHz, used for clocking the AGP and PCI internal logic. This feeds the PCI 66-MHz PLL in 66/33-MHz PCI mode.
- PCICLK, provides a 33-MHz PCI bus clock and is used to synchronize the PCI bus I/O signals to the 33-MHz PCI signal domain when operating in 33-MHz-only PCI mode.

There are two different clocking schemes for the PCI bus and Southbridge as described in the following sections.

### 66-MHz PCI Bus

The highest performance option supports a 66-MHz primary PCI bus on the AMD-762 system controller, with a 33-MHz secondary PCI bus controlled by an AMD-768 peripheral bus controller's PCI to PCI bridge. This mode also provides up to two optional slots for 66-MHz peripherals.

The AMD-762 system controller provides the three 66-MHz clocks required for the Southbridge and the two PCI bus slots in this mode. If a 33-MHz-only card is inserted in one of the 66-MHz PCI slots, then the M66EN signal is deasserted, which causes the AMD-762 system controller to drive 33 MHz on the PCI_66CLK[2:0] pins.

The 66-MHz PCI mode is illustrated in Figure 7.

**33-MHz PCI Bus**

An alternate mode of PCI bus operation is illustrated in Figure 8 on page 24, and simply supports a standard 33-MHz PCI Southbridge and up to seven PCI slots.

In this mode, all PCI devices operate at 33 MHz and clocking is provided by the motherboard clock generator chip.

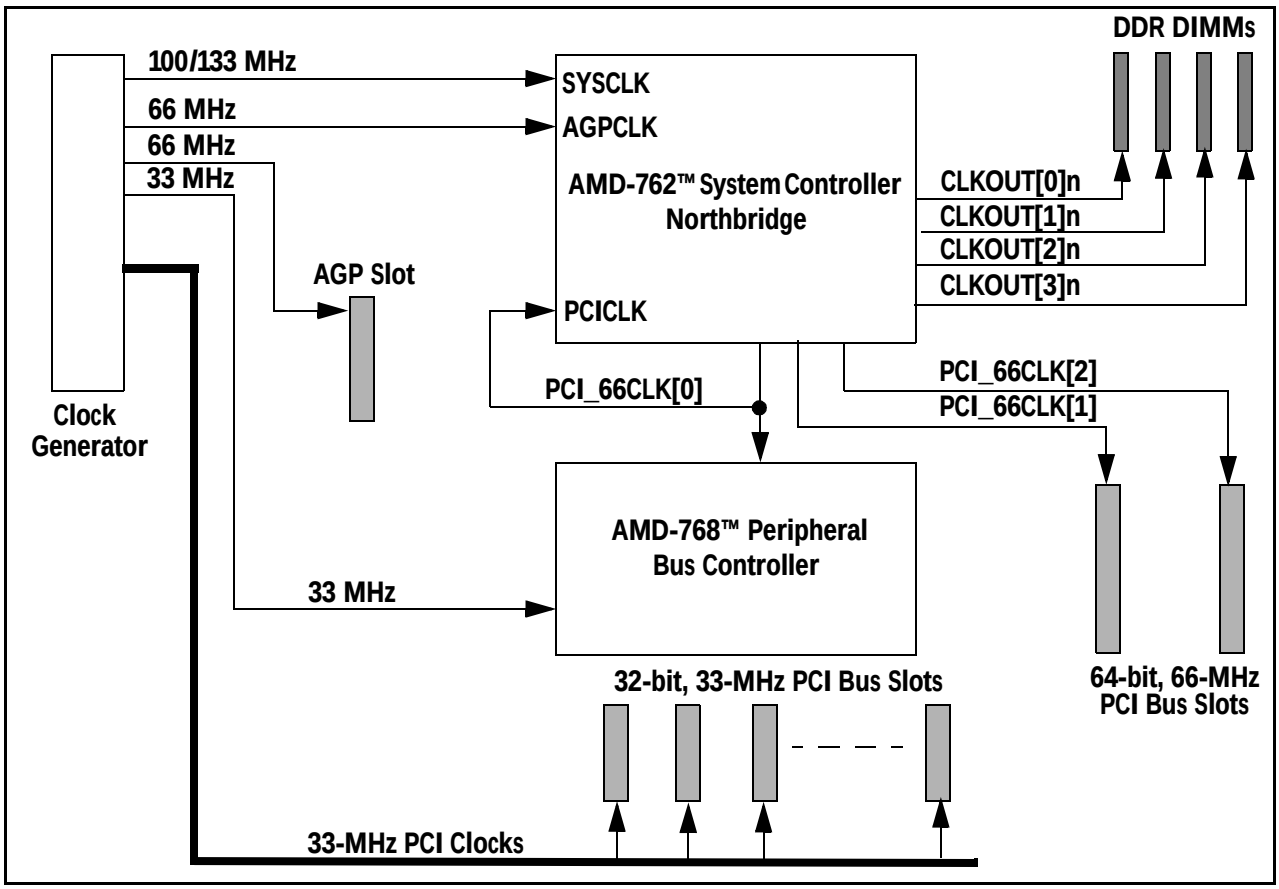



**Figure 7. System Clocking with 66-MHz PCI Primary Bus**

The AMD-762 system controller implements three internal PLLs to control clock skew on-chip for the SYSCLK, AGPCLK, and PCICLK domains. An external feedback path is required on the motherboard for the 66-MHz PCI PLL when operating in 66-MHz mode. This requires the PCI_66CLK[0] output pin to be connected back into the AMD-762 system controller's PCICLK input for skew control, as shown in Figure 7 on page 23.

These PLLs can be bypassed for motherboard testing. Refer to Chapter 3 for further details of PLL bypass testing.

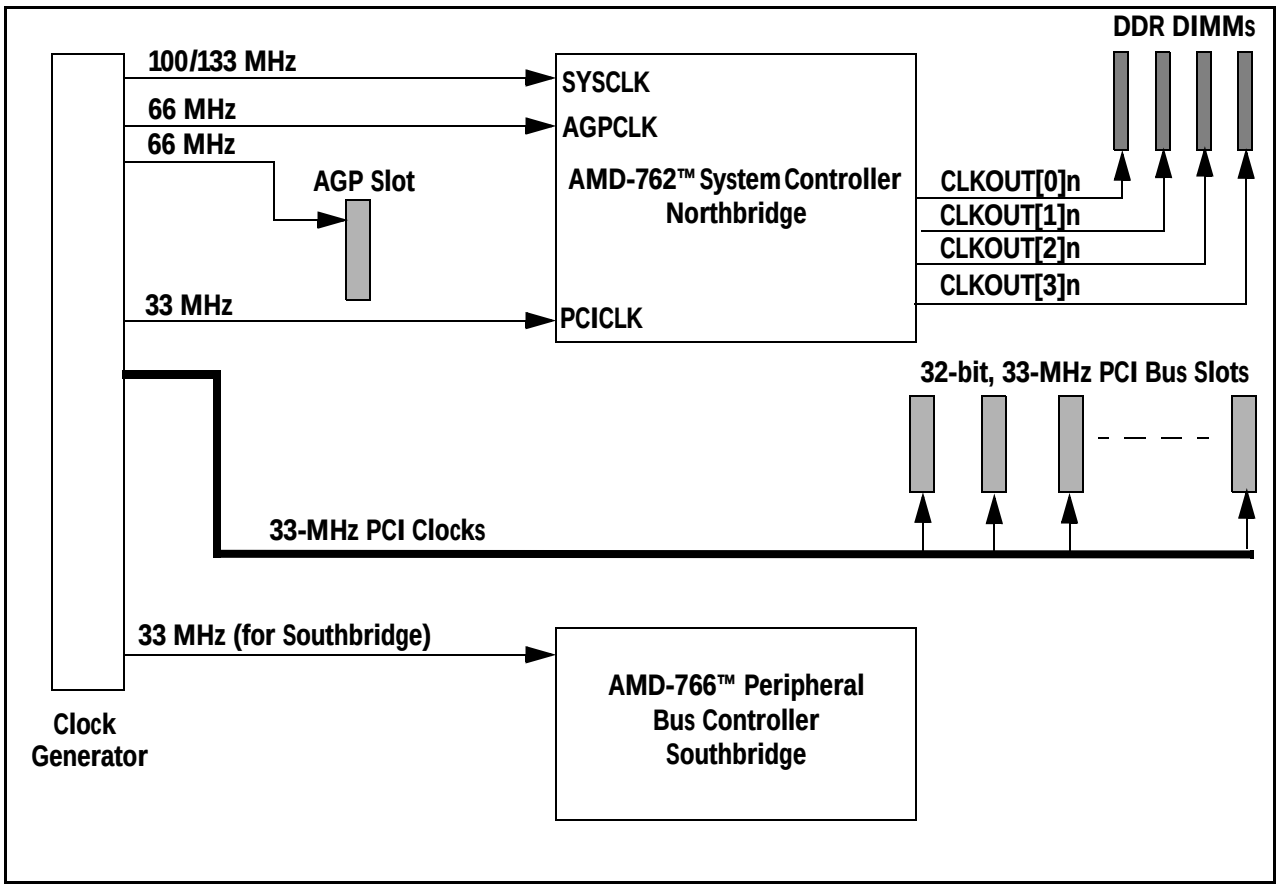



**Figure 8. System Clocking with 33-MHz PCI Bus**

# 2.6 Power Management

The AMD-762 system controller supports the Advanced Configuration Power Interface (ACPI) specification, On-Now, and PC 99 requirements through a handshake mechanism with the processor. The ACPI-defined registers required for processor and system power management are contained in the Southbridge. SMM memory remapping is handled by a model-specific register in the AMD Athlon processor. See the *AMD Athlon™ BIOS Developers Guide*, order# 21656, for more information about the SMM remapping operation.

Figure 9 shows how the processor and system controller communicate power-state transitions.

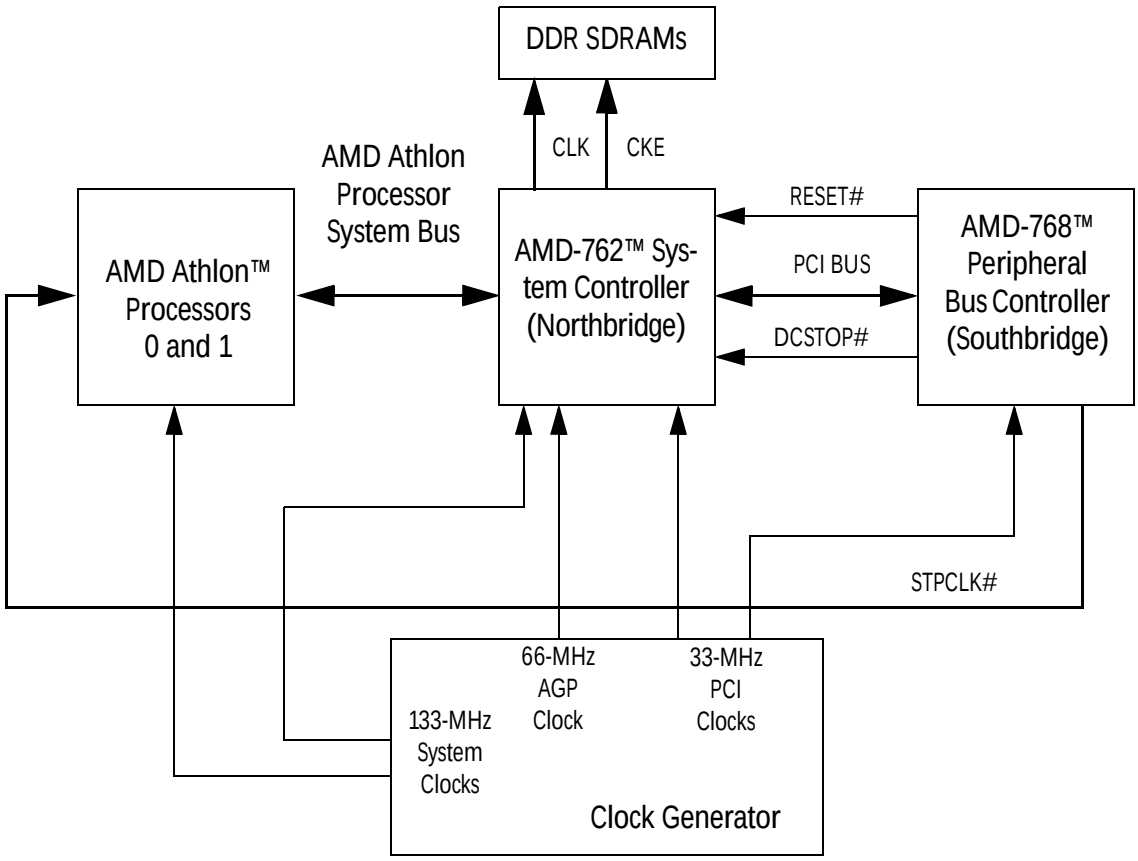



**Figure 9. Power Management Signal Connections**

The processor and the AMD-762 system controller communicate power-state transitions through the AMD Athlon system bus connect/disconnect protocol and special cycles (masked writes to a defined AMD Athlon system bus address with specific data encoding). In general, the processor initiates a request for a disconnect with a special cycle, and the AMD-762 system controller may or may not actually disconnect the processor with the connect/disconnect protocol. The AMD-762 system controller performs the requested connect/disconnect as part of the process of entering and exiting certain ACPI states. The following two special cycles are of interest:

- Halt—Generated by the AMD Athlon processors in response to executing a HALT instruction. The AMD-762 system controller forwards the Halt special cycle to the PCI bus but does not perform any further power management for Halt conditions. The processor buses remain connected and the memory is not placed in self-refresh mode.
- Stop Grant—Generated by the AMD Athlon processors in response to assertion of STPCLK#. When the AMD-762 system controller receives a Stop Grant from the processor, it waits for a Stop Grant from the second processor (if installed), then it sends a Stop Grant special cycle on the PCI bus. The AMD-762 system controller initiates the following sequence of actions if the Stop Grant disconnect bit is set (Dev 0:F0:0x60):
  A. Disables PCI/AGP arbitration and waits for all queues to memory to be empty (including refresh requests).
  B. Completes the AMD Athlon system bus cycles. The AMD-762 system controller then initiates an AMD Athlon system bus disconnect to the processors, and causes the memory to enter self-refresh.
  C. The Southbridge decodes the special cycle and enters the appropriate power state. The Southbridge can then assert DCSTOP#.

Halt special cycles are generally considered part of an ACPI state definition (C1). STPCLK#, however, can be asserted at random times while the processor is in the full-running state (C0) to conserve power (clock throttling).

The AMD-762 system controller supports the following power states:

1. ACPI C0 full-on
2. ACPI C1 Halt
3. ACPI S1 power-on suspend
4. ACPI S3 suspend to RAM

These power states are described in further detail in subsequent paragraphs.

### 2.6.1 Full-On (C0)

In this state, the AMD-762 system controller is fully operational, all clock trees are running, all voltage planes are enabled, and the AMD-762 system controller provides normal refresh to DRAM.

### 2.6.2 Halt (C1)

If the AMD-762 system controller detects a Halt special cycle from either of the processors, the Halt state (C1) is entered and the Halt special cycle is driven on the PCI bus. No further activity is required. The processor buses remain connected and the memory remains in normal refresh mode.

### 2.6.3 Throttling with STPCLK# Assertion

The AMD-762 system controller supports clock throttling via assertion of the processor's STPCLK# pin. If the AMD-762 system controller has detected a Stop Grant special cycle from the processor, the AMD-762 system controller waits for a Stop Grant from the second processor (if installed), then the Stop Grant special cycle is driven on the PCI bus. If the Stop Grant disconnect bit is set (Dev 0:F0:0x60), when the Stop Grant special cycle state is received, and there is no probe traffic, the AMD-762 system controller disconnects the processor and places system memory into self-refresh mode before passing the special cycle to the PCI Bus. If the AMD-762 system controller detects a PCI DMA master transaction that needs a snoop, then the processors are connected, DRAM is taken out of self-refresh mode, and the probe cycle(s) are initiated on the AMD Athlon processor system buses. If the processors do not start any non-NOP AMD Athlon processor system bus cycles

while the probe is in progress, then the AMD-762 system controller disconnects the AMD Athlon processor system bus following the completion of the probe. If the processors start sending non-NOP AMD Athlon processor system bus cycles while connected, then the AMD-762 system controller transitions to the full-on state.

### 2.6.4 Power-On Suspend (S1)

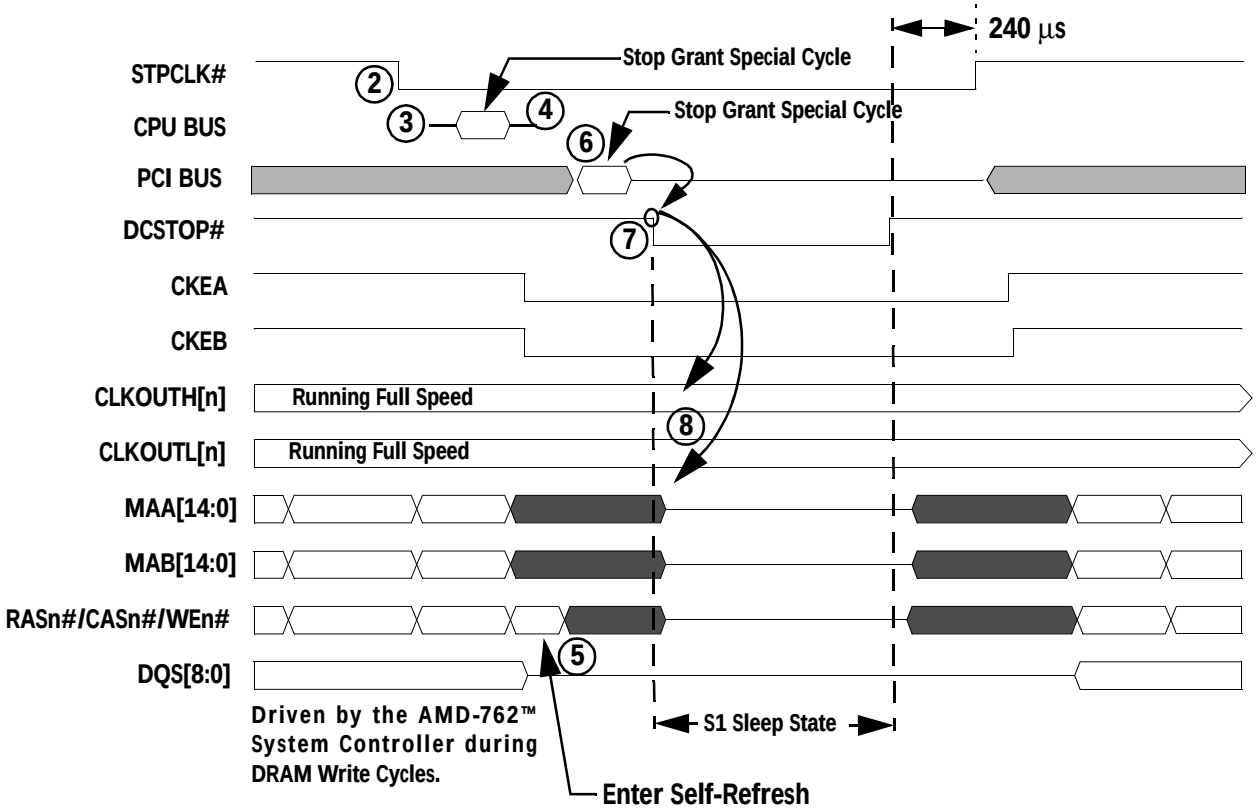
The S1 state achieves very low power by disconnecting the processors, entering self-refresh, and then gating off most of the internal high-speed clock trees in the AMD-762 system controller. Snooping is prevented by the device drivers prior to entering this state. The DDR DRAM clocks continue to be driven as required for the registered DDR DIMMs. Most internal clocks are gated off, allowing the AMD-762 system controller to achieve a low operating current.

The S1 state is entered in a similar manner to clock throttling, starting with a STPCLK# assertion and the Stop Grant state. The Southbridge asserts the DCSTOP# signal, which is used by the AMD-762 system controller to gate off internal clock trees for lower power. All power supplies remain on, and the clock synthesizer chip on the motherboard continues to drive all clocks. The sequence of operation for entering the S1 state is listed below. Figure 10 on page 30 shows a power-on suspend system timing diagram example.

**S1 Sequence**

1. The operating system communicates with all device drivers, causing them to disable their respective peripherals, thus preventing any new bus master activity (DMA) on the PCI and AGP buses. DMA activity already in progress in the AMD-762 system controller completes normally.
2. The Southbridge asserts STPCLK# to both AMD Athlon processors.
3. The processors flush their buffers and generate a Stop Grant special bus cycle on the AMD Athlon processor system bus.
4. After receiving both Stop Grant special cycles, the AMD-762 system controller flushes all internal queues and initiates a disconnect cycle to the CPUs by deasserting their CONNECT pins. The AMD Athlon processors respond by deasserting the PROCRDY signal.

5. After all queues are flushed, the AMD-762 system controller's power management logic requests the DRAM controller to place the DRAM in self-refresh mode. The DRAM controller initiates self-refresh, then acknowledges to the power management logic.
   - Self-refresh mode is initiated by generating an auto-refresh cycle and deasserting the CKE pins.
6. The AMD-762 system controller issues a Stop Grant special cycle on the PCI bus.
7. The Southbridge detects the Stop Grant special cycle on the PCI bus and asserts the DCSTOP# signal.
8. The AMD-762 system controller samples DCSTOP# active and gates off most of the internal clock trees. The DDR DRAM address/command outputs are three-stated. The CKE pins remain driven Low. The external clock sources and the AMD-762 system controller PLLs continue to run.
   - Note that the DDR DRAM clocks (CLKOUT[5:0], CLKOUT[5:0]#) continue to run. This action is required because the reset signal to the registered DIMMs is connected to the AMD-762 system controller's RESET# pin. The RESET# pin is **not asserted in the S1 state, thus the clocks cannot be removed from the registered DIMMs**.




***Note:*** *Circled numbers correspond to "S1 Sequence" on page 28.*

**Figure 10. Power On Suspend System Timing Diagram Example**

This state is exited when the DCSTOP# signal is deasserted by the Southbridge, followed by a deassertion of STPCLK#. This action causes the AMD-762 system controller to enable the clock trees and prepare to reconnect the processor. The processors assert their respective PROCRDY signal, which causes the AMD-762 system controller to exit self-refresh and reconnect the AMD Athlon processor system buses. The AMD-762 system controller retains the state of all configuration registers during the S1 state.

## 2.6.5 Suspend to RAM (S3)

The S3 state is similar to S1. However, power is removed from most of the motherboard except the AMD-762 system controller, DRAM, and a portion of the Southbridge. S3 is the

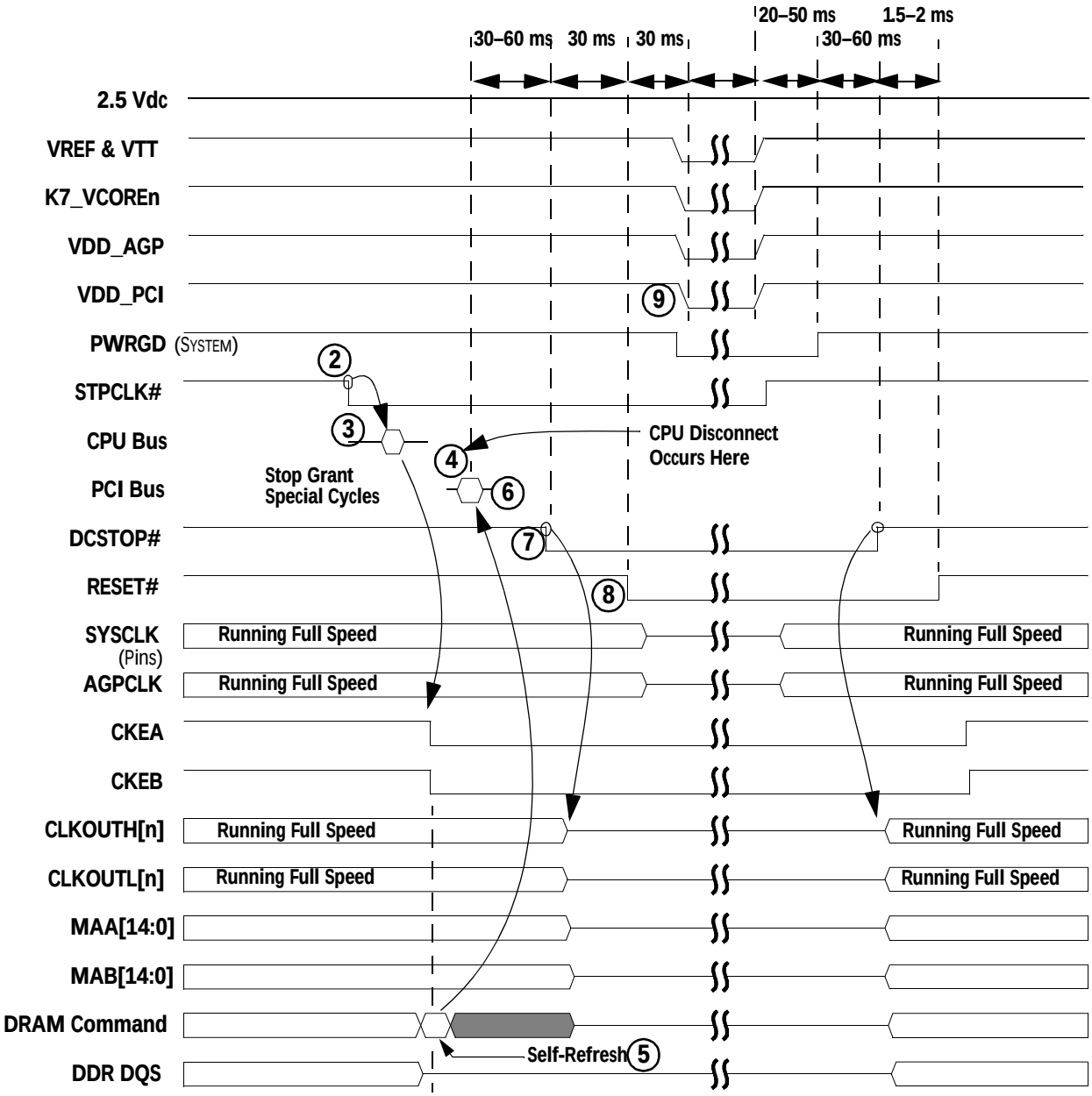
lowest power sleep state, and allows very fast resume because system context is stored in memory instead of on disk.

The S3 state is entered similarly to S1 with a Stop Grant special cycle and DCSTOP#. After entering S3 state with DCSTOP# assertion, the Southbridge asserts the RESET# signal, which causes the AMD-762 system controller to gate off its I/O rings to accommodate the voltages being removed from the AMD Athlon processor system bus, PCI bus, and AGP bus. The AMD-762 system controller core remains powered (2.5 Vdc) as does the DDR I/O interface and the DDR DIMMs, to allow the memory to remain in self-refresh mode with the CKE pins driven Low. The sequence of operation for entering the S3 state is listed below. Figure 11 on page 33 shows a suspend to RAM system timing diagram example.

**S3 Sequence**

1. As with the S1 state, the device drivers are called to place all devices into the D3 device state, which prevents them from trying to master on the bus they reside (or access system memory).
2. The ACPI driver (or BIOS under APM) writes to the appropriate registers in the Southbridge to initiate the hardware sequence into the S3 state. In response to this write, the Southbridge asserts STPCLK# to the AMD Athlon processors. Once STPCLK# has been asserted, the power management state machine in the Southbridge waits for a Stop Grant special cycle on the PCI bus before completing the transition into the S3 state.
3. The CPUs recognize that STPCLK# has been asserted, flushes internal buffers, and generates a Stop Grant cycle on the AMD Athlon processor system bus.
4. After detecting both Stop Grant special cycles on the processor buses, the AMD-762 system controller flushes all internal queues including outstanding probes, then deasserts the CONNECT pins. The CPUs respond by deasserting their respective PROCRDY pins.
5. When the disconnect is complete, the AMD-762 system controller executes a self-refresh command to the DDR SDRAM and waits for it to complete (this action is accomplished by issuing an auto-refresh command and driving the CKE signals Low to the DRAM).

6. The AMD-762 system controller issues a Stop Grant special cycle on the PCI bus.
7. The Southbridge asserts DCSTOP#. The AMD-762 system controller follows the normal DCSTOP# protocol as described in "S1 Sequence" on page 28, including gating most of the internal clocks off. The DDR output clocks (CLKOUT[5:0], CLKOUT[5:0]#) continue running for an additional six clock periods from the assertion of RESET#. This action is required because the DIMM reset signal on registered DIMMs is connected to the AMD-762 system controller RESET# pin, and the DIMM clocks must be running while the DIMM reset is first asserted.
8. The Southbridge asserts PCIRST# (RESET# on the AMD-762 system controller). The AMD-762 system controller continues driving the CKE pins Low, and gates off the I/O pads to prevent driving 1s to the unpowered I/O ring and to inhibit floating inputs from the unpowered I/O rings to the powered core logic. The input clock pins (SYSCLK, AGPCLK, and PCICLK) are also gated off because these input pins are floating when the motherboard's 3.3 Vdc is powered off. The two STR bits in the DRAM Mode/Status register (Dev 0:F0:0x58) are cleared to 0s. The state of all other memory controller configuration register bits is preserved.
9. The Southbridge signals the power supply (deasserts PWRON#) to shut down all but the 5-Vdc and 2.5-Vdc voltages. The motherboard clock generator chip shuts down, therefore the input clocks (SYSCLK, AGPCLK, and PCICLK) float.




*Note: Circled numbers correspond to "S3 Sequence" on page 31.*

**Figure 11. Suspend to RAM System Timing Diagram Example**

The S3 state is exited when the Southbridge detects an enabled resume event. The Southbridge powers up all of the voltage planes that are off during the S3 state by asserting PWRON#. After all of the voltage planes in the system are within specification, and all of the outputs of the system clock generator are running within specification, PWRGD is asserted to the Southbridge. The Southbridge then deasserts DCSTOP# followed by deassertion of PCIRST# (the RESET# pin on the AMD-762 system controller).

The AMD-762 system controller retains the state of the memory controller configuration registers, which allows BIOS to immediately access memory to retrieve and restore the system context. There are two configuration bits that BIOS uses to allow the AMD-762 system controller to differentiate between S3 and all other states following an active to inactive transition on the RESET# pin. Upon exiting the S3 sleep state, BIOS writes the appropriate value to these bits, which causes the AMD-762 system controller to exit self-refresh. The two register bits (STR_Control) are in the DRAM Mode/Status register (Dev 0:F0:0x58). Refer to the *AMD-762™ System Controller Software/BIOS Design Guide*, order# 24416 for detailed information on these bits.

# 3 Test

The AMD-762™ system controller supports test modes that may be used in some cases for motherboard manufacturing test and debug. The following test modes are available on the AMD-762 system controller:

- Three-state test
- NAND tree test
- PLL bypass test
- Clock output test

Three-state test and NAND tree test can be used to prevent the AMD-762 system controller from driving its pins and to verify connectivity of the AMD-762 system controller to the motherboard. The PLL bypass and clock output test modes are provided primarily for motherboard debug and can be used to verify system clocking and drive slower clocks into the system.

Test modes are invoked in the AMD-762 system controller by the assertion of the TEST# pin in conjunction with enabling specific pinstraps on the PCI bus AD[31:0] pins, as described in each section. These pins can be used as pinstraps for various functions by connecting either a pullup or pulldown resistor as required to enable or disable the function (a 10-kohm resistor should be used). The pinstraps are sampled at reset and latched, and the value of most pinstraps can be read in the Configuration Status register (Dev 0:F0:0x88).

Asserting the RESET# pin and de-asserting the TEST# pin causes the AMD-762 system controller to exit test modes.

## 3.1 Board (Three-State) Test Mode

Board test mode forces all AMD-762 system controller outputs to a high impedance to allow board-level test equipment to drive the nodes normally driven by AMD-762 system controller pins to test board connectivity. The outputs are three-stated after a maximum of six clocks are driven on the SYSCLK and AGPCLK pins. The minimum number of clocks is required due

to some I/O cells that cannot be asynchronously forced into a three-state mode.

Board test mode is entered when the AD[25] pin is asserted High simultaneous with the TEST# pin during RESET# assertion. The test mode is then latched coming out of reset. The AD[09] pin should also be pulled up to force the internal PLLs to be bypassed.

Three-state mode can be exited by an assertion of the RESET# pin. This reset also disables the PLL bypass mode if it was entered.

### 3.1.1 Board Test Mode Clocking

When entering three-state mode, the PLLs should also be bypassed as described above. This procedure forces the clocks driven on the SYSCLK and AGPCLK input pins to be routed directly to the appropriate clock domains. The SYSCLK and AGPCLK pins must then be clocked for six clocks as required to force some AMD-762 system controller I/O pads to the three-state mode.

## 3.2 NAND Tree Test Mode

NAND tree testing is used on the tester and can also be used during board testing to test connectivity of AMD-762 system controller inputs. In this test mode, each AMD-762 system controller input can be asserted one pin at a time, and for each pin assertion there should be a change in state on the output of the respective NAND tree. The AMD-762 system controller provides multiple NAND trees, which speeds up characterization of the device, and also reduces motherboard test time. The AMD-762 system controller NAND trees are divided by I/O type, which create the following trees:

- AMD Athlon system bus NAND tree

  This tree includes all signals on the AMD Athlon processor system bus. SYSCLK is not included in the NAND tree. The output of this tree is the GNT[0]# pin. The ordering for this NAND tree is shown in Table 2 on page 38.

- AGP/APC NAND tree

  This tree includes AGPCLK, AGP, and the PCI-type signals that are included in the AGP interface. The output of this tree is the GNT[1]# pin. The ordering for this NAND tree is shown in Table 3 on page 41.

- DDR DRAM NAND tree

  This tree includes all signals in the DDR interface. The output of this tree is the GNT[3]# pin. The ordering for this NAND tree is shown in Table 4 on page 42.

- PCI NAND tree

  This tree includes PCICLK and PCI bus signals, excluding the RESET# input. The output of this tree is the GNT[2]# pin. The ordering for this NAND tree is shown in Table 5 on page 44.

**Table 2. AMD Athlon™ Processor System Bus NAND Tree Ordering**

| # | Input Pin Name | Ball | # | Input Pin Name | Ball | # | Input Pin Name | Ball |
|---|---|---|---|---|---|---|---|---|
| 1 | P0_SADDOUT[14]# | D-1 | 32 | P0_SDATA[59]# | L-1 | 63 | P0_SDATA[19]# | R-5 |
| 2 | P0_SYSFILLVAL# | J-8 | 33 | P0_SDATA[56]# | M-2 | 64 | P0_SDATAINCLK[1]# | R-1 |
| 3 | P0_SADDOUT[10]# | F-5 | 34 | P0_SCHECK[7]# | K-3 | 65 | P0_SCHECK[3]# | T-1 |
| 4 | P0_SADDOUT[13]# | E-2 | 35 | P0_SDATA[57]# | L-4 | 66 | P0_SDATA[21]# | R-4 |
| 5 | P0_SADDOUT[07]# | E-1 | 36 | P0_SDATA[39]# | L-6 | 67 | P0_SDATA[20]# | R-3 |
| 6 | P0_SADDOUTCLK# | E-3 | 37 | P0_SDATA[35]# | M-6 | 68 | P0_SDATA[29]# | U-1 |
| 7 | P0_SADDOUT[05]# | F-4 | 38 | P0_SDATA[37]# | L-7 | 69 | P0_SDATA[23]# | U-2 |
| 8 | P0_SADDOUT[09]# | F-2 | 39 | P0_SDATA[34]# | M-8 | 70 | P0_SDATA[28]# | T-3 |
| 9 | P0_SADDOUT[12]# | F-1 | 40 | P0_SCHECK[4]# | N-7 | 71 | P0_SDATA[26]# | T-5 |
| 10 | P0_SADDOUT[11]# | G-5 | 41 | P0_SDATA[47]# | M-3 | 72 | P0_SDATA[25]# | V-1 |
| 11 | P0_SADDOUT[08]# | F-3 | 42 | P0_SDATA[46]# | L-5 | 73 | P0_SDATA[27]# | V-2 |
| 12 | P0_SADDOUT[02]# | G-1 | 43 | P0_SDATA[45]# | M-7 | 74 | P0_SDATA[24]# | T-7 |
| 13 | P0_SADDOUT[03]# | H-2 | 44 | P0_SDATAOUTCLK[2]# | N-5 | 75 | P0_SDATA[16]# | U-7 |
| 14 | P0_SADDOUT[04]# | G-3 | 45 | P0_SDATAINCLK[2]# | M-1 | 76 | P0_SDATA[15]# | U-6 |
| 15 | P0_SADDOUT[06]# | H-4 | 46 | P0_SDATA[36]# | L-3 | 77 | P0_SDATA[07]# | U-8 |
| 16 | P0_SDATA[54]# | H-6 | 47 | P0_SDATA[44]# | M-5 | 78 | P0_SDATA[06]# | U-3 |
| 17 | P0_SDATA[55]# | H-5 | 48 | P0_SDATA[42]# | N-3 | 79 | P0_SDATA[05]# | U-4 |
| 18 | P0_SDATA[61]# | H-7 | 49 | P0_SDATA[40]# | P-7 | 80 | P0_SDATA[12]# | W-1 |
| 19 | P0_SDATA[50]# | J-7 | 50 | P0_SDATA[38]# | M-4 | 81 | P0_SDATA[04]# | V-6 |
| 20 | P0_SDATA[48]# | K-7 | 51 | P0_SDATA[41]# | P-5 | 82 | P0_SDATAINCLK[0]# | U-5 |
| 21 | P0_SDATAOUTCLK[3]# | H-1 | 52 | P0_SCHECK[5]# | N-1 | 83 | P0_SDATA[02]# | V-3 |
| 22 | P0_SDATA[49]# | J-6 | 53 | P0_SDATA[32]# | P-2 | 84 | P0_SCHECK[0]# | V-7 |
| 23 | P0_SDATA[62]# | J-5 | 54 | P0_SDATA[33]# | P-4 | 85 | P0_SDATA[03]# | V-5 |
| 24 | P0_SDATA[53]# | J-2 | 55 | P0_SDATA[43]# | P-3 | 86 | P0_SDATA[01]# | V-4 |
| 25 | P0_SDATA[63]# | J-1 | 56 | P0_SDATA[31]# | P-1 | 87 | P0_SDATAOUTCLK[0]# | W-5 |
| 26 | P0_SDATAINCLK[3]# | H-3 | 57 | P0_SDATA[17]# | R-7 | 88 | P0_SDATA[08]# | Y-1 |
| 27 | P0_SDATA[52]# | J-4 | 58 | P0_SCHECK[2]# | P-8 | 89 | P0_SDATA[00]# | W-3 |
| 28 | P0_SDATA[60]# | K-1 | 59 | P0_SDATA[30]# | P-6 | 90 | P0_SCHECK[1]# | V-8 |
| 29 | P0_SDATA[58]# | L-2 | 60 | P0_SDATA[18]# | R-6 | 91 | P0_SDATA[09]# | Y-3 |
| 30 | P0_SDATA[51]# | K-5 | 61 | P0_SDATA[22]# | R-2 | 92 | P0_SDATA[14]# | Y-2 |
| 31 | P0_SCHECK[6]# | J-3 | 62 | P0_SDATAOUTCLK[1]# | R-8 | 93 | P0_SDATA[10]# | AA-1 |

**Table 2. AMD Athlon™ Processor System Bus NAND Tree Ordering (Continued)**

| # | Input Pin Name | Ball | # | Input Pin Name | Ball | # | Input Pin Name | Ball |
|---|---|---|---|---|---|---|---|---|
| 94 | P0_SDATA[13]# | W-7 | 124 | P1_SADDOUT[02]# | AJ-2 | 154 | P1_SDATA[47]# | AJ-7 |
| 95 | P0_SDATA[11]# | Y-7 | 125 | P1_SADDOUT[08]# | AJ-3 | 155 | P1_SDATA[38]# | AH-8 |
| 96 | P0_SADDIN[03]# | AA-2 | 126 | P1_SADDOUT[06]# | AF-3 | 156 | P1_SDATA[36]# | AK-8 |
| 97 | P0_SDATAINVALID# | AB-1 | 127 | P1_SADDOUT[05]# | AG-3 | 157 | P1_SDATA[37]# | AL-8 |
| 98 | P0_SADDIN[02]# | Y-4 | 128 | P1_SDATA[54]# | AL-4 | 158 | P1_SDATAOUTCLK[2]# | AG-9 |
| 99 | P0_SADDIN[05]# | Y-5 | 129 | P1_SDATA[61]# | AE-5 | 159 | P1_SDATA[42]# | AD-11 |
| 100 | P0_SADDIN[11]# | Y-6 | 130 | P1_SDATA[48]# | AF-4 | 160 | P1_SDATA[39]# | AK-9 |
| 101 | P0_SADDIN[04]# | AA-6 | 131 | P1_SDATA[55]# | AH-3 | 161 | P1_SCHECK[4]# | AL-9 |
| 102 | P0_SADDIN[07]# | AA-3 | 132 | P1_SDATA[50]# | AF-5 | 162 | P1_SDATAINCLK[2]# | AJ-8 |
| 103 | P0_SADDIN[06]# | AA-4 | 133 | P1_SCHECK[6]# | AF-6 | 163 | P1_SDATA[45]# | AH-9 |
| 104 | P0_SADDIN[10]# | AB-5 | 134 | P1_SDATA[49]# | AG-5 | 164 | P1_SDATA[35]# | AL-10 |
| 105 | P0_SADDINCLK# | AA-7 | 135 | P1_SDATA[52]# | AH-4 | 165 | P1_SDATA[34]# | AK-11 |
| 106 | P0_SADDIN[08]# | AA-5 | 136 | P1_SDATA[57]# | AE-7 | 166 | P1_SDATA[43]# | AG-10 |
| 107 | P0_SADDIN[09]# | AB-3 | 137 | P1_SDATAINCLK[3]# | AK-5 | 167 | P1_SDATA[44]# | AJ-9 |
| 108 | P0_SADDIN[14]# | AC-1 | 138 | P1_SDATAOUTCLK[3]# | AJ-4 | 168 | P1_SDATA[23]# | AF-11 |
| 109 | P0_SADDIN[12]# | AD-1 | 139 | P1_SDATA[58]# | AG-6 | 169 | P1_SDATA[18]# | AE-12 |
| 110 | P0_SADDIN[13]# | AC-3 | 140 | P1_SDATA[63]# | AL-5 | 170 | P1_SDATA[21]# | AE-11 |
| 111 | P0_CONNECT | AC-4 | 141 | P1_SDATA[51]# | AK-6 | 171 | P1_SDATAINCLK[1]# | AD-12 |
| 112 | P0_PROCRDY | AC-6 | 142 | P1_SDATA[53]# | AJ-5 | 172 | P1_SDATA[17]# | AF-12 |
| 113 | P0_CLKFWDRST | AC-5 | 143 | P1_SDATA[62]# | AH-6 | 173 | P1_SDATA[31]# | AL-11 |
| 114 | P1_SADDOUT[10]# | AD-5 | 144 | P1_SDATA[59]# | AL-6 | 174 | P1_SCHECK[3]# | AJ-10 |
| 115 | P1_SADDOUT[07]# | AD-7 | 145 | P1_SCHECK[7]# | AL-7 | 175 | P1_SDATA[22]# | AG-11 |
| 116 | P1_SADDOUT[11]# | AD-6 | 146 | P1_SDATA[56]# | AE-8 | 176 | P1_SDATA[19]# | AK-12 |
| 117 | P1_SADDOUT[09]# | AF-2 | 147 | P1_SDATA[60]# | AJ-6 | 177 | P1_SDATA[27]# | AG-13 |
| 118 | P1_SADDOUT[12]# | AF-1 | 148 | P1_SDATA[41]# | AE-9 | 178 | P1_SDATAOUTCLK[1]# | AH-11 |
| 119 | P1_SADDOUTCLK# | AG-1 | 149 | P1_SDATA[46]# | AF-8 | 179 | P1_SDATA[20]# | AJ-11 |
| 120 | P1_SADDOUT[14]# | AG-2 | 150 | P1_SDATA[32]# | AG-7 | 180 | P1_SDATA[26]# | AL-12 |
| 121 | P1_SADDOUT[04]# | AE-3 | 151 | P1_SCHECK[5]# | AG-8 | 181 | P1_SDATA[16]# | AF-14 |
| 122 | P1_SADDOUT[13]# | AH-1 | 152 | P1_SDATA[33]# | AF-9 | 182 | P1_SDATA[29]# | AG-12 |
| 123 | P1_SADDOUT[03]# | AK-3 | 153 | P1_SDATA[40]# | AE-10 | 183 | P1_SCHECK[2]# | AH-12 |
| | | | | | | 184 | P1_SDATA[25]# | AL-13 |

**Table 2. AMD Athlon™ Processor System Bus NAND Tree Ordering (Continued)**

| # | Input Pin Name | Ball | # | Input Pin Name | Ball | # | Input Pin Name | Ball |
|---|---|---|---|---|---|---|---|---|
| 185 | P1_SDATA[24]# | AK-14 | 199 | P1_SDATAOUTCLK[0]# | AH-15 | 213 | P1_SADDIN[04]# | AL-18 |
| 186 | P1_SDATA[30]# | AJ-12 | 200 | P1_SDATA[06]# | AK-15 | 214 | P1_SADDIN[02]# | AG-17 |
| 187 | P1_SDATA[28]# | AJ-13 | 201 | P1_SCHECK[1]# | AL-15 | 215 | P1_SADDIN[09]# | AD-17 |
| 188 | P1_SDATA[03]# | AD-14 | 202 | P1_SDATA[04]# | AJ-15 | 216 | P1_SADDIN[10]# | AK-18 |
| 189 | P1_SDATA[01]# | AJ-14 | 203 | P1_SDATA[02]# | AE-16 | 217 | P1_CLKFWDRST | AL-19 |
| 190 | P1_SDATA[07]# | AE-13 | 204 | P1_SDATA[08]# | AL-16 | 218 | P1_SADDINCLK# | AJ-18 |
| 191 | P1_SDATA[00]# | AE-14 | 205 | P1_SDATA[12]# | AJ-16 | 219 | P1_SADDIN[03]# | AH-18 |
| 192 | P1_SDATA[05]# | AL-14 | 206 | P1_SDATA[14]# | AJ-17 | 220 | P1_SADDIN[14]# | AF-18 |
| 193 | P1_SDATA[09]# | AD-15 | 207 | P1_SDATA[13]# | AH-17 | 221 | P1_CONNECT | AJ-19 |
| 194 | P1_SCHECK[0]# | AG-14 | 208 | P1_SADDIN[11]# | AK-17 | 222 | P1_SADDIN[08]# | AG-18 |
| 195 | P1_SDATA[15]# | AH-14 | 209 | P1_SADDIN[06]# | AF-17 | 223 | P1_SADDIN[13]# | AE-18 |
| 196 | P1_SDATA[11]# | AF-15 | 210 | P1_SADDIN[07]# | AG-16 | 224 | P1_PROCRDY | AE-19 |
| 197 | P1_SDATA[10]# | AG-15 | 211 | P1_SADDIN[05]# | AL-17 | 225 | P1_SYSFILLVAL_L | AL-20 |
| 198 | P1_SDATAINCLK[0]# | AE-15 | 212 | P1_SDATAINVALID# | AE-17 | 226 | P1_SADDIN[12]# | AG-19 |

**Table 3: AMD-762™ System Controller AGP NAND Tree Ordering**

| Order | Input Pin Name | Ball | Order | Input Pin Name | Ball | Order | Input Pin Name | Ball |
|---|---|---|---|---|---|---|---|---|
| 1 | A_GNT# | AD-27 | 23 | SBSTB# | AA-29 | 45 | A_AD[14] | N-29 |
| 2 | SBA[1] | AB-25 | 24 | A_AD[24] | W-27 | 46 | A_AD[10] | M-29 |
| 3 | PIPE# | AE-29 | 25 | A_AD[31] | Y-29 | 47 | A_AD[12] | M-28 |
| 4 | WBF# | AC-26 | 26 | A_AD[18] | U-26 | 48 | A_AD[15] | N-27 |
| 5 | SBA[5] | AA-25 | 27 | A_AD[27] | V-27 | 49 | A_AD[07] | L-29 |
| 6 | ST[1] | AD-28 | 28 | A_AD[29] | W-29 | 50 | A_TRDY# | P-25 |
| 7 | A_REQ# | AD-29 | 29 | SBA[6] | Y-28 | 51 | A_AD[11] | M-26 |
| 8 | ST[0] | AC-27 | 30 | A_AD[25] | V-28 | 52 | A_AD[08] | L-28 |
| 9 | ST[2] | AC-28 | 31 | ADSTB[1] | U-27 | 53 | A_PAR | N-25 |
| 10 | SBA[7] | AA-26 | 32 | ADSTB[1]# | V-29 | 54 | ADSTB[0] | M-27 |
| 11 | A_AD[30] | Y-25 | 33 | A_AD[16] | T-27 | 55 | ADSTB[0]# | L-27 |
| 12 | SBA[3] | AB-27 | 34 | A_AD[23] | U-28 | 56 | A_AD[05] | K-29 |
| 13 | RBF# | AC-29 | 35 | A_AD[21] | U-29 | 57 | A_AD[03] | J-29 |
| 14 | A_AD[28] | Y-26 | 36 | A_AD[19] | T-29 | 58 | A_AD[09] | L-25 |
| 15 | CBE[3]# | V-25 | 37 | A_IRDY# | R-29 | 59 | A_AD[06] | K-27 |
| 16 | SBA[2] | AA-27 | 38 | A_FRAME# | R-26 | 60 | A_CBE[0]# | L-26 |
| 17 | SBA[0] | AB-29 | 39 | A_CBE[2]# | R-28 | 61 | A_AD[01] | J-28 |
| 18 | A_AD[26] | W-25 | 40 | A_AD[17] | R-27 | 62 | A_AD[13] | M-25 |
| 19 | A_AD[20] | U-25 | 41 | A_CBE[1]# | P-29 | 63 | A_AD[04] | K-25 |
| 20 | A_AD[22] | V-26 | 42 | A_DEVSEL# | P-27 | 64 | A_AD[02] | J-26 |
| 21 | SBA[4] | Y-27 | 43 | A_SERR# | P-28 | 65 | A_AD[00] | J-25 |
| 22 | SBSTB | AA-28 | 44 | A_STOP# | P-26 | 66 | PCICLK | F-28 |

**Table 4: AMD-762™ System Controller DDR NAND Tree Ordering**

| Order | Input Pin Name | Ball | Order | Input Pin Name | Ball | Order | Input Pin Name | Ball |
|---|---|---|---|---|---|---|---|---|
| 1 | MDAT[59] | E-29 | 35 | MDAT[49] | A-24 | 69 | DQS[4] | A-16 |
| 2 | MDAT[63] | E-27 | 36 | CS[0]# | D-22 | 70 | MDAT[36] | A-15 |
| 3 | DQS[7] | D-29 | 37 | WEA# | E-20 | 71 | MAB[00] | E-15 |
| 4 | CLKOUT[5] | F-26 | 38 | MDAT[48] | C-22 | 72 | MDAT[37] | B-15 |
| 5 | DCSTOP# | G-25 | 39 | MDAT[52] | A-23 | 73 | MDAT[33] | C-15 |
| 6 | MDAT[58] | E-28 | 40 | CS[2]# | D-21 | 74 | MDAT[32] | A-14 |
| 7 | MDAT[62] | C-29 | 41 | WEB# | C-20 | 75 | MECC[7] | C-14 |
| 8 | CLKOUT[2]# | F-25 | 42 | MDAT[47] | B-22 | 76 | MECC[6] | A-13 |
| 9 | MDAT[57] | C-27 | 43 | MAB[13] | E-18 | 77 | MECC[2] | B-13 |
| 10 | DM[7] | C-28 | 44 | MDAT[43] | A-22 | 78 | DQS[8] | A-12 |
| 11 | CLKOUT[2] | E-26 | 45 | RASA# | E-19 | 79 | MECC[1] | B-12 |
| 12 | CS[6]# | D-25 | 46 | MAA[14] | E-17 | 80 | DM[8] | C-13 |
| 13 | MDAT[56] | B-28 | 47 | RASB# | D-19 | 81 | MECC[5] | A-11 |
| 14 | CLKOUT[5]# | D-27 | 48 | MDAT[46] | C-21 | 82 | MAA[00] | E-14 |
| 15 | CS[5]# | E-24 | 49 | MDAT[42] | B-21 | 83 | MECC[3] | D-13 |
| 16 | MDAT[60] | B-27 | 50 | DQS[5] | A-21 | 84 | CLKOUT[0]# | E-13 |
| 17 | CS[1]# | E-23 | 51 | MDAT[41] | C-19 | 85 | MECC[0] | C-12 |
| 18 | MDAT[61] | C-26 | 52 | DM[5] | A-20 | 86 | MECC[4] | A-10 |
| 19 | MDAT[51] | A-27 | 53 | MAA[13] | D-18 | 87 | CLKOUT[3] | C-11 |
| 20 | MDAT[55] | C-25 | 54 | MDAT[44] | C-18 | 88 | MDAT[31] | B-10 |
| 21 | CS[7]# | E-25 | 55 | MDAT[45] | B-19 | 89 | MAA[01] | E-11 |
| 22 | DM[6] | C-24 | 56 | MDAT[40] | A-19 | 90 | MDAT[27] | C-10 |
| 23 | MDAT[50] | A-26 | 57 | MDAT[35] | B-18 | 91 | MDAT[30] | B-9 |
| 24 | CASA# | E-22 | 58 | MAA[10] | E-16 | 92 | CLKOUT[0] | D-12 |
| 25 | DQS[6] | B-25 | 59 | MAB[14] | C-17 | 93 | DM[3] | C-9 |
| 26 | CS[4]# | D-24 | 60 | DM[4] | B-16 | 94 | DQS[3] | A-8 |
| 27 | CASB# | E-21 | 61 | MAB[10] | D-16 | 95 | MAB[01] | D-10 |
| 28 | MDAT[54] | A-25 | 62 | MDAT[34] | C-16 | 96 | CLKOUT[3]# | E-12 |
| 29 | MDAT[53] | B-24 | 63 | MDAT[39] | A-18 | 97 | MDAT[26] | A-9 |
| 30 | CS[3]# | C-23 | 64 | MDAT[38] | A-17 | 98 | MAB[02] | E-10 |
| 31 | MAA[03] | C-8 | 65 | MDAT[16] | B-3 | 99 | MAA[11] | H-4 |
| 32 | MAA[02] | D-9 | 66 | MAA[05] | E-5 | 100 | CKEA | K-5 |
| 33 | MDAT[25] | A-7 | 67 | MAB[08] | D-4 | 101 | MDAT[02] | H-3 |
| 34 | MDAT[29] | B-7 | 68 | MAB[07] | F-5 | 102 | MDAT[07] | G-1 |

**Table 4: AMD-762™ System Controller DDR NAND Tree Ordering (Continued)**

| Order | Input Pin Name | Ball | Order | Input Pin Name | Ball | Order | Input Pin Name | Ball |
|---|---|---|---|---|---|---|---|---|
| 103 | MAB[03] | E-9 | 120 | MAB[09] | G-5 | 137 | MAA[12] | K-4 |
| 104 | MDAT[28] | C-7 | 121 | MDAT[11] | B-2 | 138 | CKEB | J-3 |
| 105 | MDAT[24] | A-6 | 122 | MDAT[15] | D-3 | 139 | MDAT[06] | H-2 |
| 106 | MAA[04] | D-7 | 123 | MDAT[10] | C-1 | 140 | CLKOUT[1]# | M-5 |
| 107 | MDAT[22] | A-5 | 124 | DQS[1] | E-3 | 141 | DQS[0] | H-1 |
| 108 | MAB[04] | E-8 | 125 | MAA[08] | E-4 | 142 | CLKOUT[4]# | L-5 |
| 109 | MDAT[23] | C-6 | 126 | MDAT[14] | D-2 | 143 | CLKOUT[1] | N-5 |
| 110 | MDAT[19] | B-6 | 127 | MAA[07] | F-3 | 144 | CLKOUT[4] | L-4 |
| 111 | MDAT[18] | A-4 | 128 | DM[1] | D-1 | 145 | MDAT[01] | K-3 |
| 112 | MAB[06] | D-6 | 129 | MAB[11] | H-5 | 146 | DM[0] | J-1 |
| 113 | DM[2] | B-4 | 130 | MDAT[13] | E-2 | 147 | MDAT[04] | L-3 |
| 114 | MAA[06] | E-7 | 131 | MAA[09] | G-4 | 148 | MDAT[00] | K-1 |
| 115 | DQS[2] | C-5 | 132 | MAB[12] | J-5 | 149 | MDAT[05] | K-2 |
| 116 | MDAT[21] | A-3 | 133 | MDAT[09] | E-1 | | | |
| 117 | MAB[05] | E-6 | 134 | MDAT[12] | F-1 | | | |
| 118 | MDAT[17] | C-4 | 135 | MDAT[08] | G-3 | | | |
| 119 | MDAT[20] | C-3 | 136 | MDAT[03] | G-2 | | | |

**Table 5: AMD-762™ System Controller PCI NAND Tree Ordering**

| Order | Input Pin Name | Ball | Order | Input Pin Name | Ball | Order | Input Pin Name | Ball |
|---|---|---|---|---|---|---|---|---|
| 1 | AD[31] | AA-27 | 22 | CBE[1]# | AF-22 | 43 | AD[05] | AF-25 |
| 2 | REQ[6]# | AH-17 | 23 | DEVSEL# | AF-21 | 44 | AD[13] | AG-27 |
| 3 | GNT[5]# | AJ-18 | 24 | AD[28] | AJ-23 | 45 | AD[03] | AE-25 |
| 4 | REQ[5]# | AH-18 | 25 | AD[26] | AH-23 | 46 | AD[01] | AF-26 |
| 5 | GNT[6]# | AG-17 | 26 | SERR# | AE-21 | 47 | AD[11] | AH-28 |
| 6 | REQ[4]# | AJ-19 | 27 | AD[24] | AG-23 | 48 | AD[00] | AE-26 |
| 7 | AD[29] | AE-16 | 28 | AD[19] | AJ-24 | 49 | SBGNT# | AD-25 |
| 8 | AD[27] | AF-17 | 29 | AD[12] | AF-23 | 50 | AD[09] | AG-28 |
| 9 | REQ[3]# | AH-19 | 30 | AD[18] | AJ-25 | 51 | WSC# | AC-25 |
| 10 | AD[25] | AE-17 | 31 | AD[14] | AE-22 | 52 | AD[06] | AF-27 |
| 11 | GNT[4]# | AG-18 | 32 | AD[22] | AH-24 | 53 | CBE[0]# | AG-29 |
| 12 | CBE[3]# | AF-18 | 33 | AD[20] | AG-24 | 54 | SBREQ# | AE-27 |
| 13 | AD[17] | AE-19 | 34 | AD[16] | AH-25 | 55 | AD[04] | AF-28 |
| 14 | REQ[2]# | AH-20 | 35 | TRDY# | AJ-26 | 56 | AD[02] | AF-29 |
| 15 | REQ[1]# | AH-21 | 36 | AD[08] | AF-24 | | | |
| 16 | AD[21] | AF-19 | 37 | STOP# | AH-26 | | | |
| 17 | REQ[0]# | AG-21 | 38 | AD[10] | AE-23 | | | |
| 18 | CBE[2]# | AF-20 | 39 | FRAME# | AG-25 | | | |
| 19 | AD[23] | AE-18 | 40 | PAR | AJ-27 | | | |
| 20 | AD[30] | AH-22 | 41 | AD[07] | AE-24 | | | |
| 21 | IRDY# | AE-20 | 42 | AD[15] | AH-27 | | | |

# 3.3 PLL Bypass Test Mode

PLL bypass test mode provides a method to clock the Northbridge core logic directly from an external source without the need for the internal PLLs of the AMD-762 system controller. This test mode is sometimes useful for motherboard debug and is required in the three-state and NAND tree test modes.

PLL bypass mode is entered by asserting the TEST# pin Low and pulling the AD[09] pin High. There are two clocking

options for PLL bypass mode as listed in Table 6 below. Because the AMD-762 system controller internal logic normally uses clocks that are 2x the SYSCLK input and 2x/4x the AGPCLK input, the PLL bypass mode requires that either 2x or 4x clocks be driven in this mode, but they can be driven at a much lower frequency for test purposes. Note that when operating in this mode, the minimum clock frequency most likely will be dictated by the surrounding logic, such as the DDR interface.

**Table 6. Clocking Options in PLL Bypass Test Mode**

| Mode | C/BE[1]# | SYSCLK | AGPCLK | Comments |
|---|---|---|---|---|
| Normal | 0 | 2x | 2x | PLLs bypassed, drives a 2x clock to internal divider, and resulting 1x clock to internal logic. |
| AGP-4x Testing | 1 | 2x | 4x | Same as above, except allows 4x clock to accommodate 4x AGP testing. |

The PLL reset function can be invoked by asserting a Low on the PCI IRDY# pin This procedure provides a synchronous reset for the clocking, but probably is not required when using this test mode for motherboard debug.

***Note:*** *AD[29] must be pulled Low when entering PLL bypass test mode to enable the PLL reset function capability.*

## 3.4 Clock Output Test Mode

The clock output test mode provides external visibility of the two PLLs used to generate the clocks for the processor/memory and AGP clock domains. In this test mode, the PLLs are running, and the output clocks are driven to GNT[6:5]# pins. System designers that intend to make use of this test feature should provide 0-ohm resistors on these pins to isolate the PCI peripherals when observing the clocks.

This test mode is entered by the Low assertion of the TEST# pin while pulling the PCI bus PAR pin Low. Additional pinstraps are then used to select the various clock outputs as illustrated in Table 7 on page 46.

**Table 7. Clock Output Test Mode Options**

| AD[07:05] | SYSCLK PLL Output GNT[5]# Pin | AD[14:12] | AGPCLK PLL Output GNT[6]# Pin |
|---|---|---|---|
| 000 | 1x SYSCLK clock after internal divide by two | 000 | 1x AGPCLK clock after internal divide by two |
| 001 | SYSCLK input | 001 | AGPCLK input |
| 010 | Reserved, undefined | 010 | Reserved, undefined |
| 011 | Reserved, undefined | 011 | Reserved, undefined |
| 100 | 1x SYSCLK output from SYSCLK PLL | 100 | 1x SYSCLK output from SYSCLK PLL |
| 101 | Reserved, undefined | 101 | Reserved, undefined |
| 110 | Reserved, undefined | 110 | Reserved, undefined |
| 111 | Reserved, undefined | 111 | Reserved, undefined |

# 4 Electrical Data

## 4.1 Absolute Ratings

The AMD-762™ system controller is not designed to operate beyond the parameters shown in Table 8.

***Note:*** *The absolute ratings in Table 8 and associated conditions must be adhered to in order to avoid damage to the AMD-762 system controller and motherboard. Systems using the AMD-762 system controller must be designed to ensure that the power supply and system logic board guarantee that these parameters are not violated. VIOLATION OF THE ABSOLUTE RATINGS WILL VOID THE PRODUCT WARRANTY.*

**Table 8. Absolute Ratings***

| Parameter | Minimum | Maximum | Comments |
|---|---|---|---|
| VDD_CORE, A_VDD, K7_VCORE | –0.5 V | 3.6 V | Core, PLL, DDR I/O, and AMD Athlon™ System Bus I/O supplies |
| VDD_AGP, VDD_PCI | –0.5 V | 4.6 V | AGP and PCI I/O supplies |
| REF_5V | –0.5 VI | 5.25 V | |
| $V_{PIN}$ DDR | –0.5 V | 4.6 V | |
| $V_{PIN}$ AMD Athlon System Bus | –0.5 V | 3.6 V | |
| $V_{PIN}$ PCI | –0.5 V | 5.25 V | |
| $V_{PIN}$ AGP | –0.5 V | 4.6 V | |
| $V_{PIN}$ Miscellaneous | –0.5 V | 4.6 V | |
| $T_{CASE}$ (Under Bias) | | 85 °C | |
| $T_{STORAGE}$ | -65 °C | 150 °C | |

**This table contains preliminary information, which is subject to change.*

# 4.2 Operating Ranges

The AMD-762 system controller is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in Table 9.

**Table 9. Operating Ranges***

| Parameter | Minimum | Typical | Maximum | Comments |
|---|---|---|---|---|
| REF_5V | 4.75 | 5.0 | 5.25 | For PCI 5-V tolerance |
| VDD_CORE, A_VDD | 2.375 V | 2.5 V | 2.625 V | Also includes DDR I/Os |
| K7_VCORE | 1.50 V | 1.6 V | 1.70 V | AMD Athlon™ system bus I/O VDD |
| VDD_AGP | 1.425 V | 1.5 V | 1.575 V | 1x/2x/4x modes |
| VDD_AGP | 3.135 V | 3.3 V | 3.465 V | 1x/2x modes only |
| VDD_PCI | 3.135 V | 3.3 V | 3.465 V | 3.3-V signalling environment only |
| $T_{CASE}$ | | | 85 °C | |

**This table contains preliminary information, which is subject to change. The voltage applied to $V_{DD}$ should never exceed the voltage applied to REF_5V.*

# 4.3 DC Characteristics

Table 11 shows the DC characteristics for the AMD-762 system controller. Table 12 on page 50 shows DC characteristics for the PCI I/Os. Table 13 on page 51 shows DC characteristics for AGP I/Os in 1x mode. Table 14 on page 52 shows DC characteristics for AGP I/Os in 2x and 4x modes.

**Table 10. DC Characteristics (IDD)***

| Symbol | Parameter Description | Preliminary Data | | Comments |
|---|---|---|---|---|
| | | Min | Max | |
| $I_{DD1}$ | VDD_CORE (2.5 V) Dynamic | 1.9 A | 2.25 A | 133 MHz |
| $I_{DD2}$ | VDD_PCI (3.3 V) Dynamic | 80 mA | 140 mA | 66-MHz PCI |
| $I_{DD3}$ | VDD_AGP (1.5 V/3.3 V) Dynamic | 20 mA | 40 mA | |
| $I_{DD4}$ | A_VDD (2.5 V) Dynamic | 5 mA | 10 mA | |
| $I_{DD5}$ | K7_VCORE Dynamic | 250 mA | 500 mA | |

**This table contains preliminary information, which is subject to change.*

**Table 11. DC Characteristics for DDR Interface***

| Symbol | Parameter Description | Preliminary Data | | Comments |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{IL}$ | Input Low Voltage | –300 mV | $V_{REF}$ – 180 mV | Data, DQS pins |
| $V_{IH}$ | Input High Voltage | $V_{REF}$ + 180 mV | VDD_CORE + 300 mV | Data, DQS pins |
| $V_{OL}$ | Output Low Voltage | | 0.15 * VDD_CORE | |
| $V_{OH}$ | Output High Voltage | 0.85 * VDD_CORE | | |
| $V_{REF}$ | DC Input Reference Voltage | 1.15 V | 1.35 V | |
| $I_{LI}$ | Input Leakage Current | –10 µA | 10 µA | $0 < V_{IN} <$ VDD_CORE |
| $I_{LO}$ | Three-state Leakage Current | –100 µA | 100 µA | |
| $C_{IN}$ | Input Capacitance | 4 pF | 12 pF | |

** This table contains preliminary information, which is subject to change.*

### 4.3.1 Voltage Sequencing Requirements

The preferred sequence of voltages in the AMD-762 system controller is from highest (5 VDC on the REF_5V pin) to the lowest. To accommodate the Suspend to RAM feature, it is expected that the AMD-762 system controller's 2.5-VDC core must be powered from the 5-VDC standby voltage from the standard ATX power supply and therefore is powered up before the 3.3 VDC, and the AMD-762 system controller can tolerate this for up to one second.

It is also assumed that the VREF voltages are always powered from the associated power supply voltage and will therefore lag behind that voltage. For example, DDR_VREF is powered off the 2.5 VDC (VDD_CORE), thus comes up after the 2.5 VDC. The same should apply to AGP_VREF, Px_VREF, etc.

**Table 12. DC Characteristics for PCI I/Os***

| Symbol | Parameter Description | Condition | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | 0.5 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{IL}$ | Input Low Voltage | | –0.5 | 0.3 $V_{CC}$ | V | |
| $I_{IL}$ | Input Leakage Current | $0 < V_{IN} < V_{CC}$ | | ±10 | µA | 1 |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = –500 µA | 0.9 $V_{CC}$ | | V | |
| $V_{OL}$ | Output Low Voltage | $I_{OUT}$ = 1500 µA | | 0.1 $V_{CC}$ | V | |
| $C_{IN}$ | Input Pin Capacitance | | | 10 | pF | 2 |

***Notes:***

** This table contains preliminary information, which is subject to change.*

*1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with three-state outputs.*

*2. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK) with an exception granted to motherboard-only devices up to 16 pF in order to accommodate PGA packaging. Generally, this means that components for expansion boards need to use alternatives to ceramic PGA packaging—that is, PQFP, SGA, etc.*

**Table 13. AGP 1x Mode DC Specifications***

| DC Specifications for AGP 1x Signalling at 3.3 Volts | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter Description** | **Condition** | **Min** | **Max** | **Units** | **Notes** |
| $V_{IH}$ | Input High Voltage | | 0.5 $V_{DDQ}$ | $V_{DDQ}$ + 0.5 | V | |
| $V_{IL}$ | Input Low Voltage | | –0.5 | 0.3 $V_{DDQ}$ | V | |
| $I_{IL}$ | Input Leakage Current | $0 < V_{IN} < V_{DDQ}$ | | ±10 | µA | |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = –500 µA | 0.9 $V_{DDQ}$ | | V | |
| $V_{OL}$ | Output Low Voltage | $I_{OUT}$ = 1500 µA | | 0.1 $V_{DDQ}$ | V | |
| $C_{IN}$ | Input Pin Capacitance | | | 8 | pF | 1 |
| **DC Specifications for AGP 1x Signalling at 1.5 Volts** | | | | | | |
| **Symbol** | **Parameter Description** | **Condition** | **Min** | **Max** | **Units** | **Notes** |
| $V_{IH}$ | Input High Voltage | | 0.6 $V_{DDQ}$ | $V_{DDQ}$ + 0.5 | V | |
| $V_{IL}$ | Input Low Voltage | | –0.5 | 0.4 $V_{DDQ}$ | V | |
| $I_{IL}$ | Input Leakage Current | $0 < V_{IN} < V_{DDQ}$ | | ±10 | µA | |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = –200 µA | 0.85 $V_{DDQ}$ | | V | |
| $V_{OL}$ | Output Low Voltage | $I_{OUT}$ = 1000 µA | | 0.15 $V_{DDQ}$ | V | |
| $C_{IN}$ | Input Pin Capacitance | | | 8 | pF | 1 |

***Notes:***

**This table contains preliminary information, which is subject to change.*

*1. Absolute maximum pin capacitance for an AGP-compliant component input is 8 pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF in order to accommodate PGA packaging. Generally, this means that components for expansion boards need to use alternatives to ceramic PGA packaging—that is, PQFP, BGA, etc.*

**Table 14. AGP 2x and 4x Mode DC Specifications***

| **DC Specifications for 2x Mode Only at 3.3-Volt Signalling** | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter Description** | **Condition** | **Min** | **Max** | **Units** | **Notes** |
| $V_{REF}$ | Input Reference Voltage | | 0.39 $V_{DDQ}$ | 0.41 $V_{DDQ}$ | V | 1, 2 |
| $I_{REF}$ | $V_{REF}$ Pin Input Current | $0 < V_{IN} < V_{DDQ}$ | | ±10 | µA | 2 |
| $C_{IN}$ | Input Pin Capacitance | | | 8 | pF | 3 |
| $\Delta C_{IN}$ | Strobe to Data Pin Capacitance Delta | | –1 | 2 | pF | 3, 4 |
| **DC Specifications for 2x or 4x Mode at 1.5-Volt Signalling** | | | | | | |
| **Symbol** | **Parameter Description** | **Condition** | **Min** | **Max** | **Units** | **Notes** |
| $V_{REF}$ | Input Reference Voltage | | 0.48 $V_{DDQ}$ | 0.52 $V_{DDQ}$ | V | 1, 2 |
| $I_{REF}$ | $V_{REF}$ Pin Input Current | $0 < V_{IN} < V_{DDQ}$ | | ±5 | µA | 2 |
| $C_{IN}$ | Input Pin Capacitance | | | 8 | pF | 3 |
| $\Delta C_{IN}$ | Strobe to Data Pin Capacitance Delta | 2x Mode<br>4x Mode | –1<br>–1 | 2<br>1 | pF | 3, 4 |

***Notes:***

**This table contains preliminary information, which is subject to change.*

*1. AGP allows differential input receivers to achieve the tighter timing tolerances needed for 133 Mbytes/s. Nominal value of $V_{REF}$ is 0.4 $V_{DDQ}$ for 3.3-V signalling and 0.5-$V_{DDQ}$ for 1.5-V signalling. $V_{REF}$ can be designed with 2% resistors to achieve the specified minimum and maximum values. The value of $V_{REF}$ is intended to specify the center point of the $V_{IL}/V_{IH}$ range. For the 3.3-V signalling case, at nominal $V_{DDQ}$ (3.3 V), $V_{REF}$ is 1.32 V ± 2.5%. A single input interface buffer can be designed to meet the $V_{IL}/V_{IH}$ levels of both the AGP and PCI specifications. As in other AGP specifications, note that the $V_{DDQ}$ references the I/O ring supply voltage and not the component supply.*

*2. Although a differential input buffer is not a required implementation, it is recommended especially at higher data transfer rates where there is less timing margin. All designs regardless of implementation style must meet all other specifications. Component designs requiring a reference are required to adhere to the $V_{REF}$ and $I_{REF}$ specifications and to facilitate a common reference circuit. (A common reference circuit is not applicable to add-in card designs, because $V_{REF}$ is not supplied via the connector.)*

*3. Capacitance specifications refer only to pin capacitance on the AGP-compliant components used on the AGP interface.*

*4. Delta $C_{IN}$ is required to restrict timing variations resulting from differences in input pin capacitance between the strobe and associated data pins. This delta only applies between signal groups and their associated strobes: AD_STB1, AD_STB1#=>AD[31::16], and C/BE[3::2]; AD_STB0, AD_STB0#=>AD[15::00], and C/BE[1::0]#; SB_STB, SB_STB#=>SBA[7::0]. (Complementary strobes apply to 4x mode only.)*

# 4.4 Power Dissipation

Table 15 shows typical and maximum power dissipation of the AMD-762 system controller during normal and reduced power states. The measurements are taken with the $V_{DD}$ shown.

**Table 15. Typical and Maximum Power Dissipation***

| Supply | Normal Operation | | Low-Power States | |
|---|---|---|---|---|
| | Typical | Maximum | ACPI S1 State | ACPI S3 State |
| VDD_CORE | | | | |
| *100 MHz* | 3 W | 4.5 W | 125 mW | 50 mW |
| *133 MHz* | 4 W | 6 W | 165 mW | 65 mW |

**This table contains preliminary information, which is subject to change.*

# 4.5 Switching Characteristics and Requirements

The AMD-762 system controller signal switching characteristics and requirements are presented in Tables 16 through 27. All signal timings are based on the following conditions:

- The target signals are input or output signals that are switching from logical 0 to 1, or from logical 1 to 0.
- Measurements are taken from the time the reference signal (AGPCLK, PCICLK, CLKOUT, SYSCLK, or RESET#) passes through 1.5 V to the time the target signal passes through 1.5 V.
- Parameters are within the range of those listed in "Operating Ranges" on page 48.

## 4.5.1 Clock Switching Requirements

Table 16 contains the switching characteristics of the SYSCLK input to the AMD-762 system controller for 100-MHz processor bus operation. These timings are all measured with respect to the voltage levels indicated by Figure 12 on page 54. Clock skew requirements are shown in Figure 14 on page 56. Table 17 on page 55 contains the switching characteristics of the AGPCLK input for 66-MHz PCI bus operation. Table 18 on page 55 contains the switching characteristics of the PCICLK input for 33-MHz PCI bus operation. These timings are all

measured with respect to the voltage levels indicated by Figure 13 on page 55.

The clock period stability specifies the variance (jitter) allowed between successive periods of the clock inputs measured at appropriate reference voltage. This parameter must be considered as one of the elements of clock skew between the AMD-762 system controller and the system logic.

**Table 16. SYSCLK Switching Requirements**

| Symbol | Parameter Description | Preliminary Data | | Figure | Comments |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $1/t_2$ | Frequency | | 133 MHz | 12 | |
| $t_3/t_2$ x 100 | SYSCLK Duty Cycle | 45% | 55% | 12 | 1.15-V reference |
| $t_4$ | SYSCLK Falling Edge Slew Rate | TBD | 1.0 V/ns | 12 | |
| $t_5$ | SYSCLK Rising Edge Slew Rate | TBD | 1.0 V/ns | 12 | |
| | SYSCLK Period Stability<br>*100 MHz*<br>*133 MHz* | | <br>± 200 ps<br>± 150 ps | | 1.15-V reference |

**This table contains preliminary information, which is subject to change.*

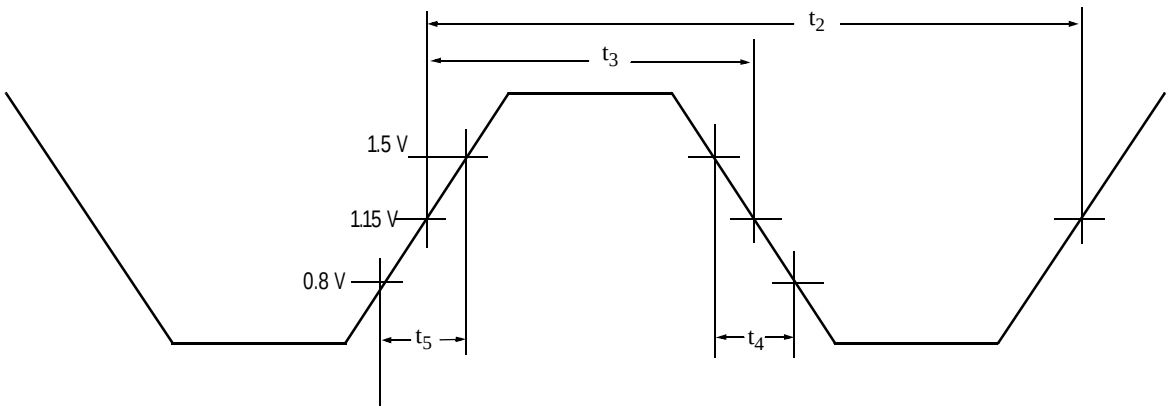



**Figure 12. SYSCLK Waveform**

**Table 17. AGPCLK Switching Requirements for 66-MHz Bus Operation**

| Symbol | Parameter Description | Preliminary Data | | Figure | Comments |
|---|---|---|---|---|---|
| | | Min | Max | | |
| 1/t1 | Frequency | | 66 MHz | 13 | |
| $t_2$ | AGPCLK High Time | 6.0 ns | | 13 | |
| $t_3$ | AGPCLK Low Time | 6.0 ns | | 13 | |
| | AGPCLK Fall Time | 0.15 ns | 2 ns | | |
| | AGPCLK Rise Time | 0.15 ns | 2 ns | | |
| $t_{SKEW}$ | SYSCLK to AGPCLK Skew | –500 ps | 500 ps | 14 | Rising to rising edges |
| | AGPCLK Period Stability | | ± 300 ps | | 1.5-V reference |

**This table contains preliminary information, which is subject to change.*

**Table 18. PCICLK Switching Requirements for 33-MHz PCI Bus***

| Symbol | Parameter Description | Preliminary Data | | Figure | Comments |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_1$ | PCICLK Cycle | 30 ns | ∞ | 13 | |
| $t_2$ | PCICLK High Time | 11.0 ns | | 13 | |
| $t_3$ | PCICLK Low Time | 11.0 ns | | 13 | |
| | PCICLK Fall Time | 1 V/ns | 2 V/ns | | |
| | PCICLK Rise Time | 1 V/ns | 2 V/ns | | |
| | PCICLK Period Stability | | ± 300 ps | | 1.5-V reference |

**This table contains preliminary information, which is subject to change.*

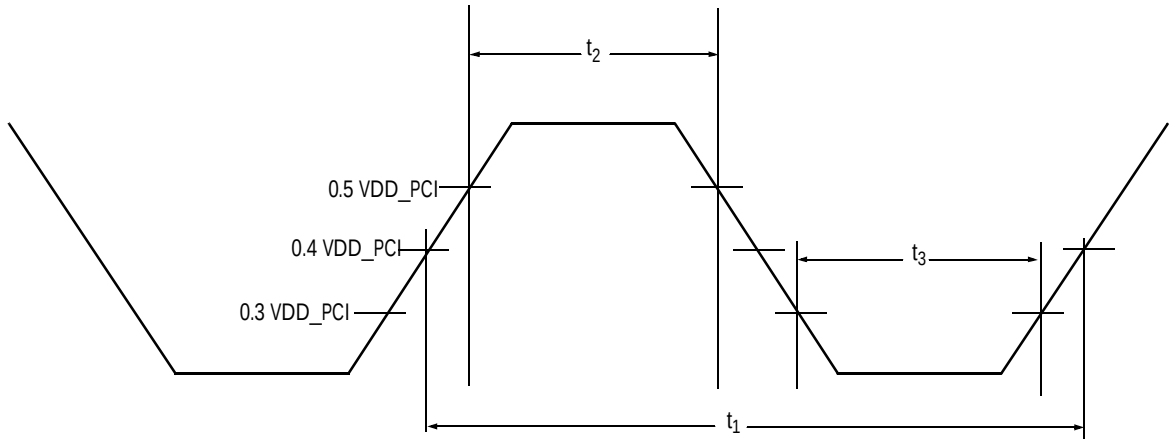



**Figure 13. AGPCLK and PCICLK Waveform**

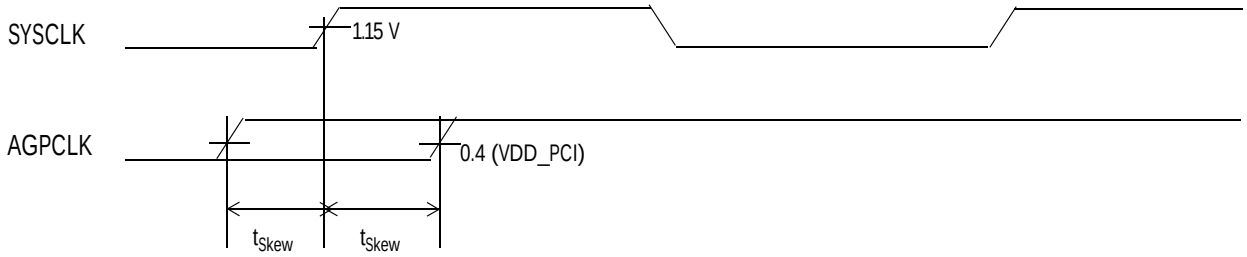



**Figure 14. Clock Skew Requirements**

## 4.5.2 DDR Interface Timing

Table 19 and Table 20 show the DDR SDRAM interface timings. Figure 15 on page 57 shows DDR clock specifications.

The AMD-762 system controller's DDR DRAM interface complies to JEDEC specifications for 100/133-MHz device timing.

**Table 19. DDR Clock Switching Characteristics for 100-MHz DDR Operation**

| Symbol | Parameter Description | Preliminary Data | | Figure | Comments |
|---|---|---|---|---|---|
| | | Min | Max | | |
| | Frequency | | 100 MHz | | |
| $t_1$ | CLKOUTH/L[5:0] High Time | 4.75 ns | | 15 | |
| $t_2$ | CLKOUTH/L[5:0] Low Time | 4.75 ns | | 15 | |
| | CLKOUTH/L[5:0] Fall Time | 0.86 ns | 1.30 ns | | Drive strength: P = 3, N = 2; $P_{SLEW}$ = 5, $N_{SLEW}$ = 5 |
| | CLKOUTH/L[5:0] Rise Time | 0.86 ns | 1.30 ns | | |
| | CLKOUTH/L[5:0] Period Stability | | ± 2% | | |
| | CLKOUTH/L[5:0] Skew | 0 | 0.12 ns | | Relative to all other CLKOUTH/L pairs |

**This table contains preliminary information, which is subject to change.*

**Table 20. DDR Clock Switching Characteristics for 133-MHz DDR Operation**

| Symbol | Parameter Description | Preliminary Data | | Figure | Comments |
|---|---|---|---|---|---|
| | | Min | Max | | |
| | Frequency | | 133 MHz | | |
| $t_1$ | CLKOUTH/L[5:0] High Time | 3.625 ns | | 15 | |
| $t_2$ | CLKOUTH/L[5:0] Low Time | 3.625 ns | | 15 | |
| | CLKOUTH/L[5:0] Fall Time | 0.86 ns | 1.30 ns | | Drive strength: P = 3, N = 2; $P_{SLEW}$ = 5, $N_{SLEW}$ = 5 |
| | CLKOUTH/L[5:0] Rise Time | 0.86 ns | 1.30 ns | | |
| | CLKOUTH/L[5:0] Period Stability | | ± 2% | | |
| | CLKOUTH/L[5:0] Skew | 0 | 0.12 ns | | Relative to all other CLKOUTH/L pairs |

**This table contains preliminary information, which is subject to change.*

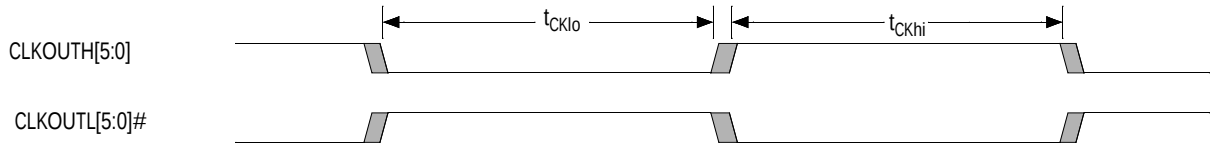



**Figure 15. DDR Clock Specifications**

Table 21 shows the AMD-762 system controller preliminary timing information.

**Table 21. AMD-762™ System Controller Preliminary DDR Timing Information***

| Symbol | Parameter Description | Min | Max | Unit | Figure |
|---|---|---|---|---|---|
| $V_{IL}$ (AC) | AC Input Low Voltage | | $V_{REF}$ – 0.35 | V | |
| $V_{IH}$ (AC) | AC Input High Voltage | $V_{REF}$ + 0.35 | | V | |
| $t_{ADsu}$ | ADDR/CMD Setup to CK | 7.5 | 8.5 | ns | Figure 17 on page 59 |
| $t_{ADhld}$ | ADDR/CMD Hold from CK | 2.5 | 3.6 | ns | |
| $t_{DQsu}$ | DQ/DM Setup to DQS | 2.4 | 2.5 | ns | |
| $t_{DQhld}$ | DQ/DM Hold from DQS | 2.4 | 2.6 | ns | |
| $t_{WPREsu}$ | Write Preamble Setup | 2.8 | 3.4 | ns | |
| $t_{WPREhld}$ | Write Preamble Hold | 5.1 | 5.8 | ns | |
| $t_{WpostA}$ | Write Postamble | 4.5 | 5.0 | ns | |
| $t_{DSsu}$ | DQS Falling Edge to Next CK Rising Edge | 5.2 | 5.6 | ns | |
| $t_{DQSdly}$ | Write Command to First DQS Latching Transition | 9.0 | 9.9 | ns | |

***Notes:***

* *This table contains preliminary information, which is subject to change. Timing reference load (applied to all chip-level outputs) used for all information contained herein is a 30-pF capacitance. A CAS latency of 2.5 is used unless otherwise indicated.*

## DDR Write Timing

Figure 16 on page 58 shows a DDR interface output block diagram. Figure 17 on page 59 shows basic AC timing for DDR write cycles.

***Note:*** *All information shown under DDR Write Timing is preliminary.*

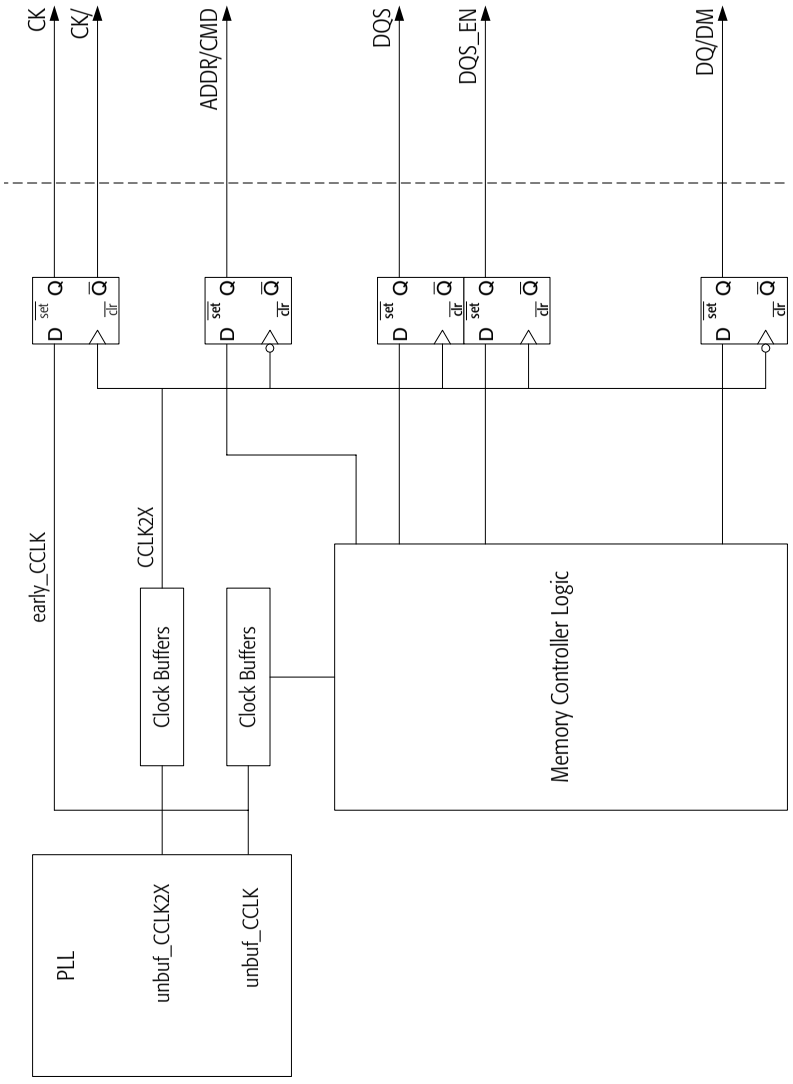
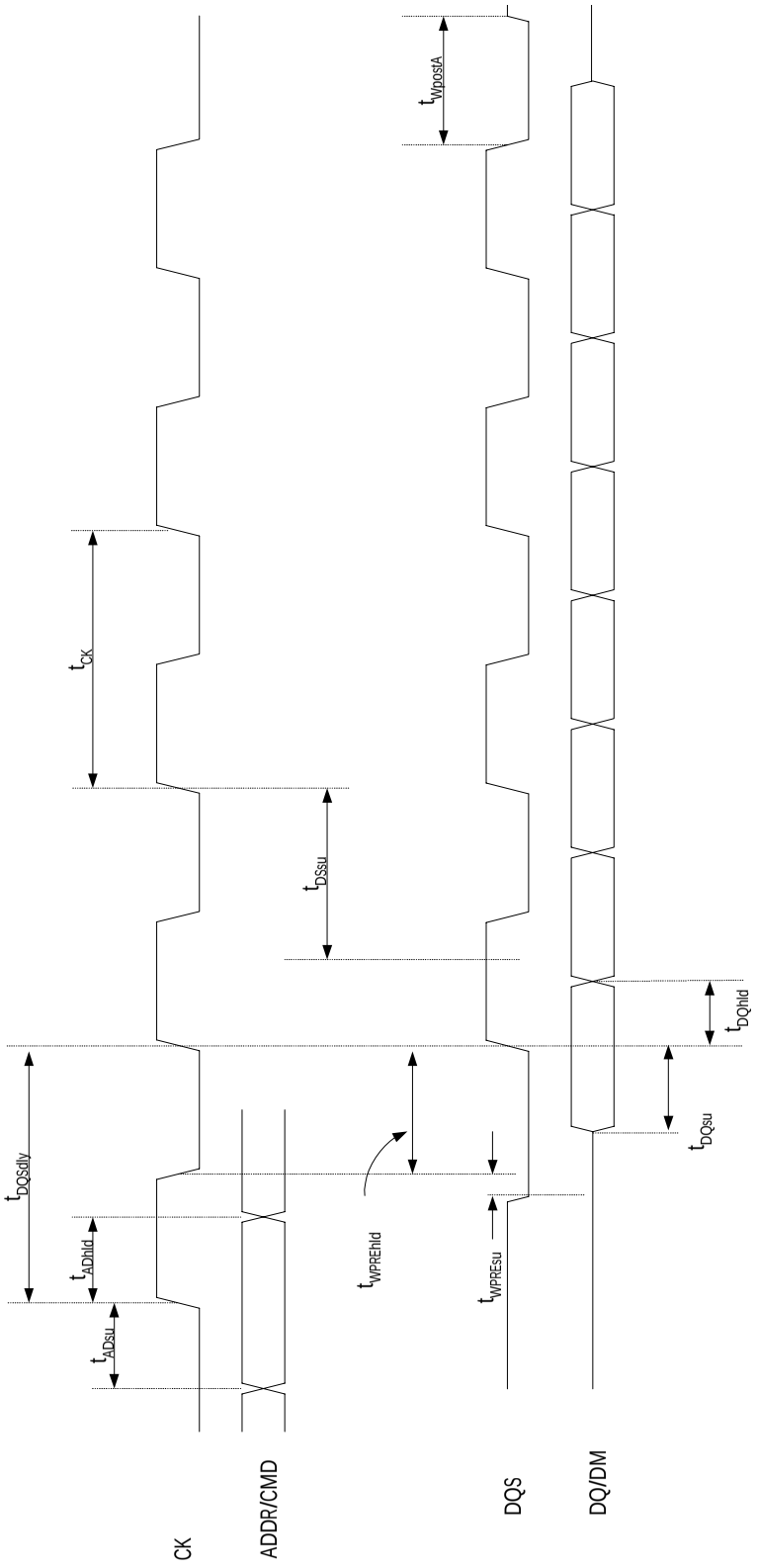



**Figure 16. AMD-762™ System Controller DDR Interface Outputs Conceptual Block Diagram**




*Note: Timing parameter symbols defined at controller interface, not at memory device interface.*

**Figure 17. Address/Command and Memory Write Cycle Timing**

## DDR Read Timing

***Note:*** *All information shown under DDR Read Timing is preliminary. Figure 18 shows a block diagram of the AMD-762 system controller DDR interface inputs, and Figure 19 on page 61 shows memory read cycle timing.*

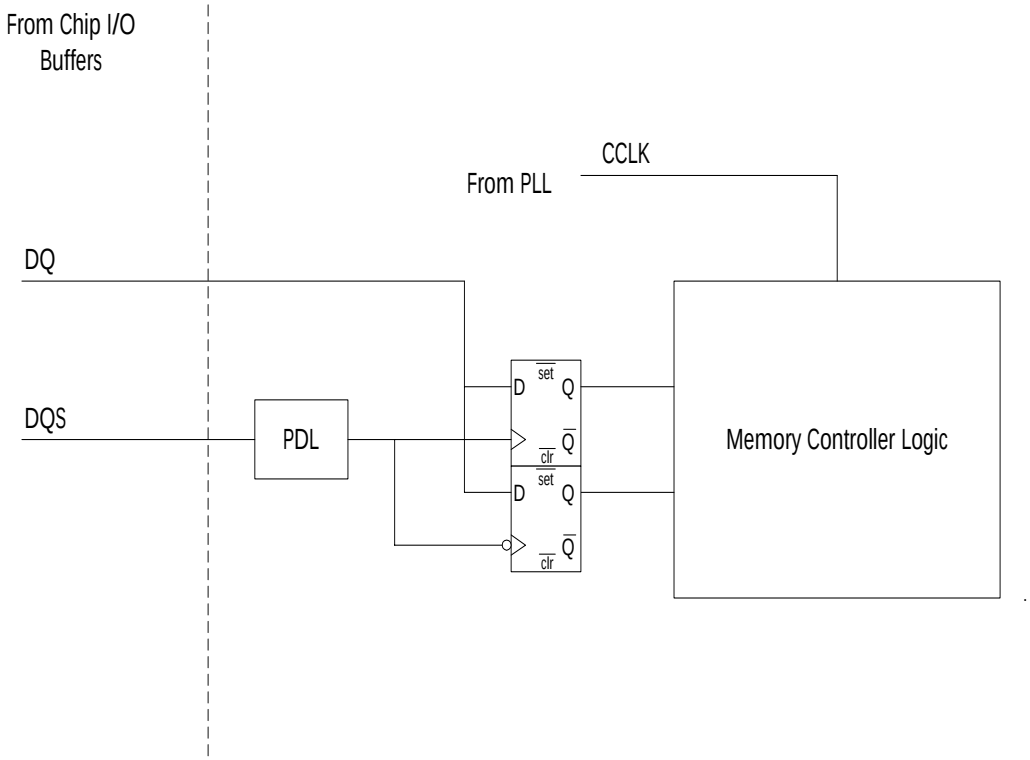
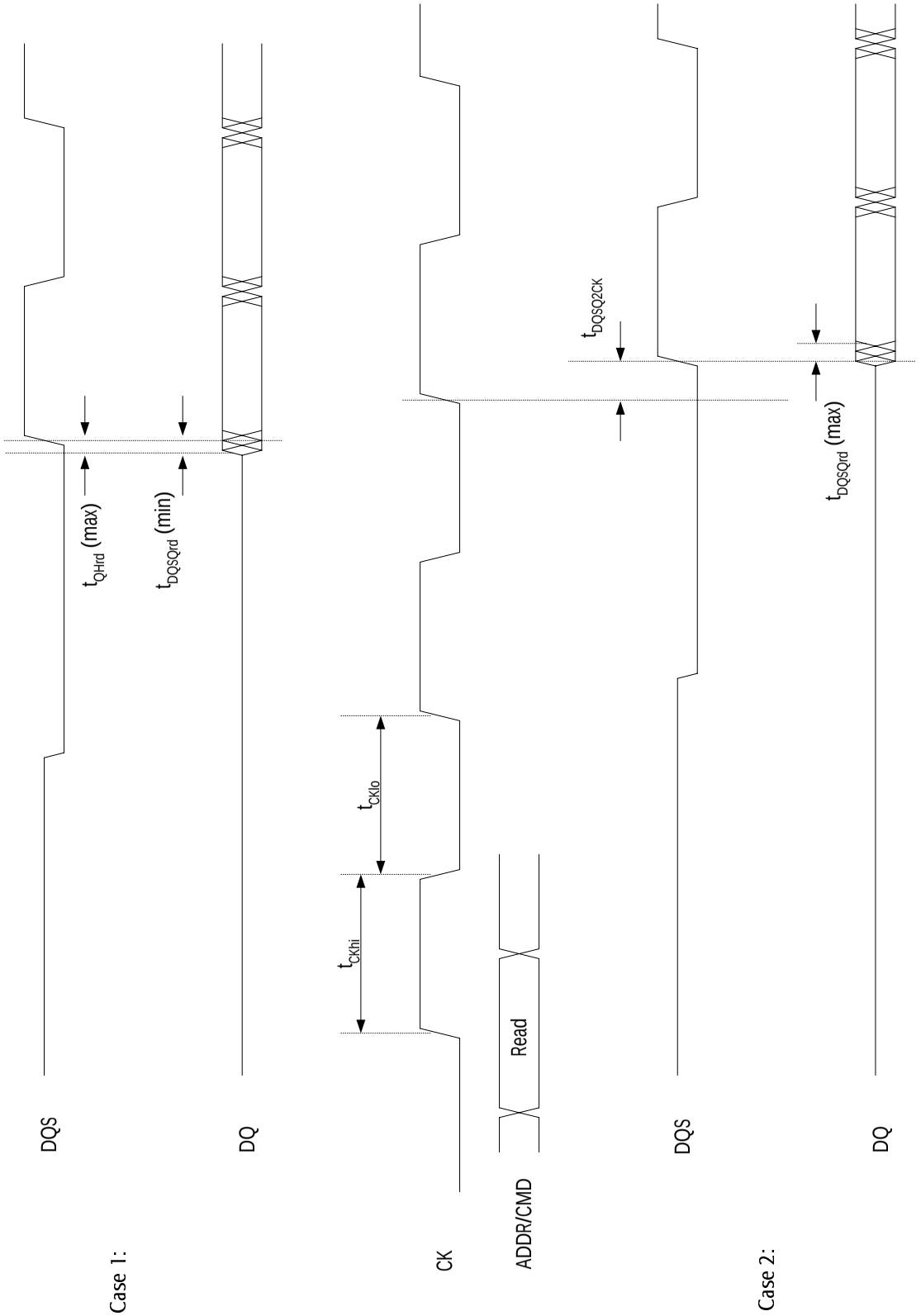



**Figure 18. AMD-762™ System Controller DDR Interface Inputs Conceptual Block Diagram**




*Note: Timing parameter symbols defined at controller interface, not at memory device interface (CAS latency = 2 shown unregistered).*

**Figure 19. Memory Read Cycle Timing**

## 4.5.3 AGP/PCI Signals

**Valid Delay, Float, Setup, and Hold Timings**

The valid delay and float timings for output signals during functional operation are relative to the rising edge of the given clock. The maximum valid delay timings are provided to allow a system designer to determine if setup times can be met. Likewise, the minimum valid delay timings are used to analyze hold times.

The setup and hold time requirements for the AMD-762 system controller input signals presented here must be met by any device that interfaces with it to assure the proper operation of the AMD-762 system controller.

Figure 20 shows the relationship between the rising clock edge and setup, hold, and valid data timings.

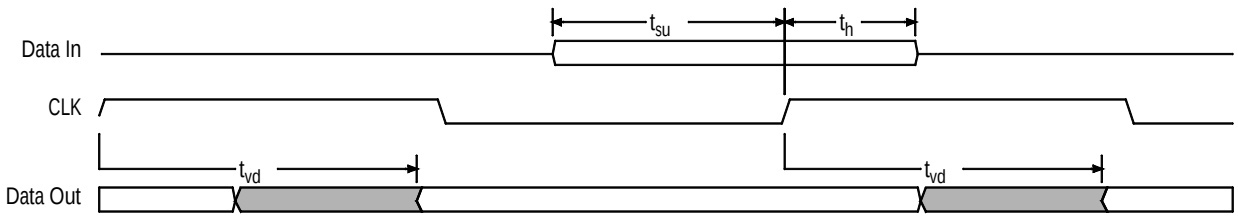



**Figure 20. Setup, Hold, and Valid Delay Timings**

**AGP Interface Timing**

The 4x AGP interface of the AMD-762 system controller can operate in three modes—1x, 2x, and 4x, and complies to the AGP specification parameters.

The timings for the 1x mode, shown in Table 22 on page 63, are relative to AGPCLK. The timings for the 2x mode, shown in Table 23 on page 64, are relative to the respective strobe.

The timings for the 4x mode, shown in Table 24 on page 65, apply only to the inner loop 4x clock mode signals (AD, C/BE#, and SBA).

Figure 21 on page 65 shows an AGP 2x strobe/data turnaround timing diagram. Figure 22 on page 66 and Figure 23 on page 66 show AGP 2x and 4x timing diagrams, respectively. Figure 24 on page 67 shows an AGP 4x strobe/data turnaround timing diagram.

**Table 22. AGP 1x Mode Timings***

| Symbol | Parameter Description | Preliminary Data | | Figure | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| **Input Signal Requirements** | | | | | |
| $t_{su}$ | A_AD[31:0] Setup Time | 5.5 ns | | 20 | 1 |
| | Setup time for A_FRAME#A_STOP# A_TRDY#A_DEVSEL# A_IRDY#A_C/BE[3:0]# A_REQ# ADSTB[1:0] SBA[7:0] SBSTB RBF#WBF# | 6 ns | | 20 | 1 |
| $t_h$ | A_AD[31:0] Hold Time | 0 ns | | 20 | 1 |
| | Hold time for A_FRAME#A_STOP# A_TRDY#A_DEVSEL# A_IRDY#A_C/BE[3:0]# A_REQ# ADSTB[1:0] SBA[7:0] SBSTB RBF#WBF# | 0 ns | | 20 | 1 |
| **Output Signal Characteristics** | | | | | |
| $t_{vd}$ | A_AD[31:0] Valid Delay | 1 ns | 6.0 ns | 20 | 1 |
| | A_C/BE[3:0]# Valid Delay | 1 ns | 5.5 ns | 20 | 1 |
| | Valid Delay for A_FRAME#A_STOP# A_TRDY#A_DEVSEL# A_IRDY# A_GNT# | 1 ns | 5.5 ns | 20 | 1 |
| $t_{fd}$ | Float Delay (Active to Float) | 1 ns | 14 ns | | |
| $t_{on}$ | Turn-on Delay (Float to Active) | 1 ns | 6 ns | | |

***Note:***

** This table contains preliminary information, which is subject to change.*

*1. These signals are specified with a 10-pF load.*

**Table 23. AGP 2x Mode Timings***

| Symbol | Parameter Description | Preliminary Data | | Figure | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| **Input Signal Requirements** | | | | | |
| $t_{RSsu}$ | Receive Strobe Setup Time to AGPCLK | 6 ns | | | |
| $t_{RSH}$ | Receive Strobe Hold Time from AGPCLK | 1 ns | | | |
| $t_{Dsu}$ | Data Setup Time Relative to Strobe | 1 ns | | 22 | 1 |
| $t_{Dh}$ | Data Hold Time Relative to Strobe | 1 ns | | 22 | 1 |
| **Output Signal Characteristics** | | | | | |
| $t_{TSf}$ | AGPCLK to Transmit Strobe Falling | 2 ns | 12 ns | 22 | |
| $t_{TSr}$ | AGPCLK to Transmit Strobe Rising | | 20 ns | 22 | |
| $t_{DVa}$ | Data Valid Delay after Strobe | 1.9 ns | | 22 | 1 |
| $t_{DVb}$ | Data Valid before Strobe | 1.7 ns | | 22 | 1 |
| $t_{fd}$ | Float Delay (Active to Float) | 1 ns | 12 ns | 21 | |
| $t_{OFFS}$ | Strobe Rising Edge to Strobe Float Delay | 6 ns | 10 ns | 21 | |
| $t_{oNd}$ | Turn-on Delay (Float to Active) | –1 ns | 9 ns | 21 | |

***Note:***

** This table contains preliminary information, which is subject to change.*

*1. These signals are specified with a 10-pF load.*

**Table 24. AGP 4x Mode Timings***

| Symbol | Parameter Description | Preliminary Data | | Figure | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| **Transmitter Output Signals** | | | | | |
| $t_{TSf}$ | CLK to First Transmit Strobe Transition | 1.9 ns | 8 ns | 23 | |
| $t_{TSr}$ | CLK to Fourth Transmit Strobe Transition | | 20 ns | 23 | |
| $t_{Dvb}$ | Data Valid Before Strobe | –0.95 ns | | 23 | |
| $t_{Dva}$ | Data Valid After Strobe | 1.15 ns | | 23 | |
| $t_{ONd}$ | Float to Active Delay | –1 ns | 7 ns | 24 | |
| $t_{OFFd}$ | Active to Float Delay | 1 ns | 14 ns | 24 | |
| $t_{ONS}$ | Strobe Active to First Strobe Edge Setup | 4 ns | 9 ns | 24 | |
| $t_{OFFS}$ | Last Strobe Edge to Strobe Float Delay | 4 ns | 9 ns | 24 | |
| **Receiver Input Signals** | | | | | |
| $t_{RSsu}$ | Receive Strobe Setup Time to CLK | 6 ns | | | 1 |
| $t_{RSh}$ | Receive Strobe Hold Time from CLK | 0.5 ns | | | 1 |
| $t_{Dsu}$ | Data to Strobe Setup Time | 0.40 ns | | 23 | |
| $t_{Dhld}$ | Strobe to Data Hold Time | 0.70 ns | | 23 | |

***Note:***
** This table contains preliminary information, which is subject to change.*
*1. These specifications refer to the setup and hold times for the strobe set started in the previous cycle.*

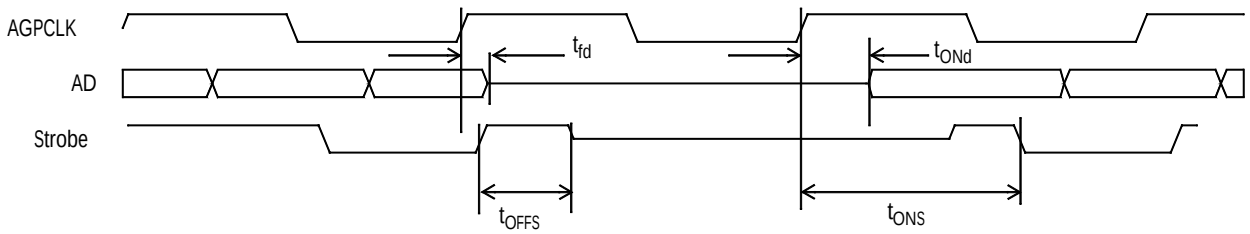



**Figure 21. AGP 2x Strobe/Data Turnaround Timings**

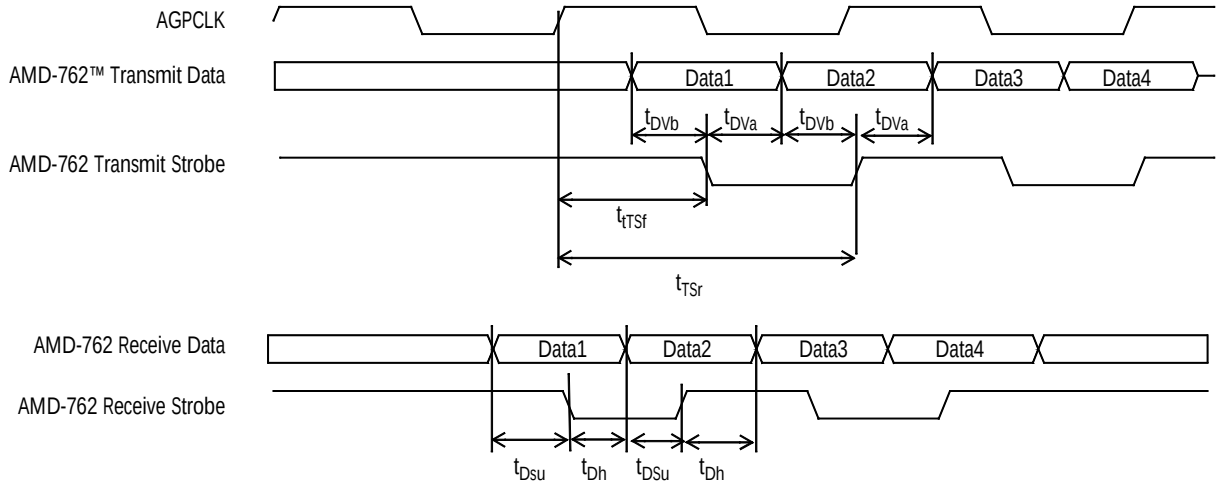



**Figure 22. AGP 2x Timing Diagram**

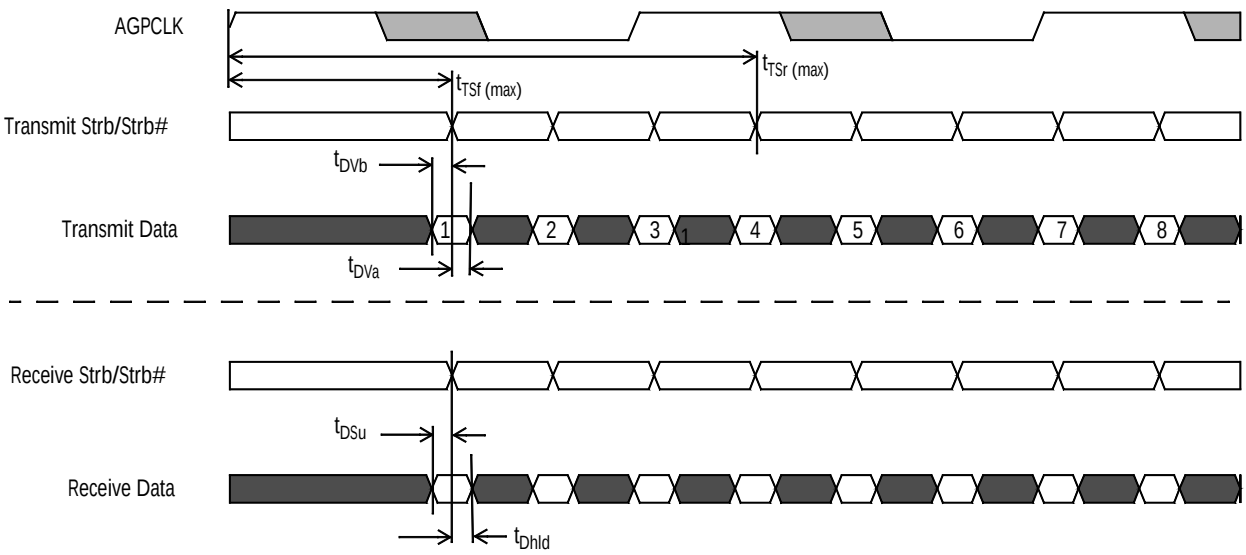



**Figure 23. AGP 4x Timing Diagram**

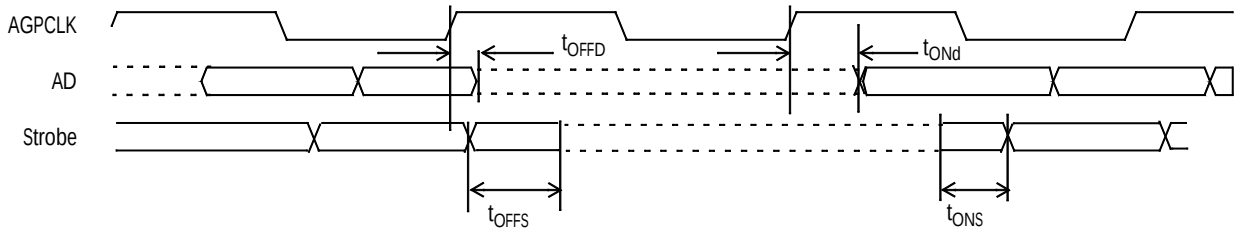



**Figure 24. AGP 4x Strobe/Data Turnaround Timing**

**PCI Interface Timings** Table 25 on page 68 shows the PCI interface timings. Table 26 shows 66-MHz PCI interface timings. All of the timings are relative to PCLK.

**Table 25. 33-MHz PCI Interface Timings***

| Symbol | Parameter Description | Preliminary Data | | Figure | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{su}$ | AD[63:0] Setup Time | 7 ns | | 20 | |
| | SBREQ#, REQ[6:0]# Setup Time | 12 ns | | 20 | |
| | Setup Time for<br>FRAME# STOP#<br>TRDY# DEVSEL#<br>IRDY# C/BE[3:0]# RESET#<br>WSC#<br>REQ64# ACK64# | 7 ns | | 20 | |
| $t_h$ | AD[63:0] Hold Time | 0 ns | | 20 | |
| | Hold Time for<br>FRAME# STOP#<br>TRDY# DEVSEL#<br>IRDY# C/BE[3:0]#<br>SBREQ# REQ[3:0]# WSC#<br>ACK64#<br>REQ64# | 0 ns | | 20 | |
| $t_{vd}$ | AD[31:0] Valid Delay (address phase) | 2 ns | 11 ns | 20 | 1 |
| | AD[63:0] Valid Delay (data phase) | 2 ns | 11 ns | 20 | 1 |
| | Valid Delay for<br>FRAME# STOP#<br>TRDY# DEVSEL#<br>IRDY# C/BE[3:0]#<br>GNT[3:0]#WSC#<br>REQ64# ACK64# | 2 ns | 11 ns | 20 | 1 |
| | SBGNT# Valid Delay | 2 ns | 12 ns | 20 | |
| $t_{fd}$ | Float Delay for<br>FRAME# STOP#<br>TRDY# DEVSEL#<br>IRDY# C/BE[3:0]# WSC#<br>REQ64#<br>ACK64# | | 28 ns | | 1 |
| $t_{pw}$ | RESET# Pulse Width | 2 clks | | 20 | |

***Note:***

** This table contains preliminary information, which is subject to change.*

*1. Measurements are taken with no load for $t_{min}$, and 50 pF for $t_{max.}$*

**Table 26. 66-MHz PCI Interface Timings***

| Symbol | Parameter Description | Preliminary Data | | Figure | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{su}$ | AD[63:0] Setup Time | 3 ns | | 20 | |
| | SBREQ#, REQ[6:0]# Setup Time | 3 ns | | 20 | |
| | Setup Time for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# RESET# WSC# REQ64# ACK64# | 5 ns | | 20 | |
| $t_h$ | AD[63:0] Hold Time | 0 ns | | 20 | |
| | Hold Time for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# SBREQ# REQ[3:0]# WSC# ACK64# REQ64# | 0 ns | | 20 | |
| $t_{vd}$ | AD[63:0] Valid Delay (address phase) | 2 ns | 6 ns | 20 | 1 |
| | AD[63:0] Valid Delay (data phase) | 2 ns | 6 ns | 20 | 1 |
| | Valid Delay for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# GNT[3:0]#WSC# REQ64# ACK64# | 2 ns | 6 ns | 20 | 1 |
| | SBGNT# Valid Delay | 2 ns | 6 ns | 20 | |
| $t_{fd}$ | Float Delay for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# WSC# REQ64# ACK64# | | 14 ns | | 1 |
| $t_{pw}$ | RESET# Pulse Width | 2 clks | | 20 | |

***Note:***

** This table contains preliminary information, which is subject to change.*

*1. Measurements are taken with no load for $t_{min}$, and 50 pF for $t_{max.}$*

## 4.5.4 AMD Athlon™ Processor System Bus Timings

Table 27 shows the AMD Athlon processor system bus timings.

**Table 27. AMD Athlon™ Processor System Bus/AMD-762™ System Controller AC Specification**

| Group | Symbol | Parameter Description | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Clock Forward Group Signals | $T_{NB-SKEW-SAMEEDGE}$ | Output skew with respect to the same clock edge | – | – | 400 | ps | 1 |
| | $T_{NB-SKEW-DIFFEDGE}$ | Output skew with respect to a different clock edge | – | – | 1025 | ps | 1 |
| | $T_{NB-SU}$ | Input Data Setup Time | 500 | – | – | ps | 1, 2 |
| | $T_{NB-HD}$ | Input Data Hold Time | 800 | – | – | ps | 1, 2 |
| | $T_{RISE}$ | Signal or Clock Rise Time | 1 | – | 3 | V/ns | |
| | $T_{FALL}$ | Signal or Clock Fall Time | 1 | – | 3 | V/ns | |
| | $C_{DATA}$ | Data Pin Capacitance | 4 | – | 12 | pF | |
| | $C_{INCLK}$ | Input Clock Capacitance | 4 | – | 12 | pF | |
| Sync Signals *3 | $T_{NB-SYSCLK-TO-PAD}$ | SYSCLK to Synchronous Signal Output at Pad (CONNECT, CLKFWDRST) | 2400 | – | 4800 | ps | 4, 5 |
| | $T_{NB-SETUP-TO-SYSCLK}$ | Input Setup Time for Synchronous Signal to SYSCLK (PROCRDY) | 1500 | – | – | ps | 4, 5 |
| | $T_{NB-HOLD-FROM-SYSCLK}$ | Input Hold Time for Synchronous Signal to SYSCLK (PROCRDY) | 1200 | – | – | ps | 4, 5 |

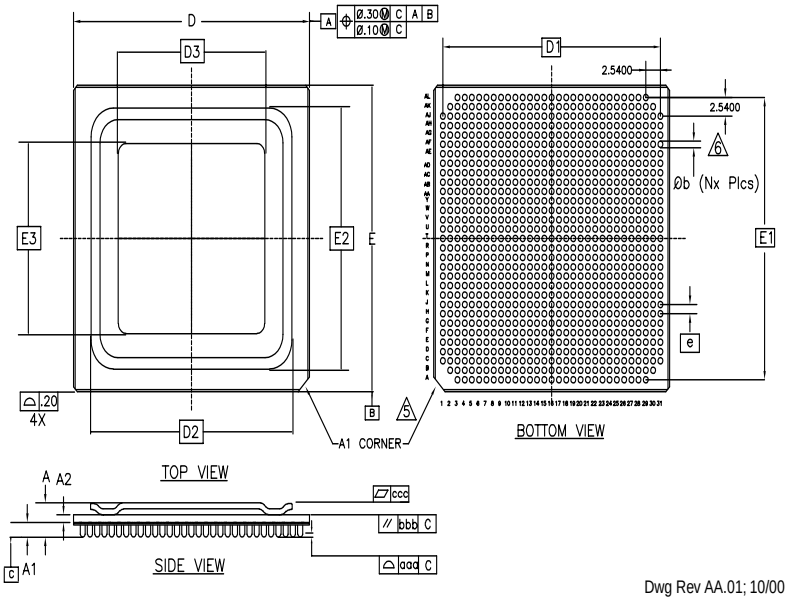
***Notes:***

** This table contains preliminary information, which is subject to change.*

1. *$T_{NB-SKEW-SAMEEDGE}$ is the maximum skew within a clock-forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.*
   *$T_{NB-SKEW-DIFFEDGE}$ is the maximum skew within a clock-forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.*
2. *Input SU and HLD times are with respect to the appropriate clock forward group input clock.*
3. *The synchronous signals include PROCREADY, CONNECT, and CLKFWDRST.*
4. *This value is measured with respect to the rising edge of SYSCLKIN.*
5. *Test load = 25 pF.*

# 5 Package Specifications

Figure 25 on page 72 shows the package specifications for the AMD-762™ system controller.




Dwg Rev AA.01; 10/00

| AMD PACKAGE | | |
|---|---|---|
| SYMBOL | MIN. | MAX. |
| D/E | 39.80 | 40.20 |
| D1/E1 | 38.10 BSC. | |
| D2/E2 | --- | 35.00 |
| D3/E3 | 21.79 | 22.89 |
| A | 4.869 | 5.257 |
| A1 | 1.688 | 1.958 |
| A2 | 1.322 | 1.522 |
| b | 0.79 | 0.99 |
| e | 1.27 BSC. | |
| M | 31 | |
| N | 949 COLUMNS | |
| aaa | 0.15 | |
| bbb | 0.26 | |
| ccc | 0.005 | |

NOTES:

1. ALL DIMENSIONS ARE SPECIFIED IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. CORNERS OF THE PACKAGE BODY MAY HAVE CHAMFERS FOR HANDLING OR ORIENTATION PURPOSES.
4. SYMBOL "M" DETERMINES PIN MATRIX SIZE AND "N" AS NUMBER OF COLUMNS.
5. THIS INDEX CORNER REPRESENTS PIN A1 IDENTIFIER ON BOTH SIDES OF THE PACKAGE AND MAY CONSIST OF NOTCHES, PINS OR METALLIZATIONS AND MAY ALSO VARY FROM THAT SHOWN IN THE DRAWING.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER COLUMN DIAMETER ON A PLANE PARALLEL TO DATUM C.
7. REFER TO 09-000 SPEC FOR DETAILED PACKAGE LISTS.

**Figure 25. 949-Pin Ceramic Column Grid Array (CCGA) Package**

# 6 Pin Designations

This chapter includes a pin connection diagram and pin designation tables with pins grouped by function.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | | NC1 | MDAT1 | DQS0 | MDAT7 | MDAT12 | DQS1 | MDAT10 | MDAT17 | DM2 | MDAT24 | MDAT29 | MDAT26 | MDAT31 | MECC1 | A |
| B | | NC28 | MDAT5 | VDD_CORE | DM0 | MDAT2 | VDD_CORE | MDAT13 | MDAT15 | VDD_CORE | MDAT21 | MDAT19 | VDD_CORE | MDAT30 | MDAT27 | VDD_CORE | B |
| C | NC30 | NC31 | MDAT4 | MDAT0 | MDAT6 | MDAT8 | MDAT9 | MDAT14 | MDAT20 | DQS2 | MDAT22 | MDAT28 | DQS3 | MECC4 | MECC0 | DQS8 | C |
| D | P0_SADDOUT14# | P0_K7_VCORE0 | PDL_OUTPUT_TEST | DDR_REF | VSS | MDAT3 | VSS | DM1 | MDAT11 | VSS | MDAT18 | MDAT23 | VSS | DM3 | MECC5 | VSS | D |
| E | P0_SADDOUT7# | P0_SADDOUT13# | P0_SADDOUTCLK# | VSS | NC36 | CLKOUTH1 | CLKOUTH4 | CLKOUTL4 | MAB12 | MDAT16 | MAA5 | MAB5 | MDAT25 | MAB4 | MAA2 | CLKOUTH3 | E |
| F | P0_SADDOUT12# | P0_SADDOUT9# | P0_SADDOUT8# | P0_SADDOUT5# | P0_SADDOUT10# | CLKOUTL1# | VDD_CORE | CKEB | MAA12 | VDD_CORE | MAB9 | MAB8 | VDD_CORE | MAA4 | MAB2 | VDD_CORE | F |
| G | P0_SADDOUT2# | P0_K7_VCORE1 | P0_SADDOUT4# | VSS | P0_SADDOUT11# | P0_K7_VCORE7 | NC38 | CKEA | MAA7 | MAA9 | MAA8 | MAA6 | MAB6 | MAA3 | MAA1 | CLKOUTH0 | G |
| H | P0_SDATAOUTCLK3# | P0_SADDOUT3# | P0_SDATAINCLK3# | P0_SADDOUT6# | P0_SDATA55# | P0_SDATA54# | P0_SDATA61# | VSS | MAB11 | VSS | MAA11 | MAB7 | VSS | MAB3 | MAB1 | VSS | H |
| J | P0_SDATA63# | P0_SDATA53# | P0_SCHECK6# | P0_SDATA52# | P0_SDATA62# | P0_SDATA49# | P0_SDATA50# | P0_SYSFILLVALID# | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | J |
| K | P0_SDATA60# | P0_K7_VCORE2 | P0_SCHECK7# | VSS | P0_SDATA51# | P0_K7_VCORE8 | P0_SDATA48# | VSS | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | K |
| L | P0_SDATA59# | P0_SDATA58# | P0_SDATA36# | P0_SDATA57# | P0_SDATA46# | P0_SDATA39# | P0_SDATA37# | NC40 | P0_K7_VCORE13 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | L |
| M | P0_SDATAINCLK2# | P0_SDATA56# | P0_SDATA47# | P0_SDATA38# | P0_SDATA44# | P0_SDATA35# | P0_SDATA45# | P0_SDATA34# | VSS | P0_K7_VCORE23 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | M |
| N | P0_SCHECK5# | P0_K7_VCORE3 | P0_SDATA42# | VSS | P0_SDATAOUTCLK2# | P0_K7_VCORE9 | P0_SCHECK4# | VSS | P0_K7_VCORE14 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | N |
| P | P0_SDATA31# | P0_SDATA32# | P0_SDATA43# | P0_SDATA33# | P0_SDATA41# | P0_SDATA30# | P0_SDATA40# | P0_SCHECK2# | VSS | P0_K7_VCORE22 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | P |
| R | P0_SDATAINCLK1# | P0_SDATA22# | P0_SDATA20# | P0_SDATA21# | P0_SDATA19# | P0_SDATA18# | P0_SDATA17# | P0_SDATAOUTCLK1# | P0_K7_VCORE15 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | R |
| T | P0_SCHECK3# | P0_K7_VCORE4 | P0_SDATA28# | VSS | P0_SDATA26# | P0_K7_VCORE10 | P0_SDATA24# | VSS | VSS | P0_K7_VCORE21 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | T |
| U | P0_SDATA29# | P0_SDATA23# | P0_SDATA6# | P0_SDATA5# | P0_SDATAINCLK0# | P0_SDATA15# | P0_SDATA16# | P0_SDATA7# | P0_K7_VCORE16 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | U |
| V | P0_SDATA25# | P0_SDATA27# | P0_SDATA2# | P0_SDATA1# | P0_SDATA3# | P0_SDATA4# | P0_SCHECK0# | P0_SCHECK1# | VSS | P0_K7_VCORE20 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | V |
| W | P0_SDATA12# | P0_K7_VCORE5 | P0_SDATA0# | VSS | P0_SDATAOUTCLK0# | P0_K7_VCORE11 | P0_SDATA13# | VSS | P0_K7_VCORE17 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | W |
| Y | P0_SDATA8# | P0_SDATA14# | P0_SDATA9# | P0_SADDIN2# | P0_SADDIN5# | P0_SADDIN11# | P0_SDATA11# | NC41 | VSS | P0_K7_VCORE19 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | Y |
| AA | P0_SDATA10# | SADDIN3# | P0_SADDIN7# | P0_SADDIN6# | P0_SADDIN8# | P0_SADDIN4# | P0_SADDINCLK# | NC6 | P0_K7_VCORE18 | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | AA |
| AB | P0_SDATAINVALID# | P0_K7_VCORE6 | P0_SADDIN9# | VSS | P0_SADDIN10# | P0_K7_VCORE12 | P1_VREF | VSS | VSS | P1_K7_VCORE20 | VSS | P1_K7_VCORE21 | VSS | P1_K7_VCORE22 | VSS | P1_K7_VCORE23 | AB |
| AC | P0_SADDIN14# | P0_VREF | P0_SADDIN13# | P0_CONNECT | P0_CLKFWDRST | P0_PROCRDY | NC11 | NC8 | P1_K7_VCORE13 | VSS | P1_K7_VCORE14 | VSS | P1_K7_VCORE15 | VSS | P1_K7_VCORE16 | VSS | AC |
| AD | P0_SADDIN12# | SI_VSS | PX_CAL | PX_CAL# | P1_SADDOUT10# | P1_SADDOUT11# | P1_SADDOUT7# | VSS | NC12 | VSS | P1_SDATA42# | P1_SDATAINCLK1# | VSS | P1_SDATA3# | P1_SDATA9# | VSS | AD |
| AE | SI_VDD | P1_K7_VCORE0 | P1_SADDOUT4# | VSS | P1_SDATA61# | P1_K7_VCORE19 | P1_SDATA57# | P1_SDATA56# | P1_SDATA41# | P1_SDATA40# | P1_SDATA21# | P1_SDATA18# | P1_SDATA7# | P1_SDATA0# | P1_SDATAINCLK0# | P1_SDATA2# | AE |
| AF | P1_SADDOUT12# | P1_SADDOUT9# | P1_SADDOUT6# | P1_SDATA48# | P1_SDATA50# | P1_SCHECK6# | P1_K7_VCORE8 | P1_SDATA46# | P1_SDATA33# | P1_K7_VCORE9 | P1_SDATA23# | P1_SDATA17# | P1_K7_VCORE10 | P1_SDATA16# | P1_SDATA11# | P1_K7_VCORE11 | AF |
| AG | P1_SADDOUTCLK# | P1_SADDOUT14# | P1_SADDOUT5# | VSS | P1_SDATA49# | P1_SDATA58# | P1_SDATA32# | P1_SCHECK5# | P1_SDATAOUTCLK2# | P1_SDATA43# | P1_SDATA22# | P1_SDATA29# | P1_SDATA27# | P1_SCHECK0# | P1_SDATA10# | P1_SADDIN7# | AG |
| AH | P1_SADDOUT13# | P1_K7_VCORE1 | P1_SDATA55# | P1_SDATA52# | VSS | P1_SDATA62# | VSS | P1_SDATA38# | P1_SDATA45# | VSS | P1_SDATAOUTCLK1# | P1_SCHECK2# | VSS | P1_SDATA15# | P1_SDATAOUTCLK0# | VSS | AH |
| AJ | NC17 | P1_SADDOUT2# | P1_SADDOUT8# | P1_SDATAOUTCLK3# | P1_SDATA53# | P1_SDATA60# | P1_SDATA47# | P1_SDATAINCLK2# | P1_SDATA44# | P1_SCHECK3# | P1_SDATA20# | P1_SDATA30# | P1_SDATA28# | P1_SDATA1# | P1_SDATA4# | P1_SDATA12# | AJ |
| AK | | NC21 | P1_SADDOUT3# | P1_K7_VCORE2 | P1_SDATAINCLK3# | P1_SDATA51# | P1_K7_VCORE3 | P1_SDATA36# | P1_SDATA39# | P1_K7_VCORE4 | P1_SDATA34# | P1_SDATA19# | P1_K7_VCORE5 | P1_SDATA24# | P1_SDATA6# | P1_K7_VCORE6 | AK |
| AL | | | NC27 | P1_SDATA54# | P1_SDATA63# | P1_SDATA59# | P1_SCHECK7# | P1_SDATA37# | P1_SCHECK4# | P1_SDATA35# | P1_SDATA31# | P1_SDATA26# | P1_SDATA25# | P1_SDATA5# | P1_SCHECK1# | P1_SDATA8# | AL |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

| | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | MECC2 | MECC7 | MDAT33 | MDAT34 | MDAT44 | DM5 | MDAT46 | MDAT52 | MDAT54 | MDAT55 | MDAT60 | DM7 | NC0 | | | A |
| B | MECC6 | MDAT32 | VDD_CORE | MDAT38 | MDAT40 | VDD_CORE | MDAT43 | MDAT49 | VDD_CORE | MDAT50 | MDAT57 | VDD_CORE | MDAT63 | NC29 | | B |
| C | DM8 | MDAT36 | DQS4 | MDAT39 | MDAT45 | DQS5 | MDAT47 | MDAT53 | DQS6 | MDAT51 | MDAT56 | DQS7 | MDAT58 | MDAT59 | NC32 | C |
| D | MECC3 | MDAT37 | VSS | MDAT35 | MDAT41 | VSS | MDAT48 | DM6 | VSS | MDAT61 | VSS | MDAT62 | GNT6# | VDD_PCI | GNT0# | D |
| E | CLKOUT3# | MAB14 | DM4 | MAB13 | WEA# | MDAT42 | CS1# | CLKOUTH2 | CLKOUTL2 | CLKOUTH5 | NC35 | VSS | REQ6# | REQ0# | GNT1# | E |
| F | MAA0 | MAA10 | VDD_CORE | RASB# | CS2# | VDD_CORE | CS3# | CS7# | VDD_CORE | CLKOUTL5 | GNT5# | GNT4# | REQ4# | REQ1# | AD32 | F |
| G | CLKOUTL0 | MAA14 | MAA13 | RASA# | CASB# | CASA# | CS5# | CS6# | NC37 | VDD_PCI | REQ5# | VSS | GNT2# | VDD_PCI | AD34 | G |
| H | MAB0 | MAB10 | VSS | WEB# | CS0# | VSS | CS4# | VSS | REQ2# | GNT3# | REQ3# | WSC# | REF_5V | AD36 | AD38 | H |
| J | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | SBREQ# | SBGNT# | AD37 | AD44 | AD39 | AD41 | AD40 | AD42 | J |
| K | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VSS | AD33 | VDD_PCI | AD46 | VSS | AD47 | VDD_PCI | AD52 | K |
| L | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_PCI | AD35 | AD43 | AD48 | AD50 | AD49 | AD51 | AD54 | AD56 | L |
| M | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | AD45 | AD55 | AD58 | AD60 | AD53 | AD59 | PAR64 | CBE5# | M |
| N | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_PCI | VSS | AD61 | VDD_PCI | AD62 | VSS | CBE6# | VDD_PCI | CBE7# | N |
| P | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | AD57 | PCI_66CLK0 | REQ64# | AD0 | PCI_66CLK1 | PCI_66CLK2 | AD2 | AD4 | P |
| R | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_PCI | AD63 | CBE4# | AD6 | CBE0# | ACK64# | AD1 | AD12 | AD9 | R |
| T | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VSS | AD3 | VDD_PCI | AD11 | VSS | AD8 | VDD_PCI | AD13 | T |
| U | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_PCI | AD5 | AD7 | AD14 | AD15 | M66EN | SERR# | STOP# | PAR | U |
| V | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | AD10 | CBE1# | AD18 | AD16 | DEVSEL# | IRDY# | TRDY# | FRAME# | V |
| W | VDD_CORE | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_PCI | VSS | CBE2# | VDD_PCI | AD22 | VSS | AD17 | VDD_PCI | AD20 | W |
| Y | VSS | VDD_CORE | VSS | VDD_CORE | VSS | VDD_AGP | VSS | CBE3# | AD23 | AD30 | AD29 | AD19 | AD21 | AD27 | AD24 | Y |
| AA | VDD_CORE | VSS | VDD_CORE | VSS | VDD_AGP | VSS | VDD_AGP | AGP_CAL | A_AD3 | A_AD1 | AD31 | AD25 | NC4 | AD28 | AD26 | AA |
| AB | VSS | P1_K7_VCORE24 | VSS | VDD_AGP | VSS | VDD_AGP | VSS | VSS | A_AD12 | VDD_AGP | A_CBE0# | VSS | A_AD5 | VDD_AGP | A_AD0 | AB |
| AC | P1_K7_VCORE17 | VSS | P1_K7_VCORE18 | VSS | VDD_AGP | VSS | VDD_AGP | A_DEVSEL# | AGP_VREF4X | A_AD7 | A_AD8 | A_AD14 | A_AD10 | A_AD4 | A_AD2 | AC |
| AD | P1_SADDIN9# | NC9 | VSS | DCSTOP# | NC10 | VSS | SBA3 | VSS | A_AD26 | A_AD16 | A_PAR | A_CBE1# | A_AD13 | ADSTB0# | A_AD6 | AD |
| AE | P1_SDATAINVALID# | P1_SADDIN13# | P1_PROCRDY | NC13 | TEST# | NC14 | SBA1 | SBA4 | A_AD31 | VDD_AGP | A_SERR# | VSS | A_AD15 | VDD_AGP | ADSTB0 | AE |
| AF | P1_SADDIN6# | P1_SADDIN14# | P1_K7_VCORE12 | DEBUG2# | RESET# | VDD_AGP | A_AD30 | A_AD27 | VDD_AGP | A_CBE3# | A_AD21 | A_IRDY# | A_FRAME# | A_TRDY# | AGP_CAL# | AF |
| AG | P1_SADDIN2# | P1_SADDIN8# | P1_SADDIN12# | S_CLKREF | VSS | A_VDD | SBA0 | A_AD29 | SBA5 | A_AD28 | A_AD23 | VSS | A_AD19 | AGP_VREF | A_AD9 | AG |
| AH | P1_SDATA13# | P1_SADDIN3# | VSS | P0_SYSCLK | PCICLK | VSS | NC2 | SBSTB# | VSS | SBA7 | VSS | A_AD17 | A_AD22 | VDD_AGP | A_AD11 | AH |
| AJ | P1_SDATA14# | P1_SADDINCLK# | P1_CONNECT | VSS | AGPCLK | DEBUG1# | ST2 | SBSTB | SBA2 | A_AD25 | ADSTB1 | ADSTB1# | A_CBE2# | A_AD18 | NC20 | AJ |
| AK | P1_SADDIN11# | P1_SADDIN10# | P1_K7_VCORE7 | DEBUG0# | ROM_SCK | VDD_AGP | A_REQ# | ST0 | VDD_AGP | WBF# | A_STOP# | VDD_AGP | A_AD20 | NC23 | | AK |
| AL | P1_SADDIN5# | P1_SADDIN4# | P1_CLKFWDRST | P1_SYSFILLVALID# | ROM_SDA | NC25 | A_GNT# | ST1 | PIPE# | RBF# | SBA6 | A_AD24 | NC26 | | | AL |
| | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | |

## Table 28. AMD-762™ System Controller Pin Functional Grouping (1 of 5)

| DDR DRAM | | | | | | | | AGP | | APCI | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | No. | Name | No. | Name | No. | Name | No. | Name | No. | Name | No. |
| MAA[14] | G-18 | CS[0]# | H-21 | MDAT[47] | C-23 | MDAT[01] | A-4 | ADSTB[1] | AJ-27 | A_AD[31] | AE-25 |
| MAA[13] | G-19 | RASB# | F-20 | MDAT[46] | A-23 | MDAT[00] | C-4 | ADSTB[1]# | AJ-28 | A_AD[30] | AF-23 |
| MAA[12] | F-9 | RASA# | G-20 | MDAT[45] | C-21 | MECC[7] | A-18 | ADSTB[0] | AE-31 | A_AD[29] | AG-24 |
| MAA[11] | H-11 | CASB# | G-21 | MDAT[44] | A-21 | MECC[6] | B-17 | ADSTB[0]# | AD-30 | A_AD[28] | AG-26 |
| MAA[10] | F-18 | CASA# | G-22 | MDAT[43] | B-23 | MECC[5] | D-15 | SBSTB | AJ-24 | A_AD[27] | AF-24 |
| MAA[09] | G-10 | WEB# | H-20 | MDAT[42] | E-22 | MECC[4] | C-14 | SBSTB# | AH-24 | A_AD[26] | AD-25 |
| MAA[08] | G-11 | WEA# | E-21 | MDAT[41] | D-21 | MECC[3] | D-17 | WBF# | AK-26 | A_AD[25] | AJ-26 |
| MAA[07] | G-9 | CKEB | F-8 | MDAT[40] | B-21 | MECC[2] | A-17 | PIPE# | AL-25 | A_AD[24] | AL-28 |
| MAA[06] | G-12 | CKEA | G-8 | MDAT[39] | C-20 | MECC[1] | A-16 | RBF# | AL-26 | A_AD[23] | AG-27 |
| MAA[05] | E-11 | DQS[8] | C-16 | MDAT[38] | B-20 | MECC[0] | C-15 | SBA[0] | AG-23 | A_AD[22] | AH-29 |
| MAA[04] | F-14 | DQS[7] | C-28 | MDAT[37] | D-18 | | | SBA[1] | AE-23 | A_AD[21] | AF-27 |
| MAA[03] | G-14 | DQS[6] | C-25 | MDAT[36] | C-18 | | | SBA[2] | AJ-25 | A_AD[20] | AK-29 |
| MAA[02] | E-15 | DQS[5] | C-22 | MDAT[35] | D-20 | | | SBA[3] | AD-23 | A_AD[19] | AG-29 |
| MAA[01] | G-15 | DQS[4] | C-19 | MDAT[34] | A-20 | | | SBA[4] | AE-24 | A_AD[18] | AJ-30 |
| MAA[00] | F-17 | DQS[3] | C-13 | MDAT[33] | A-19 | | | SBA[5] | AG-25 | A_AD[17] | AH-28 |
| MAB[14] | E-18 | DQS[2] | C-10 | MDAT[32] | B-18 | | | SBA[6] | AL-27 | A_AD[16] | AD-26 |
| MAB[13] | E-20 | DQS[1] | A-8 | MDAT[31] | A-15 | | | SBA[7] | AH-26 | A_AD[15] | AE-29 |
| MAB[12] | E-9 | DQS[0] | A-5 | MDAT[30] | B-14 | | | ST[0] | AK-24 | A_AD[14] | AC-28 |
| MAB[11] | H-9 | CLKOUTH[5] | E-26 | MDAT[29] | A-13 | | | ST[1] | AL-24 | A_AD[13] | AD-29 |
| MAB[10] | H-18 | CLKOUTL[5] | F-26 | MDAT[28] | C-12 | | | ST[2] | AJ-23 | A_AD[12] | AB-25 |
| MAB[09] | F-11 | CLKOUTH[4] | E-7 | MDAT[27] | B-15 | | | AGPCLK | AJ-21 | A_AD[11] | AH-31 |
| MAB[08] | F-12 | CLKOUTL[4] | E-8 | MDAT[26] | A-14 | | | | | A_AD[10] | AC-29 |
| MAB[07] | H-12 | CLKOUTH[3] | E-16 | MDAT[25] | E-13 | | | | | A_AD[09] | AG-31 |
| MAB[06] | G-13 | CLKOUTL[3] | E-17 | MDAT[24] | A-12 | | | | | A_AD[08] | AC-27 |
| MAB[05] | E-12 | CLKOUTH[2] | E-24 | MDAT[23] | D-12 | | | | | A_AD[07] | AC-26 |
| MAB[04] | E-14 | CLKOUTL[2] | E-25 | MDAT[22] | C-11 | | | | | A_AD[06] | AD-31 |
| MAB[03] | H-14 | CLKOUTH[1] | E-6 | MDAT[21] | B-11 | | | | | A_AD[05] | AB-29 |
| MAB[02] | F-15 | CLKOUTL[1] | F-6 | MDAT[20] | C-9 | | | | | A_AD[04] | AC-30 |
| MAB[01] | H-15 | CLKOUTH[0] | G-16 | MDAT[19] | B-12 | | | | | A_AD[03] | AA-25 |
| MAB[00] | H-17 | CLKOUTL[0] | G-17 | MDAT[18] | D-11 | | | | | A_AD[02] | AC-31 |
| DM[8] | C-17 | MDAT[63] | B-29 | MDAT[17] | A-10 | | | | | A_AD[01] | AA-26 |
| DM[7] | A-28 | MDAT[62] | D-28 | MDAT[16] | E-10 | | | | | A_AD[00] | AB-31 |
| DM[6] | D-24 | MDAT[61] | D-26 | MDAT[15] | B-9 | | | | | A_CBE[3]# | AF-26 |
| DM[5] | A-22 | MDAT[60] | A-27 | MDAT[14] | C-8 | | | | | A_CBE[2]# | AJ-29 |
| DM[4] | E-19 | MDAT[59] | C-30 | MDAT[13] | B-8 | | | | | A_CBE[1]# | AD-28 |
| DM[3] | D-14 | MDAT[58] | C-29 | MDAT[12] | A-7 | | | | | A_CBE[0]# | AB-27 |
| DM[2] | A-11 | MDAT[57] | B-27 | MDAT[11] | D-9 | | | | | A_DEVSEL# | AC-24 |
| DM[1] | D-8 | MDAT[56] | C-27 | MDAT[10] | A-9 | | | | | A_FRAME# | AF-29 |
| DM[0] | B-5 | MDAT[55] | A-26 | MDAT[09] | C-7 | | | | | A_GNT# | AL-23 |
| CS[7]# | F-24 | MDAT[54] | A-25 | MDAT[08] | C-6 | | | | | A_IRDY# | AF-28 |
| CS[6]# | G-24 | MDAT[53] | C-24 | MDAT[07] | A-6 | | | | | A_PAR | AD-27 |
| CS[5]# | G-23 | MDAT[52] | A-24 | MDAT[06] | C-5 | | | | | A_REQ# | AK-23 |
| CS[4]# | H-23 | MDAT[51] | C-26 | MDAT[05] | B-3 | | | | | A_SERR# | AE-27 |
| CS[3]# | F-23 | MDAT[50] | B-26 | MDAT[04] | C-3 | | | | | A_STOP# | AK-27 |
| CS[2]# | F-21 | MDAT[49] | B-24 | MDAT[03] | D-6 | | | | | A_TRDY# | AF-30 |
| CS[1]# | E-23 | MDAT[48] | D-23 | MDAT[02] | B-6 | | | | | | |

**Table 29. AMD-762™ System Controller Pin Functional Grouping (2 of 5)**

| PCI Bus | | | | | | Miscellaneous | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | **No.** | **Name** | **No.** | **Name** | **No.** | **Name** | **No.** | **Name** | **No.** |
| AD[63] | R-24 | AD[17] | W-29 | GNT[0]# | D-31 | P0_K7_VCORE0 | D-2 | P0_VREF | AC-2 |
| AD[62] | N-27 | AD[16] | V-27 | GNT[1]# | E-31 | P0_K7_VCORE1 | G-2 | P1_VREF | AB-7 |
| AD[61] | N-25 | AD[15] | U-27 | GNT[2]# | G-29 | P0_K7_VCORE2 | K-2 | PX_CAL | AD-3 |
| AD[60] | M-27 | AD[14] | U-26 | GNT[3]# | H-26 | P0_K7_VCORE3 | N-2 | PX_CAL# | AD-4 |
| AD[59] | M-29 | AD[13] | T-31 | GNT[4]# | F-28 | P0_K7_VCORE4 | T-2 | SI_VSS | AD-2 |
| AD[58] | M-26 | AD[12] | R-30 | GNT[5]# | F-27 | P0_K7_VCORE5 | W-2 | SI_VDD | AE-1 |
| AD[57] | P-24 | AD[11] | T-27 | GNT[6]# | D-29 | P0_K7_VCORE6 | AB-2 | AGP_VREF | AG-30 |
| AD[56] | L-31 | AD[10] | V-24 | SBREQ# | J-24 | P0_K7_VCORE7 | G-6 | AGP_VREF4X | AC-25 |
| AD[55] | M-25 | AD[09] | R-31 | SBGNT# | J-25 | P0_K7_VCORE8 | K-6 | AGP_CAL | AA-24 |
| AD[54] | L-30 | AD[08] | T-29 | RESET# | AF-21 | P0_K7_VCORE9 | N-6 | AGP_CAL# | AF-31 |
| AD[53] | M-28 | AD[07] | U-25 | PCI_66CLK2 | P-29 | P0_K7_VCORE10 | T-6 | REF_5V | H-29 |
| AD[52] | K-31 | AD[06] | R-26 | PCI_66CLK1 | P-28 | P0_K7_VCORE11 | W-6 | DDR_REF | D-4 |
| AD[51] | L-29 | AD[05] | U-24 | PCI_66CLK0 | P-25 | P0_K7_VCORE12 | AB-6 | TEST# | AE-21 |
| AD[50] | L-27 | AD[04] | P-31 | | | P0_K7_VCORE13 | L-9 | S_CLKREF | AG-20 |
| AD[49] | L-28 | AD[03] | T-25 | | | P0_K7_VCORE14 | N-9 | DCSTOP# | AD-20 |
| AD[48] | L-26 | AD[02] | P-30 | | | P0_K7_VCORE15 | R-9 | ROM_SDA | AL-21 |
| AD[47] | K-29 | AD[01] | R-29 | | | P0_K7_VCORE16 | U-9 | ROM_SCK | AK-21 |
| AD[46] | K-27 | AD[00] | P-27 | | | P0_K7_VCORE17 | W-9 | DEBUG[2]# | AF-20 |
| AD[45] | M-24 | CBE[7]# | N-31 | | | P0_K7_VCORE18 | AA-9 | DEBUG[1]# | AJ-22 |
| AD[44] | J-27 | CBE[6]# | N-29 | | | P0_K7_VCORE19 | Y-10 | DEBUG[0]# | AK-20 |
| AD[43] | L-25 | CBE[5]# | M-31 | | | P0_K7_VCORE20 | V-10 | PDL_OUTPUT_TEST | D-3 |
| AD[42] | J-31 | CBE[4]# | R-25 | | | P0_K7_VCORE21 | T-10 | P1_K7_VCORE0 | AE-2 |
| AD[41] | J-29 | CBE[3]# | Y-24 | | | P0_K7_VCORE22 | P-10 | P1_K7_VCORE1 | AH-2 |
| AD[40] | J-30 | CBE[2]# | W-25 | | | P0_K7_VCORE23 | M-10 | P1_K7_VCORE2 | AK-4 |
| AD[39] | J-28 | CBE[1]# | V-25 | | | | | P1_K7_VCORE3 | AK-7 |
| AD[38] | H-31 | CBE[0]# | R-27 | | | | | P1_K7_VCORE4 | AK-10 |
| AD[37] | J-26 | PCICLK | AH-21 | | | | | P1_K7_VCORE5 | AK-13 |
| AD[36] | H-30 | DEVSEL# | V-28 | | | | | P1_K7_VCORE6 | AK-16 |
| AD[35] | L-24 | FRAME# | V-31 | | | | | P1_K7_VCORE7 | AK-19 |
| AD[34] | G-31 | WSC# | H-28 | | | | | P1_K7_VCORE8 | AF-7 |
| AD[33] | K-25 | IRDY# | V-29 | | | | | P1_K7_VCORE9 | AF-10 |
| AD[32] | F-31 | PAR | U-31 | | | | | P1_K7_VCORE10 | AF-13 |
| AD[31] | AA-27 | PAR64 | M-30 | | | | | P1_K7_VCORE11 | AF-16 |
| AD[30] | Y-26 | SERR# | U-29 | | | | | P1_K7_VCORE12 | AF-19 |
| AD[29] | Y-27 | STOP# | U-30 | | | | | P1_K7_VCORE13 | AC-9 |
| AD[28] | AA-30 | TRDY# | V-30 | | | | | P1_K7_VCORE14 | AC-11 |
| AD[27] | Y-30 | REQ64# | P-26 | | | | | P1_K7_VCORE15 | AC-13 |
| AD[26] | AA-31 | ACK64# | R-28 | | | | | P1_K7_VCORE16 | AC-15 |
| AD[25] | AA-28 | M66EN | U-28 | | | | | P1_K7_VCORE17 | AC-17 |
| AD[24] | Y-31 | REQ[0]# | E-30 | | | | | P1_K7_VCORE18 | AC-19 |
| AD[23] | Y-25 | REQ[1]# | F-30 | | | | | P1_K7_VCORE19 | AE-6 |
| AD[22] | W-27 | REQ[2]# | H-25 | | | | | P1_K7_VCORE20 | AB-10 |
| AD[21] | Y-29 | REQ[3]# | H-27 | | | | | P1_K7_VCORE21 | AB-12 |
| AD[20] | W-31 | REQ[4]# | F-29 | | | | | P1_K7_VCORE22 | AB-14 |
| AD[19] | Y-28 | REQ[5]# | G-27 | | | | | P1_K7_VCORE23 | AB-16 |
| AD[18] | V-26 | REQ[6]# | E-29 | | | | | P1_K7_VCORE24 | AB-18 |

**Table 30. AMD-762™ System Controller Pin Functional Grouping (3 of 5)**

| No Connects | | Processor 0 AMD Athlon™ System Bus | | | | | |
|---|---|---|---|---|---|---|---|
| Name | No. | Name | No. | Name | No. | Name | No. |
| NC0 | A-29 | P0_CLKFWDRST | AC-5 | P0_SDATA[06]# | U-3 | P0_SDATA[52]# | J-4 |
| NC1 | A-3 | P0_CONNECT | AC-4 | P0_SDATA[07]# | U-8 | P0_SDATA[53]# | J-2 |
| NC2 | AH-23 | P0_PROCRDY | AC-6 | P0_SDATA[08]# | Y-1 | P0_SDATA[54]# | H-6 |
| NC4 | AA-29 | P0_SYSCLK | AH-20 | P0_SDATA[09]# | Y-3 | P0_SDATA[55]# | H-5 |
| NC6 | AA-8 | P0_SADDIN[02]# | Y-4 | P0_SDATA[10]# | AA-1 | P0_SDATA[56]# | M-2 |
| NC8 | AC-8 | P0_SADDIN[03]# | AA-2 | P0_SDATA[11]# | Y-7 | P0_SDATA[57]# | L-4 |
| NC9 | AD-18 | P0_SADDIN[04]# | AA-6 | P0_SDATA[12]# | W-1 | P0_SDATA[58]# | L-2 |
| NC10 | AD-21 | P0_SADDIN[05]# | Y-5 | P0_SDATA[13]# | W-7 | P0_SDATA[59]# | L-1 |
| NC11 | AC-7 | P0_SADDIN[06]# | AA-4 | P0_SDATA[14]# | Y-2 | P0_SDATA[60]# | K-1 |
| NC12 | AD-9 | P0_SADDIN[07]# | AA-3 | P0_SDATA[15]# | U-6 | P0_SDATA[61]# | H-7 |
| NC13 | AE-20 | P0_SADDIN[08]# | AA-5 | P0_SDATA[16]# | U-7 | P0_SDATA[62]# | J-5 |
| NC14 | AE-22 | P0_SADDIN[09]# | AB-3 | P0_SDATA[17]# | R-7 | P0_SDATA[63]# | J-1 |
| NC17 | AJ-1 | P0_SADDIN[10]# | AB-5 | P0_SDATA[18]# | R-6 | P0_SDATAINCLK[0]# | U-5 |
| NC20 | AJ-31 | P0_SADDIN[11]# | Y-6 | P0_SDATA[19]# | R-5 | P0_SDATAINCLK[1]# | R-1 |
| NC21 | AK-2 | P0_SADDIN[12]# | AD-1 | P0_SDATA[20]# | R-3 | P0_SDATAINCLK[2]# | M-1 |
| NC23 | AK-30 | P0_SADDIN[13]# | AC-3 | P0_SDATA[21]# | R-4 | P0_SDATAINCLK[3]# | H-3 |
| NC25 | AL-22 | P0_SADDIN[14]# | AC-1 | P0_SDATA[22]# | R-2 | P0_SDATAINVALID# | AB-1 |
| NC26 | AL-29 | P0_SADDINCLK# | AA-7 | P0_SDATA[23]# | U-2 | P0_SDATAOUTCLK[0]# | W-5 |
| NC27 | AL-3 | P0_SADDOUT[02]# | G-1 | P0_SDATA[24]# | T-7 | P0_SDATAOUTCLK[1]# | R-8 |
| NC28 | B-2 | P0_SADDOUT[03]# | H-2 | P0_SDATA[25]# | V-1 | P0_SDATAOUTCLK[2]# | N-5 |
| NC29 | B-30 | P0_SADDOUT[04]# | G-3 | P0_SDATA[26]# | T-5 | P0_SDATAOUTCLK[3]# | H-1 |
| NC30 | C-1 | P0_SADDOUT[05]# | F-4 | P0_SDATA[27]# | V-2 | P0_SYSFILLVALID# | J-8 |
| NC31 | C-2 | P0_SADDOUT[06]# | H-4 | P0_SDATA[28]# | T-3 | | |
| NC32 | C-31 | P0_SADDOUT[07]# | E-1 | P0_SDATA[29]# | U-1 | | |
| NC35 | E-27 | P0_SADDOUT[08]# | F-3 | P0_SDATA[30]# | P-6 | | |
| NC36 | E-5 | P0_SADDOUT[09]# | F-2 | P0_SDATA[31]# | P-1 | | |
| NC37 | G-25 | P0_SADDOUT[10]# | F-5 | P0_SDATA[32]# | P-2 | | |
| NC38 | G-7 | P0_SADDOUT[11]# | G-5 | P0_SDATA[33]# | P-4 | | |
| NC40 | L-8 | P0_SADDOUT[12]# | F-1 | P0_SDATA[34]# | M-8 | | |
| NC41 | Y-8 | P0_SADDOUT[13]# | E-2 | P0_SDATA[35]# | M-6 | | |
| | | P0_SADDOUT[14]# | D-1 | P0_SDATA[36]# | L-3 | | |
| | | P0_SADDOUTCLK# | E-3 | P0_SDATA[37]# | L-7 | | |
| | | P0_SCHECK[0]# | V-7 | P0_SDATA[38]# | M-4 | | |
| | | P0_SCHECK[1]# | V-8 | P0_SDATA[39]# | L-6 | | |
| | | P0_SCHECK[2]# | P-8 | P0_SDATA[40]# | P-7 | | |
| | | P0_SCHECK[3]# | T-1 | P0_SDATA[41]# | P-5 | | |
| | | P0_SCHECK[4]# | N-7 | P0_SDATA[42]# | N-3 | | |
| | | P0_SCHECK[5]# | N-1 | P0_SDATA[43]# | P-3 | | |
| | | P0_SCHECK[6]# | J-3 | P0_SDATA[44]# | M-5 | | |
| | | P0_SCHECK[7]# | K-3 | P0_SDATA[45]# | M-7 | | |
| | | P0_SDATA[00]# | W-3 | P0_SDATA[46]# | L-5 | | |
| | | P0_SDATA[01]# | V-4 | P0_SDATA[47]# | M-3 | | |
| | | P0_SDATA[02]# | V-3 | P0_SDATA[48]# | K-7 | | |
| | | P0_SDATA[03]# | V-5 | P0_SDATA[49]# | J-6 | | |
| | | P0_SDATA[04]# | V-6 | P0_SDATA[50]# | J-7 | | |
| | | P0_SDATA[05]# | U-4 | P0_SDATA[51]# | K-5 | | |

**Table 31. AMD-762™ System Controller Pin Functional Grouping (4 of 5)**

| Processor 1 AMD Athlon™ System Bus | | | | | |
|---|---|---|---|---|---|
| Name | No. | Name | No. | Name | No. |
| P1_CLKFWDRST | AL-19 | P1_SDATA[07]# | AE-13 | P1_SDATA[53]# | AJ-5 |
| P1_CONNECT | AJ-19 | P1_SDATA[08]# | AL-16 | P1_SDATA[54]# | AL-4 |
| P1_PROCRDY | AE-19 | P1_SDATA[09]# | AD-15 | P1_SDATA[55]# | AH-3 |
| P1_SADDIN[02]# | AG-17 | P1_SDATA[10]# | AG-15 | P1_SDATA[56]# | AE-8 |
| P1_SADDIN[03]# | AH-18 | P1_SDATA[11]# | AF-15 | P1_SDATA[57]# | AE-7 |
| P1_SADDIN[04]# | AL-18 | P1_SDATA[12]# | AJ-16 | P1_SDATA[58]# | AG-6 |
| P1_SADDIN[05]# | AL-17 | P1_SDATA[13]# | AH-17 | P1_SDATA[59]# | AL-6 |
| P1_SADDIN[06]# | AF-17 | P1_SDATA[14]# | AJ-17 | P1_SDATA[60]# | AJ-6 |
| P1_SADDIN[07]# | AG-16 | P1_SDATA[15]# | AH-14 | P1_SDATA[61]# | AE-5 |
| P1_SADDIN[08]# | AG-18 | P1_SDATA[16]# | AF-14 | P1_SDATA[62]# | AH-6 |
| P1_SADDIN[09]# | AD-17 | P1_SDATA[17]# | AF-12 | P1_SDATA[63]# | AL-5 |
| P1_SADDIN[10]# | AK-18 | P1_SDATA[18]# | AE-12 | P1_SDATAINCLK[0]# | AE-15 |
| P1_SADDIN[11]# | AK-17 | P1_SDATA[19]# | AK-12 | P1_SDATAINCLK[1]# | AD-12 |
| P1_SADDIN[12]# | AG-19 | P1_SDATA[20]# | AJ-11 | P1_SDATAINCLK[2]# | AJ-8 |
| P1_SADDIN[13]# | AE-18 | P1_SDATA[21]# | AE-11 | P1_SDATAINCLK[3]# | AK-5 |
| P1_SADDIN[14]# | AF-18 | P1_SDATA[22]# | AG-11 | P1_SDATAINVALID# | AE-17 |
| P1_SADDINCLK# | AJ-18 | P1_SDATA[23]# | AF-11 | P1_SDATAOUTCLK[0]# | AH-15 |
| P1_SADDOUT[02]# | AJ-2 | P1_SDATA[24]# | AK-14 | P1_SDATAOUTCLK[1]# | AH-11 |
| P1_SADDOUT[03]# | AK-3 | P1_SDATA[25]# | AL-13 | P1_SDATAOUTCLK[2]# | AG-9 |
| P1_SADDOUT[04]# | AE-3 | P1_SDATA[26]# | AL-12 | P1_SDATAOUTCLK[3]# | AJ-4 |
| P1_SADDOUT[05]# | AG-3 | P1_SDATA[27]# | AG-13 | P1_SYSFILLVALID# | AL-20 |
| P1_SADDOUT[06]# | AF-3 | P1_SDATA[28]# | AJ-13 | | |
| P1_SADDOUT[07]# | AD-7 | P1_SDATA[29]# | AG-12 | | |
| P1_SADDOUT[08]# | AJ-3 | P1_SDATA[30]# | AJ-12 | | |
| P1_SADDOUT[09]# | AF-2 | P1_SDATA[31]# | AL-11 | | |
| P1_SADDOUT[10]# | AD-5 | P1_SDATA[32]# | AG-7 | | |
| P1_SADDOUT[11]# | AD-6 | P1_SDATA[33]# | AF-9 | | |
| P1_SADDOUT[12]# | AF-1 | P1_SDATA[34]# | AK-11 | | |
| P1_SADDOUT[13]# | AH-1 | P1_SDATA[35]# | AL-10 | | |
| P1_SADDOUT[14]# | AG-2 | P1_SDATA[36]# | AK-8 | | |
| P1_SADDOUTCLK# | AG-1 | P1_SDATA[37]# | AL-8 | | |
| P1_SCHECK[0]# | AG-14 | P1_SDATA[38]# | AH-8 | | |
| P1_SCHECK[1]# | AL-15 | P1_SDATA[39]# | AK-9 | | |
| P1_SCHECK[2]# | AH-12 | P1_SDATA[40]# | AE-10 | | |
| P1_SCHECK[3]# | AJ-10 | P1_SDATA[41]# | AE-9 | | |
| P1_SCHECK[4]# | AL-9 | P1_SDATA[42]# | AD-11 | | |
| P1_SCHECK[5]# | AG-8 | P1_SDATA[43]# | AG-10 | | |
| P1_SCHECK[6]# | AF-6 | P1_SDATA[44]# | AJ-9 | | |
| P1_SCHECK[7]# | AL-7 | P1_SDATA[45]# | AH-9 | | |
| P1_SDATA[00]# | AE-14 | P1_SDATA[46]# | AF-8 | | |
| P1_SDATA[01]# | AJ-14 | P1_SDATA[47]# | AJ-7 | | |
| P1_SDATA[02]# | AE-16 | P1_SDATA[48]# | AF-4 | | |
| P1_SDATA[03]# | AD-14 | P1_SDATA[49]# | AG-5 | | |
| P1_SDATA[04]# | AJ-15 | P1_SDATA[50]# | AF-5 | | |
| P1_SDATA[05]# | AL-14 | P1_SDATA[51]# | AK-6 | | |
| P1_SDATA[06]# | AK-15 | P1_SDATA[52]# | AH-4 | | |

**Table 32. AMD-762™ System Controller Pin Functional Grouping (5 of 5)**

| VDD | | | | | | VSS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | No. | Name | No. | Name | No. | Name | No | Name | No. | Name | No. | Name | No. |
| VDD_CORE | AA-11 | VDD_CORE | M-22 | VDD_CORE | Y-18 | VSS | D-5 | VSS | M-9 | VSS | U-10 | VSS | AB-15 |
| VDD_CORE | AA-13 | VDD_CORE | N-11 | VDD_CORE | Y-20 | VSS | D-7 | VSS | M-11 | VSS | U-12 | VSS | AB-17 |
| VDD_CORE | AA-15 | VDD_CORE | N-13 | VDD_CORE | F-7 | VSS | D-10 | VSS | M-13 | VSS | U-14 | VSS | AB-19 |
| VDD_CORE | AA-17 | VDD_CORE | N-15 | | | VSS | D-13 | VSS | M-15 | VSS | U-16 | VSS | AB-21 |
| VDD_CORE | AA-19 | VDD_CORE | N-17 | | | VSS | D-16 | VSS | M-17 | VSS | U-18 | VSS | AB-23 |
| VDD_CORE | B-10 | VDD_CORE | N-19 | | | VSS | D-19 | VSS | M-19 | VSS | U-20 | VSS | AB-24 |
| VDD_CORE | B-13 | VDD_CORE | N-21 | | | VSS | D-22 | VSS | M-21 | VSS | U-22 | VSS | AB-28 |
| VDD_CORE | B-16 | VDD_CORE | P-12 | VDD_AGP | AA-23 | VSS | D-25 | VSS | M-23 | VSS | V-9 | VSS | AC-10 |
| VDD_CORE | B-19 | VDD_CORE | P-14 | VDD_AGP | AB-26 | VSS | D-27 | VSS | N-4 | VSS | V-11 | VSS | AC-12 |
| VDD_CORE | B-22 | VDD_CORE | P-16 | VDD_AGP | AB-30 | VSS | E-4 | VSS | N-8 | VSS | V-13 | VSS | AC-14 |
| VDD_CORE | B-25 | VDD_CORE | P-18 | VDD_AGP | AC-23 | VSS | E-28 | VSS | N-10 | VSS | V-15 | VSS | AC-16 |
| VDD_CORE | B-28 | VDD_CORE | P-20 | VDD_AGP | AF-22 | VSS | G-4 | VSS | N-12 | VSS | V-17 | VSS | AC-18 |
| VDD_CORE | B-4 | VDD_CORE | P-22 | VDD_AGP | AE-26 | VSS | G-28 | VSS | N-14 | VSS | V-19 | VSS | AC-20 |
| VDD_CORE | B-7 | VDD_CORE | R-11 | VDD_AGP | AE-30 | VSS | H-8 | VSS | N-16 | VSS | V-21 | VSS | AC-22 |
| VDD_CORE | F-10 | VDD_CORE | R-13 | VDD_AGP | AH-30 | VSS | H-10 | VSS | N-18 | VSS | V-23 | VSS | AD-8 |
| VDD_CORE | F-13 | VDD_CORE | R-15 | VDD_AGP | AK-22 | VSS | H-13 | VSS | N-20 | VSS | W-4 | VSS | AD-10 |
| VDD_CORE | F-16 | VDD_CORE | R-17 | VDD_AGP | AK-25 | VSS | H-16 | VSS | N-22 | VSS | W-8 | VSS | AD-13 |
| VDD_CORE | F-19 | VDD_CORE | R-19 | VDD_AGP | AK-28 | VSS | H-19 | VSS | N-24 | VSS | W-10 | VSS | AD-16 |
| VDD_CORE | F-22 | VDD_CORE | R-21 | VDD_AGP | AF-25 | VSS | H-22 | VSS | N-28 | VSS | W-12 | VSS | AD-19 |
| VDD_CORE | F-25 | VDD_CORE | T-12 | VDD_AGP | Y-22 | VSS | H-24 | VSS | P-9 | VSS | W-14 | VSS | AD-22 |
| VDD_CORE | J-11 | VDD_CORE | T-14 | VDD_AGP | AB-22 | VSS | J-10 | VSS | P-11 | VSS | W-16 | VSS | AD-24 |
| VDD_CORE | J-13 | VDD_CORE | T-16 | VDD_AGP | AC-21 | VSS | J-12 | VSS | P-13 | VSS | W-18 | VSS | AE-4 |
| VDD_CORE | J-15 | VDD_CORE | T-18 | VDD_AGP | AA-21 | VSS | J-14 | VSS | P-15 | VSS | W-20 | VSS | AE-28 |
| VDD_CORE | J-17 | VDD_CORE | T-20 | VDD_AGP | AB-20 | VSS | J-16 | VSS | P-17 | VSS | W-22 | VSS | AG-4 |
| VDD_CORE | J-19 | VDD_CORE | T-22 | | | VSS | J-18 | VSS | P-19 | VSS | W-24 | VSS | AG-21 |
| VDD_CORE | J-21 | VDD_CORE | U-11 | VDD_PCI | D-30 | VSS | J-20 | VSS | P-21 | VSS | W-28 | VSS | AG-28 |
| VDD_CORE | J-23 | VDD_CORE | U-13 | VDD_PCI | G-30 | VSS | J-22 | VSS | P-23 | VSS | Y-9 | VSS | AH-5 |
| VDD_CORE | J-9 | VDD_CORE | U-15 | VDD_PCI | K-30 | VSS | K-4 | VSS | R-10 | VSS | Y-11 | VSS | AH-7 |
| VDD_CORE | K-10 | VDD_CORE | U-17 | VDD_PCI | N-30 | VSS | K-8 | VSS | R-12 | VSS | Y-13 | VSS | AH-10 |
| VDD_CORE | K-12 | VDD_CORE | U-19 | VDD_PCI | G-26 | VSS | K-9 | VSS | R-14 | VSS | Y-15 | VSS | AH-13 |
| VDD_CORE | K-14 | VDD_CORE | U-21 | VDD_PCI | K-26 | VSS | K-11 | VSS | R-16 | VSS | Y-17 | VSS | AH-16 |
| VDD_CORE | K-16 | VDD_CORE | V-12 | VDD_PCI | N-26 | VSS | K-13 | VSS | R-18 | VSS | Y-19 | VSS | AH-19 |
| VDD_CORE | K-18 | VDD_CORE | V-14 | VDD_PCI | T-26 | VSS | K-15 | VSS | R-20 | VSS | Y-21 | VSS | AH-22 |
| VDD_CORE | K-20 | VDD_CORE | V-16 | VDD_PCI | W-26 | VSS | K-17 | VSS | R-22 | VSS | Y-23 | VSS | AH-25 |
| VDD_CORE | K-22 | VDD_CORE | V-18 | VDD_PCI | L-23 | VSS | K-19 | VSS | T-4 | VSS | AA-10 | VSS | AH-27 |
| VDD_CORE | L-11 | VDD_CORE | V-20 | VDD_PCI | N-23 | VSS | K-21 | VSS | T-8 | VSS | AA-12 | VSS | AJ-20 |
| VDD_CORE | L-13 | VDD_CORE | V-22 | VDD_PCI | R-23 | VSS | K-23 | VSS | T-9 | VSS | AA-14 | | |
| VDD_CORE | L-15 | VDD_CORE | W-11 | VDD_PCI | U-23 | VSS | K-24 | VSS | T-11 | VSS | AA-16 | | |
| VDD_CORE | L-17 | VDD_CORE | W-13 | VDD_PCI | W-23 | VSS | K-28 | VSS | T-13 | VSS | AA-18 | | |
| VDD_CORE | L-19 | VDD_CORE | W-15 | VDD_PCI | T-30 | VSS | L-10 | VSS | T-15 | VSS | AA-20 | | |
| VDD_CORE | L-21 | VDD_CORE | W-17 | VDD_PCI | W-30 | VSS | L-12 | VSS | T-17 | VSS | AA-22 | | |
| VDD_CORE | M-12 | VDD_CORE | W-19 | A_VDD | AG-22 | VSS | L-14 | VSS | T-19 | VSS | AB-4 | | |
| VDD_CORE | M-14 | VDD_CORE | W-21 | | | VSS | L-16 | VSS | T-21 | VSS | AB-8 | | |
| VDD_CORE | M-16 | VDD_CORE | Y-12 | | | VSS | L-18 | VSS | T-23 | VSS | AB-9 | | |
| VDD_CORE | M-18 | VDD_CORE | Y-14 | | | VSS | L-20 | VSS | T-24 | VSS | AB-11 | | |
| VDD_CORE | M-20 | VDD_CORE | Y-16 | | | VSS | L-22 | VSS | T-28 | VSS | AB-13 | | |

# 7 Signal Descriptions

Table 34 on page 82 contains a description of the AMD-762™ system controller signals.

Table 33 describes the terms used in the signal description table. The signals are organized within the following functional groups:

- Processor interface signals (page 82)
- PCI interface signals (page 84)
- DRAM interface signals (page 87)
- AGP/PCI signals (page 89)
- AGP-only signals (page 91)
- Initialization pinstrapping (page 94)
- Miscellaneous signals (page 92)
- Pin multiplexing options (page 98)

**Table 33. Signal Descriptions Table Definitions**

| Signal Types | |
|---|---|
| B | Bidirectional |
| I | Input |
| O | Output |
| STS | Sustained three-state |
| TS | Three-state |

**Table 34. Signal Descriptions**

| Signal | Type | Description |
|---|---|---|
| **Processor Interface Signals** | | |
| CLKFWDRST | O | **AMD Athlon™ Processor System Bus Clock Forward Reset**<br>CLKFWDRST resets the source-synchronous clock circuitry for the processor. Forwarded clocks are driven continuously beginning three clocks after CLKFWDRST is negated.<br>This signal is negated by RESET#. It changes on the rising edge of SYSCLK. |
| CONNECT | O | **AMD Athlon Processor System Bus Connect**<br>CONNECT is an output from the AMD-762™ system controller and is used for power management and source-synchronous clock initialization at reset.<br>This signal is negated by RESET#. It changes on the rising edge of SYSCLK. |
| PROCRDY | I | **AMD Athlon Processor System Bus Connect Processor Ready**<br>PROCRDY is an input to the AMD-762 system controller and is used for power management and source-synchronous clock initialization at reset.<br>This signal is sampled on the rising edge of SYSCLK. |
| SADDIN[14:2]# | O | **AMD Athlon Processor System Bus Connect Address/Command**<br>SADDIN[14:2]# is a unidirectional system command bus to the processor. It is used to transfer probe and data movement commands into the processor. SADDIN[14:2]# are skew-aligned with the source-synchronous clock, SADDINCLK#. The AMD-762 system controller drives the SADDIN[14:2]# channel on each edge of SADDINCLK#. |
| SADDINCLK# | O | **AMD Athlon Processor System Bus Connect System Address In Clock**<br>SADDINCLK# is the single-ended source-synchronous clock for the SADDIN[14:2]# bus, driven by the AMD-762 system controller. Each clock edge is used to transfer probe and data movement commands to the processor.<br>This signal is driven inactive (negated) when the CLKFWDRST signal is asserted (true). When CLKFWDRST is negated, SADDINCLK# runs continuously after a three clock delay. |
| SADDOUT[14:2]# | I | **AMD Athlon Processor System Bus Connect System Address Out**<br>SADDOUT[14:2]# is a unidirectional system address interface from the processor to the AMD-762 system controller. The SADDOUT[14:2]# channel is used to transfer processor requests and probe responses to the system. This channel is skew-aligned with the source-synchronous clock, SADDOUTCLK#. The SADDOUT[14:2]# channel is sampled by the AMD-762 system controller on each edge of SADDOUTCLK#.<br>The AMD-762 system controller samples commands driven by the processor on the SADDOUT[14:2]# channel and forwards them to the PCI bus, AGP bus, or DRAM, depending on the address range and AMD-762 system controller configuration. |
| SADDOUTCLK# | I | **AMD Athlon Processor System Bus Connect System Address Out Clock**<br>SADDOUTCLK# is a single-ended source synchronous clock for the SADDOUT[14:2]# channel driven by the processor. Each edge is used to transfer commands.<br>This signal is driven inactive (negated) when the CLKFWDRST signal is asserted (true). When CLKFWDRST is negated, SADDOUTCLK# runs continuously after a three-clock delay. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| SCHECK[7:0]# | B | **AMD Athlon™ Processor System Bus Data Bus Check Byte**<br>SCHECK[7:0]# transfer ECC check bits for data transferred on the SDATA[63:0]# bus.<br>*As Outputs:* The AMD-762™ system controller drives SCHECK[7:0]# with each valid data quadword. SCHECK[7:0]# are skew-aligned with the source-synchronous clocks, SDATAINCLK[3:0]#.<br>*As Inputs:* The AMD-762 system controller samples SCHECK[7:0]# and transfers the data to the memory. SCHECK[7:0]# are sampled by the AMD-762™ system controller on each edge of SDATAOUTCLK[3:0]#.<br>SCHECK[7:0]# are floated by RESET#. Check bits for write data are driven by the processor and check bits for read data are driven by the system controller. The AMD-762 system controller drives the previous data value between transfers to prevent floating inputs. |
| SDATA[63:0]# | B | **AMD Athlon Processor System Bus Processor Data Channel**<br>The SDATA[63:0]# transfer data between the processor and system.<br>*As Outputs:* The AMD-762 system controller drives SDATA[63:0]# with each valid data quadword. SDATA[63:0]# are skew-aligned with the source-synchronous clocks, SDATAINCLK[3:0]#.<br>*As Inputs:* The AMD-762 system controller samples SDATA[63:0]# and transfers the data to the memory. The SDATA[63:0]# are sampled by the AMD-762 system controller on each edge of SDATAOUTCLK[3:0]#.<br>SDATA[63:0]# are floated out of RESET#. Write data is driven by the processor and read data is driven by the system controller. The AMD-762 system controller drives the previous data value between transfers to prevent floating inputs. |
| SDATAINCLK[3:0]# | O | **AMD Athlon Processor System Bus System Data In Clock**<br>SDATAINCLK[3:0]# is the single-ended source-synchronous clock driven by the AMD-762 system controller to transfer data on SDATA[63:0]# and check bits on SCHECK[7:0]#. Sixteen bits of data and two check bits are skew-aligned with each clock. Data is transferred on each clock edge.<br>These signals are driven inactive (negated) when the CLKFWDRST signal is asserted (true). When CLKFWDRST is negated, SDATAINCLK[3:0]# run continuously after three clock delays. |
| SDATAINVAL# | O | **AMD Athlon Processor System Bus System Data In Valid**<br>SDATAINVAL# is driven by the AMD-762 system controller and controls the flow of data into the processor. SDATAINVAL# can be used to introduce an arbitrary number of cycles between quadword pairs (128 bits). SDATAINVAL# is skew-aligned with the source-synchronous clock, SADDINCLK#. |
| SDATAOUTCLK[3:0]# | I | **AMD Athlon Processor System Bus System Address Out Clock**<br>SDATAOUTCLK[3:0]# is the single-ended source-synchronous clock driven by the processor and is used to transfer data and check bits on the SDATA[63:0]# and SCHECK[7:0]#. Sixteen bits of data and two check bits are skew-aligned with each clock. Data is transferred on each clock edge.<br>These signals are driven inactive (negated) when the CLKFWDRST signal is asserted (true). When CLKFWDRST is negated, SDATAOUTCLK[3:0]# run continuously after three clock delays. |
| SYSCLK | I | **AMD Athlon Processor System Bus System Clock**<br>SYSCLK is a single-ended input clock signal provided by the system clock generator to the phase locked loop (PLL) of the AMD-762 system controller. Frequencies of 66.67 MHz, 100 MHz, or 133.33 MHz are supported. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| SYSFILLVALID# | O | **AMD Athlon™ Processor System Bus Fill Valid**<br>This pin is asserted by the AMD-762™ system controller to validate the current memory or I/O data transfer to the processor. SYSFILLVALID# can be sampled by the CPU during D0 or D1 data phases. |
| **PCI Interface Signals** | | |
| AD[63:00] | B<br>*TS* | **PCI Address/Data Bus**<br>This is the multiplexed address/data bus, sampled on the rising edge of PCICLK. The address is valid on AD[63:00] during the first clock when FRAME# is asserted. Write data is valid on AD[63:00] when IRDY# is asserted and read data is valid when TRDY# is asserted. Data transfers occur on AD[63:00] when both IRDY# and TRDY# are asserted. Data transfers may be 32 bits or 64 bits based on the REQ64#/ACK64# protocol.<br>The AD[31:0] pins are also used for initialization pinstrapping to configure various startup parameters of the AMD-762 system controller. The initialization pinstraps are configured with a weak pullup or pulldown and sampled by the AMD-762 system controller during system reset. Refer to the “Initialization Pinstrapping” section at the end of this table for further details. |
| C/BE[7:0]# | B<br>*TS* | **PCI Command/Byte Enables**<br>During the address phase, these pins define the PCI command. During the data phase these pins are used as byte enables. The byte enables for the upper 32 bits of data (C/BE[7:4]) are used only during 64-bit transfers that are determined by the REQ64#/ACK64# protocol.<br>These pins are also used for initialization pinstrapping to configure various startup parameters of the AMD-762 system controller. The initialization pinstraps are configured with a weak pullup or pulldown and sampled by the AMD-762 system controller during system reset. Refer to the “Initialization Pinstrapping” section at the end of this table for further details. |
| DEVSEL# | B<br>*STS* | **PCI Device Select**<br>The AMD-762 system controller asserts this pin when an external bus master drives a valid address within the AMD-762 system controller’s memory region, as defined by the PCI Top of Memory register (Dev 0:F0:0x9C). The AMD-762 system controller responds only to memory cycles. This pin is sampled by the AMD-762 system controller when the CPU accesses a PCI target. |
| FRAME# | B<br>*STS* | **PCI Cycle Frame**<br>The FRAME# pin is asserted by the AMD-762 system controller to indicate the beginning of a bus transaction. FRAME# is sampled by the AMD-762 PCI target controller when an external bus master is performing a transaction on the PCI bus. |
| GNT[6:0]# | O<br>*TS* | **PCI Bus Grant**<br>As the PCI bus arbiter, the AMD-762 system controller asserts one of these device-specific bus grant signals off the rising clock edge to indicate to an initiator that it has been granted control of the PCI bus the next time the bus is idle. In 66-MHz PCI mode only, GNT[2:0]# are used and all other grant pins are unconnected on the motherboard.<br>GNT[6:0]# signals are never floated. They are negated off the rising edge of the PCICLK input, indicating that no device has been granted the bus. One of the GNT[6:0]# signals is asserted off the rising edge of the clock, indicating the particular channel that is granted use of the bus.<br>These pins are also optionally used in test modes as described in Table 36 on page 98, and in Chapter 3. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| IRDY# | B<br>*STS* | **PCI Initiator Ready**<br>The AMD-762™ system controller asserts this signal during PCI transactions to indicate that write data is valid or it is ready to receive read data. It is sampled by the AMD-762 system controller during memory transactions by external bus masters to DRAM.<br>This pin is also optionally used in test modes as described in Table 36 on page 98, and in Chapter 3. |
| PAR | B<br>*TS* | **PCI Bus Parity**<br>PAR is used to generate and check for even parity across the AD[31:0] and C/BE[3:]# pins. The AMD-762 system controller generates but does not check parity.<br>This pin is also optionally used in test modes as described in Table 36 on page 98, and in Chapter 3. |
| PAR64 | B<br>*TS* | **Parity 64**<br>This pin is used to provide the parity bit for the upper 32 bits of data and upper four byte enables. |
| PCICLK | I | **PCI Clock**<br>PCICLK is a 33.33-MHz clock provided by the system clock generator. It is used by the AMD-762 system controller logic in the PCI clock domain when operating in 33-MHz mode only. When operating in 66/33-MHz mode, this pin is used as the feedback clock to the internal PLL. Refer to Chapter 2 for details on the PCI clocking options in the AMD-762 system controller. |
| M66EN | I | **66-MHz Enable**<br>This signal indicates that all peripherals on the PCI bus segment support 66-MHz operation. When Low, this signal indicates that a card is installed that supports only 33-MHz (or below) operation, and the AMD-762 system controller must operate at this speed instead of 66 MHz. |
| PCI_66CLK[2:0] | O | **66-MHz PCI Clock Outputs**<br>These clocks are provided to a 66-MHz Southbridge and two 66-MHz PCI slots when operating in 66/33-MHz PCI mode. When operating in 33-MHz-only mode, these pins are unused. Note that if the M66EN pin (see above) is deasserted, then these clocks are scaled back to 33 MHz. Refer to Chapter 2 for details on the PCI clocking options in the AMD-762 system controller. |
| SBGNT# | O<br>*TS* | **PCI Grant to Peripheral Bus Controller**<br>SBGNT# grants control of the PCI bus to the PCI-ISA/IDE bridge functions implemented in the AMD-768™ peripheral bus controller or AMD-766™ peripheral bus controller.<br>SBGNT# is driven off the rising edge of PCICLK. RESET# forces SBGNT# inactive. SBGNT# is asserted in response to a SBREQ#. SBGNT# and GNT[6:0]# all grant control of the bus to an external device. |
| SBREQ# | I | **PCI Request from Peripheral Bus Controller**<br>The AMD-762 system controller samples SBREQ# to determine if the AMD-768 or AMD-766 peripheral bus controller needs PCI bus access.<br>This signal is sampled by the rising edge of every PCICLK. If asserted, the arbiter issues a SBGNT# when the bus is available. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| REQ[6:0]# | I | **PCI Bus Request**<br>As the PCI bus arbiter, the AMD-762™ system controller samples these device-specific bus request signals to determine if another agent requires control of the PCI bus. In 66-MHz PCI mode only, REQ[2:0]# is used and all remaining request signals must be pulled up to the inactive state.<br>These signals are sampled by the rising edge of every PCICLK. If active, the arbiter issues the corresponding GNT[6:0]# when the bus is available. |
| REQ64# | B<br>*STS* | **Request 64**<br>This pin is used to signal that the master requests a 64-bit transfer. The AMD-762 system controller must assert this signal (Low) during reset (RESET# asserted Low) to signal 64-bit devices that they can operate in 64-bit mode. |
| ACK64# | B<br>*STS* | **Acknowledge 64**<br>This pin is used to signal that the agent is capable of completing a 64-bit transfer. |
| RESET# | I | **System Reset**<br>Asserting RESET# resets the AMD-762 system controller and sets all register bits to their default values (except memory controller registers as required for ACPI S3 support). Bidirectional signals are three-stated and outputs are driven inactive. RESET# is driven by the PCIRST# output of the AMD-768™ peripheral bus controller or AMD-766™ peripheral bus controller. See "Pin States at Reset" on page 98.<br>This signal may be asynchronous to SYSCLK and PCICLK. It is synchronized internally, therefore it must be active for a minimum of four PCICLK periods. |
| SERR# | O<br>*OD* | **PCI System Error**<br>SERR# is used by the AMD-762 system controller to transfer GART errors, ECC errors, or AGP A_SERR# pin assertion errors to error reporting logic on the AMD-766 peripheral bus controller. |
| STOP# | B<br>*STS* | **PCI Stop**<br>As a target, the STOP# signal is asserted by the AMD-762 PCI target logic to initiate a target disconnect, ending the current transfer. As a master, the AMD-762 system controller ends the current transfer when it samples the STOP# signal asserted. |
| TRDY# | B<br>*STS* | **PCI Target Ready**<br>TRDY# is asserted by the AMD-762 system controller during accesses of DRAM by an external bus master when read data is valid or when the target logic is ready to receive write data. This signal is sampled by the AMD-762 PCI master logic when the AMD-762 system controller is accessing an external PCI target.<br>This pin is also optionally used in test modes as described in Table 36 on page 98, and in Chapter 3. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| WSC# | B<br>*TS* | **PCI Write Snoop Complete**<br>WSC# is asserted to indicate that all of the snoop activity on the processor bus on behalf of the last PCI-to-DRAM write transaction is complete. It indicates that an APIC interrupt message can be sent. This signal is used only in configurations where an I/O APIC is installed.<br>WSC# is driven asserted on the rising edge of PCICLK to indicate to the AMD-766™ peripheral bus controller that all probes due to PCI DMA (direct memory access) are complete.<br>The AMD-768™ peripheral bus controller or AMD-766™ peripheral bus controller requests that the AMD-762™ system controller issue a fence command to its buffers by placing a single PCICLK pulse on WSC#. The AMD-762 system controller then marks the data currently in its buffers and waits for this data to reach processor-accessible (coherent) space. When this data reaches processor-accessible space, the AMD-762 system controller responds by sending a two-clock pulse back to the AMD-768 or AMD-766 peripheral bus controller. After this pulse is received, the AMD-766 peripheral bus controller transmits the interrupt message over the interrupt message bus (IMB). |
| **DDR DRAM Interface Signals**<br>***Note:*** *DDR outputs are SSTL-2 compatible.* | | |
| CS[7:0]# | O | **DDR DIMM Chip Selects**<br>CS[7:0]# function as chip-select signals for the DDR DRAMs.<br>These signals are negated by RESET#. The memory controller asserts or negates these signals relative to CLKOUT at the appropriate time in the memory access sequence. CS[7:0] are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, “Functional Operation” starting on page 7 for more information. |
| DM[8:0] | B | **DDR Data Masks/Data Strobes (for x4 DIMMs only)**<br>DM[8:0] provides data masks for each byte during DDR writes to x8 and x16 DIMMs only. For x4 DIMMs, these pins are used to provide the additional DQS pins required in x4 DIMM configurations. DM signals are not provided by x4 DIMMs. In the absence of the DM function, partial writes result in full-line read-modify-write cycles with all bytes being written active on the DIMM.<br>These control signals are three-stated by RESET# and remain three-stated until driven by the AMD-762 system controller during writes or by the DDR DRAM during reads. During DDR writes to x8 and x16 DIMMs, the memory controller asserts or negates these signals relative to the DQS[8:0] clock signals (described below). For x4 DIMMs, these pins function as additional DQS strobe signals. See Chapter 2, “Functional Operation” starting on page 7 for more information. |
| DQS[8:0] | B | **DDR Data Strobes**<br>DQS[8:0] are bidirectional data strobes between the memory devices and the memory controller that are used to capture data. The data strobes (DQS signals) are source-synchronous, which means that the DQS signals are driven by the device that is driving the data. The “source-synchronous strobe” scheme is also referred to as the “clock-forwarded” scheme. The AMD-762 system controller provides one DQS signal per byte of data for x8 and x16 DIMMs, or one DQS signal per nibble of x4 DIMMs. During a x4 DIMM access, the DM pins provide the additional DQS strobe signals, which function the same as the DQS strobe signals. An access to a x4 DIMM requires 18 data strobes (including ECC), which are the DQS[8:0] and DM[8:0] pins combined. The AMD-762 system controller implements a DQS scheme on the DDR interface that is similar to the clock-forwarded scheme used on the AMD Athlon system bus interface. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| MAA[14:0] and MAB[14:0] | O | **DDR Memory Address**<br>The multiplexed row and column address bits MAA[14:0] and MAB[14:0] connect to the system DDR SDRAMs. Two sets of memory addresses are provided to reduce signal loading for motherboard designs with more than one DIMM slot. In an effort to reduce switching noise on the DDR interface, the MAB bus is an inverted copy of the MAA bus, with the exception of the MA[10] bit that remains un-inverted on the MAB bus. The MAB bus is **not** inverted from the MAA bus during the DDR device initialization phase.<br>The memory controller asserts or de-asserts these signals relative to CLKOUT at the appropriate time in the memory access sequence. MAA[14:0] and MAB[14:0] are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, "Functional Operation" starting on page 7 for more information. |
| CKEA and CKEB | O | **DDR Clock Enables**<br>CKEA and CKEB are clock enable signals for the DDR DRAMs and are used for power saving modes. They operate in parallel to drive greater loads than a single signal can support.<br>These control signals are driven inactive (negated) by RESET# or when the DDR devices are placed in self refresh mode. The memory controller asserts or de-asserts these signals relative to CLKOUT at the appropriate time in the memory access sequence. CKEA and CKEB are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, "Functional Operation" beginning on page 7 for more information. |
| MDAT[63:0] | B | **DDR Memory Data**<br>MDAT[63:0] connect to the DRAM data I/O. They are driven by the DDR DRAM during reads and are driven by the AMD-762™ system controller during writes. During writes, the AMD-762 system controller provides the clock-forwarded DQS[8:0] strobes centered within the write data. The DQS strobes are used to capture the write data at the DDR DRAMs. (The DM pins provide additional strobes when accessing a x4 DIMM.) During reads, the DDR DRAMs source the DQS strobes **aligned** with MDAT and are used within the AMD-762 system controller to capture read data. (The DM pins are used to receive the DQS signals from the DDR DRAMs when accessing a x4 DIMM.)<br>MDAT[63:0] are floated when neither the AMD-762 system controller nor the memory are driving the bus. |
| MECC[7:0] | B | **DDR ECC**<br>MECC[7:0] carry error correction codes for the eight bytes of data on MDAT[63:0]. These signals are inputs to the AMD-762 system controller during DRAM read cycles and outputs during DRAM write cycles. During writes, the AMD-762 system controller provides the clock-forwarded DQS[8:0] strobes centered within the write data. The DQS strobes are used to capture the ECC write data at the DDR DRAMs. (The DM pins provide additional strobes when accessing a x4 DIMM.) During reads, the DDR DRAMs source the DQS strobes **aligned** with MECC and are used within the AMD-762 system controller to capture the ECC read data. (The DM pins are used to receive the DQS signals from the DDR DRAMs when accessing a x4 DIMM.)<br>MECC[7:0] are floated when neither the AMD-762 system controller nor the memory are driving the bus. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| CASA# and CASB# | O | **DDR Column Address Strobes**<br>CASA# and CASB# are column address strobe signals for the DDR DRAMs. They operate in parallel to drive greater loads than a single signal can support. The CASx signal is 1 bit of the 3-bit DDR DRAM command bus.<br>These control signals are driven inactive (negated) by RESET#. The memory controller asserts or de-asserts these signals relative to CLKOUT at the appropriate time in the memory access sequence. CASA and CASB are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, "Functional Operation" starting on page 7 for more information. |
| CLKOUT[5:0] and CLKOUT[5:0]# | O | **DDR Clock Outputs**<br>CLKOUT[5:0] and CLKOUT[5:0]# are differential clock pairs to the DDR DIMMs. The clock pairs can be individually disabled for unpopulated DIMM sockets. |
| RASA# and RASB# | O | **DDR Row Address Strobes**<br>RASA# and RASB# are row address strobe signals for the DDR DRAM. They operate in parallel to drive greater loads than a single signal can support. The RASx signal is 1 bit of the 3-bit DDR DRAM command bus.<br>These control signals are driven inactive (negated) by RESET#. The memory controller asserts or de-asserts these signals relative to CLKOUT at the appropriate time in the memory access sequence. RASA and RASB are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, "Functional Operation" starting on page 7 for more information. |
| WEA# and WEB# | O | **DDR Memory Write Enables**<br>WEA# and WEB# are write enable signals for the DDR DRAM. They operate in parallel to drive greater loads than a single signal can support. The WEx signal is 1 bit of the 3-bit DDR DRAM command bus.<br>These control signals are driven inactive (negated) by RESET#. The memory controller asserts or de-asserts these signals relative to CLKOUT at the appropriate time in the memory access sequence. WEA and WEB are driven a quarter of a cycle off from the CLKOUT rising edge to provide additional HOLD time. See Chapter 2, "Functional Operation" starting on page 7 for more information. |
| **AGP/PCI Signals** | | |
| A_AD[31:00] | B<br>*TS* | **AGP/APCI Address/Data Bus**<br>These pins are the multiplexed address/data bus, sampled on the rising edge of AGPCLK. The address is valid on A_AD[31:00] during the first clock when FRAME# is asserted. Write data is valid on A_AD[31:00] when A_IRDY# is asserted and read data is valid when A_TRDY# is asserted. Data transfers occur on A_AD[31:00] when both A_IRDY# and A_TRDY# are asserted. |
| A_C/BE[3:0]# | B<br>*TS* | **AGP/APCI Command/Byte Enables**<br>During the address phase, these pins define the PCI command. During the data phase these pins are used as byte enables. |
| AGPCLK | I | **AGP/APCI Clock**<br>AGPCLK receives a 66-MHz clock from the system clock generator. AGPCLK is used by the AMD-762™ system controller logic in the AGP clock domain. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| A_DEVSEL# | B<br>*STS* | **APCI Device Select**<br>The AMD-762™ system controller asserts this pin when an external bus master drives a valid address within the memory region of the AMD-762 system controller. The AMD-762 system controller responds only to memory cycles. This pin is sampled by the AMD-762 system controller when the CPU accesses a PCI target.<br>A_DEVSEL# is not used during AGP transfers. |
| A_FRAME# | B<br>*STS* | **APCI Cycle Frame**<br>The A_FRAME# pin is asserted by the AMD-762 system controller to indicate the beginning of a bus transaction. A_FRAME# is sampled by the AMD-762 APCI target controller when an external bus master is performing a transaction on the PCI bus.<br>A_FRAME# is not used during AGP transfers. |
| A_GNT# | O<br>*TS* | **AGP/APCI Bus Grant**<br>As the AGP bus arbiter, the AMD-762 system controller asserts A_GNT# in response to A_REQ# from the initiator (graphics controller) to indicate to the initiator that it has been granted control of the bus. At the same time, the system controller provides status information on status signals ST[2:0] to indicate to the initiator whether it is to supply data or receive data in response to a previously queued request.<br>A_GNT# is asserted in response to an A_REQ#. A reset forces A_GNT# to be negated. |
| A_IRDY# | B<br>*STS* | **AGP/APCI Initiator Ready**<br>The AMD-762 system controller asserts this signal during APCI transactions to indicate that write data is valid or it is ready to receive read data. It is sampled by the AMD-762 system controller during transactions by the AGP master. |
| A_PAR | B<br>*TS* | **APCI Bus Parity**<br>PAR is used to generate and check for even parity across the AAD[31:00] and A_C/BE[3:]# pins. The AMD-762 system controller generates but does not check parity.<br>A_PAR# is not used during AGP transfers. |
| A_REQ# | I | **AGP/APCI Bus Request**<br>As the bus arbiter, the AMD-762 system controller monitors A_REQ# to determine if the graphics controller requests access to the AGP bus. If A_REQ# is sampled asserted, the arbiter asserts A_GNT# as soon as the bus is available. |
| A_SERR# | I | **APCI System Error**<br>A_SERR# is not used during AGP transfers. An assertion on the A_SERR# pin during APCI transfers can be forwarded to the PCI SERR# pin when enabled in AMD-762 configuration registers. |
| A_STOP# | B<br>*STS* | **APCI Bus Stop**<br>The A_STOP# signal is asserted by the AMD-762 APCI target logic to initiate a disconnect by the AGP master. As a master, the AMD-762 system controller stops the current transfer when it samples the A_STOP# signal asserted.<br>A_STOP# is not used during AGP transfers. |
| A_TRDY# | B<br>*STS* | **AGP/APCI Target Ready**<br>The A_TRDY# signal is asserted by the AMD-762 system controller during accesses by an external bus master when read data is valid or when the target logic is ready to receive write data. This signal is sampled by the AMD-762 AGP master logic when the AMD-762 system controller is accessing an external APCI target. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| **AGP-Only Signals** | | |
| ADSTB[1:0] | B<br>*STS* | **AGP AD Bus Strobe**<br>These signals are driven by the agent that is providing the data and are used to generate a timing strobe for 2x AGP transfers. ADSTB[0] is used for A_AD[15:00], and ADSTB[1] is used for A_AD[31:16]. |
| ADSTB[1:0]# | B<br>*STS* | **AGP AD Bus Strobe (4x Timing)**<br>These signals are driven by the agent that is providing the data, and are used to generate a timing strobe for 4x AGP transfers. ADSTB[0]# is used for A_AD[15:00], and ADSTB[1]# is used for A_AD[31:16]. |
| PIPE# | I<br>*STS* | **APG Pipelined Request**<br>This signal is asserted by the current master to indicate that a full-width request should be enqueued by the AMD-762™ system controller AGP target controller. The AMD-762 system controller enqueues a new request each edge of AGPCLK while the PIPE# signal is asserted. |
| RBF# | I | **AGP Read Buffer Full**<br>This signal indicates that the AGP master's input buffer is full, and that it cannot accept more read data. When this signal is asserted by the AGP master, the AMD-762 system controller does not attempt to return previously requested low-priority read data. |
| WBF# | I | **AGP Write Buffer Full**<br>This signal indicates that the AGP master cannot accept more fast writes from the AMD-762 system controller. When this signal is asserted by the AGP master, the AMD-762 system controller does not attempt to initiate fast writes. |
| SBA[7:0] | I | **AGP Sideband Address Bus**<br>These pins provide an additional bus that can be used to pass commands (address and data) from the AGP master to the AMD-762 system controller. The sideband bus is driven by an external AGP master. |
| SBSTB/SBSTB# | I<br>*STS* | **AGP Sideband Strobes**<br>These strobes are driven by the AGP master to provide timing for the sideband address bus (SBA[7:0] pins). The SBSTB# pin provides the complement of SBSTB and is used only for AGP 4x timing mode. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| ST[2:0] | O | **AGP Status**<br>This bus is used to provide status from the AMD-762™ system controller to the AGP master. These signals are valid only when the A_GNT# signal is asserted (Low) and must be ignored by the AGP master at all other times. The status bits are encoded as follow:<br>000 = Indicates that previously requested low-priority read or flush data is being returned to the master.<br>001 = Indicates that previously requested high-priority read data is being returned to the master.<br>010 = Indicates that the master provides low-priority write data for a previous enqueued write command.<br>011 = Indicates that the master provides high-priority write data for a previous enqueued write command.<br>100 = Reserved<br>101 = Reserved<br>110 = Reserved<br>111 = Indicates that the master has been given permission to start a bus transaction. The master can enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting FRAME#. ST[2:0] are always an output from the core logic and an input to the master. |
| **Miscellaneous Signals** | | |
| TEST# | I | **Test Mode Enable**<br>The TEST# pin is used by AMD for internal chip testing. It is also used to enter NAND tree and three-state test modes for motherboard manufacturing test, as described in Chapter 3. |
| DEBUG[2:0]# | VSS/ VDD | **Debug**<br>These pins are reserved for general-purpose debug. DEBUG[0]# is used for device scan testing; the other two pins are reserved. These pins are not used for normal operation but must be routed to vias on the motherboard to allow test access. The I/O pads for these signals contain weak pullup resistors, therefore there are no termination requirements on the motherboard. |
| PDL_OUTPUT_TEST | O | **Programmable Delay Line Output**<br>This pin provides the output of programmable delay line (PDL) 0 for debug use only. This pin is not used for normal operation but can be routed to a via on the motherboard to allow scope access. |
| DCSTOP# | I | **DRAM Controller Stop**<br>This pin is used to support ACPI S1 and S3 power management modes. It is asserted by the AMD-768™ peripheral bus controller or AMD-766™ peripheral bus controller to enter the S1 power state, and asserted in conjunction with RESET# to enter the S3 state. Refer to “Power Management” on page 25 for details of AMD-762 system controller power management modes. |
| ROM_SDA | I | **SIP ROM Serial Data**<br>This pin provides the serial data input from an optional serial ROM or microcontroller when used for loading the SIP parameters for the AMD Athlon processor. This is required only for cases when SIP parameters are required which are different than those supplied by the AMD-762 system controller. |

**Table 34. Signal Descriptions (Continued)**

| Signal | Type | Description |
|---|---|---|
| ROM_SCK | B | **SIP ROM Clock**<br>This pin provides the clock output to an optional serial ROM or microcontroller when used for loading the SIP parameters for the AMD Athlon processor. This function is required only for cases when SIP parameters are required that are different than those supplied by the AMD-762™ system controller.<br>This pin must be pulled Low when using the internal SIP ROM table on the AMD-762 system controller or pulled High to use the external ROM. |
| **VSS/VDD, I/O Pad and Voltage Reference, and Compensation Pins** | | |
| VSS | | VSS |
| VDD_CORE | | AMD-762 system controller VDD pins, 2.5 Vdc. |
| VDD_PCI | | VDD for PCI I/O cells, 3.3 Vdc. |
| VDD_AGP | | This pin functions as VDD for AGP I/O cells, and can be 1.5 Vdc or 3.3 Vdc as determined by TYPEDET# pin on the motherboard. The motherboard drives this input to 1.5 Vdc when the TYPEDT# pin is asserted Low by an AGP card or 3.3 Vdc when the TYPEDET# pin is High. |
| AVDD | | Separately filtered 2.5 Vdc for analog PLL circuitry. |
| AGP_CAL and AGP_CAL# | | Compensation pads for matching impedance of motherboard AGP traces. |
| P0_CAL and P0_CAL# | | Compensation pads for matching impedance of motherboard AMD Athlon system bus traces. |
| AGP_VREF | | Voltage reference for 3.3 Vdc AGP I/O cells. |
| AGP_VREF4x | | Voltage reference for 1.5 Vdc AGP I/O cells. |
| REF_5V | | Voltage reference to support 5 Vdc PCI signalling. |
| P0_VREF | | AMD Athlon system bus I/O voltage reference. |
| DDR_REF | | DDR I/O voltage reference. |
| S_CLKREF | | System clock reference voltage. |
| CPU_VCORE | | Voltage for push-pull I/O pads. |
| SI_VSS and SI_VDD | | Connected to the AMD-762 system controller VSS and VDD_CORE planes. These are intended only for signal integrity testing and should be connected to the motherboard VSS and VDD_CORE planes, respectively. |

# 7.1 Initialization Pinstrapping

The AMD-762 system controller requires various pinstrapping options to define the SIP stream returned to the AMD Athlon processor after reset, as well as to define specific AMD-762 system controller operating parameters. The pinstraps are set by 10K pullup or pulldown resistors attached externally to PCI bus pins, and they are sampled during reset. Unless otherwise defined, strapping options are enabled when pulled High, disabled when pulled Low. BIOS can read the value latched on most of these pinstraps in the Configuration Status register (Dev 0:F0:0x88). See Table 35 for a description of the pinstraps.

**Table 35. Initialization Pinstrapping**

| Signal | Type | Description |
|---|---|---|
| AD[31:30] | I | **ClkSpeed**<br>These pinstraps are used to define the clock speed of the AMD Athlon™ processor system bus and DDR SDRAM interface, and are encoded as follows:<br>00: 100 MHz<br>01: 66 MHz (test and debug only)<br>10: Reserved<br>11: 133 MHz<br>The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88). |
| AD[29] | I | **PLL Reset**<br>This pin must be driven Low when using the PLL bypass test mode. This pin is also optionally used in test modes as described in Chapter 3. A pullup resistor is required on this pinstrap for normal operation. |
| AD[28] | I | **SysClkThresh**<br>This pin functions as the AMD Athlon processor system bus threshold range select for the system clock input receiver. When Low, the system clock input senses thresholds between 0.6 V and 1.0 V. When High, the inputs sense thresholds between 1.0 V and 1.4 V.<br>The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88). |
| AD[27:26] | I | **Length 1**<br>This bit field selects the CPU 1 physical AMD Athlon processor system bus length:<br>00: Short, non-slot A<br>01: Single slot A or “close”<br>10: Far dual slot A<br>11: Farthest possible slot A<br>See the *AMD Athlon System Bus Design Guide*, order# 22666, for details of the bus length assumptions used in the bus timing calculations. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88). |

**Table 35. Initialization Pinstrapping (Continued)**

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>AD[25]</td><td>I</td><td>Three-State-Enable (For Test Only)<br>When pulled High, this pin enables board test mode when TEST# is asserted. Refer to Chapter 3 for details of this test mode bit. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88).</td></tr>
<tr><td>AD[24]</td><td>I</td><td>Inclk_Delay_Enable<br>When this pin is pulled High, forwarded clocks originating in the AMD-762™ system controller are delayed 1/4 SysClk period to place their edge in the nominal center of the associated data. Certain SIP parameters are also adjusted. When pulled Low, the forwarded clock edges are concurrent with the associated data transitions. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88).</td></tr>
<tr><td>AD[23]</td><td>I</td><td>NAND_TreeEnable (for Test Only)<br>When this pin is pulled High, NAND tree test mode is enabled when TEST# is asserted. Refer to Chapter 3 for details of this test mode bit. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88).</td></tr>
<tr><td>AD[22:21]</td><td>I</td><td>CPU_ClkHist<br>This field selects the amount of hysteresis applied to the SysDataOutClk[3:0]# and SysAddrOutClk# inputs for noise immunity. This field is encoded as follows:<br>00: No hysteresis<br>01: Low hysteresis (preferred setting)<br>10: Medium hysteresis<br>11: Maximum hysteresis</td></tr>
<tr><td>AD[20]</td><td>I</td><td>TypeDet#<br>This pin functions as the AGP card type detect, used by the AGP I/O cells for impedance compensation. The latched value of the TYPEDET# pin can also be read in the Configuration Status register (Dev 0:F0:0x88).<br>0: AGP card with 1.5-V referencing installed<br>1: AGP card with 3.3-V referencing installed<br>The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88).</td></tr>
<tr><td>AD[19:16]</td><td>I</td><td>CPU_Div 1<br>These pins define the clock multiplier for CPU 1, and are generated by the CPU. They are used internally to create the frequency ID (FID) value, which is used in the generation of SIP values sent to the AMD Athlon™ processor during initialization. The table below lists the clock multipliers for each FID value.
<table>
<tr><th>FID Value</th><th>Multiplier</th><th>FID Value</th><th>Multiplier</th><th>FID Value</th><th>Multiplier</th><th>FID Value</th><th>Multiplier</th></tr>
<tr><td>0000</td><td>11.0</td><td>0100</td><td>5.0</td><td>1000</td><td>7.0</td><td>1100</td><td>9.0</td></tr>
<tr><td>0001</td><td>11.5</td><td>0101</td><td>5.5</td><td>1001</td><td>7.5</td><td>1101</td><td>9.5</td></tr>
<tr><td>0010</td><td>12.0</td><td>0110</td><td>6.0</td><td>1010</td><td>8.0</td><td>1110</td><td>10.0</td></tr>
<tr><td>0011</td><td>12.5</td><td>0111</td><td>6.5</td><td>1011</td><td>8.5</td><td>1111</td><td>10.5</td></tr>
</table>
The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88).</td></tr>
</table>

**Table 35. Initialization Pinstrapping (Continued)**

| Signal | Type | Description |
|---|---|---|
| AD[15] | I | **66-MHz PCI Mode**<br>This bit is used to specify that the desired PCI clock speed is 66 MHz. This pin should be pulled up if the motherboard supports the 66/33-MHz PCI speed option as described in 2.5 “System Clocking” on page 22. This should be pulled down for systems that support a maximum PCI bus speed of 33 MHz.<br>The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88). |
| AD[14:12] | I | **AGPClock_Mux[2:0] (For Test Only)**<br>This bit field selects input to APLL clock mux for PLL test mode. Refer to Chapter 3 for details of these bits. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88). |
| AD[11:10] | I | **Length 0**<br>This bit field selects the CPU 0 physical AMD Athlon™ system bus length:<br>00: Short, non-slot A<br>01: Single slot A or “close”<br>10: Far dual slot A<br>11: Farthest possible slot A<br>For details of the bus length assumptions used in the bus timing calculations, see the *AMD Athlon™ System Bus Design Guide*, order# 22666. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88). |
| AD[9] | I | **Bypass_PLLs (For Test Only)**<br>If this pin is pulled High, PLL bypass mode is enabled when TEST# is asserted. Refer to Chapter 3 for details of PLL bypass mode. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88). |
| AD[8] | I | **OutClk_Delay_Enable**<br>When this pin is pulled High, forwarded clocks originating in the AMD Athlon processor are delayed to the nominal center of the associated data. This control is provided by adjusting SIP parameters. When pulled Low, the AMD Athlon processor forwarded clock edges are concurrent with the associated data transitions.<br>Refer to the SIP mapping description in the AMD Athlon system bus specification (#21902) for details. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88). |
| AD[7:5] | I | **SysClock_Mux[2:0] (For Test Only)**<br>This bit field selects input to SPLL clock mux for PLL test mode. Refer to Chapter 3 for details of these bits. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88). |
| AD[4] | I | **CPU_Thresh**<br>This pin functions as the AMD Athlon processor system bus threshold range select for AMD Athlon processor system bus I/O cells. When Low, the AMD Athlon processor system bus inputs sense thresholds between 0.6 V and 1.0 V. When High, the inputs sense thresholds between 1.0 V and 1.4 V. The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88). |

**Table 35. Initialization Pinstrapping (Continued)**

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>AD[3:0]</td><td>I</td><td>CPU_Div 0<br>These pins define the clock multiplier for CPU 0, and are generated by the CPU. They are used internally to create the frequency ID (FID) value, which is used in the generation of SIP values sent to the AMD Athlon™ processor during initialization. The table below lists the clock multipliers for each FID value.
<table>
<tr><th>FID Value</th><th>Multiplier</th><th>FID Value</th><th>Multiplier</th><th>FID Value</th><th>Multiplier</th><th>FID Value</th><th>Multiplier</th></tr>
<tr><td>0000</td><td>11.0</td><td>0100</td><td>5.0</td><td>1000</td><td>7.0</td><td>1100</td><td>9.0</td></tr>
<tr><td>0001</td><td>11.5</td><td>0101</td><td>5.5</td><td>1001</td><td>7.5</td><td>1101</td><td>9.5</td></tr>
<tr><td>0010</td><td>12.0</td><td>0110</td><td>6.0</td><td>1010</td><td>8.0</td><td>1110</td><td>10.0</td></tr>
<tr><td>0011</td><td>12.5</td><td>0111</td><td>6.5</td><td>1011</td><td>8.5</td><td>1111</td><td>10.5</td></tr>
</table>
The value of this pinstrap can be read in the Configuration Status register (Dev 0:F0:0x88).</td></tr>
<tr><td>C/BE[3]#</td><td>I</td><td>Reserved<br>This pin must always have a pullup resistor installed for proper operation.</td></tr>
<tr><td>C/BE[2]#</td><td>I</td><td>Reserved<br>This pin must always have a pullup resistor installed for proper operation.</td></tr>
<tr><td>C/BE[1]#</td><td>I</td><td>AGP4x Test Mode<br>This pin should be pulled up when testing AGP in the 4x rate mode. This allows a 4x clock to be driven on the AGPCLK pin, and sets the appropriate internal clock dividers.</td></tr>
<tr><td>C/BE[0]</td><td>I</td><td>Reserved<br>This pin must always have a pulldown resistor installed for proper operation.</td></tr>
</table>

# 7.2 Pin Multiplexing

Some pin functions are multiplexed on PCI pins as described in Table 36 on page 98 . Note that additional pin multiplexing is required for scan testing and is described in Chapter 3. The pin multiplexing for scan mode does not affect normal operation.

Pin multiplexing is defined for test modes only, and requires specific PCI bus signalling pins to be pulled Low during reset (RESET# asserted). Note that if these test functions are used on the motherboard in lab debugging, the normal PCI signal pullup resistors need replacing temporarily with pulldown resistors. This action should be done only for lab testing and not in a production environment. These signals include the following:

- IRDY# pin for the TEST_RESET# function
- PAR pin for PLL output test mode.

These functions are described in detail in Chapter 3.

**Table 36. Pin Multiplexing Options**

| Primary/Secondary Pin Name | Primary Function | Secondary Function |
|---|---|---|
| GNT[6]#/AGPCLKOUT | PCI bus grant #6 | APLL clock output for PLL test. Refer to Chapter 3 for details of this function. |
| GNT[5]#/SYSCLKOUT | PCI bus grant #5 | SPLL clock output for PLL test. Refer to Chapter 3 for details of this function. |
| GNT[3]#/DDR_NAND | PCI bus grant #3 | Output of the DDR DRAM interface NAND tree. |
| GNT[2]#/PCI_NAND | PCI bus grant #2 | Output of the PCI bus interface NAND tree. |
| GNT[1]#/AGP_NAND | PCI bus grant #1 | Output of the AGP interface NAND tree. |
| GNT[0]#/CPU_NAND | PCI bus grant #0 | Output of the AMD Athlon™ processor system bus interface NAND tree. |
| IRDY#/TEST_RST# | PCI bus IRDY# pin | Reset pin dedicated to PLL clock dividers. Refer to Chapter 3 for details of this function. Used only for PLL testing. |
| TRDY#/SCAN_EN# | PCI bus TRDY# pin | Enables scan testing when TEST# is asserted. Not used in normal operation. |
| PAR/PLL_TEST# | PCI bus PAR (parity) pin | Enables clock testing when TEST# is asserted. The values on pinstraps AGPClock_Mux[2:0] and SysClock_Mux[2:0] strapping pins select the clock mux inputs. Refer to Chapter 3 for details of PLL test mode. |

# 7.3 Pin States at Reset

The AMD-762 system controller default pin states are defined in Table 37 on page 99. These are listed for all output and bidirectional pins in the power-on reset state (reset) as well as the ACPI S1 and S3 power management states. Refer to “Power Management” on page 25 for details of the S1 and S3 modes.

Note that most AMD-762 system controller internal configuration registers are initialized to a known value when RESET# is asserted. To accommodate the ACPI S3 (suspend to RAM) power management state, the memory controller registers are not initialized at power-up and must be programmed by BIOS following the first power-up. For further details, refer to Chapter 2, “Functional Operation” and the *AMD-762™ System Controller Software/BIOS Design Guide*, order# 24462.

**Table 37. Reset Pin States**

| Pin Name | RESET# State | S1 State | S3 State | Comments |
|---|---|---|---|---|
| Pn_CLKFWDRST | 1 | 1 | Z | |
| Pn_CONNECT | 1 | 0 | Z | |
| Pn_SADDIN[14:2]# | 1 | 1 | Z | |
| Pn_SADDINCLK# | 1 | 1 | Z | |
| Pn_SDATA[63:0]# | 1 | Park | Z | Parked signals maintain their previous value. |
| Pn_SDATAINCLK[3:0]# | 1 | 1 | Z | |
| Pn_SDATAINVAL# | 1 | 1 | Z | |
| Pn_SYSFILLVALID# | 1 | 1 | Z | |
| AD[63:00] | Z | Park | Z | |
| C/BE[7:0]# | Z | Park | Z | |
| DEVSEL# | Z | Z | Z | |
| FRAME# | Z | Z | Z | |
| GNT[6:0]# | Z | 1 | Z | |
| IRDY# | Z | Z | Z | |
| PAR64 | Z | Park | Z | |
| PAR | Z | Park | Z | |
| REQ64# | 0 | Park | Z | AMD-762™ system controller asserts per PCI 64-bit protocol. |
| ACK64# | Z | Park | Z | |
| SBGNT# | Z | 1 | Z | |
| SERR# | Z | Z | Z | |
| STOP# | Z | Z | Z | |
| TRDY# | Z | Z | Z | |
| WSC# | Z | Z | Z | |
| PCI_66CLK[2] | Active | Active | Z | Can be disabled via configuration register. |
| PCI_66CLK[1] | Active | Active | Z | Can be disabled via configuration register. |
| PCI_66CLK[0] | Active | Active | Z | Can be disabled via configuration register. |
| CS[7:0]# | 1 | 1 | Z | |
| DM[8:0] | Z | Z | Z | |
| DQS[8:0] | Z | Z | Z | |
| MAA[14:0] | 0 | Park | Z | Equals previous value. |
| MAB[14:0] | 0x7BFF | Park | Z | Equals previous value. |
| CKEA | 0 | 0 | 0 | |
| CKEB | 0 | 0 | 0 | |

**Table 37. Reset Pin States (Continued)**

| Pin Name | RESET# State | S1 State | S3 State | Comments |
|---|---|---|---|---|
| MDAT[63:0] | Z | Z | Z | |
| MECC[7:0] | Z | Z | Z | |
| CASA# | 1 | 1 | Z | |
| CASB# | 1 | 1 | Z | |
| CLKOUT[5:0] | Active | Active | Z | |
| CLKOUT[5:0]# | Active | Active | Z | |
| RASA# | 1 | 1 | Z | |
| RASB# | 1 | 1 | Z | |
| WEA# | 1 | 1 | Z | |
| WEB# | 1 | 1 | Z | |
| A_AD[31:00] | Z | Park | Z | |
| A_C/BE[3:0]# | Z | Park | Z | |
| A_DEVSEL# | Z | Z | Z | |
| A_FRAME# | Z | Z | Z | |
| A_GNT# | 1 | 1 | Z | |
| A_IRDY# | Z | Z | Z | |
| A_PAR | Z | Park | Z | |
| A_STOP# | Z | Z | Z | |
| A_TRDY# | Z | Z | Z | |
| ADSTB[1:0] | Z | Z | Z | |
| ADSTB[1:0]# | Z | Z | Z | |
| SBSTB | Z | Z | Z | Input only |
| SBSTB# | Z | Z | Z | Input only |
| ST[2:0] | 1 | Park | Z | |

# 8 Ordering Information

AMD standard products are available in several packages and operating ranges. The order number is formed by a combination of the elements below. Table 38 shows valid combinations of elements. Contact your AMD representative for detailed ordering information.

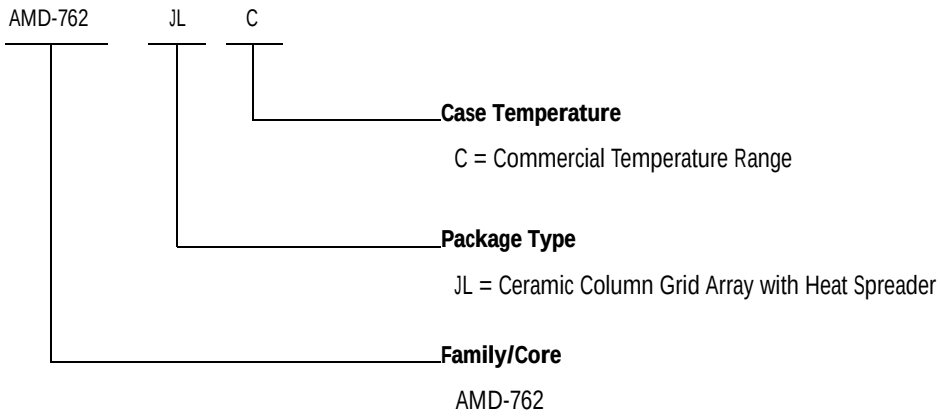



**Table 38. Valid Combinations for Ordering Parts**

| OPN | Package Type | Operating Voltage | Case Temperature |
|---|---|---|---|
| AMD-762JLC | 949-pin CCGA | 2.375 V–2.625 V | 85 °C |

*Note:*
*Valid combinations are configurations that are or will be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.*

# Conventions, Abbreviations, and References

This section contains information about the conventions and abbreviations used in this document and a list of related publications.

## Signals and Bits

- Active-Low Signals—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- Three-State—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.
- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

## Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
  - An AMD Athlon™ processor cache line is eight quadwords (64 bytes)

- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

  See Table 40 for more abbreviations.
- Little-Endian Convention—The byte with the address xx...xx00 is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

## Abbreviations and Acronyms

Table 40 contains the definitions of abbreviations used in this document.

**Table 39. Abbreviations**

| Abbreviation | Meaning |
|---|---|
| A | Ampere |
| F | Farad |
| G | Giga- |
| Gbit | Gigabit |
| Gbyte | Gigabyte |
| H | Henry |

**Table 39. Abbreviations (Continued)**

| Abbreviation | Meaning |
|---|---|
| h | Hexadecimal |
| K | Kilo- |
| Kbyte | Kilobyte |
| M | Mega- |
| Mbit | Megabit |
| Mbyte | Megabyte |
| MHz | Megahertz |
| m | Milli- |
| ms | Millisecond |
| mW | Milliwatt |
| µ | Micro- |
| µA | Microampere |
| µF | Microfarad |
| µH | Microhenry |
| µs | Microsecond |
| µV | Microvolt |
| n | nano- |
| nA | nanoampere |
| nF | nanofarad |
| nH | nanohenry |
| ns | nanosecond |
| ohm | Ohm |
| p | pico- |
| pA | picoampere |
| pF | picofarad |
| pH | picohenry |
| ps | picosecond |
| s | Second |
| V | Volt |
| W | Watt |

Table 40 contains the definitions of acronyms used in this document.

**Table 40. Acronyms**

| Abbreviation | Meaning |
|---|---|
| AAT | AGP Address Translator |
| ACK | Acknowledge |
| ACPI | Advanced Configuration and Power Interface |
| AGP | Accelerated Graphics Port |
| APCI | AGP Peripheral Component Interconnect |
| API | Application Programming Interface |
| APIC | Advanced Programmable Interrupt Controller |
| BAR | Base Address Register |
| BIOS | Basic Input/Output System |
| BIST | Built-In Self-Test |
| BIU | Bus Interface Unit |
| CCGA | Ceramic Column Grid Array |
| CS | Chip Select |
| DDR | Double-Data Rate |
| DIMM | Dual Inline Memory Module |
| DMA | Direct Memory Access |
| DRAM | Direct Random Access Memory |
| ECC | Error Correcting Code |
| EIDE | Enhanced Integrated Device Electronics |
| EISA | Extended Industry Standard Architecture |
| EPROM | Enhanced Programmable Read Only Memory |
| EV6 | Digital™ Alpha™ Bus |
| FID | Frequency Integer Divisor |
| FIFO | First In, First Out |
| GART | Graphics Address Remapping Table |
| HSTL | High-Speed Transistor Logic |
| IACK | Interrupt Acknowledge |
| IDE | Integrated Device Electronics |
| IMB | Interrupt Message Bus |
| ISA | Industry Standard Architecture |
| JEDEC | Joint Electron Device Engineering Council |
| JTAG | Joint Test Action Group |

**Table 40. Acronyms (Continued)**

| Abbreviation | Meaning |
|---|---|
| LAN | Large Area Network |
| LRU | Least-Recently Used |
| LSB | Least Significant Bit |
| LVTTL | Low Voltage Transistor Transistor Logic |
| MA | Memory Address |
| MCT | Memory Controller |
| MD | Memory Data |
| MDA | Monochrome Display Adapter |
| MRL | Memory Read Line |
| MRM | Memory Read Multiple |
| MSB | Most Significant Bit |
| MTRR | Memory Type and Range Registers |
| MWF | Memory Write FIFO |
| MWI | Memory Write-and-Invalidate |
| MUX | Multiplexer |
| NMI | Non-Maskable Interrupt |
| OD | Open Drain |
| PBGA | Plastic Ball Grid Array |
| PA | Physical Address |
| PCI | Peripheral Component Interconnect |
| PH | Page Hit |
| PLL | Phase Locked Loop |
| POS | Power-On Suspend |
| POST | Power-On Self-Test |
| PPA | Physical Page Address |
| PT | Page Tables |
| PTE | Page Table Entries |
| RAM | Random Access Memory |
| ROM | Read Only Memory |
| SBA | Sideband Address |
| SDRAM | Synchronous Direct Random Access Memory |
| SIP | Serial Initialization Packet |
| SMbus | System Management Bus |
| SMC | SDRAM Memory Controller |

**Table 40. Acronyms (Continued)**

| Abbreviation | Meaning |
|---|---|
| SPD | Serial Presence Detect |
| SRAM | Synchronous Random Access Memory |
| SROM | Serial Read Only Memory |
| TLB | Translation Lookaside Buffer |
| TOM | Top of Memory |
| TTL | Transistor Transistor Logic |
| VAS | Virtual Address Space |
| VPA | Virtual Page Address |
| VGA | Video Graphics Adapter |
| WBT | Write Buffer Tag |
| WP | Write Protect |
| USB | Universal Serial Bus |
| ZDB | Zero Delay Buffer |

## Related Publications

The following books discuss various aspects of computer architecture that may enhance your understanding of AMD products:

**AMD Publications**

*AMD Athlon™ Processor Data Sheet*, order# 21016

*AMD-766™ Peripheral Bus Controller Data Sheet*, order# 23167

*AMD-768™ Peripheral Bus Controller Data Sheet*, order# 24467

*Ceramic Column Grid Array (CCGA) Motherboard Mounting Guide*, order# 24598 (NDA)

**Bus Architecture**

*PCI Local Bus Specification*, Revision 2.2, PCI Special Interest Group, Hillsboro, Oregon, 1998.

*AT Bus Design*, Edward Solari, IEEE P996 Compatible, Annabooks, San Diego, CA, 1990.

*Accelerated Graphics Port Interface Specification*, Revision 2.0, Intel Corporation, AGP Forum, 1998.

**x86 Architecture**

*Programming the 80386*, John Crawford and Patrick Gelsinger, Sybex, San Francisco, 1987.

*80x86 Architecture & Programming*, Rakesh Agarwal, Volumes I and II, Prentice-Hall, Englewood Cliffs, NJ, 1991.

**General References**

*Computer Architecture*, John L. Hennessy and David A. Patterson, Morgan Kaufman Publishers, San Mateo, CA, 1990.

**Websites**

Visit the AMD website for documentation of AMD products.

**www.amd.com**

Other websites of interest include the following:

- JEDEC home page—www.jedec.org
- IEEE home page—www.computer.org
- AGP Forum—www.agpforum.org