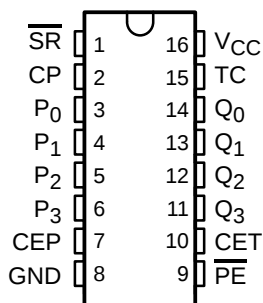


CY54FCT163T, CY74FCT163T 4-BIT BINARY COUNTERS

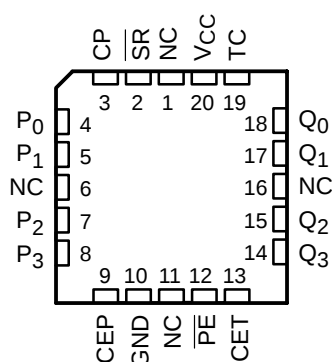
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- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT163T
 - 32-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT163T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current

CY74FCT163CT . . . Q OR SO PACKAGE
(TOP VIEW)



CY54FCT163T . . . L PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'FCT163T devices are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers. These devices have two types of count-enable (CEP and CET) inputs, plus a terminal-count (TC) output for versatility in forming synchronous multistaged counters. The 'FCT163T devices have a synchronous-reset ($\overline{SR}$) input that overrides counting and parallel loading, and allows the outputs to be reset simultaneously on the rising edge of the clock.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	DESCRIPTION
CEP	Count-enable parallel input
CET	Count-enable trickle input
CP	Clock pulse input (active rising edge)
$\overline{SR}$	Synchronous-reset input (active low)
P	Parallel data inputs
$\overline{PE}$	Parallel-enable input (active low)
Q	Flip-flop outputs
TC	Terminal-count output



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT163T, CY74FCT163T 4-BIT BINARY COUNTERS

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ORDERING INFORMATION

T _A	PACKAGE [†]		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.8	CY74FCT163CTQCT	FT163-3
	SOIC – SO	Tube	5.8	CY74FCT163CTSOC	FCT163C
		Tape and reel	5.8	CY74FCT163CTSOCT	
–55°C to 125°C	LCC – L	Tube	11.5	CY54FCT163TLMB	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

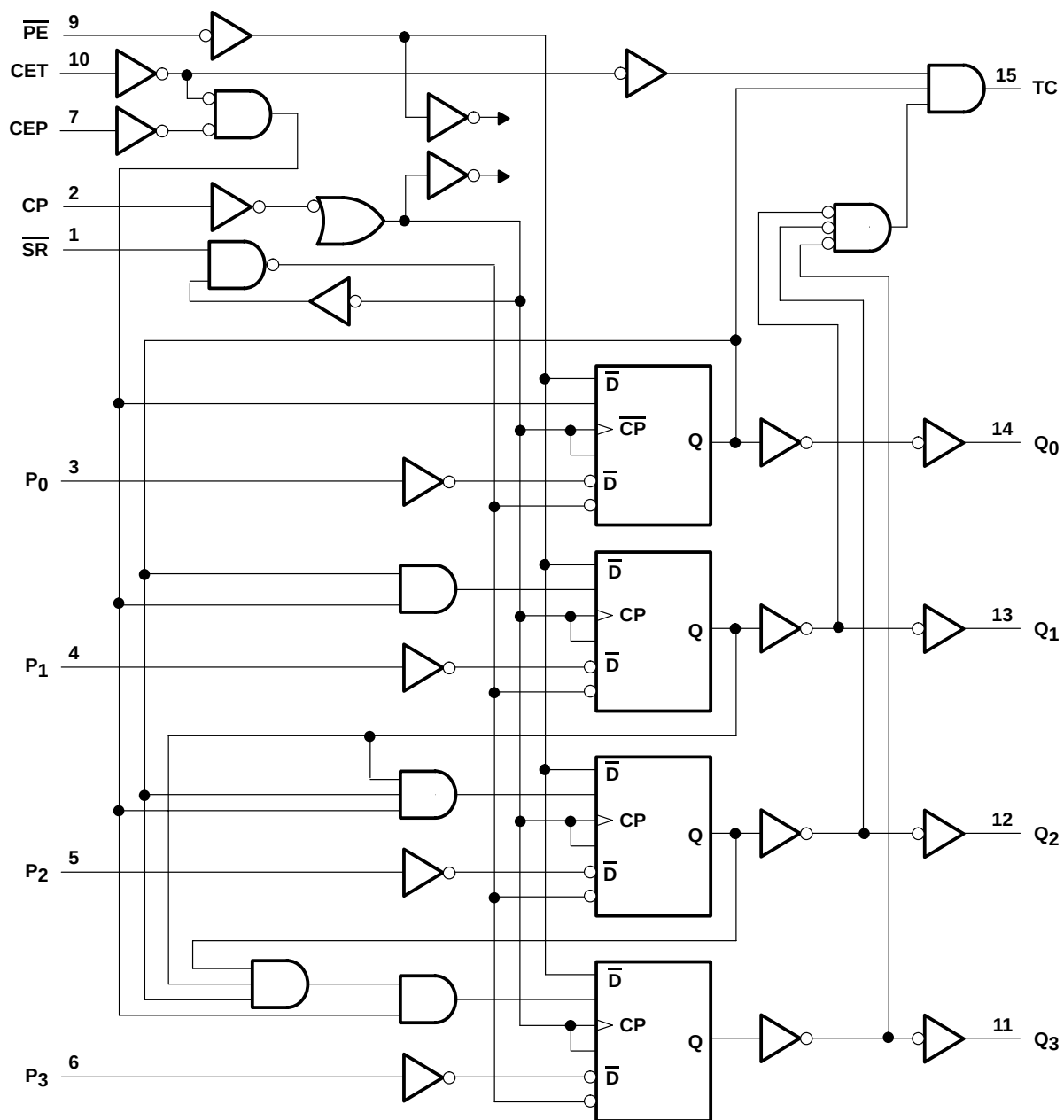
INPUTS				ACTION ON THE RISING CLOCK EDGE(S)
$\overline{\text{SR}}$	$\overline{\text{PE}}$	CET	CEP	
L	X	X	X	Reset (clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (incremental)
H	H	L	X	No change (hold)
H	H	X	L	No change (hold)

H = High logic level, L = Low logic level, X = Don't care



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logic diagram (positive logic)



CY54FCT163T, CY74FCT163T

4-BIT BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	90°C/W
SO package	57°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	CY54FCT163T			CY74FCT163T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			–12			–32	mA
I_{OL} Low-level output current			32			64	mA
T_A Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT163T			CY74FCT163T			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$		-0.7	-1.2				V
	$V_{CC} = 4.75 \text{ V}$, $I_{IN} = -18 \text{ mA}$					-0.7	-1.2	
V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75 \text{ V}$, $I_{OH} = -32 \text{ mA}$				2			
	$V_{CC} = 4.75 \text{ V}$, $I_{OH} = -15 \text{ mA}$				2.4	3.3		
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 32 \text{ mA}$		0.3	0.55				V
	$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 64 \text{ mA}$					0.3	0.55	
V_{hys}	All inputs		0.2			0.2		V
I_I	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = V_{CC}$			5				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = V_{CC}$						5	
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.7 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 2.7 \text{ V}$						± 1	
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.5 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 0.5 \text{ V}$						± 1	
$I_{OS}^{\ddagger}$	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$	-60	-120	-225				mA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0 \text{ V}$				-60	-120	-225	
I_{off}	$V_{CC} = 0 \text{ V}$, $V_{OUT} = 4.5 \text{ V}$			± 1			± 1	μA
I_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$		0.1	0.2				mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$					0.1	0.2	
ΔI_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 3.4 \text{ V}^{\S}$, $f_1 = 0$, Outputs open		0.2	2				mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 3.4 \text{ V}^{\S}$, $f_1 = 0$, Outputs open					0.2	2	
$I_{CCD}^{\parallel}$	$V_{CC} = 5.5 \text{ V}$, Load mode, Outputs open, One bit switching at 50% duty cycle, CEP = CET = PE = GND, SR = V_{CC} , $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$		0.06	0.12				mA/MHz
	$V_{CC} = 5.25 \text{ V}$, Load mode, Outputs open, One bit switching at 50% duty cycle, CEP = CET = PE = GND, SR = V_{CC} , $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$					0.06	0.12	

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

[§] Per TTL-driven input ($V_{IN} = 3.4 \text{ V}$); all other inputs at V_{CC} or GND

^{||} This parameter is derived for use in total power-supply calculations.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			CY54FCT163T			CY74FCT163T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
IC#	VCC = 5.5 V, Load mode, f0 = 10 MHz, Outputs open, CEP = CET = PE = GND, SR = VCC	One bit switching at f1 = 5 MHz at 50% duty cycle	VIN ≤ 0.2 V or VIN ≥ VCC – 0.2 V	0.7	1.4				mA	
			VIN = 3.4 V or GND	1.2	3.4					
		Four bits switching at f1 = 5 MHz at 50% duty cycle	VIN ≤ 0.2 V or VIN ≥ VCC – 0.2 V	1.6	3.2					
			VIN = 3.4 V or GND	2.9	8.2					
	VCC = 5.25 V, f0 = 10 MHz, Load mode, Outputs open, CEP = CET = PE = GND, SR = VCC	One bit switching at f1 = 5 MHz at 50% duty cycle	VIN ≤ 0.2 V or VIN ≥ VCC – 0.2 V				0.7	1.4		
			VIN = 3.4 V or GND				1.2	3.4		
		Four bits switching at f1 = 5 MHz at 50% duty cycle	VIN ≤ 0.2 V or VIN ≥ VCC – 0.2 V				1.6	3.2		
			VIN = 3.4 V or GND				2.9	8.2		
CI				5	10				pF	
CO				9	12				pF	

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

$I_C^{\#} = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4\text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY54FCT163T		CY74FCT163CT		UNIT
		MIN	MAX	MIN	MAX	
t_W Pulse duration, high or low	Clock (load)	5		4		ns
	Clock (count)	8		5		
t_{SU} Setup time, high or low	P before $CP\uparrow$	5.5		3.5		ns
	$\overline{PE}$ or $\overline{SR}$ before $CP\uparrow$	13.5		7.6		
	$\overline{CEP}$ or $\overline{CET}$ before $CP\uparrow$	13		7.6		
t_H Hold time, high or low	P after $CP\uparrow$	2		1.5		ns
	$\overline{PE}$ or $\overline{SR}$ after $CP\uparrow$	1.5		1		
	$\overline{CEP}$ or $\overline{CET}$ after $CP\uparrow$	0		0		



CY54FCT163T, CY74FCT163T 4-BIT BINARY COUNTERS

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switching characteristics over operating free-air temperature range (see Figure 1)

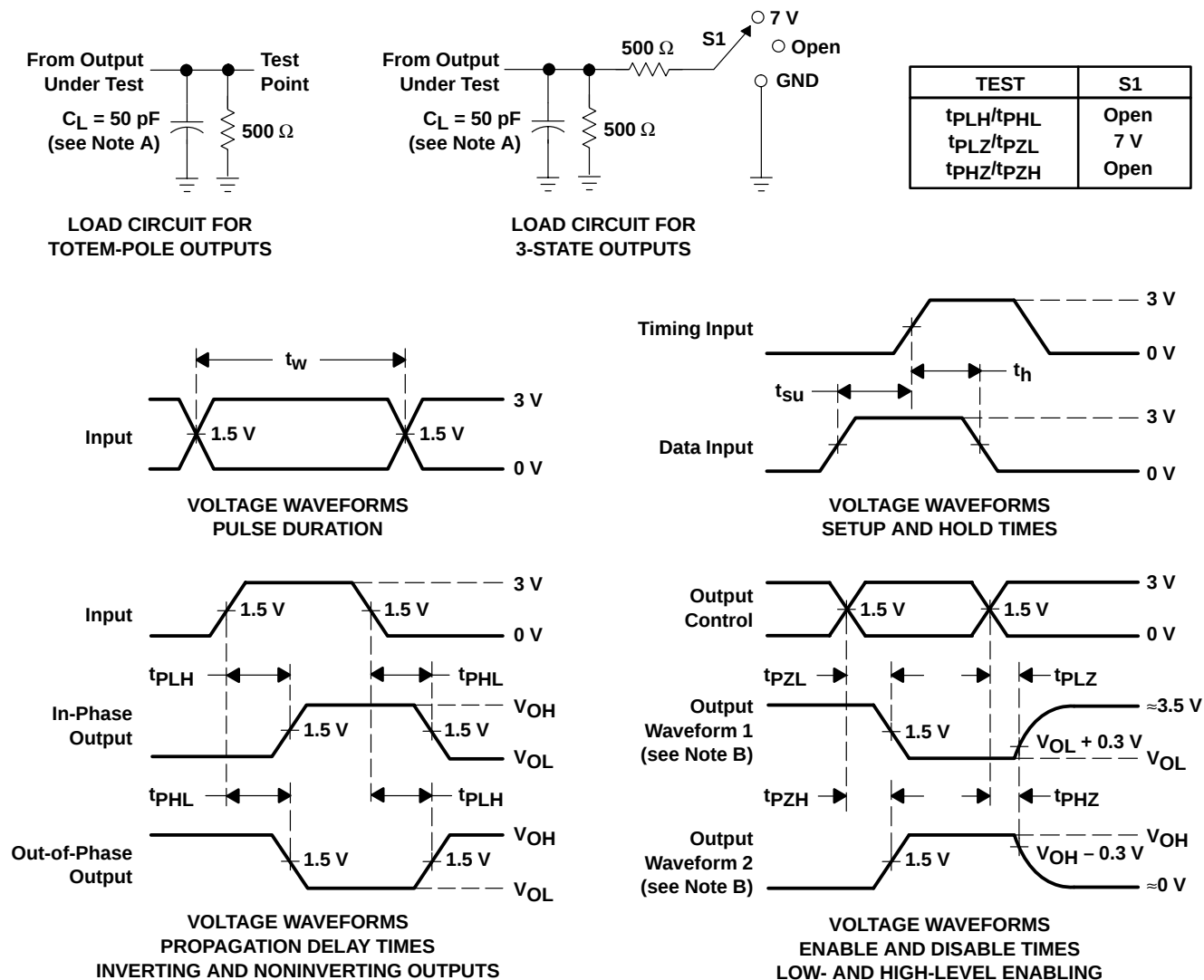
PARAMETER		FROM (INPUT)	TO (OUTPUT)	CY54FCT163T		CY74FCT163CT		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	Propagation delay ($\overline{PE}$ high)	CP	Q	2	11.5	1.5	5.8	ns
t _{PHL}				2	11.5	1.5	5.8	
t _{PLH}	Propagation delay ($\overline{PE}$ low)	CP	TC	2	10	1.5	5.2	ns
t _{PHL}				2	10	1.5	5.2	
t _{PLH}		CP	TC	2	16.5	1.5	7.8	ns
t _{PHL}				2	16.5	1.5	7.8	
t _{PLH}		CET	TC	1.5	9	1.5	4.4	ns
t _{PHL}				1.5	9	1.5	4.4	



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CY54FCT163TLMB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CY54FCT 163TLMB
CY74FCT163CTQCT	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT163-3
CY74FCT163CTQCT.B	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT163-3
CY74FCT163CTQCTG4	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT163-3
CY74FCT163CTQCTG4.B	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT163-3
CY74FCT163CTSOC	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT163C
CY74FCT163CTSOC.B	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT163C

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT163CTQCT	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
CY74FCT163CTQCTG4	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT163CTQCT	SSOP	DBQ	16	2500	353.0	353.0	32.0
CY74FCT163CTQCTG4	SSOP	DBQ	16	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY54FCT163TLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT163CTSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT163CTSOC.B	DW	SOIC	16	40	506.98	12.7	4826	6.6

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