TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91C025FG

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

CAUTION
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = (INT0 to INT3, INTRTC, INTALM0 to INTALM4, INTKEY), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontrollers

TMP91C025FG/JTMP91C025-S

1. Outline and Features

TMP91C025 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

TMP91C025FG comes in a 100-pin flat package. JTMP91C025-S comes in a 100-pad chip.

Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)

- Instruction mnemonics are upward-compatible with TLCS-90
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: 4 channels (444 ns/ 2 bytes at 36 MHz)

(2) Minimum instruction execution time: 111 ns (at 36 MHz)

(3) Built-in RAM: None
Built-in ROM: None

(4) External memory expansion
- Expandable up to 104 Mbytes (Shared program/data area)
- Can simultaneously support 8-/16-bit width external data bus
  ... Dynamic data bus sizing
- Separate bus system

(5) 8-bit timers: 4 channels

(6) General-purpose serial interface: 2 channels
- UART/Synchronous mode: 2 channels
- IrDA Ver.1.0 (115.2 kbps) mode selectable: 1 channel

(7) LCD controller
- Adapt to both shift register type and built-in RAM type LCD driver

(8) Timer for real-time clock (RTC)
- Based on TC8521A

(9) Key-on wakeup (Interrupt key input)

(10) 10-bit AD converter: 4 channels

(11) Touch screen interface
- Available to reduce external components

(12) Watchdog timer

(13) Melody/alarm generator
- Melody: Output of clock 4 to 5461 Hz
- Alarm: Output of the 8 kinds of alarm pattern
- Output of the 5 kinds of interval interrupt

(14) Chip select/wait controller: 4 channels

(15) MMU
- Expandable up to 104 Mbytes

(16) Interrupts: 37 interrupt
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 23 internal interrupts: 7 priority levels are selectable
- 5 external interrupts: 7 priority levels are selectable
  (among 4 interrupts are selectable edge mode)

(17) Input/output ports: 49 pins (Except Data bus (8bit), Address bus (24bit) and $\overline{\text{RD}}$ pin)

(18) Standby function
Three HALT modes: IDLE2 (Programmable), IDLE1 and STOP

(19) Hardware standby function (Power save function)

(20) Triple-clock controller

- Clock doubler (DFM) circuit is inside
- Clock gear function: Select a high-frequency clock fc/1 to fc/16
- SLOW mode (fs = 32.768 kHz)

(21) Operating voltage

- V_{CC} = 3.0 V to 3.6 V (fc max = 36 MHz)
- V_{CC} = 2.7 V to 3.6 V (fc max = 27 MHz)
- V_{CC} = 2.4 V to 3.6 V (fc max = 16 MHz)

(22) Package

- 100-pin QFP: P-LQFP100-1414-0.50F, chip form supply also available. For details, contact your local Toshiba sales representative.

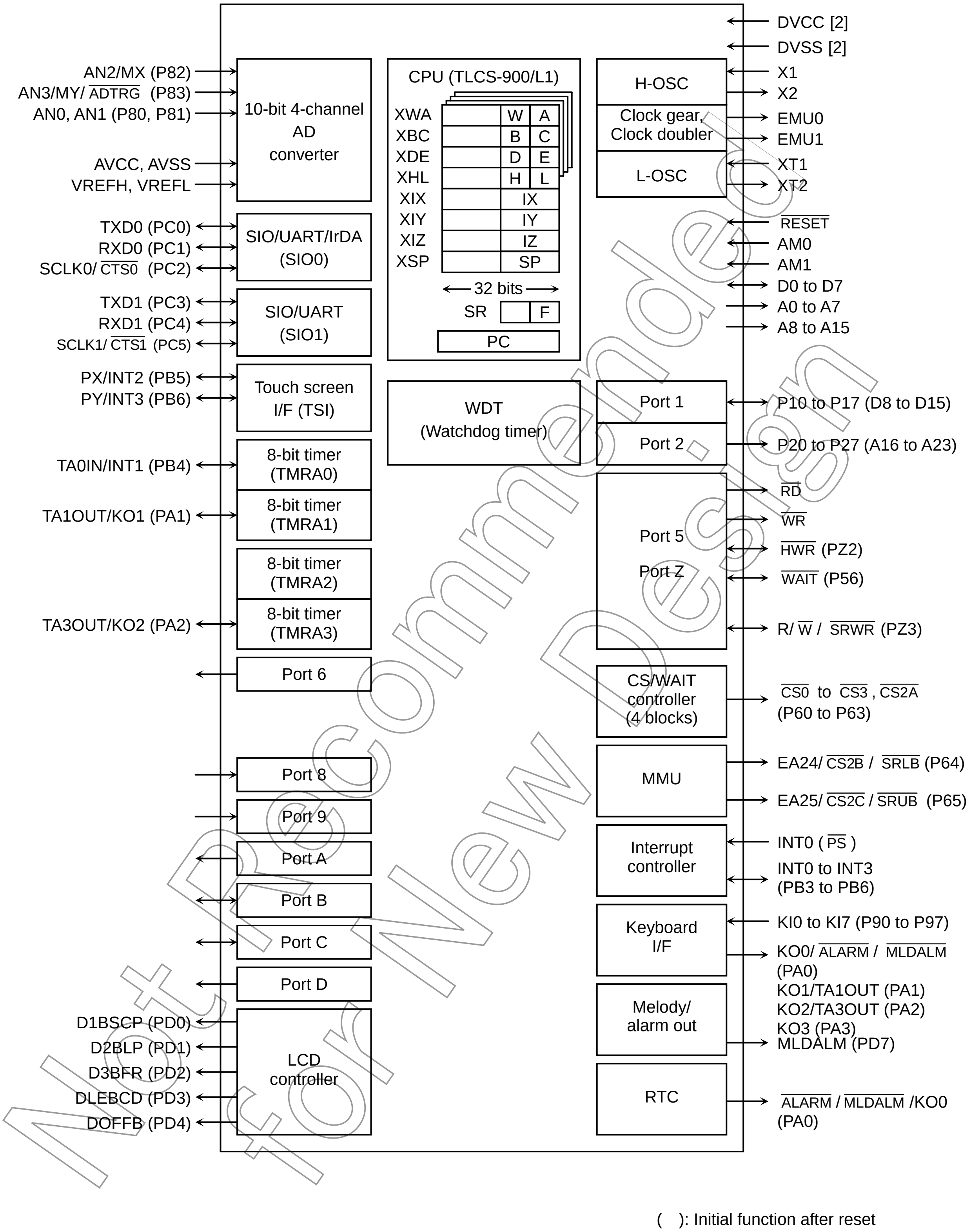


Figure 1.1 TMP91C025 Block Diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91C025, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91C025FG.

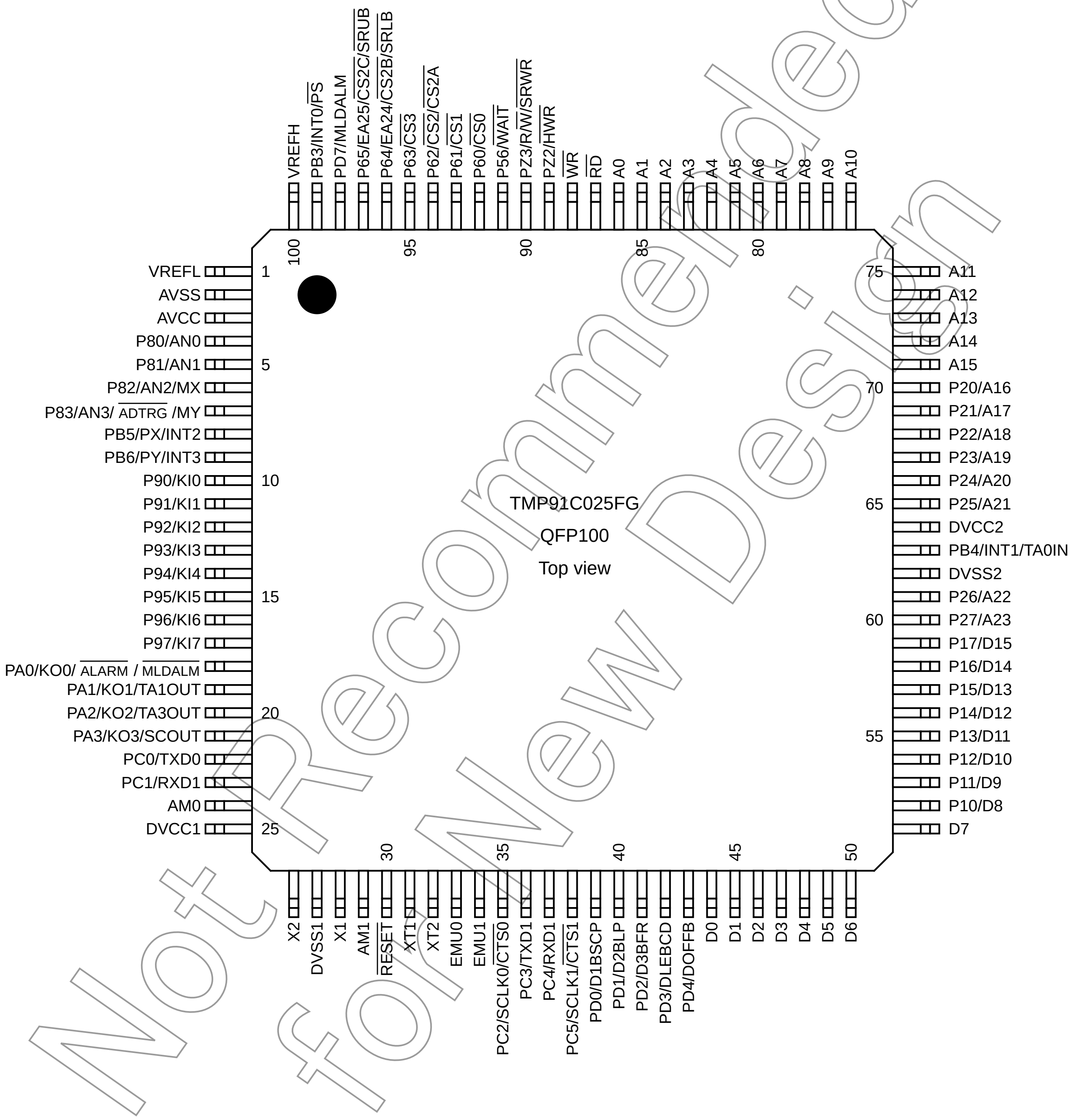


Figure 2.1.1 Pin Assignment Diagram (100-pin QFP)

2.2 PAD Layout

(Chip size 4.58 mm × 4.63 mm) Unit (μm)

Pin No.	Name	X Point	Y Point	Pin No.	Name	X Point	Y Point	Pin No.	Name	X Point	Y Point
1	VREFL	–2151	1627	44	D0	852	–2175	87	$\overline{\text{RD}}$	210	2175
2	AVSS	–2151	1502	45	D1	977	–2175	88	$\overline{\text{WR}}$	83	2175
3	AVCC	–2151	1376	46	D2	1103	–2175	89	PZ2	–42	2175
4	P80	–2151	1251	47	D3	1228	–2175	90	PZ3	–169	2175
5	P81	–2151	1126	48	D4	1353	–2175	91	P56	–296	2175
6	P82	–2151	1001	49	D5	1478	–2175	92	P60	–421	2175
7	P83	–2151	876	50	D6	1603	–2175	93	P61	–548	2175
8	PB5	–2151	751	51	D7	2151	–1636	94	P62	–674	2175
9	PB6	–2151	625	52	P10	2151	–1490	95	P63	–801	2175
10	P90	–2151	336	53	P11	2151	–1359	96	P64	–926	2175
11	P91	–2151	211	54	P12	2151	–1228	97	P65	–1051	2175
12	P92	–2151	86	55	P13	2151	–1096	98	PD7	–1177	2175
13	P93	–2151	–38	56	P14	2151	–965	99	PB3	–1302	2175
14	P94	–2151	–163	57	P15	2151	–834	100	VREFH	–1606	2175
15	P95	–2151	–289	58	P16	2151	–703				
16	P96	–2151	–414	59	P17	2151	–571				
17	P97	–2151	–539	60	P27	2151	–440				
18	PA0	–2151	–664	61	P26	2151	–309				
19	PA1	–2151	–789	62	DVSS2	2151	–153				
20	PA2	–2151	–914	63	PB4	2151	2				
21	PA3	–2151	–1040	64	DVCC2	2151	158				
22	PC0	–2151	–1165	65	P25	2151	315				
23	PC1	–2151	–1290	66	P24	2151	446				
24	AM0	–2151	–1415	67	P23	2151	577				
25	DVCC1	–2151	–1636	68	P22	2151	708				
26	X2	–1603	–2175	69	P21	2151	839				
27	DVSS1	–1438	–2175	70	P20	2151	971				
28	X1	–1273	–2175	71	A15	2151	1102				
29	AM1	–1147	–2175	72	A14	2151	1233				
30	$\overline{\text{RESET}}$	–1022	–2175	73	A13	2151	1364				
31	XT1	–897	–2175	74	A12	2151	1495				
32	XT2	–649	–2175	75	A11	2151	1627				
33	EMU0	–524	–2175	76	A10	1603	2175				
34	EMU1	–398	–2175	77	A9	1477	2175				
35	PC2	–273	–2175	78	A8	1350	2175				
36	PC3	–148	–2175	79	A7	1224	2175				
37	PC4	–23	–2175	80	A6	1097	2175				
38	PC5	101	–2175	81	A5	970	2175				
39	PD0	226	–2175	82	A4	844	2175				
40	PD1	352	–2175	83	A3	717	2175				
41	PD2	477	–2175	84	A2	590	2175				
42	PD3	602	–2175	85	A1	464	2175				
43	PD4	727	–2175	86	A0	337	2175				

2.3 Pin Names and Functions

The names of the input/output pins and their functions are described below.

Table 2.3.1 Pin Names and Functions (1/3)

Pin Name	Number of Pins	I/O	Functions
D0 to D7	8	I/O	Data (lower): bits 0 to 7 of data bus
P10 to P17 D8 to D15	8	I/O I/O	Port 1: I/O port that allows I/O to be selected at the bit level (When used to the external 8bit bus) Data (upper): Bits 8 to15 of data bus
P20 to P27 A16 to A23	8	Output Output	Port 2: Output port Address: Bits 16 to 23 of address bus
A8 to A15	8	Output	Address: Bits 8 to 15 of address bus
A0 to A7	8	Output	Address: Bits 0 to 7 of address bus
$\overline{RD}$	1	Output	Read: Strobe signal for reading external memory
$\overline{WR}$	1	Output	Write: Strobe signal for writing data to pins D0 to D7
PZ2 $\overline{HWR}$	1	I/O Output	Port Z2: I/O port (with pull-up resistor) High Write: Strobe signal for writing data to pins D8 to D15
PZ3 R/ $\overline{W}$ $\overline{SRWR}$	1	I/O Output Output	Port Z3: I/O port (with pull-up resistor) Read/Write: 1 represents read or dummy cycle; 0 represents write cycle. Write: Strobe signal for writing data to pins D0 to D15 for SRAM
P56 $\overline{WAIT}$	1	I/O Input	Port 56: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P60 $\overline{CS0}$	1	Output Output	Port 60:Output port Chip select 0: Outputs 0 when address is within specified address area.
P61 $\overline{CS1}$	1	Output Output	Port 61:Output port Chip select 1: Outputs 0 when address is within specified address area
P62 $\overline{CS2}$ $\overline{CS2A}$	1	Output Output Output	Port 62: Output port Chip select 2: Outputs 0 when address is within specified address area Expand chip select: 2A: Outputs 0 when address is within specified address area
P63 $\overline{CS3}$	1	Output Output	Port 63:Output port Chip select 3: Outputs 0 when address is within specified address area
P64 EA24 $\overline{CS2B}$ $\overline{SRLB}$	1	Output Output Output Output	Port 64: Output port Chip select 24: Outputs 0 when address is within specified address area Expand chip select: 2B: Outputs 0 when address is within specified address area Low byte enable for SRAM
P65 EA25 $\overline{CS2C}$ $\overline{SRUB}$	1	Output Output Output Output	Port 65: Output port Chip select 25: Outputs 0 when address is within specified address area Expand chip select: 2C: Outputs 0 when address is within specified address area High byte enable for SRAM

Table 2.3.2 Pin Names and Functions (2/3)

Pin Name	Number of Pins	I/O	Functions
P80 to P81 AN0 to AN1	2	Input Input	Port 80 to 81 port: Pin used to input ports Analog input 0 to 1: Pin used to input to AD converter
P82 AN2 MX	1	Input Input Input	Port 82 port: Pin used to input ports Analog input 2: Pin used to input to AD converter X-Minus: Pin connected to X- for touch screen panel
P83 AN3 $\overline{\text{ADTRG}}$ MY	1	Input Input Input Input	Port 83 port: Pin used to input ports Analog input 3: Pin used to input to AD converter AD trigger: Signal used to request AD start Y-Minus: Pin connected to Y- for touch screen panel
P90 to P97 KI0 to KI7	8	Input Input	Port: 90 to 97 port: Pin used to input ports Key input 0 to 7: Pin used of key-on wakeup 0 to 7 (Schmitt input, with pull-up resistor)
PA0 KO0 $\overline{\text{ALARM}}$ $\overline{\text{MLDALM}}$	1	Output Output Output Output	Port: A0 port: Pin used to output ports Key output 0: Pin used of key-scan strobe 0 RTC alarm output pin Melody/alarm output pin (Inverted)
PA1 KO1 TA1OUT	1	Output Output Output	Port: A1 port: Pin used to output ports Key output 1: Pin used of key-scan strobe 1 8-bit timer 1 output: Timer 0 input or timer 1 output
PA2 KO2 TA3OUT	1	Output Output Output	Port: A2 port: Pin used to output ports Key output 2: Pin used of key-scan strobe 2 8-bit timer 3 output: Timer 2 input or timer 3 output
PA3 KO3 SCOUT	1	Output Output Output	Port: A3 port: Pin used to output ports Key output 3: Pin used of key-scan strobe 3 System clock output: Output f_{FPH} clock
PB3 INT0 $\overline{\text{PS}}$	1	I/O Input Input	Port B3: I/O port Interrupt request pin0: Interrupt request with programmable level/rising edge Power save: Pin used as input pin for H/W standby mode
PB4 INT1 TA0IN	1	I/O Input Input	Port B4: I/O port Interrupt request pin1: Interrupt request with programmable rising/falling edge 8-bit timer 0 input: Timer 0 input
PB5 INT2 PX	1	Input Input Output	Port B5: Input port Interrupt request pin2: Interrupt request with programmable rising/falling edge X-Plus: Pin connected to X+ for touch screen panel
PB6 INT3 PY	1	Input Input Output	Port B6: Input port Interrupt request pin3: Interrupt request with programmable rising/falling edge Y-Plus: Pin connected to Y+ for touch screen panel
PC0 TXD0	1	I/O Output	Port C0: I/O port Serial 0 send data: Open-drain output pin by programmable
PC1 RXD0	1	I/O Output	Port C1: I/O port Serial 0 receive data

Note: After reset, input “1” to PB3 (INT0, $\overline{\text{PS}}$)-pin, because it is worked as $\overline{\text{PS}}$ input pin.

Table 2.3.3 Pin Names and Functions. (3/3)

Pin Name	Number of Pins	I/O	Functions
PC2 SCLK0 $\overline{\text{CTS0}}$	1	I/O I/O Input	Port C2: I/O port (with pull-up resistor) Serial clock I/O 0 Serial data send enable 0 (Clear to send)
PC3 TXD1	1	I/O Output	Port C3: I/O port Serial send data 1 Open-drain output pin by programmable
PC4 RXD1	1	I/O Input	Port C4: I/O port Serial receive data 1
PC5 SCLK1 $\overline{\text{CTS1}}$	1	I/O I/O Input	Port C5: I/O port (with pull-up resistor) Serial clock I/O 1 Serial data send enable 1 (Clear to send)
XT1	1	Input	Low-frequency oscillator connecting pin
XT2	1	Output	Low-frequency oscillator connecting pin
PD0 D1BSCP	1	Output Output	Port D0: Output port LCD controller output pin
PD1 D2BLP	1	Output Output	Port D1: Output port LCD controller output pin
PD2 D3BFR	1	Output Output	Port D2: Output port LCD controller output pin
PD3 DLEBCD	1	Output Output	Port D3: Output port LCD controller output pin
PD4 DOFFB	1	Output Output	Port D4: Output port LCD controller output pin
PD7 MLDALM	1	Output Output	Port D7: Output port Melody/alarm output pin
AM0 to AM1	2	Input	Operation mode: Fixed to AM1 = 0, AM0 = 1 16-bit external bus or 8-/16-bit dynamic sizing. Fixed to AM1 = 0, AM0 = 0 8-bit external bus fixed.
EMU0	1	Output	Open pin
EMU1	1	Output	Open pin
$\overline{\text{RESET}}$	1	Input	Reset: initializes TMP91C025. (with pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)
X1, X2	2	I/O	High-frequency oscillator connection pins
DVCC	2		Power supply pins (All VCC pins should be connected with the power supply pin.)
DVSS	2		GND pins (0 V) (All pins should be connected with GND (0 V).)

3. Operation

This following describes block by block the functions and operation of the TMP91C025.

Notes and restrictions for eatch book are outlined in 6, precautions and restrictions at the end of this manual.

3.1 CPU

The TMP91C025 incorporates a high-performance 16-bit CPU (the 900/L1-CPU). For CPU operation, see the TLCS-900/L1 CPU.

The following describe the unique function of the CPU used in the TMP91C025; these functions are not covered in the TLCS-900/L1 CPU section.

3.1.1 Reset

When resetting the TMP91C025 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks (9 μs at 36 MHz).

Thus, when turn on the switch, be set to the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks.

Clock gear is initialized 1/16 mode by reset operation. It means that the system clock mode f_{SYS} is set to fc/32(= fc/16 × 1/2).

When the reset is accept, the CPU:

- Sets as follows the program counter (PC) in accordance with the reset vector stored at address FFFF00H to FFFF02H:

  PC<0:7> ← Value at FFFF00H address

  PC<15:8> ← Value at FFFF01H address

  PC<23:16> ← Value at FFFF02H address
- Sets the stack pointer (XSP) to 100H.
- Sets bits <IFF2:0> of the status register (SR) to 111 (Sets the interrupt level mask register to level 7).
- Sets the <MAX> bit of the status register (SR) to 1 (MAX mode).
  Note: As this product does not support MIN mode, do not write a 0 to the <MAX>
- Clears bits <RFP2:0> of the status register(SR) to 000 (Sets the register bank to 0).

When reset is released,the CPU starts executing instructions in accordance with the program counter settings. CPU internal registers not mentioned above do not change when the reset is released.

When the reset is accepted, the CPU sets internal I/O, ports, and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to general-purpose input or output port mode.

Note: The CPU internal register (Except to PC, SR, XSP) do not change by resetting.

Figure 3.1.1 is a reset timing chart of the TMP91C025.

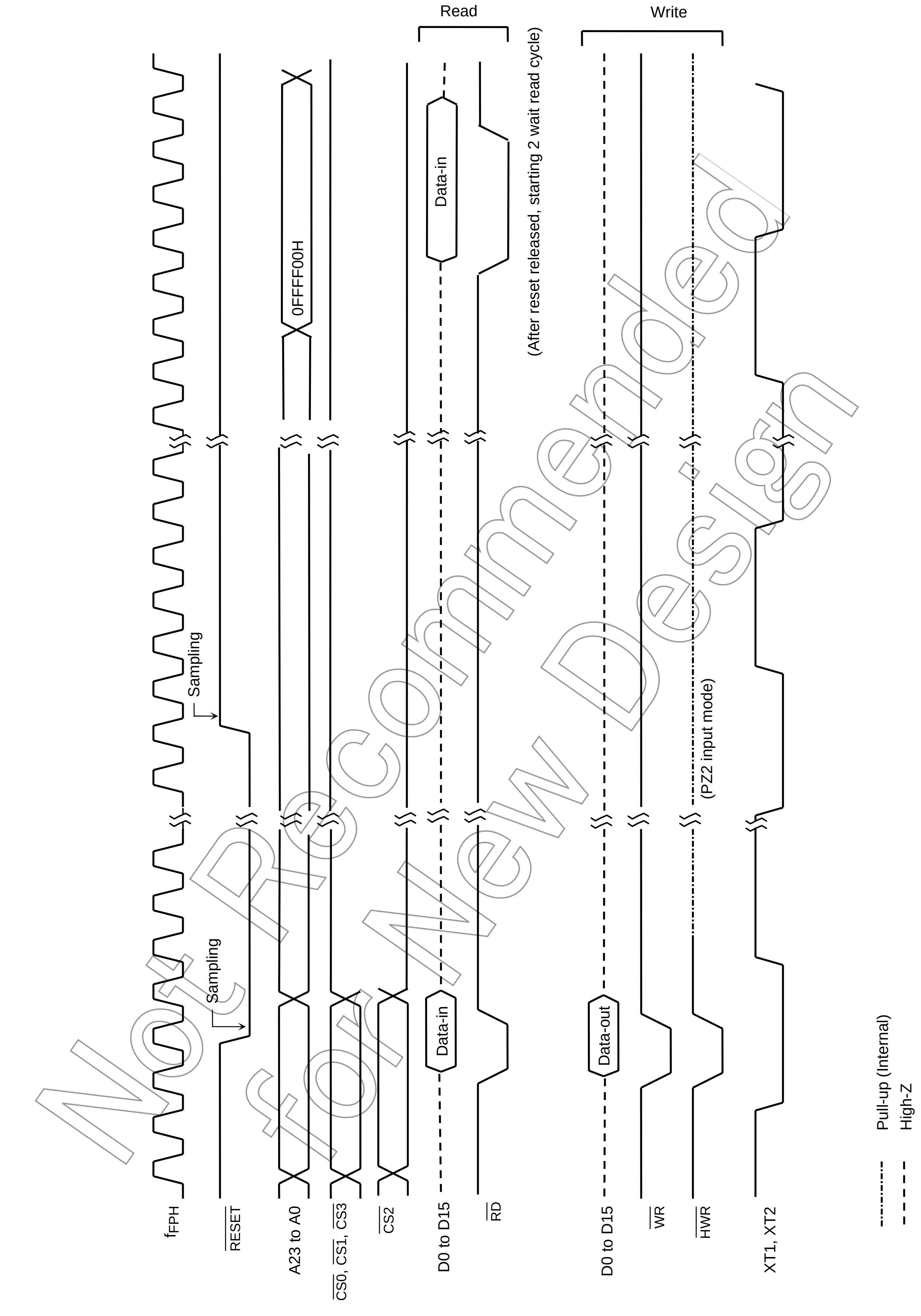


Figure 3.1.1 Reset Timing Chart

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP91C025.

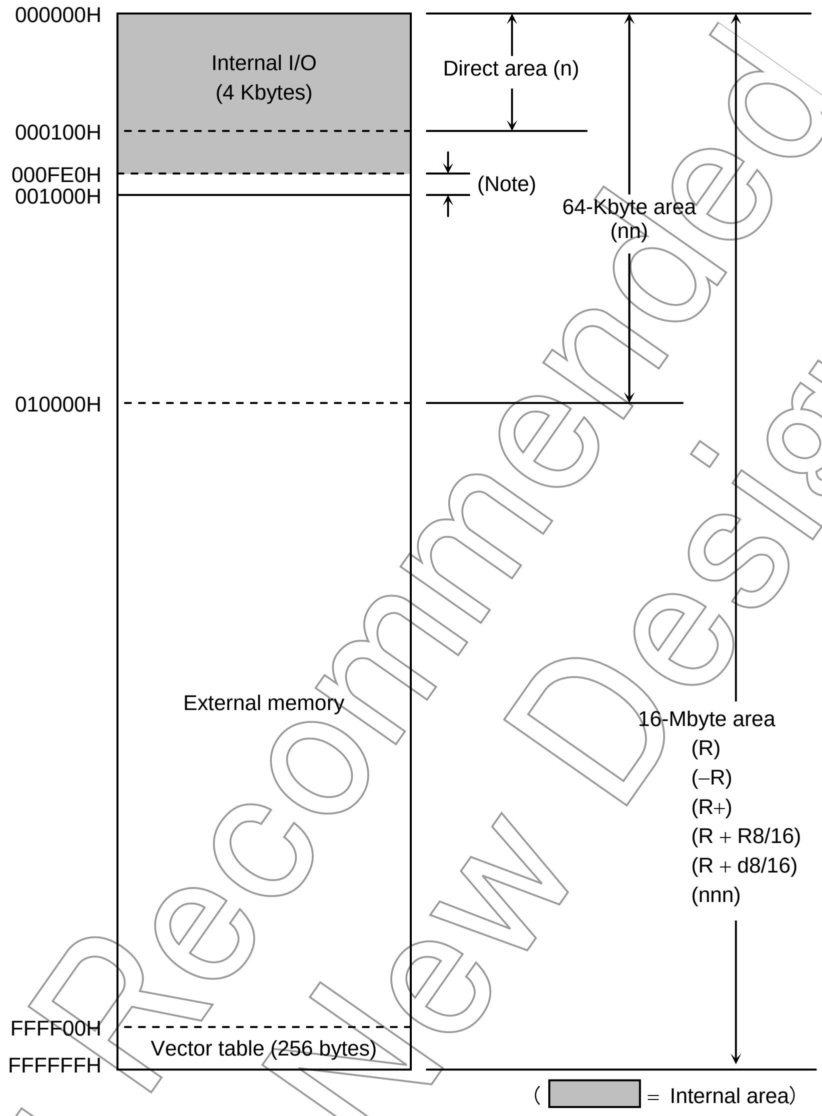


Figure 3.2.1 Memory Map

Note: Address 000FE0H to 000FEFH is assigned for the external memory area of built-in RAM type LCD driver.
Address 000FF0H to 000FFFH is assingned for the external memory area as reserved.

3.3 Triple Clock Function and Standby Function

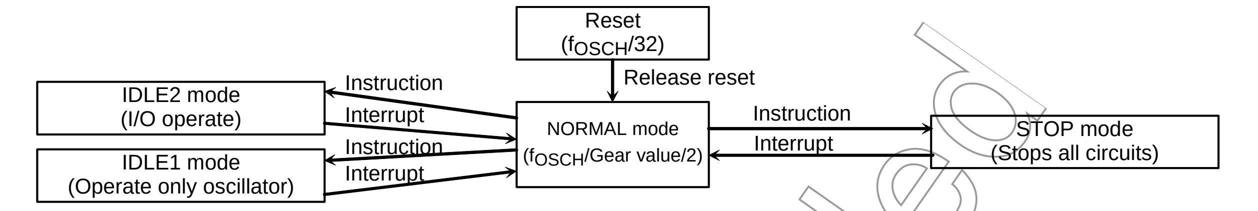
TMP91C025 contains a clock gear, clock doubler (DFM), standby controller and noise-reduction circuit. It is used for low-power and low-noise systems.

This chapter is organized as follows:

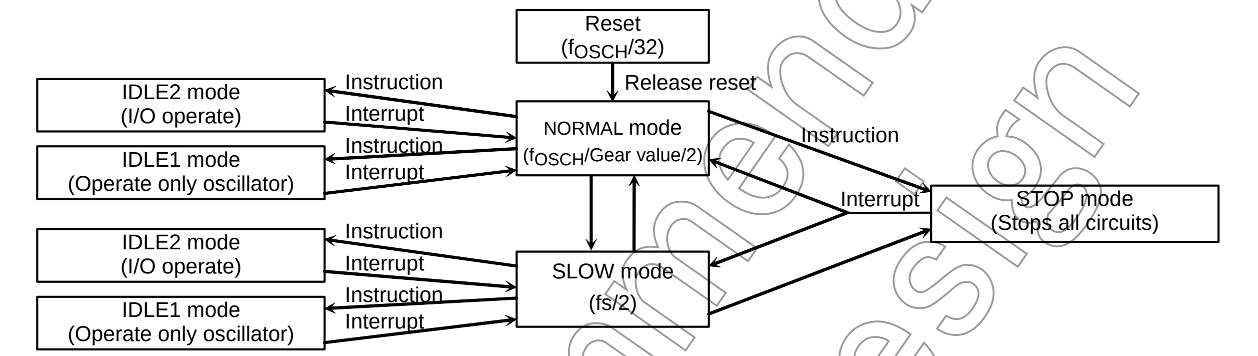
3.3.1 Block Diagram of System Clock
3.3.2 SFRs
3.3.3 System Clock Controller
3.3.4 Prescaler Clock Controller
3.3.5 Clock Doubler (DFM)
3.3.6 Noise reducing Circuit
3.3.7 Standby Controller

The clock operating modes are as follows: (a) Single clock mode (X1, X2 pins only), (b) Dual clock mode (X1, X2, XT1 and XT2 pins) and (c) Triple clock mode (the X1, X2, XT1 and XT2 pins and DFM).

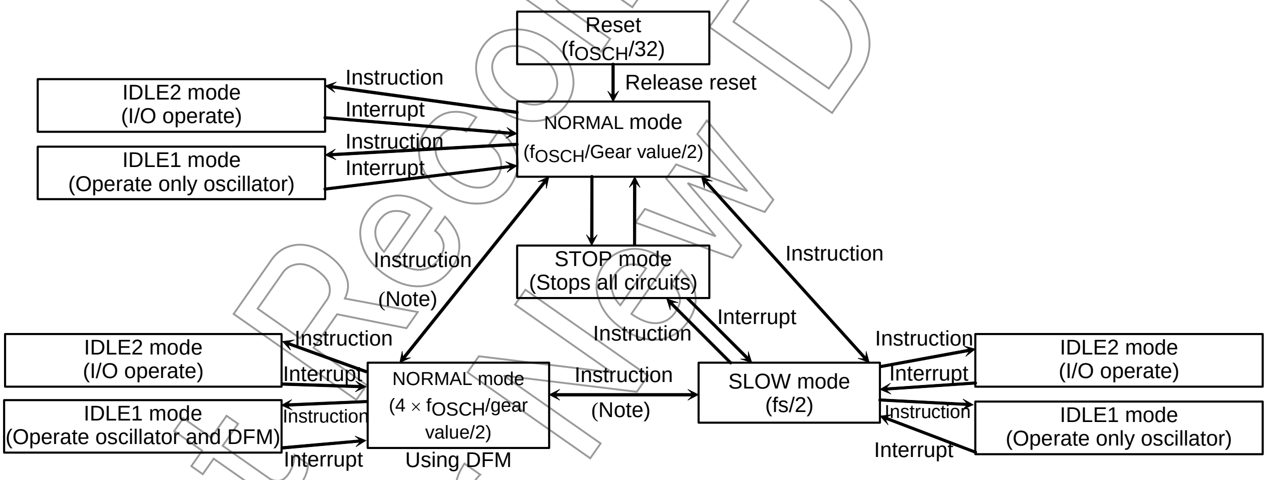
Figure 3.3.1 shows a transition figure.



(a) Single clock mode transition figure



(b) Dual clock mode transition figure



(c) Triple clock mode trasision figure

Note 1: It's prohibited to control DFM in SLOW mode when shifting from SLOW mode to NORMAL mode with use of DFM. (DFM start up/stop/change write to DFMCR0<ACT1:0> register)

Note 2: If you shift from NORMAL mode with use of DFM to NORMAL mode, the instruction should be separated into two procedures as below. Change CPU clock → Stop DFM circuit

Note 3: It's prohibited to shift from NORMAL mode with use of DFM to STOP mode directly. You should set NORMAL mode once, and then shift to STOP mode.(You should stop high frequency oscillator after you stop DFM.)

Figure 3.3.1 System Clock Block Diagram

The clock frequency input from the X1 and X2 pins is called fc and the clock frequency input from the XT1 and XT2 pins is called fs. The clock frequency selected by SYSCR1<SYSCK> is called the system clock f_{FPH}. The system clock f_{SYS} is defined as the divided clock of f_{FPH}, and one cycle of f_{SYS} is defined to as one state.

3.3.1 Block Diagram of System Clock

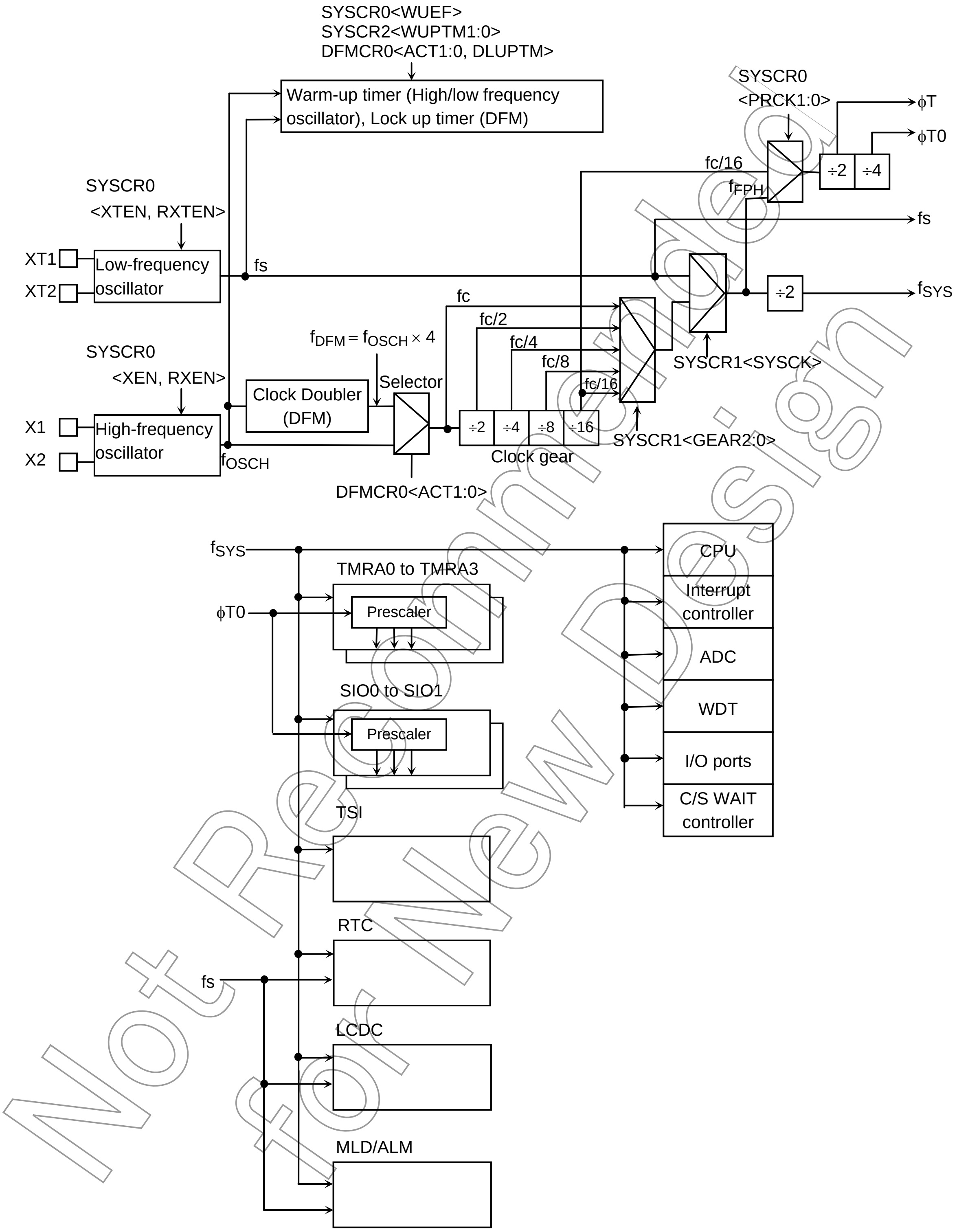


Figure 3.3.2 Block Diagram of System Clock

3.3.2 SFRs

SYSCR0 (00E0H)

	7	6	5	4	3	2	1	0
Bit symbol	XEN	XTEN	RXEN	RXTEN	RSYSCK	WUEF	PRCK1	PRCK0
Read/Write	R/W							
After reset	1	1	1	0	0	0	0	0
Function	High-frequency oscillator (fc) 0: Stop 1: Oscillation	Low-frequency oscillator (fs) 0: Stop 1: Oscillation (Note 1)	High-frequency oscillator (fc) after release of STOP mode 0: Stop 1: Oscillation	Low-frequency oscillator (fs) after release of STOP mode 0: Stop 1: Oscillation	Selects clock after release of STOP mode 0: fc 1: fs	Warm-up timer 0: Write Don't care 1: Write start timer 0: Read end warm-up 1:Read do not end warm-up	Select prescaler clock 00: f_{FPH} 01: Reserved 10: fc/16 11: Reserved	

SYSCR1 (00E1H)

	7	6	5	4	3	2	1	0
Bit symbol					SYSCK	GEAR2	GEAR1	GEAR0
Read/Write					R/W			
After reset					0	1	0	0
Function					Select system clock 0: fc 1: fs	Select gear value of high-frequency (fc) 000: fc 001: fc/2 010: fc/4 011: fc/8 100: fc/16 101: (Reserved) 110: (Reserved) 111: (Reserved)		

SYSCR2 (00E2H)

	7	6	5	4	3	2	1	0
Bit symbol	PSENV		WUPTM1	WUPTM0	HALTM1	HALTM0	SELDRV	DRVE
Read/Write	R/W		R/W	R/W	R/W	R/W	R/W	R/W
After reset	0		1	0	1	1	0	0
Function	0: Power save mode enable 1: Disable (Note 2)		Warm-up timer 00: Reserved 01: 2^8/inputted frequency 10: 2^{14} 11: 2^{16}		HALT mode 00: Reserved 01: STOP mode 10: IDLE1 mode 11: IDLE2 mode		<DRVE> mode select 0: IDLE1 1: STOP (Note 3)	Pin state control in STOP/IDLE1 mode 0: I/O off 1: Remains the state before halt

Note 1: By reset, low-frequency oscillator is enabled.

Note 2: When hard ware standby mode is entered, the meaning of SYSCR2<HALTM1:0> = 11 shows IDLE1 mode.

Note 3: "0" means IDLE1 and "1" means STOP. Please be carefull because this setting is sometimes different from others.

Figure 3.3.3 SFRs for System Clock

Symbol	Name	Address	7	6	5	4	3	2	1	0
DFMCR0	DFM control register 0	E8H	ACT1	ACT0	DLUPFG	DLUPTM				
			R/W	R/W	R	R/W				
			0	0	0	0				
			DFM LUP select f_{FPH} 00 STOP STOP f_{OSCH} 01 RUN RUN f_{OSCH} 10 RUN STOP f_{DFM} 11 RUN STOP f_{OSCH}		Lock up status Flag 0: End 1: Not end	Lock up Time 0: $2^{12}/f_{OSCH}$ 1: $2^{10}/f_{OSCH}$				
DFMCR1	DFM control register 1	E9H	D7	D6	D5	D4	D3	D2	D1	D0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	1	0	0	1	1
			DFM revision Input frequency 4 to 9 MHz (at 3.0 V to 3.6 V): write 0BH Input frequency 4 to 6.75 MHz (at 2.7 V to 3.6 V): write 0BH							

Figure 3.3.4 SFRs for DFM

Limitation point on the use of DFM

1. It's prohibited to execute DFM enable/disable control in the SLOW mode (fs) (write to DFMCR0<ACT1:0> = "10"). You should control DFM in the NORMAL mode.

2. If you stop DFM operation during using DFM(DFMCR0<ACT1:0> = "10"), you shouldn't execute that change the clock f_{DFM} to f_{OSCH} and stop the DFM at the same time. Therefore the above execution should be separated into two procedures as showing below.

```
LD    (DFMCR0), C0H    ;  Change the clock fDFM to fOSCH
LD    (DFMCR0), 00H    ;  DFM stop
```

3. If you stop high-frequency oscillator during using DFM (DFMCR0<ACT1:0> = "10"), you should stop DFM before you stop high-frequency oscillator.

Please refer to 3.3.5 Clock Doubler (DFM) for the Details.

Register		7	6	5	4	3	2	1	0
EMCCR0 (00E3H)	Bit symbol	PROTECT	TA3LCDE	AHOLD	TA3MLDE	–	EXTIN	DRVOSCH	DRVOSCL
	Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	After reset	0	0	0	0	0	0	1	1
	Function	Protect flag 0: Off 1: On	LCDC source CLK 0: 32 kHz 1: TA3OUT	Address hold 0: Disable 1: Enable (Note)	Melody/alarm source clock 0: 32 kHz 1: TA3OUT	Always write 0.	1: External clock	fc oscillator driver ability 1: Normal 0: Weak	fs oscillator driver ability 1: Normal 0: Weak
EMCCR1 (00E4H)	Bit symbol	Switching the protect ON/OFF by write to following 1st-KEY, 2nd-KEY 1st-KEY: EMCCR1 = 5AH, EMCCR2 = A5H in succession write 2nd-KEY: EMCCR1 = A5H, EMCCR2 = 5AH in succession write							
	Read/Write								
	After reset								
	Function								
EMCCR2 (00E5H)	Bit symbol								
	Read/Write								
	After reset								
	Function								
EMCCR3 (00E6H)	Bit symbol		ENFROM	ENDROM	ENPROM		FFLAG	DFLAG	PFLAG
	Read/Write		R/W	R/W	R/W		R/W	R/W	R/W
	After reset		0	0	0		0	0	0
	Function		CS1A area detect control 0: Disable 1: Enable	CS2B-2C area detect control 0: Disable 1: Enable	CS2A area detect control 0: Disable 1: Enable		CS1A write operation flag	CS2B-2C write operation flag	CS2A write operation flag
							When reading 0: Not written 1: Written		When writing 0: Clear flag

Note1: When getting access to the logic address 000000H to 000FDFH, A0 to A23 holds the previous address of external access.

Note2: In case restarting the oscillator in the stop oscillation state (e.g. Restart the oscillator in STOP mode), set EMCCR0<DRVOSCH>, <DRVOSCL>="1".

Figure 3.3.5 SFRs for Noise Reduction

3.3.3 System Clock Controller

The system clock controller generates the system clock signal (f_{SYS}) for the CPU core and internal I/O. It contains two oscillation circuits and a clock gear circuit for high-frequency (fc) operation. The register SYSCR1<SYSCK> changes the system clock to either fc or fs, SYSCR0<XEN> and SYSCR0<XTEN> control enabling and disabling of each oscillator, and SYSCR1<GEAR0:2> sets the high-frequency clock gear to either 1, 2, 4, 8 or 16 (fc, fc/2, fc/4, fc/8 or fc/16). These functions can reduce the power consumption of the equipment in which the device is installed.

The combination of settings <XEN> = 1, <XTEN> = 0, <SYSCK> = 0 and <GEAR0:2> = 100 will cause the system clock (f_{SYS}) to be set to fc/32 (fc/16 × 1/2) after a reset.

For example, f_{SYS} is set to 1.1 MHz when the 36 MHz oscillator is connected to the X1 and X2 pins.

(1) Switching from NORMAL mode to SLOW mode

When the resonator is connected to the X1 and X2 pins, or to the XT1 and XT2 pins, the warm-up timer can be used to change the operation frequency after stable oscillation has been attained.

The warm-up time can be selected using SYSCR2<WUPTM0:1>.

This warm-up timer can be programmed to start and stop as shown in the following examples 1 and 2.

Table 3.3.1 shows the warm-up time.

Note 1: When using an oscillator (other than a resonator) with stable oscillation, a warm-up timer is not needed.

Note 2: The warm-up timer is operated by an oscillation clock. Hence, there may be some variation in warm-up time.

Table 3.3.1 Warm-up Times

Warm-up Time SYSCR2 <WUPTM1:0>	Change to NORMAL Mode	Change to SLOW Mode
01 (2^8/frequency)	7.1 (μs)	7.8 (ms)
10 (2^{14}/frequency)	0.455 (ms)	500 (ms)
11 (2^{16}/frequency)	1.820 (ms)	2000 (ms)

at f_{OSCH} = 36 MHz, fs = 32.768 kHz

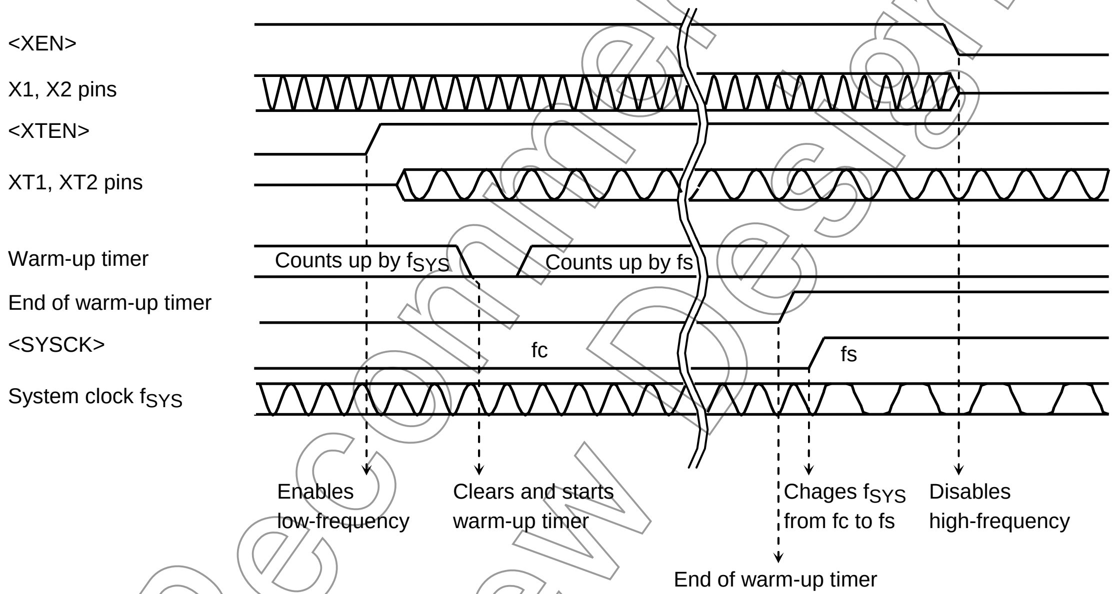
(Example 1: Setting the clock)

Changing from high-frequency (fc) to low-frequency (fs).

```
SYSCR0   EQU   00E0H
SYSCR1   EQU   00E1H
SYSCR2   EQU   00E2H
         LD    (SYSCR2), - X11 - - - - B   ;  Sets warm-up time to 2^16/fs.
         SET   6, (SYSCR0)                 ;  Enables low-frequency oscillation.
         SET   2, (SYSCR0)                 ;  Clears and starts warm-up timer.
WUP:     BIT   2, (SYSCR0)                 ;  } Detects stopping of warm-up timer.
         JR    NZ, WUP                     ;  }
         SET   3, (SYSCR1)                 ;  Changes fSYS from fc to fs.
         RES   7, (SYSCR0)                 ;  Disables high-frequency oscillation.
```

x: Don’t care

-: No change



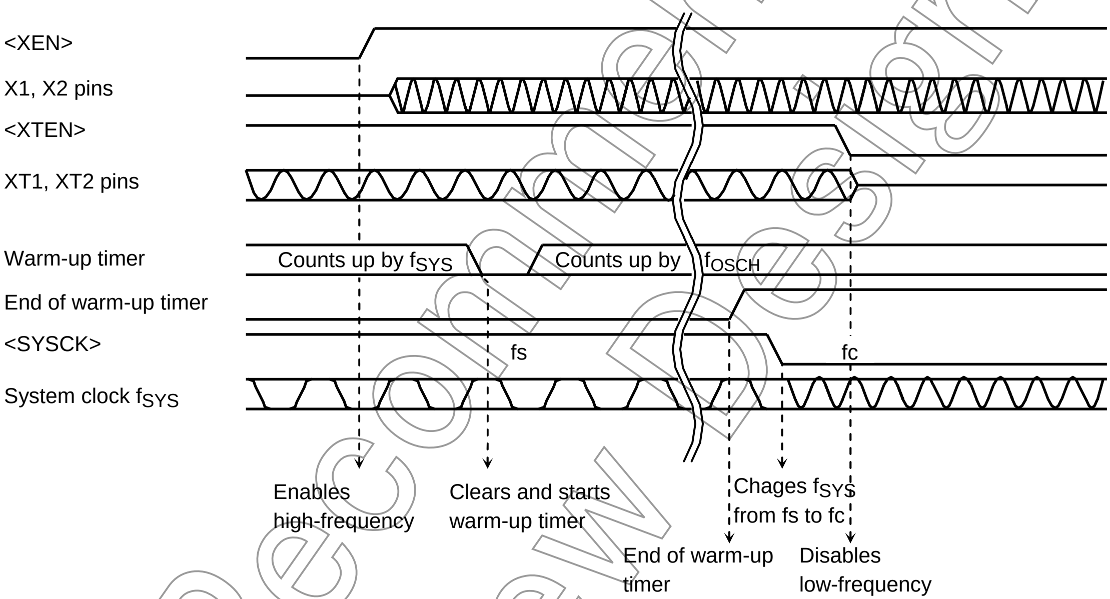
(Example 2: Setting the clock)

Changing from low-frequency (fs) to high-frequency (fc).

```
SYSCR0   EQU   00E0H
SYSCR1   EQU   00E1H
SYSCR2   EQU   00E2H
         LD    (SYSCR2), -X10 - - - - B   ;  Sets warm-up time to 2^14/fc.
         SET   7, (SYSCR0)                ;  Enables high-frequency oscillation.
         SET   2, (SYSCR0)                ;  Clears and starts warm-up timer.
WUP:     BIT   2, (SYSCR0)                ;  } Detects stopping of warm-up timer.
         JR    NZ, WUP                    ;  }
         RES   3, (SYSCR1)                ;  Changes fSYS from fs to fc.
         RES   6, (SYSCR0)                ;  Disables low-frequency oscillation.
```

x: Don’t care

-: No change



(2) Clock gear controller

When the high-frequency clock fc is selected by setting SYSCR1<SYSCK> = 0, f_{FPH} is set according to the contents of the clock gear select register SYSCR1<GEAR2:0> to either fc, fc/2, fc/4, fc/8 or fc/16. Using the clock gear to select a lower value of f_{FPH} reduces power consumption.

(Example 3)

Changing to a high-frequency gear

```
SYSCR1    EQU    00E1H
          LD     (SYSCR1), XXXX0000B        ;    Changes fSYS to fc/2.
```

X: Don't care

(High-speed clock gear changing)

To change the clock gear, write the register value to the SYSCR1<GEAR2:0> register.It is necessary the warm-up time until changing after writing the register value.

There is the possibility that the instruction next to the clock gear changing instruction is executed by the clock gear before changing.To execute the instruction next to the clock gear switching instruction by the clock gear after changing,input the dummy instruction as follows (Instruction to execute the write cycle).

(Example)

```
SYSCR1    EQU    00E1H
          LD     (SYSCR1), XXXX0001B        ;    Changes fSYS to fc/4.
          LD     (DUMMY), 00H               ;    Dummy instruction
          Instruction to be executed after clock gear has changed
```

(3) Internal clock output pin

An internal clock f_{FPH} can be output to the PA3/SCOUT pin. By setting “1” to the PAFC2<PA3F2> register, the PA3 pin functions as the SCOUT pin.

3.3.4 Prescaler Clock Controller

For the internal I/O (TMRA01 to TMRA23, SIO0 to SIO1) there is a prescaler which can divide the clock.

The φT0 clock input to the prescaler is either the clock f_{FPH} divided by 4 or the clock fc/16 divided by 4. The setting of the SYSCR0<PRCK0:1> register determines which clock signal is input.

3.3.5 Clock Doubler (DFM)

DFM outputs the f_{DFM} clock signal, which is four times as fast as f_{OSCH}. It can use the low-frequency oscillator, even though the internal clock is high frequency .

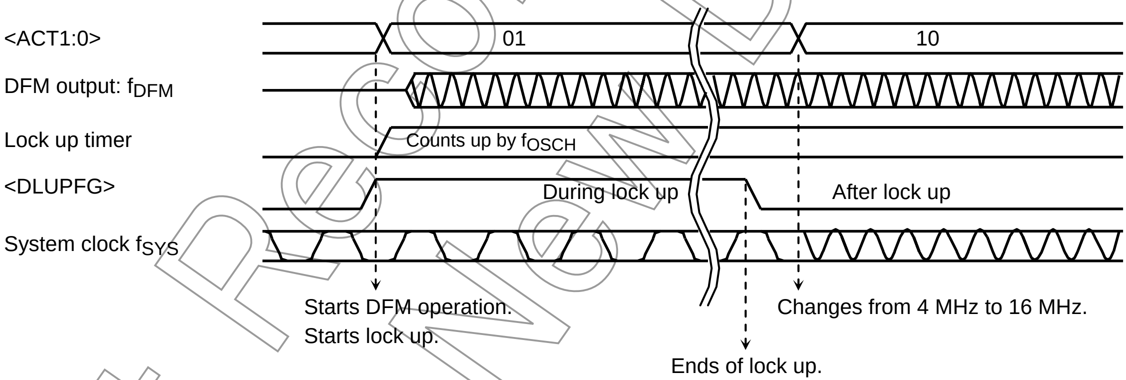
A reset initializes DFM to stop status, setting to DFMCR0-register is needed before use.

Like an oscillator, this circuit requires time to stabilize. This is called the lock up time.

The following example shows how DFM is used.

```
DFMCR0   EQU   00E8H
DFMCR1   EQU   00E9H
         LD    (DFMCR1), 00001011B        DFM parameter setting.
         LD    (DFMCR0), 01X0XXXXB   ;    Set lock up time to 2^12/4 MHz.
                                          Enables DFM operation and starts lock up.
LUP:     BIT   5, (DFMCR0)           ; }
         JR    NZ, LUP               ; }  Detects end of lock up.
         LD    (DFMCR0), 10X0XXXXB   ;    Changes fc from 4 MHz to 16 MHz.
                                          (Changes fSYS from 2 MHz to 8 MHz.)
```

X: Don't care



Note: Input frequency limitation and correction for DFM

Recommend to use Input frequency (High-speed oscillation) for DFM in the following condition.

- f_{OSCH} = 4 to 9 MHz (Vcc = 3.0 to 3.6 V): Write 0BH to DFMCR1
- f_{OSCH} = 4 to 6.75 MHz (Vcc = 2.7 to 3.6 V): Write 0BH to DFMCR1

Limitation point on the use of DFM

1. It's prohibited to execute DFM enable/disable control in the SLOW mode (fs) (write to DFMCR0<ACT1:0> = "10"). You should control DFM in the NORMAL mode.
2. If you stop DFM operation during using DFM (DFMCR0<ACT1:0> = "10"), you shouldn't execute the commands that change the clock f_{DFM} to f_{OSCH} and stop the DFM at the same time. Therefore the above executions should be separated into two procedures as showing below.

```
        LD      (DFMCR0), C0H               ;  Change the clock fDFM to fOSCH.
        LD      (DFMCR0), 00H               ;  DFM stop.
```

3. If you stop high-frequency oscillator during using DFM (DFMCR0<ACT1:0> = "10"), you should stop DFM before you stop high-frequency oscillator.

Examples of settings are below.

(1) Start up/change control

(OK) Low-frequency oscillator operation mode (fs) (High-frequency oscillator STOP) → High-frequency oscillator start up → High-frequency oscillator operation mode (f_{OSCH}) → DFM start up → DFM use mode (f_{DFM})

```
        LD      (SYSCR0), 11 - - - 1 - - B  ;  High-frequency oscillator start up/warm-up start.
WUP:    BIT     2, (SYSCR0)                 ;  } Check for the flag of warm-up end.
        JR      NZ, WUP                     ;  }
        LD      (SYSCR1), - - - - 0 - - - B ;  Change the system clock fs to fOSCH.
        LD      (DFMCR0), 01 - 0 - - - - B  ;  DFM start up/lock up start.
LUP:    BIT     5, (DFMCR0)                 ;  } Check for the flag of lock up end.
        JR      NZ, LUP                     ;  }
        LD      (DFMCR0), 10 - 0 - - - - B  ;  Change the system clock fOSCH to fDFM.
```

(OK) Low-frequency oscillator operation mode (fs) (High-frequency oscillator operate) → High-frequency oscillator operation mode (f_{OSCH}) → DFM start up → DFM use mode (f_{DFM})

```
        LD      (SYSCR1), - - - - 0 - - - B ;  Change the system clock fs to fOSCH.
        LD      (DFMCR0), 01 - 0 - - - - B  ;  DFM start up/lock up start.
LUP:    BIT     5, (DFMCR0)                 ;  } Check for the flag of lock up end.
        JR      NZ, LUP                     ;  }
        LD      (DFMCR0), 10 - 0 - - - - B  ;  Change the system clock fOSCH to fDFM.
```

(Error) Low-frequency oscillator operation mode (fs) (High-frequency oscillator STOP) → High-frequency oscillator start up → DFM start up → DFM use mode (f_{DFM})

```
        LD      (SYSCR0), 11 - - - 1 - - B  ;  High-frequency oscillator starts up/warm-up start.
WUP:    BIT     2, (SYSCR0)                 ;  } Check for the flag of warm-up end.
        JR      NZ, WUP                     ;  }
        LD      (DFMCR0), 01 - 0 - - - - B  ;  DFM start up/lock up start.
LUP:    BIT     5, (DFMCR0)                 ;  } Check for the flag of lock up end.
        JR      NZ, LUP                     ;  }
        LD      (DFMCR0), 10 - 0 - - - - B  ;  Change the internal clock fOSCH to fDFM.
        LD      (SYSCR1),  - - - - 0 - - - B ;  Change the system clock fs to fDFM.
```

(2) Change/stop control

(OK) DFM use mode (f_{DFM}) → High-frequency oscillator operation mode (f_{OSCH}) → DFM stop → Low-frequency oscillator operation mode (fs) → High-frequency oscillator stop

```
LD    (DFMCR0), 11 - - - - - - B    ;  Change the system clock fDFM to fOSCH.
LD    (DFMCR0), 00 - - - - - - B    ;  DFM stop.
LD    (SYSCR1), - - - - 1 - - - B   ;  Change the system clock fOSCH to fs.
LD    (SYSCR0), 0 - - - - - - - B   ;  High-frequency oscillator stop.
```

(Error) DFM use mode (f_{DFM}) → Low-frequency oscillator operation mode (fs) → DFM stop → High-frequency oscillator stop

```
LD    (SYSCR1), - - - - 1 - - - B   ;  Change the system clock fDFM to fs.
LD    (DFMCR0), 11 - - - - - - B    ;  Change the internal clock (fc) fDFM to fOSCH.
LD    (DFMCR0), 00 - - - - - - B    ;  DFM stop.
LD    (SYSCR0), 0 - - - - - - - B   ;  High-frequency oscillator stop.
```

(OK) DFM use mode (f_{DFM}) → Set the STOP mode → High-frequency oscillator operation mode (f_{OSCH}) → DFM stop → HALT (High-frequency oscillator stop)

```
LD    (SYSCR2), - - - - 01 - - B    ;  Set the STOP mode.
                                       (This command can execute before use of DFM.)
LD    (DFMCR0), 11 - - - - - - B    ;  Change the system clock fDFM to fOSCH.
LD    (DFMCR0), 00 - - - - - - B    ;  DFM stop.
HALT                                ;  Shift to STOP mode.
```

(Error) DFM use mode (f_{DFM}) → Set the STOP mode → HALT (High-frequency oscillator stop)

```
LD    (SYSCR2), - - - - 01 - - B    ;  Set the STOP mode.
                                       (This command can execute before use of DFM.)
HALT                                ;  Shift to STOP mode.
```

3.3.6 Noise Reduction Circuits

Noise reduction circuits are built in, allowing implementation of the following features.

(1) Reduced drivability for high-frequency oscillator
(2) Reduced drivability for low-frequency oscillator
(3) Single drive for high-frequency oscillator
(4) SFR protection of register contents
(5) ROM protection of register contents

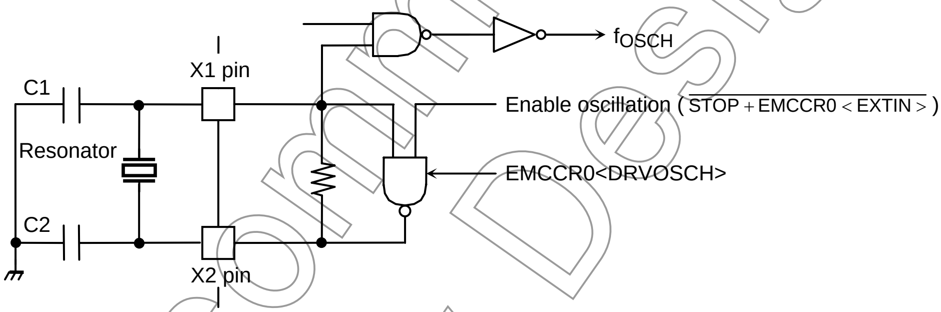
The above functions are performed by making the appropriate settings in the EMCCR0 to EMCCR3 registers.

(1) Reduced drivability for high-frequency oscillator

(Purpose)

Reduces noise and power for oscillator when a resonator is used.

(Block diagram)



(Setting method)

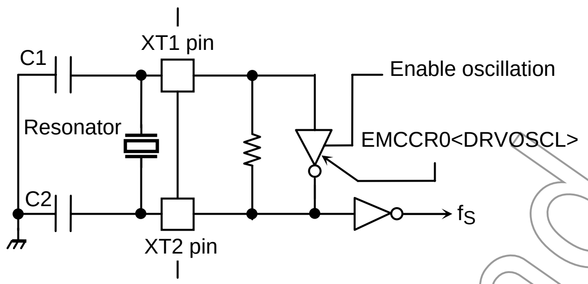
The drivability of the oscillator is reduced by writing 0 to EMCCR0<DRVOSCH> register. By reset, <DRVOSCH> is initialized to 1 and the oscillator starts oscillation by normal-drivability when the power-supply is on.

(2) Reduced drivability for low-frequency oscillator

(Purpose)

Reduces noise and power for oscillator when a resonator is used.

(Block diagram)



(Setting method)

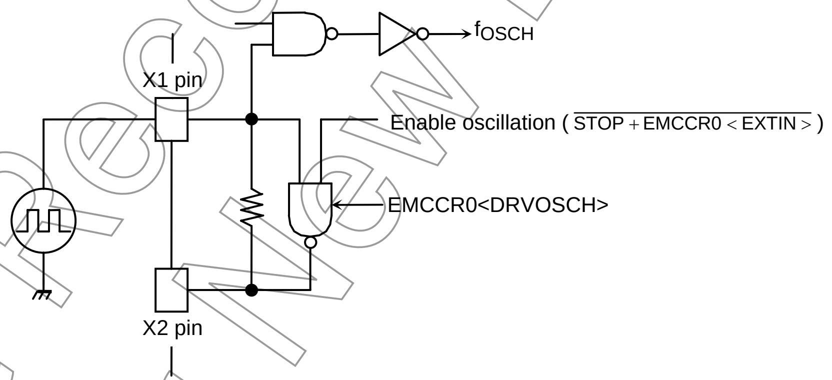
The drivability of the oscillator is reduced by writing 0 to the EMCCR0<DRVOSCL> register. By reset, <DRVOSCL> is initialized to 1.

(3) Single drive for high-frequency oscillator

(Purpose)

Not need twin-drive and protect mistake operation by inputted noise to X2 pin when the external-oscillator is used.

(Block diagram)



(Setting method)

The oscillator is disabled and starts operation as buffer by writing 1 to EMCCR0<EXTIN> register. X2-pin is always outputted 1.

By reset, <EXTIN> is initialized to 0.

Note: Do not write EMCCR0<EXTIN> = “1” when using external resonator.

(4) Runaway provision with SFR protection register

(Purpose)

Provision in runaway of program by noise mixing.

Write operation to specified SFR is prohibited so that provision program in runaway prevents that it is it in the state which is fetch impossibility by stopping of clock, memory control register (CS/WAIT controller, MMU) is changed.

And error handling in runaway becomes easy by INTP0 interruption.

Specified SFR list

1. CS/WAIT controller
   B0CS, B1CS, B2CS, B3CS, BEXCS,
   MSAR0, MSAR1, MSAR2, MSAR3,
   MAMR0, MAMR1, MAMR2, MAMR3
2. MMU
   LOCAL0/1/2/3
3. Clock gear
   SYSCR0, SYSCR1, SYSCR2, EMCCR0, EMCCR3
4. DFM
   DFMCR0, DFMCR1

(Operation explanation)

Execute and release of protection (write operation to specified SFR) becomes possible by setting up a double key to EMCCR1 and EMCCR2 register.

(Double key)

1st-KEY: Succession writes in 5AH at EMCCR1 and A5H at EMCCR2
2nd-KEY: Succession writes in A5H at EMCCR1 and 5AH at EMCCR2

A state of protection can be confirmed by reading EMCCR0<PROTECT>.

By reset, protection becomes OFF.

And INTP0 interruption occurs when write operation to specified SFR was executed with protection ON state.

(5) Runaway provision with ROM protection register

(Purpose)

Provision in runaway of program by noise mixing.

(Operation explanation)

When write operation was executed for external three kinds of ROM by runaway of program, INTP1 is occurred and detects runaway function.

Three kinds of ROM is fixed as for Flash ROM (Option program ROM), Data ROM, Program ROM are as follows on the logical address memory map.

1. Flash ROM: Address 400000H to 7FFFFFH
2. Data ROM: Address 800000H to BFFFFFH
3. Program ROM: Address C00000H to FFFFFFH

For these address, admission/prohibition of detection of write operation sets it up with EMCCR3<ENFROM, ENDROM, ENPROM>. And INTP1 interruption occurred within which ROM area in the case that occurred can confirm each with EMCCR3<FFLAG, DFLAG, PFLAG>. This flag is cleared when write in 0.

3.3.7 Standby Controller

(1) HALT modes

When the HALT instruction is executed, the operating mode switches to IDLE2, IDLE1 or STOP mode, depending on the contents of the SYSCR2<HALTM1:0> register.

The subsequent actions performed in each mode are as follows:

a. IDLE2: Only the CPU halts.

The internal I/O is available to select operation during IDLE2 mode. By setting the following register.

Table 3.3.2 Shows the registers of setting operation during IDLE2 mode.

Table 3.3.2 SFR Setting Operation during IDLE2 Mode

Internal I/O	SFR
TMRA01	TA01RUN<I2TA01>
TMRA23	TA23RUN<I2TA23>
SIO0	SC0MOD1<I2S0>
SIO1	SC1MOD1<I2S1>
AD converter	ADMOD1<I2AD>
WDT	WDMOD<I2WDT>

b. IDLE1: Only the oscillator and the RTC (Real-time clock) and MLD continue to operate.

c. STOP: All internal circuits stop operating.

The operation of each of the different HALT modes is described in Table 3.3.3.

Table 3.3.3 I/O Operation during HALT Modes

<table>
<tr><th colspan="2">HALT Mode</th><th>IDLE2</th><th>IDLE1</th><th>STOP</th></tr>
<tr><td colspan="2">SYSCR2<HALTM1:0></td><td>11</td><td>10</td><td>01</td></tr>
<tr><td rowspan="8">Block</td><td>CPU</td><td colspan="3">Stop</td></tr>
<tr><td>I/O ports</td><td>Keep the state when the HALT instruction was executed.</td><td colspan="2">See Table 3.3.6, Table 3.3.7</td></tr>
<tr><td>TMRA</td><td rowspan="4">Available to select operation block</td><td rowspan="5" colspan="2">Stop</td></tr>
<tr><td>SIO</td></tr>
<tr><td>AD converter</td></tr>
<tr><td>WDT</td></tr>
<tr><td>LCDC,
Interrupt controller</td><td rowspan="2">Operate</td></tr>
<tr><td>RTC, MLD</td><td>Possible to operate</td><td></td></tr>
</table>

(2) How to release the HALT mode

These halt states can be released by resetting or requesting an interrupt. The halt release sources are determined by the combination between the states of interrupt mask register <IFF2:0> and the HALT modes. The details for releasing the halt status are shown in Table 3.3.4.

- Released by requesting an interrupt

  The operating released from the HALT mode depends on the interrupt enabled status. When the interrupt request level set before executing the HALT instruction exceeds the value of interrupt mask register, the interrupt due to the source is processed after releasing the HALT mode, and CPU status executing an instruction that follows the HALT instruction. When the interrupt request level set before executing the HALT instruction is less than the value of the interrupt mask register, releasing the HALT mode is not executed. (In non-maskable interrupts, interrupt processing is processed after releasing the HALT mode regardless of the value of the mask register.) However only for INT0 to INT3, INTKEY, INTRTC and INTALM0 to INTALM4 interrupts, even if the interrupt request level set before executing the HALT instruction is less than the value of the interrupt mask register, releasing the the HALT mode is executed. In this case,interrupt processing, and CPU starts executing the instruction next to the HALT instruction,but the interrupt request flag is held at 1.

  Note: Usually, interrupts can release all halts status. However, the interrupts (INT0 to INT3, INTRTC, INTALM0 to INTALM4, INTKEY) which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)
  If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficulty. The priority of this interrupt is compared with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

- Releasing by resetting

  Releasing all halt status is executed by resetting.

  When the STOP mode is released by RESET, it is necessry enough resetting time (see Table 3.3.5) to set the operation of the oscillator to be stable.

Table 3.3.4 Source of Halt State Clearance and Halt Clearance Operation

Status of Received Interrupt		Interrupt Enabled (Interrupt level) ≥ (Interrupt mask)			Interrupt Disabled (Interrupt level) < (Interrupt mask)		
HALT Mode		IDLE2	IDLE1	STOP	IDLE2	IDLE1	STOP
Source of halt state clearance: Interrupt	INTWDT	♦	×	×	–	–	–
	INT0 to INT3 (Note 1)	♦	♦	♦ *1	○	○	○ *1
	INTALM0 to INTALM4	♦	♦	×	○	○	×
	INTTA0 to INTTA3	♦	×	×	×	×	×
	INTRX0 to INTRX1, TX0 to TX1	♦	×	×	×	×	×
	INTAD	♦	×	×	×	×	×
	INTKEY	♦	♦	♦ *1	○	○	○ *1
	INTRTC	♦	♦	×	○	○	×
	INTLCD	♦	×	×	×	×	×
Source of halt state clearance	RESET	Initialize LSI					

♦: After clearing the HALT mode, CPU starts interrupt processing.

○: After clearing the HALT mode, CPU resumes executing starting from instruction following the HALT instruction.

×: It can not be used to release the HALT mode.

–: The priority level (Interrupt request level) of non-maskable interrupts is fixed to 7, the highest priority level. There is not this combination type.

*1: Releasing the HALT mode is executed after passing the warm-up time.

Note 1: When the HALT mode is cleared by an INT0 interrupt of the level mode in the interrupt enabled status, hold level H until starting interrupt processing. If level L is set before holding level L, interrupt processing is correctly started.

(Example) Releasing IDLE1 mode

An INT0 interrupt clears the halt state when the device is in IDLE1 mode.

```
Address
8200H    LD     (PBFC), 00H      ; Sets PB3 to INT0.
8203H    LD     (IIMC), 00H      ; Selects INT0 interrupt rising edge.
8206H    LD     (INTE0AD), 06H   ; Sets INT0 interrupt level to 6.
8209H    EI     5                ; Sets interrupt level to 5 for CPU.
820BH    LD     (SYSCR2), 88H    ; Sets HALT mode to IDLE1 Mode.
820EH    HALT                    ; Halts CPU.
```


```
820FH    LD     XX, XX
```

(3) Operation

a. IDLE2 mode

In IDLE2 mode only specific internal I/O operations, as designated by the IDLE2 setting register, can take place. Instruction execution by the CPU stops.

Figure 3.3.6 illustrates an example of the timing for clearance of the IDLE2 mode halt state by an interrupt.

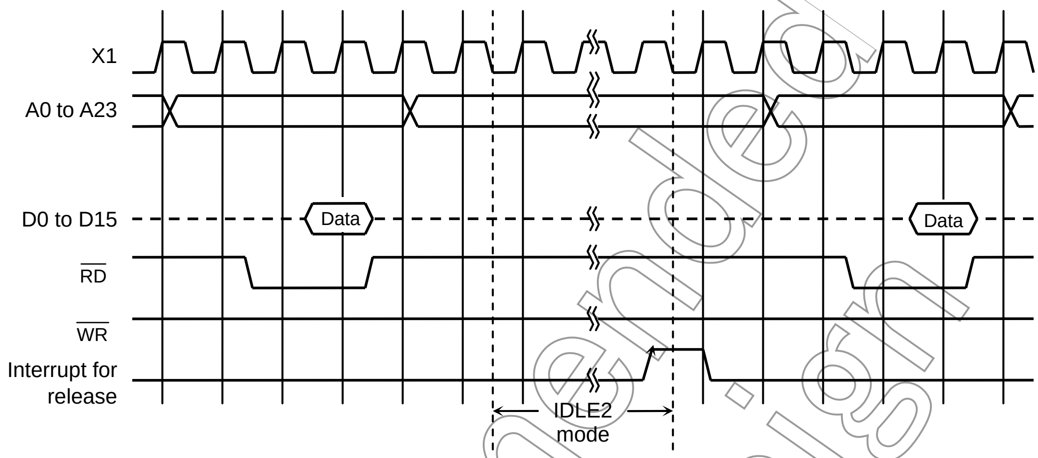


Figure 3.3.6 Timing Chart for IDLE2 Mode Halt State Cleared by Interrupt

b. IDLE1 mode

In IDLE1 mode, only the internal oscillator and the RTC, MLD continue to operate. The system clock in the MCU stops. The pin status in the IDLE1 mode is depended on setting the register SYSCR2<SELDRV, DRVE>. Table 3.3.6, Table 3.3.7 summarizes the state of these pins in the IDLE mode1.

In the halt state, the interrupt request is sampled asynchronously with the system clock; however, clearance of the halt state (e.g. restart of operation) is synchronous with it.

Figure 3.3.7 illustrates the timing for clearance of the IDLE1 mode halt state by an interrupt.

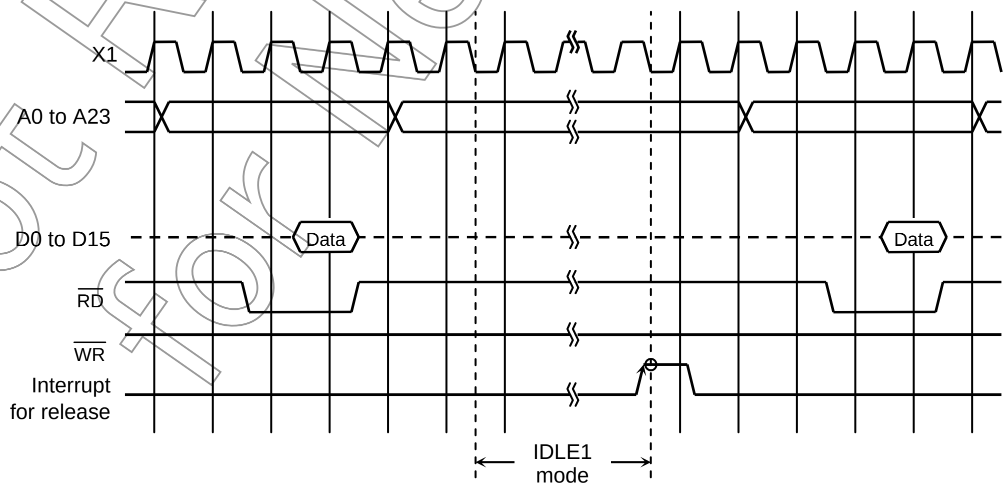


Figure 3.3.7 Timing Chart for IDLE1 Mode Halt State Cleared by Interrupt

c. STOP mode

When STOP mode is selected, all internal circuits stop, including the internal oscillator pin status in STOP mode depends on the settings in the SYSCR2<DRVE> register. Table 3.3.6, Table 3.3.7 summarizes the state of these pins in STOP mode.

After STOP mode has been cleared system clock output starts when the warm-up time has elapsed, in order to allow oscillation to stabilize. After STOP mode has been cleared, either NORMAL mode or SLOW mode can be selected using the SYSCR0<RSYSCK> register. Therefore, <RSYSCK>, <RXEN> and <RXTEN> must be set see the sample warm-up times in Table 3.3.5.

Figure 3.3.8 illustrates the timing for clearance of the STOP mode halt state by an interrupt.

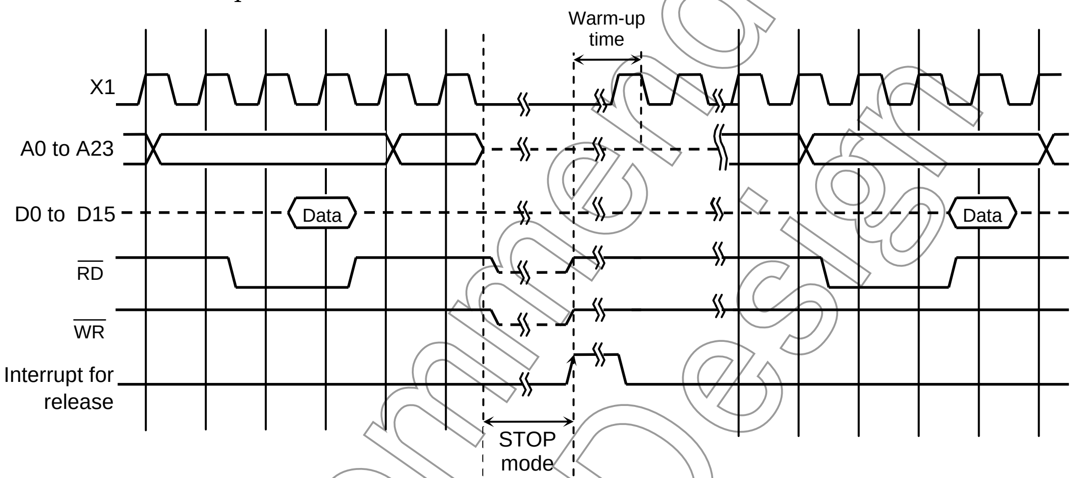


Figure 3.3.8 Timing Chart for STOP Mode Halt State Cleared by Interrupt

Table 3.3.5 Sample Warm-up Times after Clearance of STOP Mode

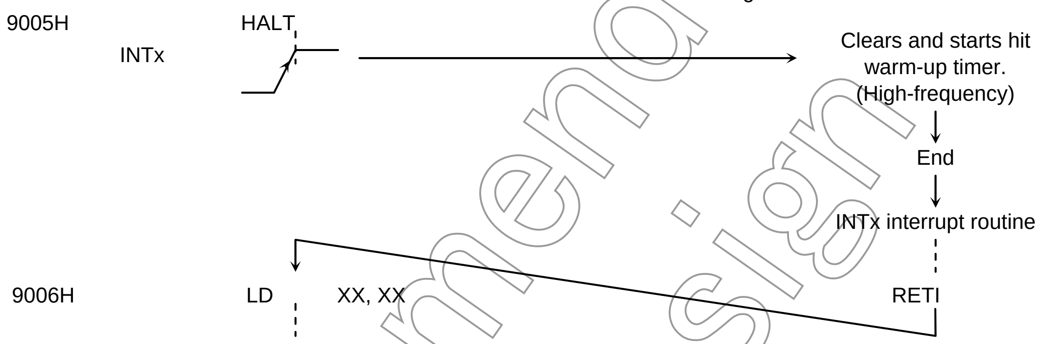
at f_{OSCH} = 36 MHz, fs =32.768 kHz

SYSCR0 <RSYSCK>	SYSCR2<WUPTM1:0>		
	01 (2^8)	10 (2^{14})	11 (2^{16})
0 (fc)	7.1 μs	0.455 ms	1.820 ms
1 (fs)	7.8 ms	500 ms	2000 ms

(Setting example)

The STOP mode is entered when the low-frequency operates, and high-frequency operates after releasing due to INTx.

```
Address
            SYSCR0    EQU    00E0H
            SYSCR1    EQU    00E1H
            SYSCR2    EQU    00E2H
8FFDH                 LD     (SYSCR1), 08H           ; fSYS = fs/2.
9000H                 LD     (SYSCR2), - X1001-1B    ; Sets warm-up time to 2^14/fOSCH.
9002H                 LD     (SYSCR0), 011000 - - B  ; Operates high-frequency after released.
                                                       – : No change
```



Note: When different modes are used before and after STOP mode as the above mentioned , there is possible to release the HALT mode without changing the operation mode by acceptance of the halt release interrupt request during execution of HALT instruction (during 6 states). In the system which accepts the interrupts during execution HALT instruction, set the same operation mode before and after the STOP mode.

Table 3.3.6 Input Buffer State Table

Port Name	Input Function Name	Input Buffer State								
		During Reset	When the CPU is operating		In HALT mode(IDLE2)		In HALT mode(IDLE1/STOP)			
							Condition A (Note)		Condition B (Note)	
			When Used as function Pin	When Used as Input Port	When Used as function Pin	When Used as Input Port	When Used as function Pin	When Used as Input Port	When Used as function Pin	When Used as Input Port
D0-7	–	OFF	ON upon external read	–	OFF	–	OFF	–	OFF	–
P10-17	D8-15			ON		OFF		OFF		OFF
P56 (*1)	$\overline{WAIT}$	ON	ON		ON	ON			ON	ON
P80-82 (*2)	–	OFF	–	ON upon port read	–	OFF	–		–	OFF
P83 (*2)	$\overline{ADTRG}$		ON		ON		ON		ON	
P90 (*1)	KI0	ON		ON		ON		ON		ON
P91 (*1)	KI1									
P92 (*1)	KI2									
P93 (*1)	KI3									
P94 (*1)	KI4									
P95 (*1)	KI5									
P96 (*1)	KI6									
P97 (*1)	KI7									
PB3	INT0, $\overline{PS}$									
PB4	INT1, TA0IN									
PB5	INT2	OFF				OFF		OFF		OFF
PB6	INT3									
PC0	–	ON	–		–	ON	–		–	ON
PC3 (*1)	–									
PC1	RXD0		ON		ON		OFF		ON	
PC2	SCLK0, $\overline{CTS0}$									
PC4	RXD1									
PC5 (*1)	SCLK1, $\overline{CTS1}$									
PZ2-Z3	–		–		–	OFF	–		–	OFF
$\overline{RESET}$, AM0,AM1	–		ON	–	ON	–	ON	–	ON	–
X1,XT1	–						IDLE1 : ON , STOP : OFF			

ON: The buffer is always turned on. A current flows the input buffer if the input pin is not driven.

OFF: The buffer is always turned off.

–: No applicable

*1: Port having a pull-up/pull-down resistor.

*2:AIN input does not cause a current to flow through the buffer.

Note: Condition A/B are as follows.

SYSCR2 register setting		HALT mode	
<DRVE>	<SELDRV>	IDLE1	STOP
0	0	Condition A	Condition A
0	1	Condition B	
1	0		Condition B
1	1		

Table 3.3.7 Output Buffer State Table

<table>
<tr><th rowspan="4">Port Name</th><th rowspan="4">Output Function Name</th><th colspan="9">Output Buffer State</th></tr>
<tr><th rowspan="3">During Reset</th><th colspan="2" rowspan="2">When the CPU is operating</th><th colspan="2" rowspan="2">In HALT mode(IDLE2)</th><th colspan="4">In HALT mode(IDLE1/STOP)</th></tr>
<tr><th colspan="2">Condition A (Note)</th><th colspan="2">Condition B (Note)</th></tr>
<tr><th>When Used as function Pin</th><th>When Used as Output Port</th><th>When Used as function Pin</th><th>When Used as Output Port</th><th>When Used as function Pin</th><th>When Used as Output Port</th><th>When Used as function Pin</th><th>When Used as Output Port</th></tr>
<tr><td>D0-7</td><td>–</td><td rowspan="2">OFF</td><td rowspan="2">ON upon external write</td><td>–</td><td rowspan="2">OFF</td><td>–</td><td rowspan="4">OFF</td><td>–</td><td rowspan="2">OFF</td><td>–</td></tr>
<tr><td>P10-17</td><td>D8-15</td><td>ON</td><td>ON</td><td>OFF</td><td>ON</td></tr>
<tr><td>A0-15</td><td>–</td><td rowspan="2">ON</td><td rowspan="2">ON</td><td>–</td><td rowspan="2">ON</td><td>–</td><td>–</td><td rowspan="2">ON</td><td>–</td></tr>
<tr><td>P20-27</td><td>A16-23</td><td rowspan="13">ON</td><td rowspan="13">ON</td><td rowspan="13">OFF</td><td rowspan="13">ON</td></tr>
<tr><td>P56 (*1)</td><td>–</td><td>OFF</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>P60</td><td>$\overline{CS0}$</td><td rowspan="10">ON</td><td rowspan="10">ON</td><td rowspan="10">ON</td><td rowspan="10">OFF</td><td rowspan="10">ON</td></tr>
<tr><td>P61</td><td>$\overline{CS1}$</td></tr>
<tr><td>P62</td><td>$\overline{CS2}$, $\overline{CS2A}$</td></tr>
<tr><td>P63</td><td>$\overline{CS3}$</td></tr>
<tr><td>P64</td><td>EA24, $\overline{CS2B}$, $\overline{SRLB}$</td></tr>
<tr><td>P65</td><td>EA25, $\overline{CS2C}$, $\overline{SRUB}$</td></tr>
<tr><td>PA0</td><td>KO0, $\overline{ALARM}$, $\overline{MLDALM}$</td></tr>
<tr><td>PA1</td><td>KO1,TA1OUT</td></tr>
<tr><td>PA2</td><td>KO2,TA3OUT</td></tr>
<tr><td>PA3</td><td>KO3,SCOUT</td></tr>
<tr><td>PB3-B4</td><td>–</td><td rowspan="8">OFF</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>PB5</td><td>PX</td><td rowspan="3">ON</td><td rowspan="2">–</td><td rowspan="3">ON</td><td rowspan="2">–</td><td rowspan="2">ON</td><td rowspan="2">–</td><td rowspan="3">ON</td><td rowspan="2">–</td></tr>
<tr><td>PB6</td><td>PY</td></tr>
<tr><td>PC0</td><td>TXD0</td><td rowspan="11">ON</td><td rowspan="11">ON</td><td>OFF</td><td rowspan="11">OFF</td><td rowspan="11">ON</td></tr>
<tr><td>PC1,C4</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>PC2</td><td>SCLK0</td><td rowspan="12">ON</td><td rowspan="12">ON</td><td rowspan="12">OFF</td><td rowspan="12">ON</td></tr>
<tr><td>PC3 (*1)</td><td>TXD1</td></tr>
<tr><td>PC5</td><td>SCLK1</td></tr>
<tr><td>PD0 (*1)</td><td>D1BSCP</td><td rowspan="7">ON</td></tr>
<tr><td>PD1</td><td>D2BLP</td></tr>
<tr><td>PD2</td><td>D3BFR</td></tr>
<tr><td>PD3</td><td>DLEBCD</td></tr>
<tr><td>PD4</td><td>DOFFB</td></tr>
<tr><td>PD7</td><td>MLDALM</td></tr>
<tr><td>$\overline{RD}$, $\overline{WR}$</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>PZ2 (*1)</td><td>$\overline{HWR}$</td><td rowspan="2">OFF</td><td rowspan="2">ON</td><td rowspan="2">ON</td><td rowspan="2">OFF</td><td rowspan="2">ON</td></tr>
<tr><td>PZ3 (*1)</td><td>R/W, $\overline{SRWR}$</td></tr>
<tr><td>X2</td><td>–</td><td rowspan="2">ON</td><td rowspan="2">ON</td><td rowspan="2">–</td><td rowspan="2">ON</td><td rowspan="2">–</td><td colspan="4">IDLE1 : ON , STOP : Output “H” level</td></tr>
<tr><td>XT2</td><td>–</td><td colspan="4">IDLE1 : ON , STOP : High-Z</td></tr>
</table>

ON : The buffer is always turned on. When the bus is released , however ,output buffers for some pins are turned off.

*1:Port having a pull-up/pull-down resistor.

OFF: The buffer is always turned off.

– : No applicable

Note: Condition A/B are as follows.

<table>
<tr><th colspan="2">SYSCR2 register setting</th><th colspan="2">HALT mode</th></tr>
<tr><th><DRVE></th><th><SELDRV></th><th>IDLE1</th><th>STOP</th></tr>
<tr><td>0</td><td>0</td><td>Condition A</td><td rowspan="2">Condition A</td></tr>
<tr><td>0</td><td>1</td><td rowspan="3">Condition B</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">Condition B</td></tr>
<tr><td>1</td><td>1</td></tr>
</table>

3.4 Interrupts

Interrupts are controlled by the CPU interrupt mask register SR<IFF2:0> and by the built-in interrupt controller.

The TMP91C025 has a total of 37 interrupts divided into the following three types:

- Interrupts generated by CPU: 9 sources
  (Software interrupts, illegal instruction interrupt)
- Internal interrupts: 23 sources
- Interrupts on external pins (INT0 to INT3, INTKEY): 5 sources

A (fixed) individual interrupt vector number is assigned to each interrupt.

One of six (variable) priority level can be assigned to each maskable interrupt.

The priority level of non-maskable interrupts are fixed at 7 as the highest level.

When an interrupt is generated, the interrupt controller sends the piority of that interrupt to the CPU.If multiple interrupts are generated simultaneously, the interrupt controller sends the interrupt with the highest priority to the CPU. (The highest priority is level 7 using for non-maskable interrupts.)

The CPU compares the priority level of the interrupt with the value of the CPU interrupt mask register <IFF2:0>. If the priority level of the interrupt is higher than the value of the interrupt mask register, the CPU accepts the interrupt.

The interrupt mask register <IFF2:0> value can be updated using the value of the EI instruction (EI num sets <IFF2:0> data to num).

For example, specifying EI 3 enables the maskable interrupts which priority level set in the interrupt controller is 3 or higher, and also non-maskable interrupts.

Operationally, the DI instruction (<IFF2:0> = 7) is identical to the EI 7 instruction. DI instruction is used to disable maskable interrupts because of the priority level of maskable interrupts is 1 to 6. The EI instruction is vaild immediately after execution.

In addition to the above general-purpose interrupt processing mode, TLCS-900/L1 has a micro DMA interrupt processing mode as well. The CPU can transfer the data (1/2/4 bytes) automatically in micro DMA mode, therefore this mode is used for speed-up interrupt processing, such as transferring data to the internal or external peripheral I/O. Moreover, TMP91C025 has software start function for micro DMA processing request by the software not by the hardware interrupt.

Figure 3.4.1 shows the overall interrupt processing flow.

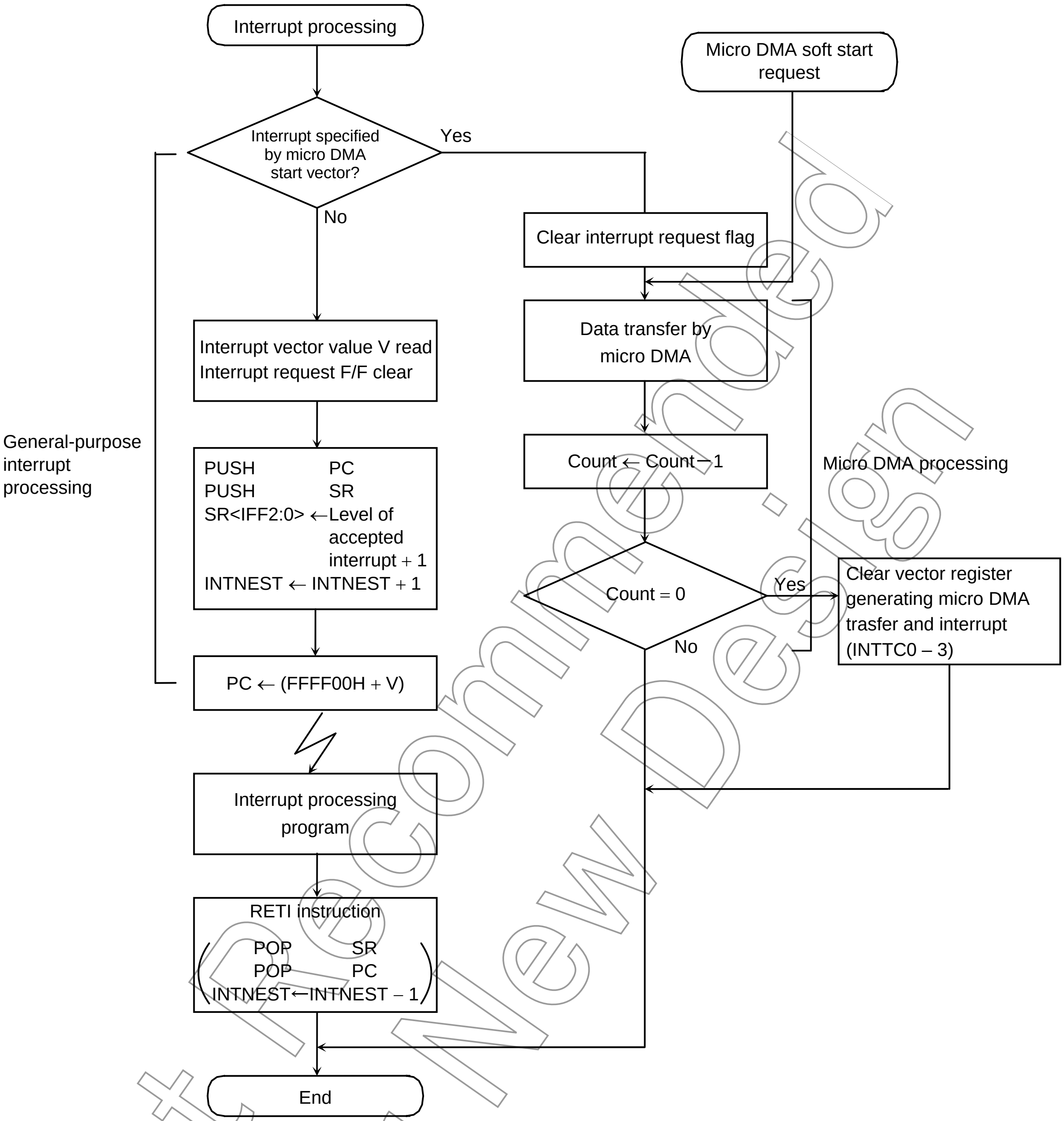


Figure 3.4.1 Overall Interrupt Processing Flow

3.4.1 General-purpose Interrupt Processing

When the CPU accepts an interrupt, it usually performs the following sequence of operations. That is also the same as TLCS-900/L and TLCS-900/H.

(1) The CPU reads the interrupt vector from the interrupt controller.
If the same level interrupts occur simultaneously, the interrupt controller generates an interrupt vector in accordance with the default priority and clears the interrupt request.
(The default priority is already fixed for each interrupt: the smaller vector value has the higher priority level.)

(2) The CPU pushes the value of program counter (PC) and status register (SR) onto the stack area (indicated by XSP).

(3) The CPU sets the value which is the priority level of the accepted interrupt plus 1 (+1) to the interrupt mask register <IFF2:0>. However, if the priority level of the accepted interrupt is 7, the register's value is set to 7.

(4) The CPU increases the interrupt nesting counter INTNEST by 1 (+1).

(5) The CPU jumps to the address indicated by the data at address FFFF00H + interrupt vector and starts the interrupt processing routine.
The above processing time is 18 states (1.00 μs at 36 MHz) as the best case (16-bit data bus width and 0 waits).

When the CPU compled the interrupt processing, use the RETI instruction to return to the main routine. RETI restores the contents of program counter (PC) and status register (SR) from the stack and decreases the Interrupt Nesting counter INTNEST by 1 (–1).

Non-maskable interrupts cannot be disabled by a user program. Maskable interrupts, however, can be enabled or disabled by a user program. A program can set the priority level for each interrupt source. (A priority level setting of 0 or 7 will disable an interrupt request.)

If an interrupt request which has a priority level equal to or greater than the value of the CPU interrupt mask register <IFF2:0> comes out, the CPU accepts its interrupt. Then, the CPU interrupt mask register <IFF2:0> is set to the value of the priority level for the accepted interrupt plus 1 (+1).

Therefore, if an interrupt is generated with a higher level than the current interrupt during its processing, the CPU accepts the later interrupt and goes to the nesting status of interrupt processing.

Moreover, if the CPU receives another interrupt request while performing the said (1) to (5) processing steps of the current interrupt, the latest interrupt request is sampled immediately after execution of the first instruction of the current interrupt processing routine. Specifying DI as the start instruction disables maskable interrupt nesting.

A reset initializes the interrupt mask register <IFF2:0> to 111, disabling all maskable interrupts.

Table 3.4.1 shows the TMP91C025 interrupt vectors and micro DMA start vectors. The address FFFF00H to FFFFFFH (256 bytes) is assigned for the interrupt vector area.

Table 3.4.1 TMP91C025 Interrupt Vectors Table

Default Priority	Type	Interrupt Source and Source of Micro DMA Request	Vector Value (V)	Vector Reference Address	Micro DMA Start Vector
1	Non-Maskable	Reset or “SWI 0” instruction	0000H	FFFF00H	–
2		“SWI 1” instruction	0004H	FFFF04H	–
3		INTUNDEF: illegal instruction or “SWI 2” instruction	0008H	FFFF08H	–
4		“SWI 3” instruction	000CH	FFFF0CH	–
5		“SWI 4” instruction	0010H	FFFF10H	–
6		“SWI 5” instruction	0014H	FFFF14H	–
7		“SWI 6” instruction	0018H	FFFF18H	–
8		“SWI 7” instruction	001CH	FFFF1CH	–
9		INTWD: Watchdog timer	0024H	FFFF24H	–
–	Maskable	Micro DMA (MDMA)	–	–	–
10		INT0 pin	0028H	FFFF28H	0AH
11		INT1 pin	002CH	FFFF2CH	0BH
12		INT2 pin	0030H	FFFF30H	0CH
13		INT3 pin	0034H	FFFF34H	0DH
14		INTALM0: ALM0 (8192 Hz)	0038H	FFFF38H	0EH
15		INTALM1: ALM1 (512 Hz)	003CH	FFFF3CH	0FH
16		INTALM2: ALM2 (64 Hz)	0040H	FFFF40H	10H
17		INTALM3: ALM3 (2 Hz)	0044H	FFFF44H	11H
18		INTALM4: ALM4 (1 Hz)	0048H	FFFF48H	12H
19		INTTA0: 8-bit timer0	004CH	FFFF4CH	13H
20		INTTA1: 8-bit timer1	0050H	FFFF50H	14H
21		INTTA2: 8-bit timer2	0054H	FFFF54H	15H
22		INTTA3: 8-bit timer3	0058H	FFFF58H	16H
23		INTRX0: Serial reception (Channel 0)	005CH	FFFF5CH	17H
24		INTTX0: Serial transmission (Channel 0)	0060H	FFFF60H	18H
25		INTRX1: Serial reception (Channel 1)	0064H	FFFF64H	19H
26		INTTX1: Serial transmission (Channel 1)	0068H	FFFF68H	1AH
27		INTAD: AD conversion end	006CH	FFFF6CH	1BH
28		INTKEY: Key wake up	0070H	FFFF70H	1CH
29		INTRTC: RTC (Alarm interrupt)	0074H	FFFF74H	1DH
30		INTLCD: LCDC/LP pin	007CH	FFFF7CH	1FH
31		INTP0: Protect 0 (WR to special SFR)	0080H	FFFF80H	20H
32		INTP1: Protect 1 (WR to ROM)	0084H	FFFF84H	21H
33		INTTC0: Micro DMA end (Channel 0)	0088H	FFFF88H	–
34		INTTC1: Micro DMA end (Channel 1)	008CH	FFFF8CH	–
35		INTTC2: Micro DMA end (Channel 2)	0090H	FFFF90H	–
36		INTTC3: Micro DMA end (Channel 3)	0094H	FFFF94H	–
		(Reserved) to (Reserved)	0098H to 00FCH	FFFF98H to FFFFFCH	– to –

3.4.2 Micro DMA Processing

In addition to general-purpose interrupt processing, the TMP91C025 supprots a micro DMA function. Interrupt requests set by micro DMA perform micro DMA processing at the highest priority level (level 6) among maskable interrupts, regardless of the priority level of the particular interrupt source. The micro DMA has 4 channels and is possible continuous transmission by specifing the say later burst mode.

Because the micro DMA function has been implemented with the cooperative operation of CPU, when CPU goes to a standby mode by HALT instruction, the requirement of micro DMA will be ignored (Pending).

(1) Micro DMA operation

When an interrupt request specified by the micro DMA start vector register is generated, the micro DMA triggers a micro DMA request to the CPU at interrupt priority level 6 and starts processing the request in spite of any interrupt source's level. The micro DMA is ignored on <IFF2:0> = 7.

The 4 micro DMA channels allow micro DMA processing to be set for up to 4 types of interrupts at any one time. When micro DMA is accepted, the interrupt request flip-flop assigned to that channel is cleared.

The data are automatically transferred once (1/2/4 bytes) from the transfer source address to the transfer destination address set in the control register, and the transfer counter is decreased by 1 (−1).

If the decreased result is 0, the micro DMA transfer end interrupt (INTTC0 to INTTC3) passes from the CPU to the interrupt controller. In addition, the micro DMA start vector register DMAnV is cleared to 0, the next micro DMA is disabled and micro DMA processing completes. If the decreased result is other than 0, the micro DMA processing completes if it isn't specified the say later burst mode. In this case, the micro DMA transfer end interrupt (INTTC0 to INTTC3) aren't generated.

If an interrupt request is triggered for the interrupt source in use during the interval between the clearing of the micro DMA start vector and the next setting, general-purpose interrupt processing executes at the interrupt level set. Therefore, if only using the interrupt for starting the micro DMA (not using the interrupts as a general-purpose interrupt: level 1 to 6), first set the interrupts level to 0 (Interrupt requests disabled).

If using micro DMA and general-purpose interrupts together, first set the level of the interrupt used to start micro DMA processing lower than all the other interrupt levels. (Note) In this case, the cause of general interrupt is limited to the edge interrupt.

The priority of the micro DMA transfer end interrupt (INTTC0 to INTTC3) is defined by the interrupt level and the default priority as the same as the other maskable interrupt.

Note: If the priority level of micro DMA is set higher than that of other interrupts, CPU operates as follows.
In case INTxxx interrupt is generated first and then INTyyy interrupt is generated between checking "Interrupt specified by micro DMA start vector" (in the Figure 3.4.1) and reading interrupt vector with setting below. The vector shifts to that of INTyyy at the time.
This is because the priority level of INTyyy is higher than that of INTxxx.
In the interrupt routine, CPU reads the vector of INTyyy because cheking of micro DMA has finished.
And INTyyy is generated regardless of transfer counter of micro DMA.
INTxxx: level 1 without micro DMA
INTyyy: level 6 with micro DMA

If a micro DMA request is set for more than one channel at the same time, the priority is not based on the interrupt priority level but on the channel number. The smaller channel number has the higher priority (Channel 0 (High) > channel 3 (Low)).

While the register for setting the transfer source/transfer destination addresses is a 32-bit control register, this register can only effectively output 24-bit addresses. Accordingly, micro DMA can access 16 Mbytes (the upper eight bits of the 32 bits are not valid).

Three micro DMA transfer modes are supported: 1-byte transfer, 2-byte (one word) transfer, and 4-byte transfer. After a transfer in any mode, the transfer source/destination addresses are increased, decreased, or remain unchanged.

This simplifies the transfer of data from I/O to memory, from memory to I/O , and from I/O to I/O. For details of the transfer modes, see 3.4.2 (4) Transfer mode register. As the transfer counter is a 16-bit counter, micro DMA processing can be set for up to 65536 times per interrupt source. (The micro DMA processing count is maximized when the transfer counter initial value is set to 0000H.)

Micro DMA processing can be started by the 24 interrupts shown in the micro DMA start vectors of Table 3.4.1 and by the micro DMA soft start, making a total of 25 interrupts.

Figure 3.4.2 shows the word transfer micro DMA cycle in transfer destination address INC mode (except for counter mode, the same as for other modes).

(The conditions for this cycle are based on an external 16-bit bus, 0 waits, trandfer source/transfer destination addresses both even-numberd values).

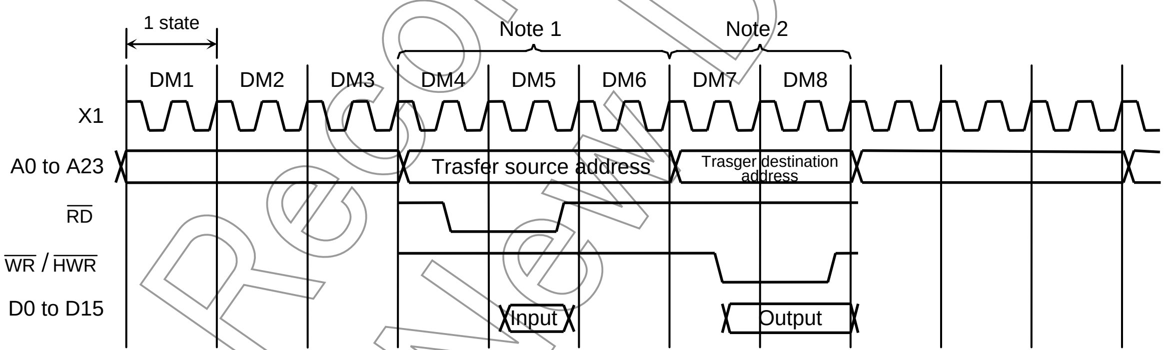


Figure 3.4.2 Timing for Micro DMA Cycle

States 1 to 3: Instruction fetch cycle (Gets next address code).
If 3 bytes and more instruction codes are inserted in the instruction queue buffer, this cycle becomes a dummy cycle.

States 4 to 5: Micro DMA read cycle

State 6: Dummy cycle (the address bus remains unchanged from state 5)

States 7 to 8: Micro DMA write cycle

Note 1: If the source address area is an 8-bit bus, it is increased by two states.
If the source address area is a 16-bit bus and the address starts from an odd number, it is increased by two states.

Note 2: If the destination address area is an 8-bit bus, it is increased by two states.
If the destination address area is a 16-bit bus and the address starts from an odd number, it is increased by two states.

(2) Soft start function

In addition to starting the micro DMA function by interrupts, TMP91C025 includes a micro DMA software start function that starts micro DMA on the generation of the write cycle to the DMAR register.

Writing 1 to each bit of DMAR register causes micro DMA once (If write 0 to each bits, micro DMA doesn't operate). At the end of transfer, the corresponding bit of the DMAR register is automatically cleared to 0.

Only one-channel can be set for micro DMA at once. (Do not write 1 to plural bits.)

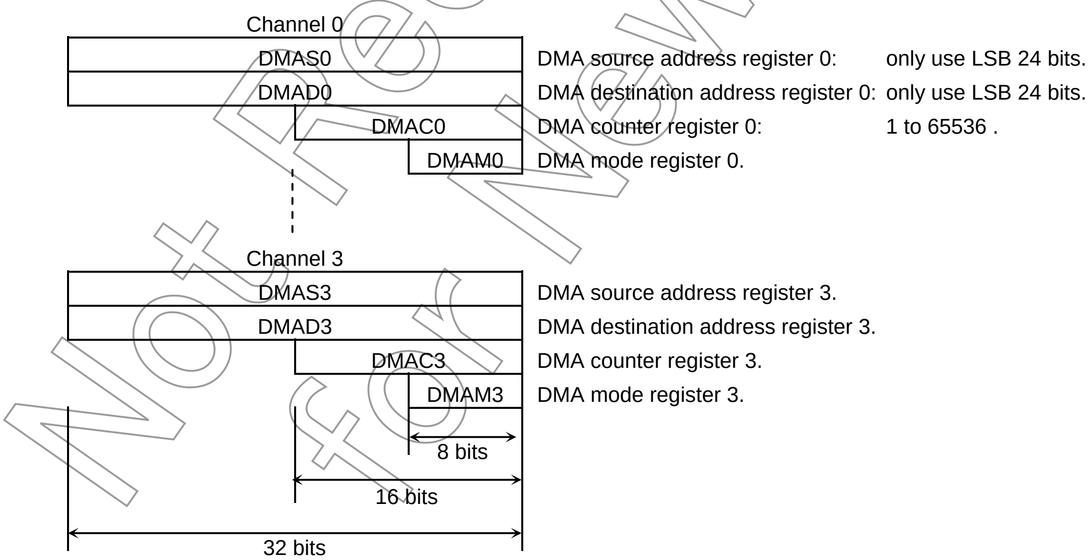
When writing again 1 to the DMAR register, check whether the bit is 0 before writing 1. If read 1, micro DMA transfer isn't started yet.

When a burst is specified by DMAB register, data is continuously transferred until the value in the micro DMA transfer counter is 0 after start up of the micro DMA. If the value in the micro DMA transfer counter is 0 after start up of the micro DMA transfer counter doesn't change. Don't use Read-modify-write instruction to avoid writing to other bits by mistake.

Symbol	Name	Address	7	6	5	4	3	2	1	0
DMAR	DMA request register	89H (Prohibit RMW)					DMAR3	DMAR2	DMAR1	DMAR0
							R/W			
							0	0	0	0
							DMA request			

(3) Transfer control registers

The transfer source address and the transfer destination address are set in the following registers in CPU. Data setting for these registers is done by an LDC cr,r instruction.



(4) Detailed description of the transfer mode register

DMAM0 to DMAM3 (8 bits)

0	0	0	Mode				

Note: When setting a value in this register, write 0 to the upper 3 bits.

			Number of Transfer Bytes	Mode Description	Number of Execution States	Minimum Execution Time at fc = 36 MHz
000 (fixed)	000	 00 01 10	 Byte transfer Word transfer 4-bit transfer	Transfer destination address INC mode .... I/O to memory (DMADn+) ← (DMASn) DMACn ← DMACn − 1 If DMACn = 0, then INTTCn is generated.	8 states 12 states	444 ns 667 ns
	001	 00 01 10	 Byte transfer Word transfer 4-bit transfer	Transfer destination address DEC mode .... I/O to memory (DMADn−) ← (DMASn) DMACn ← DMACn − 1 If DMACn = 0, then INTTCn is generated.	8 states 12 states	444 ns 667 ns
	010	 00 01 10	 Byte transfer Word transfer 4-bit transfer	Transfer source address INC mode .... Memory to I/O (DMADn) ← (DMASn+) DMACn ← DMACn − 1 If DMACn = 0, then INTTCn is generated.	8 states 12 states	444 ns 667 ns
	011	 00 01 10	 Byte transfer Word transfer 4-bit transfer	Transfer source address DEC mode .... Memory to I/O (DMADn) ← (DMASn−) DMACn ← DMACn − 1 If DMACn = 0, then INTTCn is generated.	8 states 12 states	444 ns 667 ns
	100	 00 01 10	 Byte transfer Word transfer 4-bit transfer	Fixed address mode .... I/O to I/O (DMADn) ← (DMASn−) DMACn ← DMACn − 1 If DMACn = 0, then INTTCn is generated.	8 states 12 states	444 ns 667 ns
	101	00	Counter mode .... For counting number of times interrupt is generated DMASn ← DMASn + 1 DMACn ← DMACn − 1 If DMACn = 0, then INTTCn is generated.		5 states	278 ns

Note 1: n is the corresponding micro DMA channels 0 to 3
DMADn+/DMASn+: Post-increment (increment register value after transfer)
DMADn−/DMASn−: Post-decrement (decrement register value after transfer)
The I/Os in the table mean fixed address and the memory means increment (INC) or decrement (DEC) addresses.

Note 2: Execution time is under the condition of:
16-bit bus width (both translation and destination address area) /0 waits/
fc = 36 MHz/selected high frequency mode (fc × 1)

Note 3: Do not use an undefined code for the transfer mode register except for the defined codes listed in the above table.

3.4.3 Interrupt Controller Operation

The block diagram in Figure 3.4.3 shows the interrupt circuits. The left-hand side of the diagram shows the interrupt controller circuit. The right-hand side shows the CPU interrupt request signal circuit and the halt release circuit.

For each of the 36 interrupt channels there is an interrupt request flag (consisting of a flip-flop), an interrupt priority setting register and a micro DMA start vector register. The interrupt request flag latches interrupt requests from the peripherals. The flag is cleared to 0 in the following cases:

- When reset occurs
- When the CPU reads the channel vector after accepted its interrupt
- When executing an instruction that clears the interrupt
  (Write DMA start vector to INTCLR register)
- When the CPU receives a micro DMA request (When micro DMA is set)
- When the micro DMA burst transfer is terminated

An interrupt priority can be set independently for each interrupt source by writing the priority to the interrupt priority setting register (e.g. INTE0AD or INTE12). 6 interrupt priorities levels (1 to 6) are provided. Setting an interrupt source's priority level to 0 (or 7) disables interrupt requests from that source. The priority of non-maskable interrupts (Watchdog timer interrupts) is fixed at 7. If interrupt request with the same level are generated at the same time, the default priority (The interrupt with the lowest priority or, in other words, the interrupt with the lowest vector value) is used to determine which interrupt request is accepted first.

The 3rd and 7th bits of the interrupt priority setting register indicate the state of the interrupt request flag and thus whether an interrupt request for a given channel has occurred.

The interrupt controller sends the interrupt request with the highest priority among the simulateous interrupts and its vector address to the CPU. The CPU compares the priority value <IFF2:0> in the status register by the interrupt request signal with the priority value set; if the latter is higher, the interrupt is accepted. Then the CPU sets a value higher than the priority value by 1 (+1) in the CPU SR<IFF2:0>. Interrupt request where the priority value equals or is higher than the set value are accepted simultaneously during the previous interrupt routine.

When interrupt processing is completed (after execution of the RETI instruction), the CPU restores the priority value saved in the stack before the interrupt was generated to the CPU SR<IFF2:0>.

The interrupt controller also has registers (4 channels) used to store the micro DMA start vector. Writing the start vector of the interrupt source for the micro DMA processing (see Table 3.4.1), enables the corresponding interrupt to be processed by micro DMA processing. The values must be set in the micro DMA parameter register (e.g. DMAS and DMAD) prior to the micro DMA processing.

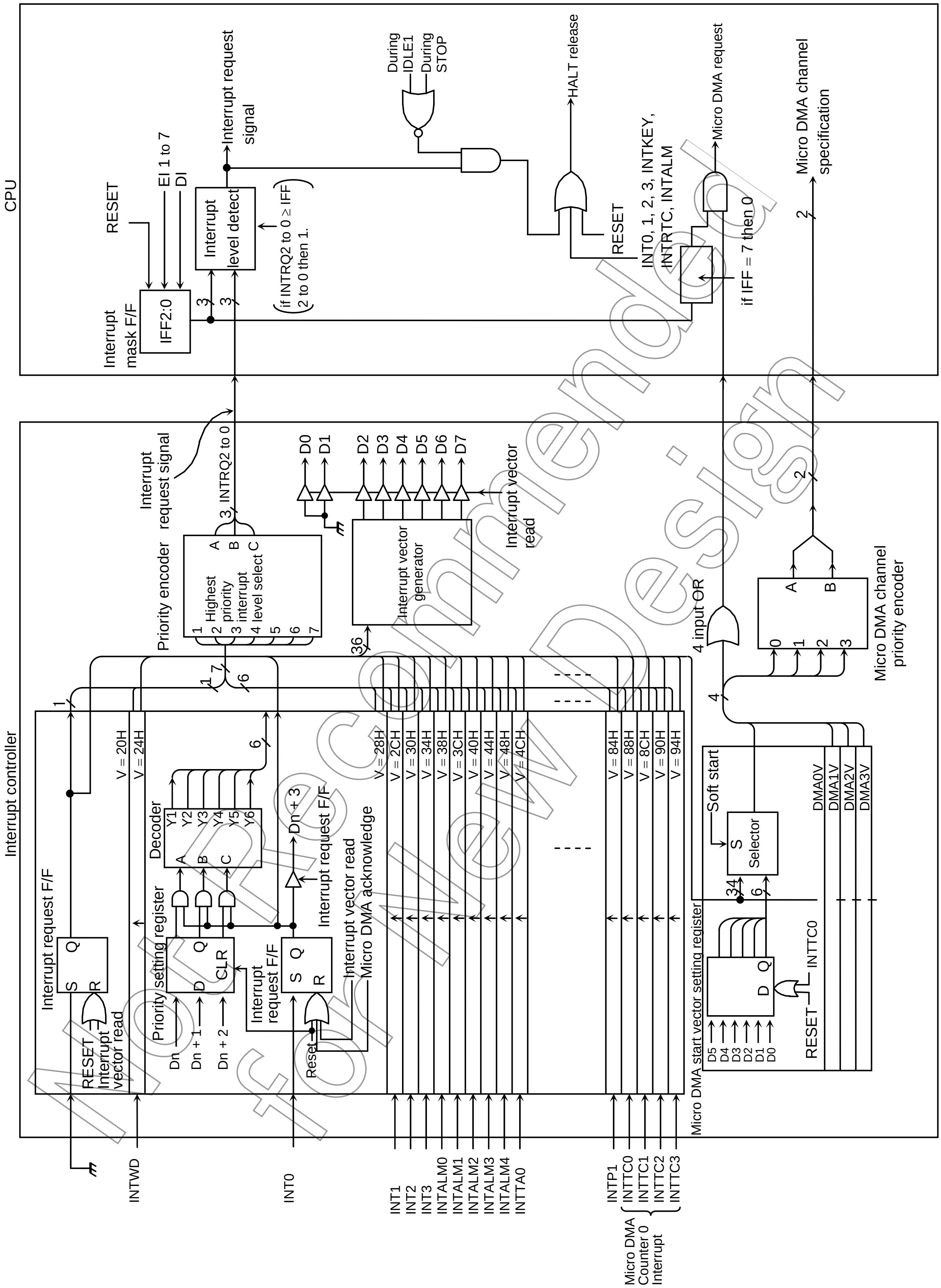


Figure 3.4.3 Block Diagram of Interrupt Controller

(1) Interrupt level setting registers

Symbol	Name	Address	7	6	5	4	3	2	1	0
INTE0AD	INT0 and INTAD enable	90H	INTAD				INT0			
			IADC	IADM2	IADM1	IADM0	I0C	I0M2	I0M1	I0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTE12	INT1 and INT2 enable	91H	INT2				INT1			
			I2C	I2M2	I2M1	I2M0	I1C	I1M2	I1M1	I1M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTE3ALM4	INT3 and INTALM4 enable	92H	INTALM4				INT3			
			IA4C	IA4M2	IA4M1	IA4M0	I3C	I3M2	I3M1	I3M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTEALM01	INTALM0 and INTALM1 enable	93H	INTALM1				INTALM0			
			IA1C	IA1M2	IA1M1	IA1M0	IA0C	IA0M2	IA0M1	IA0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTEALM23	INTALM2 and INTALM3 enable	94H	INTALM3				INTALM2			
			IA3C	IA3M2	IA3M1	IA3M0	IA2C	IA2M2	IA2M1	IA2M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTETA01	INTTA0 and INTTA1 enable	95H	INTTA1 (TMRA1)				INTTA0 (TMRA0)			
			ITA1C	ITA1M2	ITA1M1	ITA1M0	ITA0C	ITA0M2	ITA0M1	ITA0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTETA23	INTTA2 and INTTA3 enable	96H	INTTA3 (TMRA3)				INTTA2 (TMRA2)			
			ITA3C	ITA3M2	ITA3M1	ITA3M0	ITA2C	ITA2M2	ITA2M1	ITA2M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTERTCKEY	INTRTC and INTKEY enable	97H	INTKEY				INTRTC			
			IKC	IKM2	IKM1	IKM0	IRC	IRM2	IRM1	IRM0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0

Interrupt request flag

IxxM2	IxxM1	IxxM0	Function (Write)
0	0	0	Disables interrupt requests
0	0	1	Sets interrupt priority level to 1
0	1	0	Sets interrupt priority level to 2
0	1	1	Sets interrupt priority level to 3
1	0	0	Sets interrupt priority level to 4
1	0	1	Sets interrupt priority level to 5
1	1	0	Sets interrupt priority level to 6
1	1	1	Disables interrupt requests

Symbol	Name	Address	7	6	5	4	3	2	1	0
INTES0	Interrupt enable serial 0	98H	INTTX0				INTRX0			
			ITX0C	ITX0M2	ITX0M1	ITX0M0	IRX0C	IRX0M2	IRX0M1	IRX0M0
			R	R/W		R	R/W			
			0	0	0	0	0	0	0	0
INTES1	INTRX1 & INTTX1 enable	99H	INTTX1				INTRX1			
			ITXT1C	ITX1M2	ITX1M1	ITX1M0	IRX1C	IRX1M2	IRX1M1	IRX1M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTELCD	INTLCD enable	9AH	INTLCD				–			
			ILCD1C	ILCDM2	ILCDM1	ILCDM0	–	–	–	–
			R	R/W			–	–		
			0	0	0	0	–	–	–	–
INTETC01	INTTC0 & INTTC1 enable	9BH	INTTC1				INTTC0			
			ITC1C	ITC1M2	ITC1M1	ITC1M0	ITC0C	ITC0M2	ITC0M1	ITC0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTETC23	INTTC2 & INTTC3 enable	9CH	INTTC3				INTTC2			
			ITC3C	ITC3M2	ITC3M1	ITC3M0	ITC2C	ITC2M2	ITC2M1	ITC2M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTEP01	INTP0 & INTP1 enable	9DH	INTP1				INTP0			
			IP1C	IP1M2	IP1M1	IP1M0	IP0C	IP0M2	IP0M1	IP0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0

Interrupt request flag

IxxM2	IxxM1	IxxM0	Function (Write)
0	0	0	Disables interrupt requests
0	0	1	Sets interrupt priority level to 1
0	1	0	Sets interrupt priority level to 2
0	1	1	Sets interrupt priority level to 3
1	0	0	Sets interrupt priority level to 4
1	0	1	Sets interrupt priority level to 5
1	1	0	Sets interrupt priority level to 6
1	1	1	Disables interrupt requests

(2) External interrupt control

Symbol	Name	Address	7	6	5	4	3	2	1	0
IIMC	Interrupt input mode control	8CH (Prohibit RMW)	–	–	I3EDGE	I2EDGE	I1EDGE	I0EDGE	I0LE	–
			W							
			0	0	0	0	0	0	0	0
			Always write 0.	Always write 0.	INT3EDGE 0: Rising 1: Falling	INT2EDGE 0: Rising 1: Falling	INT1EDGE 0: Rising 1: Falling	INT0EDGE 0: Rising 1: Falling	INT0 mode 0: Edge 1: Level	Always write 0.

INT0 level enable

0	edge detect INT
1	High level INT

(3) Interrupt request flag clear register

The interrupt request flag is cleared by writing the appropriate micro DMA start vector, to the register INTCLR.

For example, to clear the interrupt flag INT0, perform the following register operation after execution of the DI instruction.

INTCLR ← 0AH: Clears interrupt request flag INT0.

Symbol	Name	Address	7	6	5	4	3	2	1	0
INTCLR	Interrupt clear control	88H (Prohibit RMW)			CLRV5	CLRV4	CLRV3	CLRV2	CLRV1	CLRV0
					W					
					0	0	0	0	0	0
					Interrupt Vector					

(4) Micro DMA start vector registers

This register assigns micro DMA processing to which interrupt source. The interrupt source with a micro DMA start vector that matches the vector set in this register is assigned as the micro DMA start source.

When the micro DMA transfer counter value reaches zero, the micro DMA transfer end interrupt corresponding to the channel is sent to the interrupt controller, the micro DMA start vector register is cleared, and the micro DMA start source for the channel is cleared. Therefore, to continue micro DMA processing, set the micro DMA start vector register again during the processing of the micro DMA transfer end interrupt.

If the same vector is set in the micro DMA start vector registers of more than one channel, the channel with the lowest number has a higher priority.

Accordingly, if the same vector is set in the micro DMA start vector registers of two channels, the interrupt generated in the channel with the lower number is executed until micro DMA transfer is complete. If the micro DMA start vector for this channel is not set again, the next micro DMA is started for the channel with the higher number. (Micro DMA chaining.)

Symbol	Name	Address	7	6	5	4	3	2	1	0
DMA0V	DMA0 start vector	80H			DMA0V5	DMA0V4	DMA0V3	DMA0V2	DMA0V1	DMA0V0
					R/W					
					0	0	0	0	0	0
					DMA0 start vector					
DMA1V	DMA1 start vector	81H			DMA1V5	DMA1V4	DMA1V3	DMA1V2	DMA1V1	DMA1V0
					R/W					
					0	0	0	0	0	0
					DMA1 start vector					
DMA2V	DMA2 start vector	82H			DMA2V5	DMA2V4	DMA2V3	DMA2V2	DMA2V1	DMA2V0
					R/W					
					0	0	0	0	0	0
					DMA2 start vector					
DMA3V	DMA3 start vector	83H			DMA3V5	DMA3V4	DMA3V3	DMA3V2	DMA3V1	DMA3V0
					R/W					
					0	0	0	0	0	0
					DMA3 start vector					

(5) Micro DMA burst specification

Specifying the micro DMA burst continues the micro DMA transfer until the transfer counter register reaches zero after micro DMA start. Setting a bit which corresponds to the micro DMA channel of the DMAB registers mentioned below to 1 specifies a burst.

Symbol	Name	Address	7	6	5	4	3	2	1	0
DMAR	DMA software request register	89H (Prohibit RMW)					DMAR3	DMAR2	DMAR1	DMAR0
							R/W	R/W	R/W	R/W
							0	0	0	0
							1: DMA software request			
DMAB	DMA burst register	8AH					DMAB3	DMAB2	DMAB1	DMAB0
							R/W			
							0	0	0	0
							1: DMA burst request			

(6) Attention point

The instruction execution unit and the bus interface unit of this CPU operate independently. Therefore, immediately before an interrupt is generated, if the CPU fetches an instruction that clears the corresponding interrupt request flag, the CPU may execute the instruction that clears the interrupt request flag (Note) between accepting and reading the interrupt vector. In this case, the CPU reads the default vector 0008H and reads the interrupt vector address FFFF08H.

To avoid the avobe plogram, place instructions that clear interrupt request flags after a DI instruction. And in the case of setting an interrupt enable again by EI instruction after the execution of clearing instruction, execute EI instruction after clearing and more than 1-instructions (ex. "NOP" × 1 times)

In the case of changing the value of the interrupt mask register <IFF2:0> by execution of POP SR instruction, disable an interrupt by DI instruction before execution of POP SR instruction.

In addition, take care as the following 2 circuits are exceptional and demand special attention.

INT0 level mode	In level mode INT0 is not an edge-triggered interrupt. Hence, in level mode the interrupt request flip-flop for INT0 does not function. The peripheral interrupt request passes through the S input of the flip-flop and becomes the Q output. If the interrupt input mode is changed from edge mode to level mode, the interrupt request flag is cleared automatically.

	If the CPU enters the interrupt response sequence as a result of INT0 going from 0 to 1, INT0 must then be held at 1 until the interrupt response sequence has been completed. If INT0 is set to level mode so as to release a halt state, INT0 must be held at 1 from the time INT0 changes from 0 to 1 until the halt state is released. (Hence, it is necessary to ensure that input noise is not interpreted as a 0, causing INT0 to revert to 0 before the halt state has been released.)
	When the mode changes from level mode to edge mode, interrupt request flags which were set in level mode will not be cleared. Interrupt request flags must be cleared using the following sequence.
	DI
	LD (IIMC), 00H ; Switches interrupt input mode from level mode to edge mode.
	LD (INTCLR), 0AH; Clears interrupt request flag.
	NOP ; Wait EI instruction
	EI

INTRX	The interrupt request flip-flop can only be cleared by a reset or by reading the serial channel receive buffer. It cannot be cleared by writing INTCLR register.

Note: The following instructions or pin input state changes are equivalent to instructions that clear the interrupt request flag.

INT0: Instructions which switch to level mode after an interrupt request has been generated in edge mode.
The pin input change from high to low after interrupt request has been generated in level mode. (H → L)

INTRX: Instruction which read the receive buffer.

3.5 Port Functions

The TMP91C025 features 38-bit settings which relate to the various I/O ports.

As well as general-purpose I/O port functionality, the port pins also have I/O functions which relate to the built-in CPU and internal I/Os. Table 3.5.1 lists the functions of each port pin. Table 3.5.2, Table 3.5.4 lists I/O registers and their specifications.

Table 3.5.1 Port Functions

(R: PU = with programmable pull-up resistor/U = with pull-up resistor)

Port Name	Pin Name	Number of Pins	Direction	R	Direction Setting Unit	Pin Name for Built-in Function
Port 1	P10 to P17	8	I/O	–	Bit	D8 to D15
Port 2	P20 to P27	8	Output	–	(Fixed)	A16 to A23
Port 5	P56	1	I/O	PU	Bit	$\overline{WAIT}$
Port 6	P60	1	Output	–	(Fixed)	$\overline{CS0}$
	P61	1	Output	–	(Fixed)	$\overline{CS1}$
	P62	1	Output	–	(Fixed)	$\overline{CS2}$, $\overline{CS2A}$
	P63	1	Output	–	(Fixed)	$\overline{CS3}$
	P64	1	Output	–	(Fixed)	EA24, $\overline{CS2B}$, $\overline{SRLB}$
	P65	1	Output	–	(Fixed)	EA25, $\overline{CS2C}$, $\overline{SRUB}$
Port 8	P80	1	Input	–	(Fixed)	AN0
	P81	1	Input	–	(Fixed)	AN1
	P82	1	Input	–	(Fixed)	AN2, MX
	P83	1	Input	–	(Fixed)	AN3, $\overline{ADTRG}$, MY
Port 9	P90 to P97	8	Input	U	(Fixed)	KI0 to KI7
Port A	PA0	1	Output	–	(Fixed)	KO0, $\overline{ALARM}$, $\overline{MLDALM}$
	PA1	1	Output	–	(Fixed)	KO1, TA1OUT
	PA2	1	Output	–	(Fixed)	KO2, TA3OUT
	PA3	1	Output	–	(Fixed)	KO3, SCOUT
Port B	PB3	1	I/O	–	Bit	INT0, $\overline{PS}$
	PB4	1	I/O	–	Bit	INT1, TA0IN
	PB5	1	Input	–	(Fixed)	INT2, PX
	PB6	1	Input	–	(Fixed)	INT3, PY
Port C	PC0	1	I/O	–	Bit	TXD0
	PC1	1	I/O	–	Bit	RXD0
	PC2	1	I/O	PU	Bit	SCLK0, $\overline{CTS0}$
	PC3	1	I/O	–	Bit	TXD1
	PC4	1	I/O	–	Bit	RXD1
	PC5	1	I/O	PU	Bit	SCLK1, $\overline{CTS1}$
Port D	PD0	1	Output	–	(Fixed)	D1BSCP
	PD1	1	Output	–	(Fixed)	D2BLP
	PD2	1	Output	–	(Fixed)	D3BFR
	PD3	1	Output	–	(Fixed)	DLEBCD
	PD4	1	Output	–	(Fixed)	DOFFB
	PD7	1	Output	–	(Fixed)	MLDALM
Port Z	PZ2	1	I/O	PU	Bit	$\overline{HWR}$
	PZ3	1	I/O	PU	Bit	R/ $\overline{W}$, $\overline{SRWR}$

Table 3.5.2 I/O Registers and Specifications (1/2) X: Don't care

Port	Pin Name	Specification	I/O Register			
			Pn	PnCR	PnFC	PnFC2
Port 1 (Note 1)	P10 to P17	Input port	X	0	None	None
		Output port	X	1		
		D8 to D15 bus	X	X		
Port 2	P20 to P27	Output port	X	None	0	
		A16 to A23 output	X		1	
Port 5	P56	$\overline{\text{WAIT}}$ input (Without PU)	0	0	None	
		$\overline{\text{WAIT}}$ input (With PU)	1	0		
Port 6	P60 to P65	Output port	X	None	0	0
	P60	$\overline{\text{CS0}}$ output	X		1	None
	P61	$\overline{\text{CS1}}$ output	X		1	
	P62	$\overline{\text{CS2}}$ output	X		1	0
		$\overline{\text{CS2A}}$ output	X		X	1
	P63	$\overline{\text{CS3}}$ output	X		1	None
	P64	$\overline{\text{SRLB}}$ output	X		0	1
		$\overline{\text{CS2B}}$ output	X		1	1
		EA24 output	X		1	0
	P65	$\overline{\text{SRUB}}$ output	X		0	1
		$\overline{\text{CS2C}}$ output	X		1	1
		EA25 output	X		1	0
Port 8	P80 to P83	Input port	X	None		None
		AN0 to 3 input (Note 2)	X			
	P83	$\overline{\text{ADTRG}}$ input (Note 3)	X			
Port 9	P90 to P97	Input port	X	None	0	
		KI0 to 7 input	X		1	
Port A	PA0 to PA3	Output port	X	None	0	0
		KO0 to 3 output (CMOS)	X		0	0
		KO0 to 3 output (Open drain)	X		1	0
	PA0	$\overline{\text{ALARM}}$ output	1		0	1
		$\overline{\text{MLDALM}}$ output	0		0	1
	PA1	TA1OUT output	X		0	1
	PA2	TA3OUT output	X		0	1
	PA3	SCOUT output	X		0	1
Port B	PB3 to PB4	Input port	X	0	0	None
		Output port	X	1	0	
	PB3	INT0 input	X	0	1	
		$\overline{\text{PS}}$ input	X	0	X	
	PB4	INT1 input	X	0	1	
		TA0IN input	X	0	X	
	PB5	INT2 input	X	0	1	
		PX output	X	0	None	
	PB6	INT3 input	X	0	1	
		PY output	X	0	None	

Table 3.5.3 I/O Registers and Specifications (2/2) X: Don’t care

Port	Pin Name	Specification	I/O Register			
			Pn	PnCR	PnFC	PnFC2
Port C	PC0 to PC5	Input port	X	0	0	None
		Output port	X	1	0	
	PC0	TXD0 output (Note 4)	1	1	1	
	PC1	RXD0 input (Note 4)	1	0	None	
	PC2	SCLK0 input (Note 4)	1	0	0	
		SCLK0 output (Note 4)	1	1	1	
		$\overline{CTS0}$ input (Note 4)	1	0	0	
	PC3	TXD1 output (Note 4)	1	1	1	
	PC4	RXD1 input (Note 4)	1	0	None	
	PC5	SCLK1 input (Note 4)	1	0	0	
		SCLK1 output (Note 4)	1	1	1	
		$\overline{CTS1}$ input (Note 4)	1	0	0	
Port D	PD0 to PD7	Output port	X	None	0	
	PD0	D1BSCP output	X		1	
	PD1	D2BLP output	X		1	
	PD2	D3BFR output	X		1	
	PD3	DLEBCD output	X		1	
	PD4	DOFFB output	X		1	
	PD7	MLDALM output	X		1	
Port Z	PZ2 to PZ3	Input port	X	0	0	
		Output port	X	1	0	
	PZ2	$\overline{HWR}$ output	X	1	1	
	PZ3	R/ $\overline{W}$ output	X	0	1	
		$\overline{SRWR}$ output	X	1	1	

Note 1: Port1 is only use for port or DATA bus (D8 to D15) by setting AM1 and AM0 pins.

Note 2: In case using P80 to P83 for analog input ports of AD converter, set to ADMOD1<ADCH2:0>.

Note 3: In case using P83 for $\overline{ADTRG}$ input port, set to ADMOD1<ADTRGE>.

Note 4: As for input ports of SIO0 and SIO1: (TXD0, RXD0, SCLK0, $\overline{CTS0}$, TXD1, RXD1, SCLK1, $\overline{CTS1}$), logical selection for output data or input data is determined by the output latch register Pn of each port.

3.5.1 Port 1 (P10 to P17)

Port 1 is an 8-bit general-purpose I/O port. Each bit can be set individually for input or output using the control register P1CR. Resetting , the control register P1CR to 0 and sets port 1 to input mode.

In addition to functioning as a general-purpose I/O port, port 1 can also function as an address data bus (D8 to 15).

Table 3.5.4 Function Setting of AM0/AM1

AM1	AM0	Function Setting after Reset
0	0	Input port
0	1	Data bus (D8 to D15)
1	0	Don't use this setting
1	1	Don't use this setting

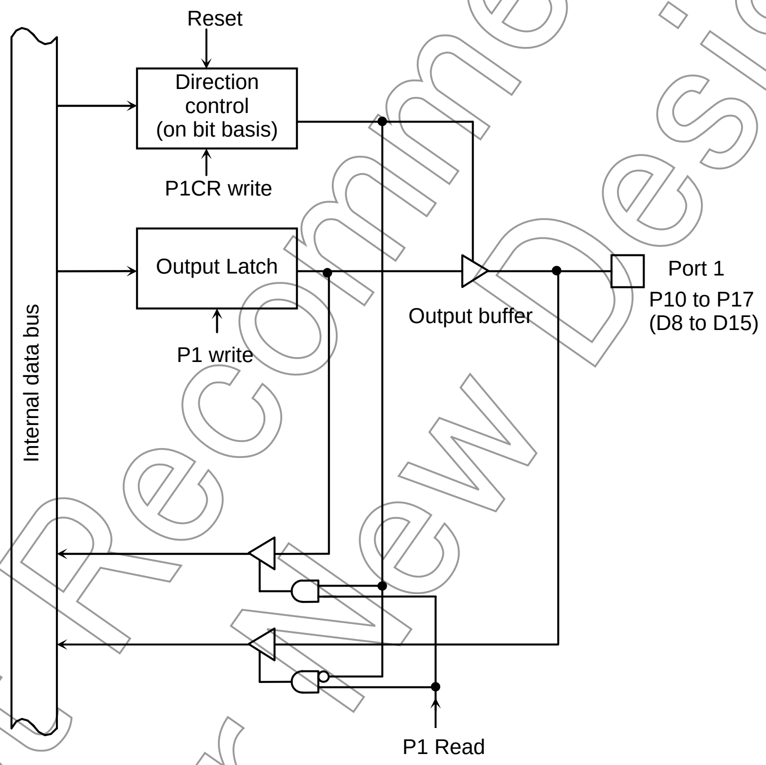


Figure 3.5.1 Port 1

3.5.2 Port 2 (P20 to P27)

Port 2 is an 8-bit output port. In addition to functioning as a output port, port 2 can also function as an address bus (A16 to A23).

Each bit can be set individually for address bus using the function register P2FC. Resetting sets all bits of the function register P2FC to 1 and sets port 2 to address bus.

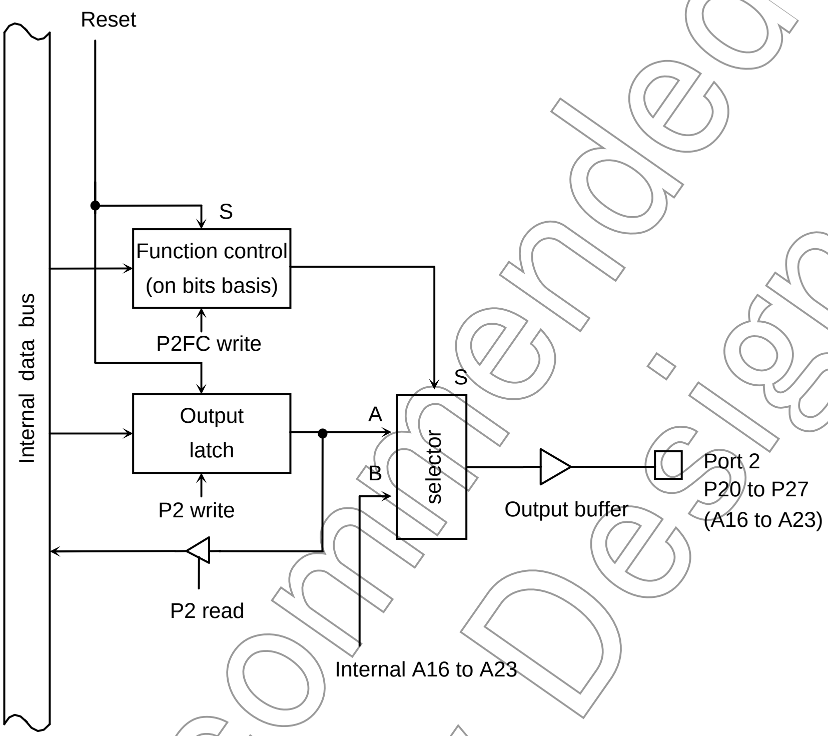


Figure 3.5.2 Port 2

Port 1 Register

		7	6	5	4	3	2	1	0
P1 (0001H)	Bit symbol	P17	P16	P15	P14	P13	P12	P11	P10
	Read/Write	R/W							
	After reset	Data from external port (Output latch register is cleared to 0.)							

Port 1 Control Register

		7	6	5	4	3	2	1	0
P1CR (0004H)	Bit symbol	P17C	P16C	P15C	P14C	P13C	P12C	P11C	P10C
	Read/Write	W							
	After reset (Note2)	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
	Function	0: Input 1: Output							

Port 1 I/O setting
0: Input
1: Output

Port 2 Register

		7	6	5	4	3	2	1	0
P2 (0006H)	Bit symbol	P27	P26	P25	P24	P23	P22	P21	P20
	Read/Write	R/W							
	After reset	1	1	1	1	1	1	1	1

Port 2 Function Register

		7	6	5	4	3	2	1	0
P2FC (0009H)	Bit symbol	P27F	P26F	P25F	P24F	P23F	P22F	P21F	P20F
	Read/Write	W							
	After reset	1	1	1	1	1	1	1	1
	Function	0: Port 1: Address bus (A23 to A16)							

Note1: Read-modify-write is prohibited for P1CR and P2FC.

Note2: It is set to “Port” or “Data bus” by AM pins state.

Figure 3.5.3 Registers for Ports 1 and 2

3.5.3 Port Z (PZ2 to PZ3)

Port Z is an 2-bit general-purpose I/O port. I/O is set using control register PZCR and PZFC.

Resetting sets all bits of the output latch PZ to 1.

In addition to functioning as a general-purpose I/O port, port Z also functions as I/O for the CPU's control/status signal.

Resetting initializes PZ2 and PZ3 pins to input mode with pull-up register.

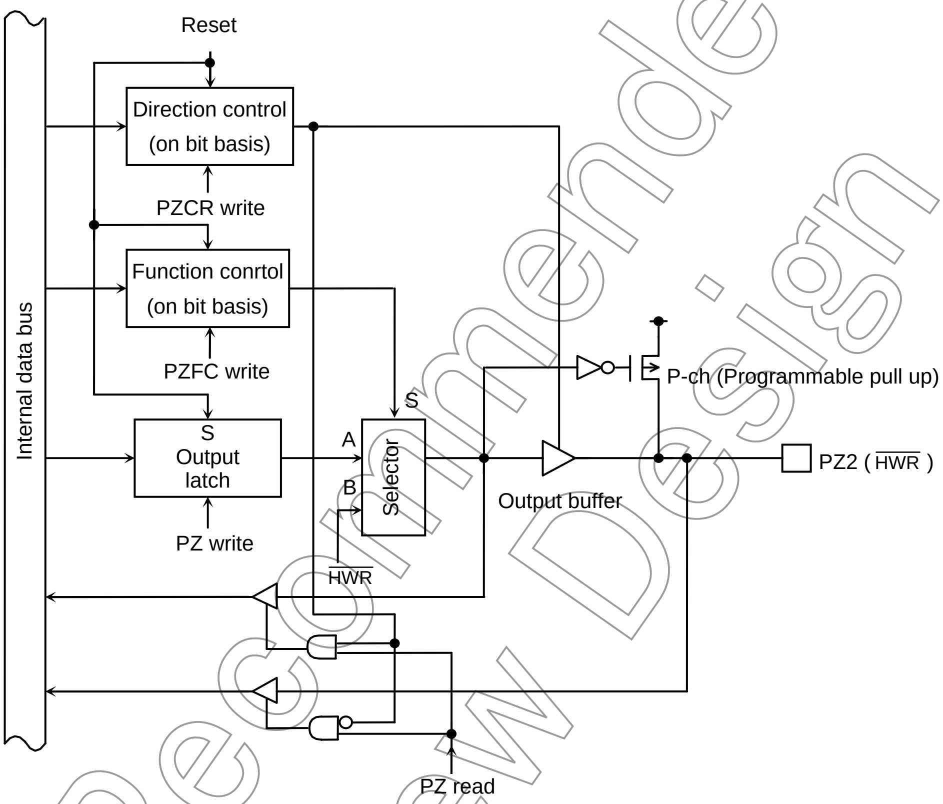


Figure 3.5.4 Port Z2

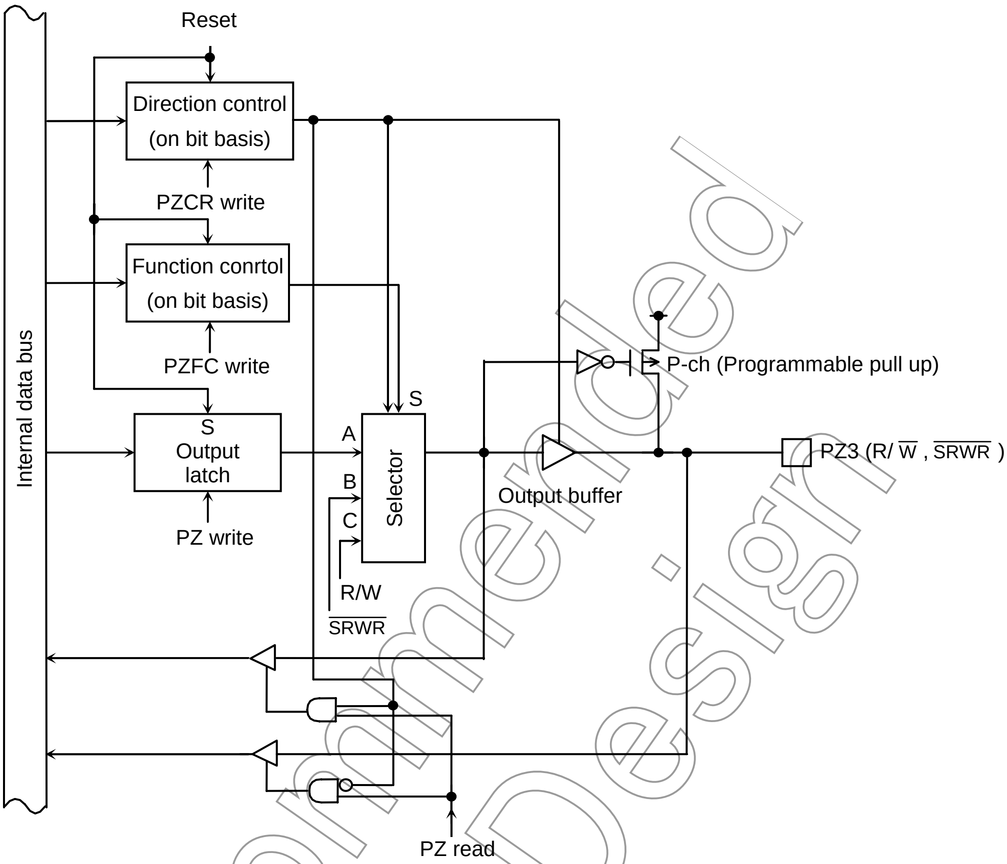


Figure 3.5.5 Port Z3

Port Z register

PZ (007DH)		7	6	5	4	3	2	1	0
	Bit symbol					PZ3	PZ2		
	Read/Write					R/W			
	After reset					Data from external port (Note 1)			
	Function					0(Output latch register) : Pull-up resistor OFF 1(Output latch register) : Pull-up resistor ON			

Port Z control register

PZCR (007EH)		7	6	5	4	3	2	1	0
	Bit symbol					PZ3C	PZ2C		
	Read/Write					W			
	After reset					0	0		
	Function					0: Input 1: Output			

Port Z function register

PZFC (007FH)		7	6	5	4	3	2	1	0
	Bit symbol					PZ3F	PZ2F		
	Read/Write					W			
	After reset					0	0		
	Function					0: Port 1: R/$\overline{W}$, $\overline{SRWR}$	0: Port 1: $\overline{HWR}$		

Note 1: Output latch register is set to 1.

Note 2: Read-modify-write is prohibited for registers PZCR and PZFC.

Note 3: When port Z is used in Input mode, the PZ register controls the built-in pull-up resistor. Read-modify-write is prohibited in input mode or I/O mode. Setting the built-in pull-up resistor may be depended on the states of the input pin.

R/W, $\overline{SRWR}$ setting

<PZ3F> \ <PZ3C>	0	1
0	Input	Output
1	R/$\overline{W}$	$\overline{SRWR}$

Figure 3.5.6 Registers for Port Z

3.5.4 Port 5 (P56)

Port 5 is an 1-bit general-purpose I/O port. I/O is set using control register P5CR and P5FC. Resetting sets all bits of the output latch P5 to 1.

In addition to functioning as a general-purpose I/O port, port 5 also functions as I/O for the CPU's control/status signal.

Resetting initializes P56 pins to input mode with pull-up resistor.

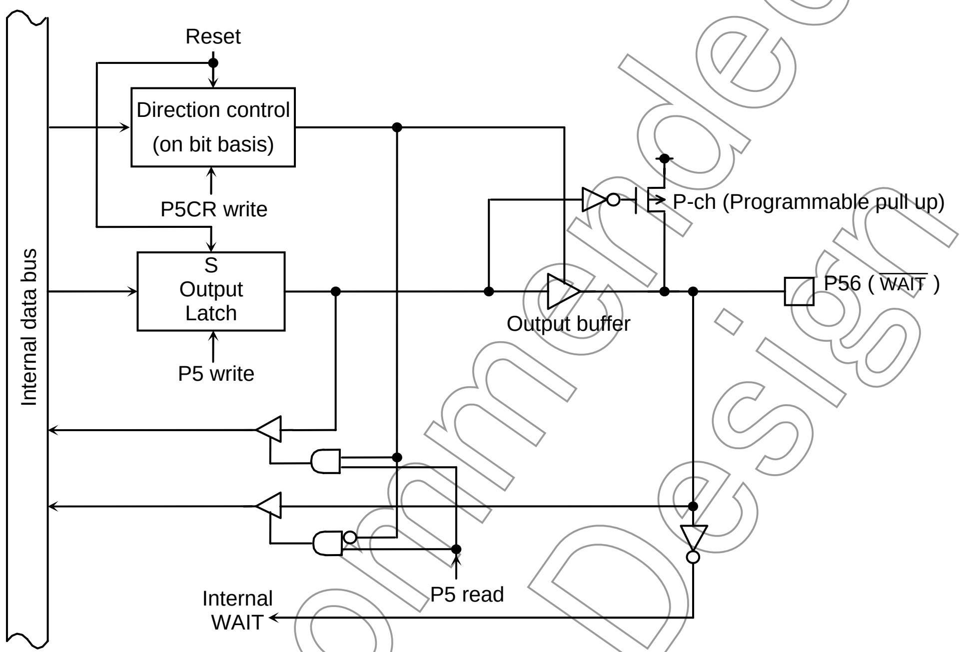


Figure 3.5.7 Port 5 (P56)

Port 5 register

P5 (000DH)		7	6	5	4	3	2	1	0
	Bit symbol		P56						
	Read/Write		R/W						
	After reset		Data from external port (Output latch register is set to 1.)						
	Function		0(Output latch register) : Pull-up resistor OFF 1(Output latch register) : Pull-up resistor ON						

Port 5 control register

P5CR (0010H)		7	6	5	4	3	2	1	0
	Bit symbol		P56C						
	Read/Write		W						
	After reset		0						
	Function		0: Input 1: Output						

Note1: Read-modify-write is prohibited for registers P5CR.

Note2: When the P56/WAIT pin is to be use as the WAIT pin, P5CR<P56C> must be set to 0 and <BnW2:0> in the chip select/wait control register must be set 010.

Figure 3.5.8 Registers for Port 5

3.5.5 Port 6 (P60 to P65)

Port 60 to 65 are 6-bit output ports. Resetting sets output latch of P62 to "0" and output latches of P60 to P61, P63 to P65 to 1.

Port6 also function as chip-select output ($\overline{CS0}$ to $\overline{CS3}$), extend address output (EA24, EA25) and extend chip-select output ($\overline{CS2A}$, $\overline{CS2B}$ and $\overline{CS2C}$).

Writing 1 in the corresponding bit of P6FC, P6FC2 enables the respective functions.

Resetting resets the P6FC, P6FC2 to 0, and sets all bits to output ports.

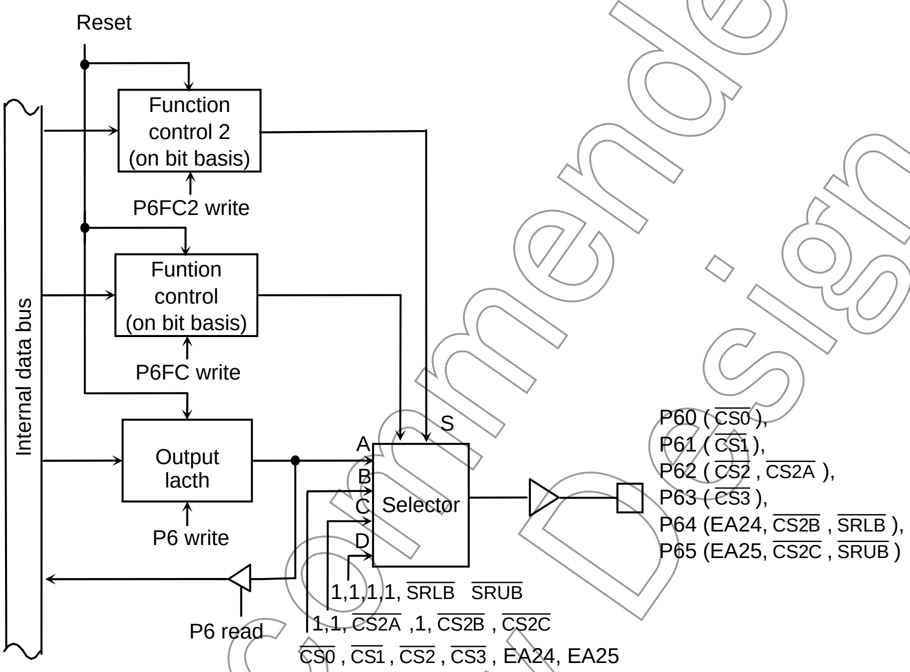


Figure 3.5.9 Port 6

Port 6 Register

P6 (0012H)		7	6	5	4	3	2	1	0
	Bit symbol			P65	P64	P63	P62	P61	P60
	Read/Write			R/W					
	After reset			1	1	1	0	1	1

Port 6 Function Register

P6FC (0015H)		7	6	5	4	3	2	1	0
	Bit symbol			P65F	P64F	P63F	P62F	P61F	P60F
	Read/Write			W					
	After reset			0	0	0	0	0	0
	Function			0: Port 1: EA25	0: Port 1: EA24	0: Port 1: $\overline{CS3}$	0: Port 1: $\overline{CS2}$	0: Port 1: $\overline{CS1}$	0: Port 1: $\overline{CS0}$

Port 6 Function Register 2

P6FC2 (001BH)		7	6	5	4	3	2	1	0
	Bit symbol			P65F2	P64F2	–	P62F2	–	–
	Read/Write			W		W	W	W	W
	After reset			0	0	0	0	0	0
	Function			0: <P65F> 1: $\overline{SRUB}$, $\overline{CS2C}$, EA25	0: <P64F> 1: $\overline{SRLB}$, $\overline{CS2B}$, EA24	Always write 0.	0: <P62F> 1: $\overline{CS2A}$	Always write 0.	

$\overline{SRUB}$, $\overline{CS2C}$, EA25 setting

<P65F2> \ <P65F>	0	1
0	P65	EA25
1	$\overline{SRUB}$	$\overline{CS2C}$

$\overline{SRLB}$, $\overline{CS2B}$, EA24 setting

<P64F2> \ <P64F>	0	1
0	P64	EA24
1	$\overline{SRLB}$	$\overline{CS2B}$

Note: Read-modify-write is prohibited for P6FC and P6FC2.

Figure 3.5.10 Registers for Port 6

3.5.6 Port 8 (P80 to P83)

Port 8 is a 4-bit input port and can also be used as the analog input pins for the internal AD converter.

P83 can also be used as ADTRG pin for the AD converter. P82, P83 can also be used as MX, MY pin for touch screen interface.

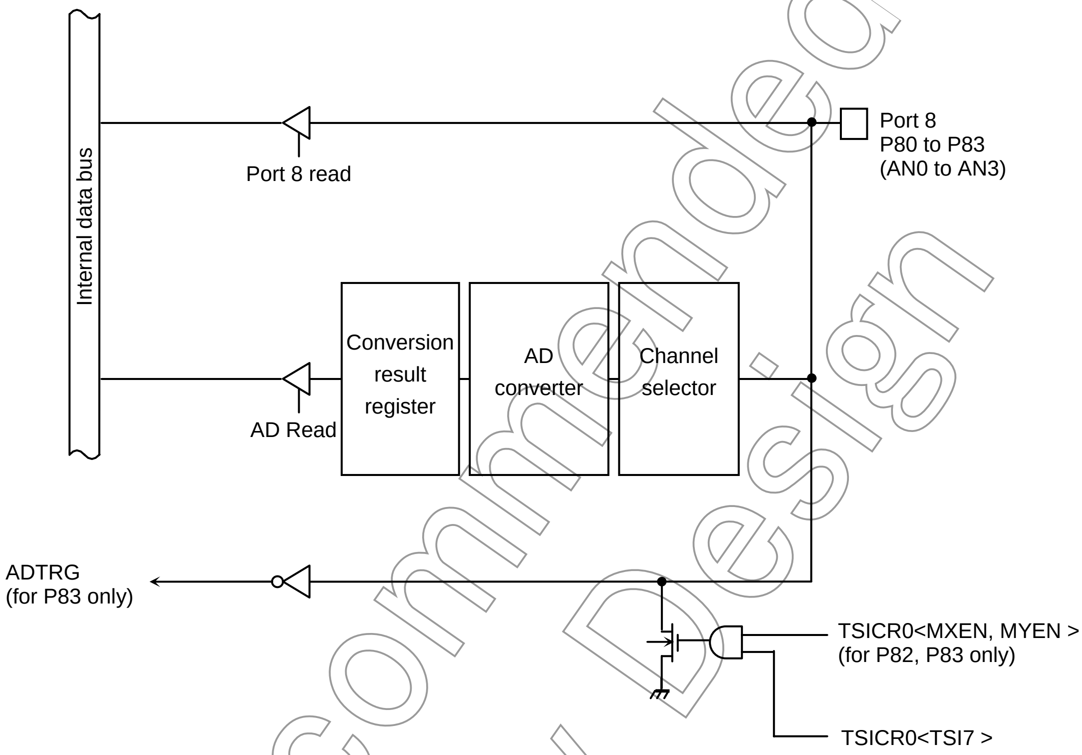


Figure 3.5.11 Port 8

Port 8 Register

		7	6	5	4	3	2	1	0
P8 (0018H)	Bit symbol					P83	P82	P81	P80
	Read/Write					R			
	After reset					Data from external port.			

Note: The input channel selection of AD Converter, the permission of ADTRG input are set by AD Converter mode register ADMOD1.
The input channel selection of AD Converter, the permission of MX, MY input are set by touch screen control register TSICR.

Figure 3.5.12 Registers for Port 8

3.5.7 Port 9 (P90 to P97)

Port 90 to 97 are 8-bit input ports with pull-up resistors. In addition to functioning as general-purpose I/O port, port 90 to 97 can also Key-on wakeup function as Key board interface. The various functions can each be enabled by writing 1 to the corresponding bit of the port 9 function register (P9FC).

Resetting resets all bits of the register P9FC to 0 and sets all pins to be input port.

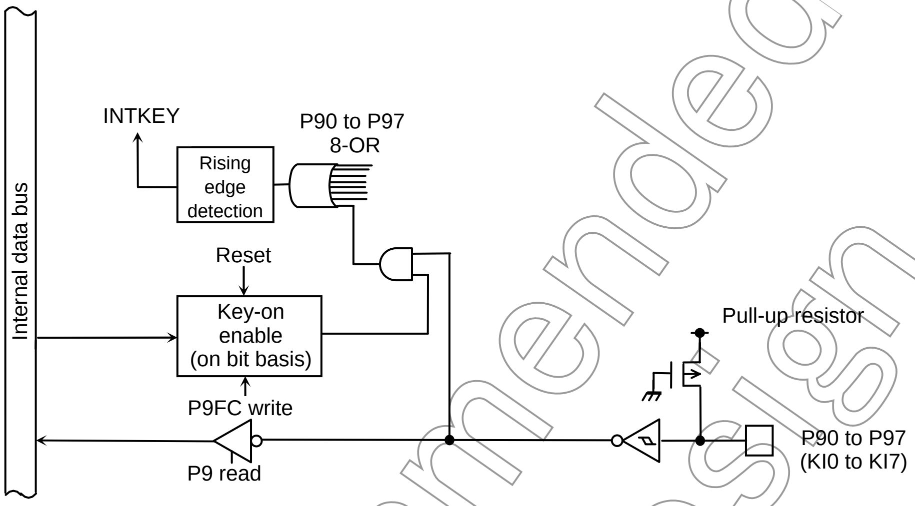


Figure 3.5.13 Port 9

When P9FC = 1, if either of input of KI0 to KI7 pins falls down, INTKEY interrupt is generated. INTKEY interrupt can be used to release all HALT mode.

Port 9 register

P9 (0019H)		7	6	5	4	3	2	1	0
	Bit symbol	P97	P96	P95	P94	P93	P92	P91	P90
	Read/Write	R							
	After reset	Data from external port.							

Port 9 function register

P9FC (001DH)		7	6	5	4	3	2	1	0
	Bit symbol	P97F	P96F	P95F	P94F	P93F	P92F	P91F	P90F
	Read/Write	W							
	After reset	0	0	0	0	0	0	0	0
	Function	0: Key-in disable 1: Key-in enable							

Key-in of Port 9

Disable	0
Enable	1

Note: Read-modify-write is prohibited for the registers P9FC.

Figure 3.5.14 Registers for Port 9

3.5.8 Port A (PA0 to PA3)

Port A0 to PA3 are 4-bit output ports, and also used Key board interface pin KO0 to KO3 which can set open drain output buffer.

Writing 1 to the corresponding bit of the port A function register (PAFC) enable the open drain output.

In addition to functioning as output port, port A also function as output pin for internal clock (SCOUT), output pin for RTC alarm ($\overline{\text{ALARM}}$) and output pin for melody/alarm generator (MLDALM, $\overline{\text{MLDALM}}$). Above setting is used the function register PAFC2

Resetting reset bits of the registers PA to 1 and PAFC, PAFC2 to 0, and all pin outputs 1.

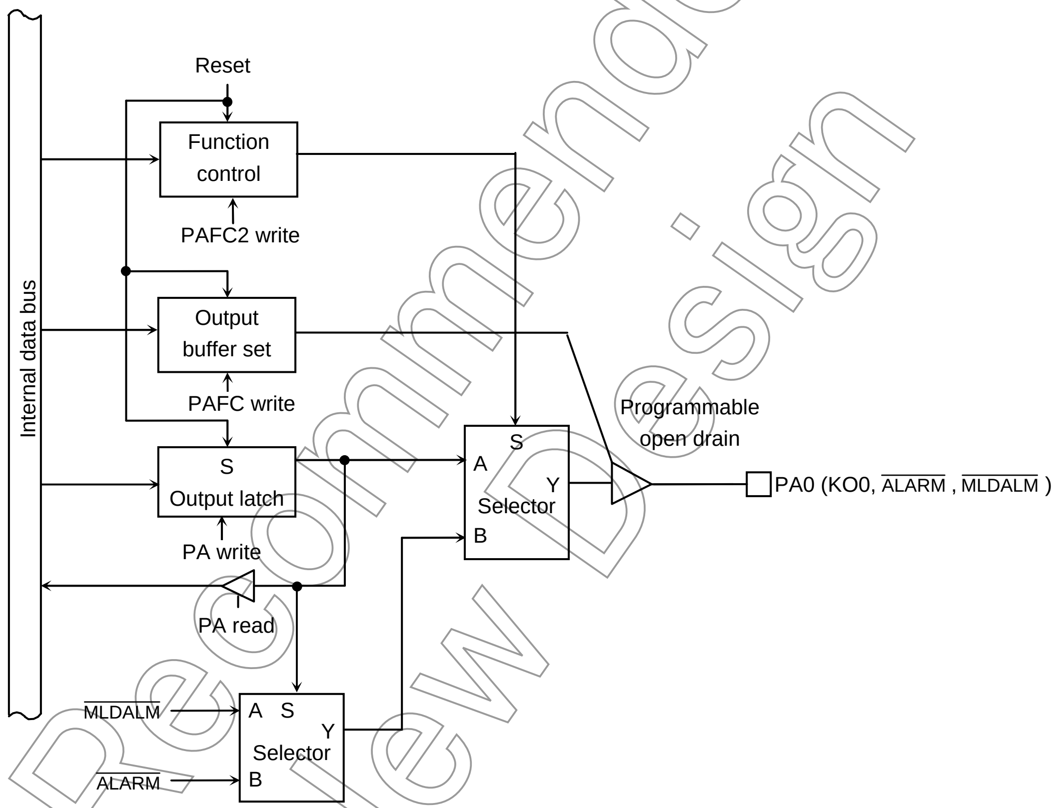


Figure 3.5.15 Port A0

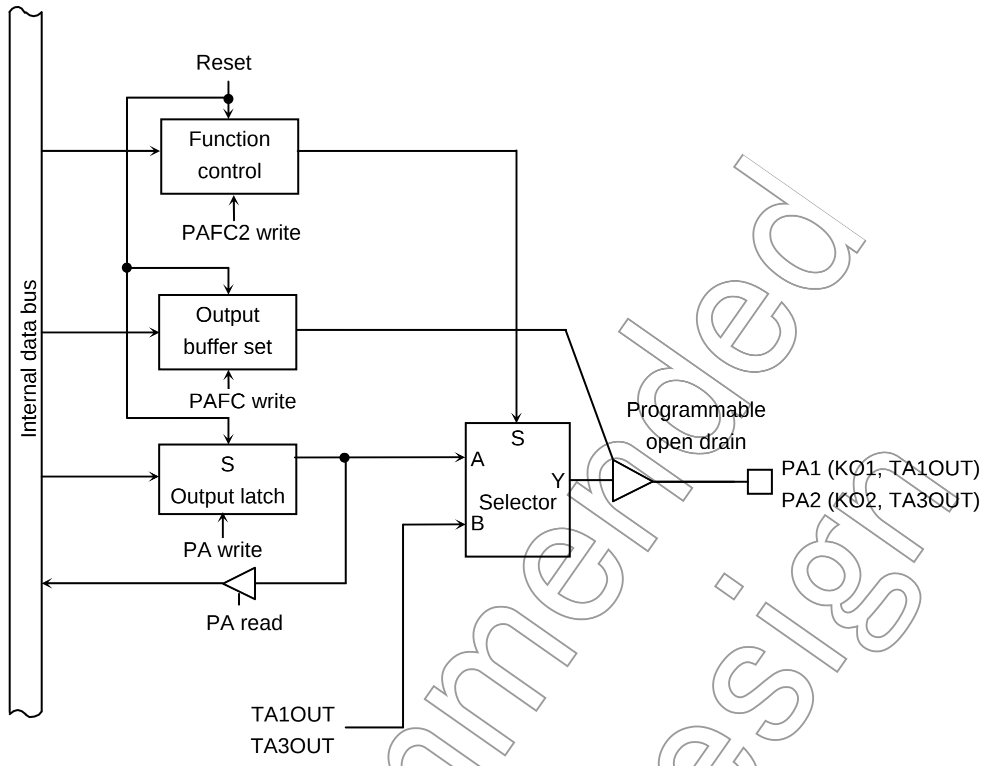


Figure 3.5.16 Port A1, 2

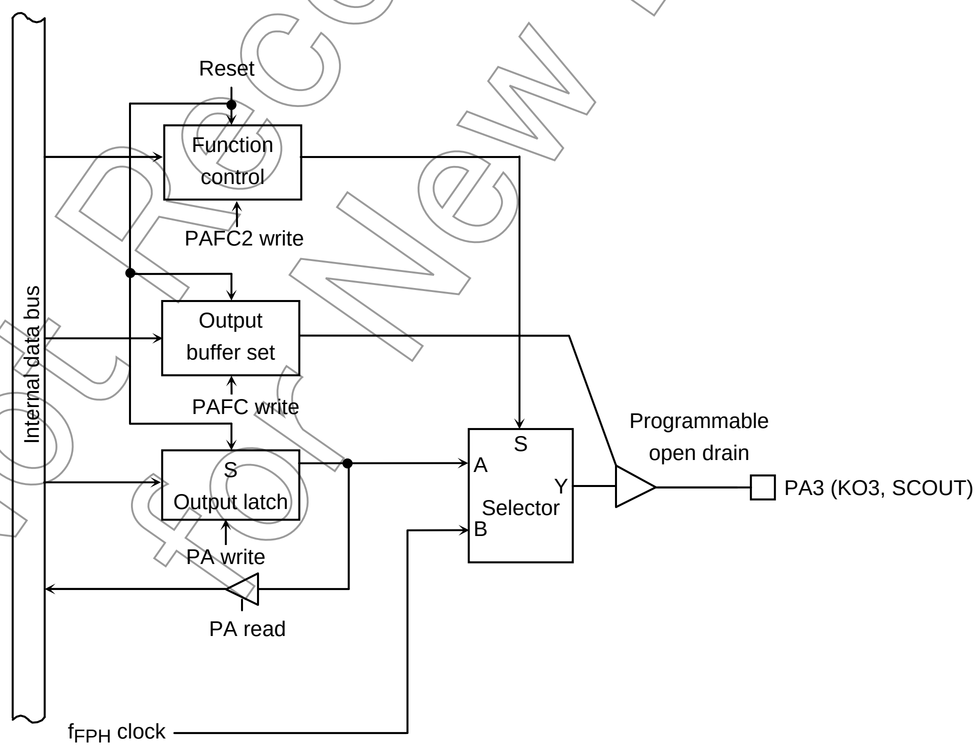


Figure 3.5.17 Port A3

Port A register

PA (001EH)		7	6	5	4	3	2	1	0
	Bit symbol					PA3	PA2	PA1	PA0
	Read/Write					R/W			
	After reset					1	1	1	1

Port A function register

PAFC (0021H)		7	6	5	4	3	2	1	0
	Bit symbol					PA3F	PA2F	PA1F	PA0F
	Read/Write					W			
	After reset					0	0	0	0
	Function					0: CMOS output 1: Open drain			

PAFC2 (0020H)		7	6	5	4	3	2	1	0
	Bit symbol					PA3F2	PA2F2	PA1F2	PA0F2
	Read/Write					W			
	After reset					0	0	0	0
	Function					0: Port 1: SCOUT	0: Port 1: TA3OUT	0: Port 1: TA1OUT	0: Port 1: $\overline{\text{ALARM}}$ at <PA0>=1 1: $\overline{\text{MLDALM}}$ at <PA0>=0

Note: Read-modify-write is prohibited for PAFC and PAFC2.

Figure 3.5.18 Registers for Port A

3.5.9 Port B (PB3 to PB6)

Port B3 to PB6 is a 4-bit general-purpose I/O port. Each bit can be set individually for input or output. Resetting sets port B to be an input port.

In addition to functioning as a general-purpose I/O port, port B3 to B6 has each external interruption input facility of INT0 to INT3. Edge selection of external interruption is establishes by IIMC register in the interrupt controller. And also, port B3 has $\overline{PS}$ input terminal, and port B4 has clock input terminal TA0IN of 8 bits timer 0, and port B5, B6 each has touch screen block listing PX, PY terminal.

Timer output function and external interrupt function can be enabled by writing 1 to the corresponding bits in the port B function register (PBFC). Resetting resets all bits of the registers PBCR and PBFC to 0, and sets all bits to be input ports.

(1) PB3 (INT0)

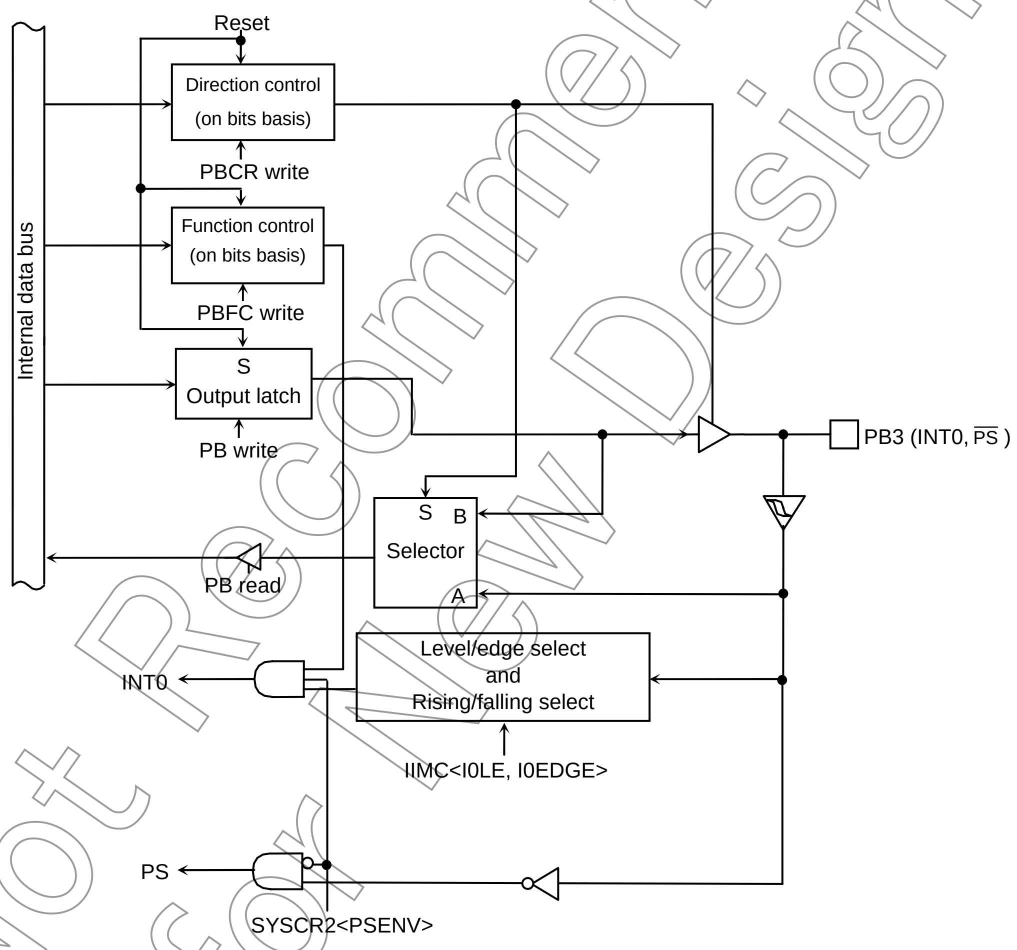


Figure 3.5.19 Port B3

Note: After reset, input 1 to PB3 (INT0, $\overline{PS}$) -pin, because it is worked as $\overline{PS}$ input pin.

(2) PB4 (INT1)

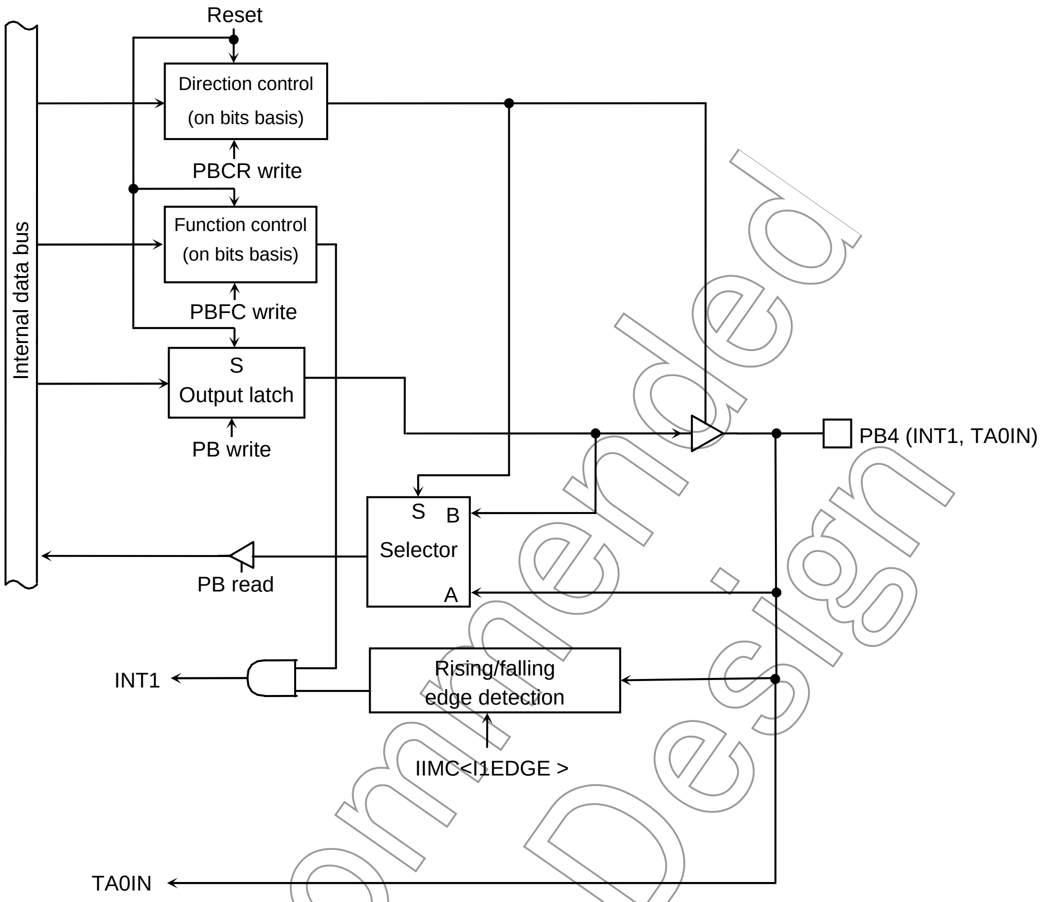


Figure 3.5.20 Port B4

(3) PB5 (INT2), PB6(INT3)

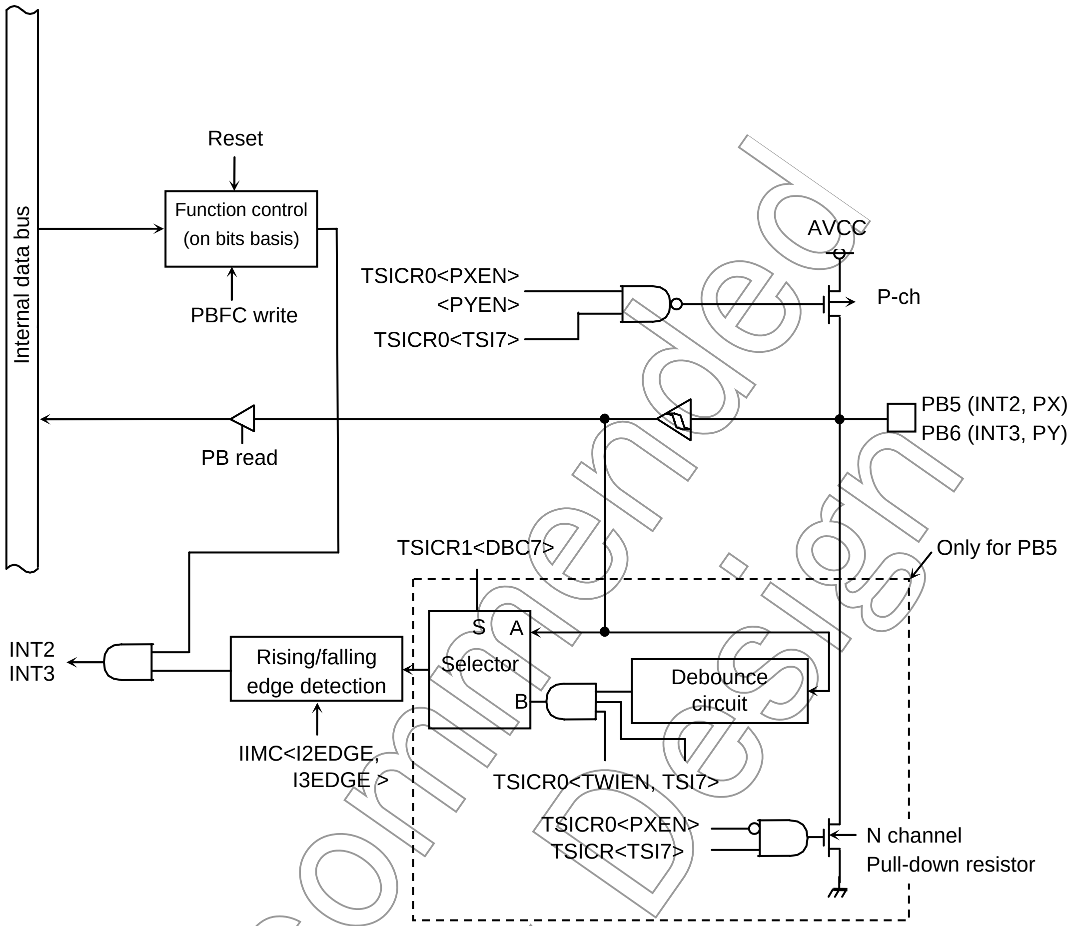


Figure 3.5.21 Port B5, B6

Port B Register

PB (0022H)		7	6	5	4	3	2	1	0
	Bit symbol		PB6	PB5	PB4	PB3			
	Read/Write		R/W						
	After reset		Data from external port (Note 1).						

Port B Control Register

PBCR (0024H)		7	6	5	4	3	2	1	0
	Bit symbol				PB4C	PB3C			
	Read/Write				W				
	After reset				0	0			
	Function				0: Input 1: Output				

Port B Function Register

PBFC (0025H)		7	6	5	4	3	2	1	0
	Bit symbol		PB6F	PB5F	PB4F	PB3F			
	Read/Write		W						
	After reset		0	0	0	1			
	Function		0: Port 1: INT3	0: Port 1: INT2	0: Port 1: INT1	0: Port 1: INT0			

Note 1: Output latch register is set to 1.

Note 2: Read-modify-write is prohibited for the registers PBCR and PBFC.

Note 3: PB4/TA0IN pins do not have a register changing port/function .
For example, when it is used as an input port, the input signal is inputted to 8-bit timer 0 as the timer input 0.

Figure 3.5.22 Registers for Port B

3.5.10 Port C (PC0 to PC5)

Port C0 to C5 are 6-bit general-purpose I/O ports. Each bit can be set individually for input or output. Resetting sets PC0 to PC5 to be an input ports. It also sets all bits of the output latch register to 1.

In addition to functioning as general-purpose I/O port pins, PC0 to PC5 can also function as the I/O for serial channels 0 and 1. A pin can be enabled for I/O by writing 1 to the corresponding bit of the port C function register (PCFC).

Resetting resets all bits of the registers PCCR and PCFC to 0 and sets all pins to be input ports .

(1) Port C0, C3 (TXD0/TXD1)

As well as functioning as I/O port pins, port C0 and C3 can also function as serial channel TXD output pins. In case of use TXD0/TXD1, it is possible to logical invert by setting the register PC<PC0, PC3>.

And port C0 to C3 have a programmable open drain function which can be controlled by the register PCODE<ODEPC0, ODEPC3>.

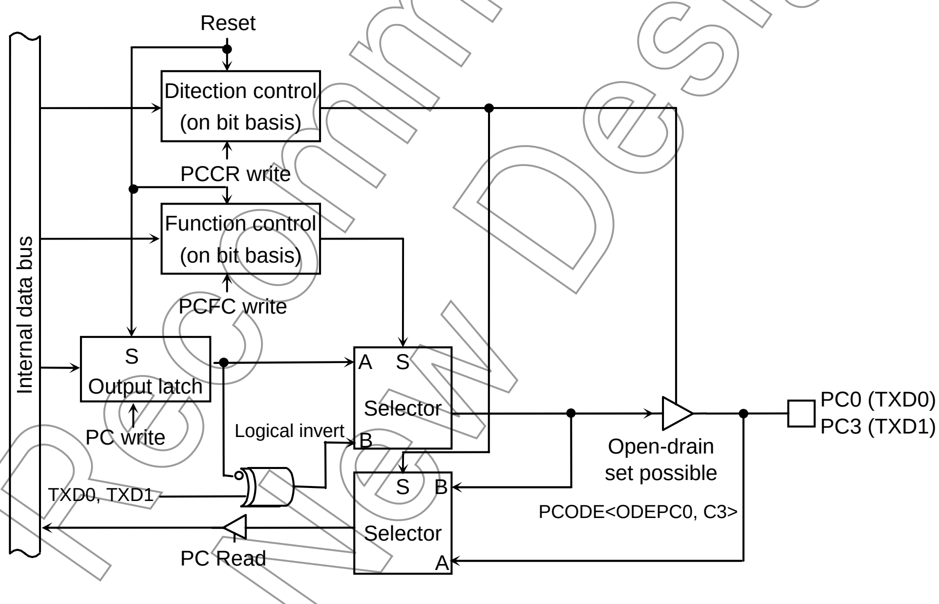


Figure 3.5.23 Port C0 and C3

(2) Port C1, C4 (RXD0, RXD1)

Port C1 and C4 are I/O port pins and can also is used as RXD input for the serial channels. In case of use RXD0/RXD1, it is possible to logical invert by setting the register PC<PC1, PC4>.

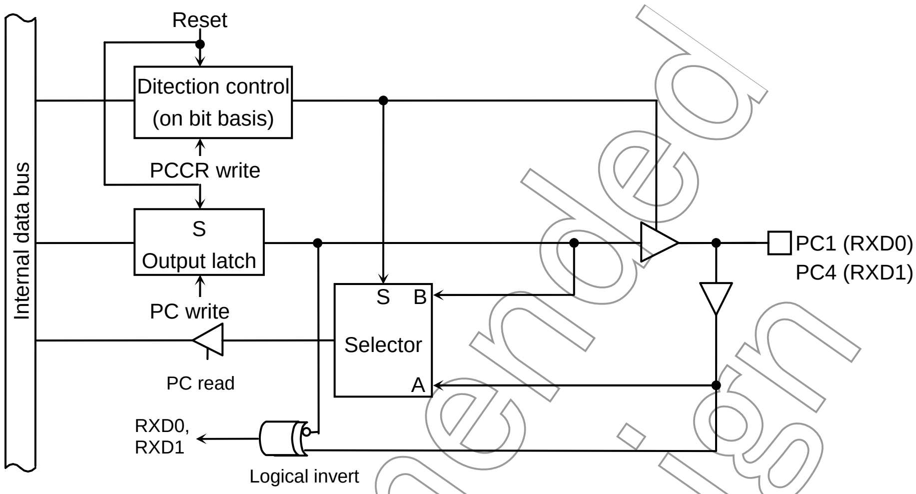


Figure 3.5.24 Port C1 and C4

(3) Port C2 ($\overline{\text{CTS0}}$, SCLK0), C5 ($\overline{\text{CTS1}}$, SCLK1)

Port C2 and C5 are I/O port pins and can also is used as $\overline{\text{CTS}}$ input or SCLK input/output for the serial channels. In case of use $\overline{\text{CTS}}$, SCLK, it is possible to logical invert by setting the register PC<PC2, PC5>.

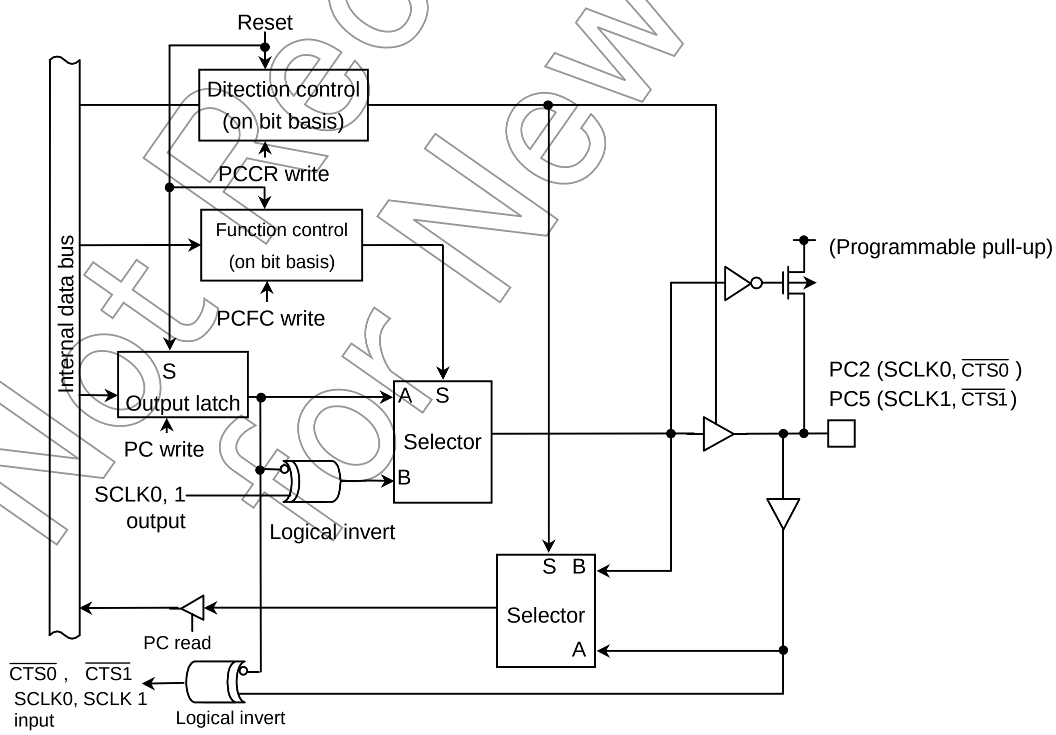


Figure 3.5.25 Port C2 and C5

Port C Register

PC (0023H)

	7	6	5	4	3	2	1	0
Bit symbol			PC5	PC4	PC3	PC2	PC1	PC0
Read/Write			R/W					
After reset			Data from external port (Output latch register is set to 1).					

Port C Control Register

PCCR (0026H)

	7	6	5	4	3	2	1	0
Bit symbol			PC5C	PC4C	PC3C	PC2C	PC1C	PC0C
Read/Write			W					
After reset			0	0	0	0	0	0
Function			0: Input 1: Output					

Port C Functon Register

PCFC (0027H)

	7	6	5	4	3	2	1	0
Bit symbol			PC5F		PC3F	PC2F		PC0F
Read/Write			W		W	W		W
After reset			0		0	0		0
Function			0: Port 1: SCLK1 output		0: Port 1: TXD1	0: Port 1: SCLK0 output		0: Port 1: TXD0

Port C ODE Register

PCODE (0028H)

	7	6	5	4	3	2	1	0
Bit symbol					ODEPC3			ODEPC0
Read/Write					W			W
After reset					0			0
Function					TXD1 0: CMOS 1: Open drain			TXD0 0: CMOS 1: Open drain

Note 1: Read-modify-write is prohibited for the registers PCCR, PCFC and PCODE.

Note 2: PC1/RXD0, PC4/RXD1 pins do not have a register changing port/function. For example, when it is used as an input port, the input signal is inputted to SIO as the cereal receive data.

Figure 3.5.26 Registers for Port C

3.5.11 Port D (PD0 to PD4, PD7)

Port D is a 6-bit output port. Resetting sets the output latch PD to "1", and PD0 to PD4, PD7 pin output "1".

In addition to functioning as output port, port D also function as output pin for LCD controller (D1BSCP, D2BLP, D3BFR, DLEBCD and DOFFB) and output pin for melody/alarm generator (MLDALM). Above setting is used the function register PDFC.

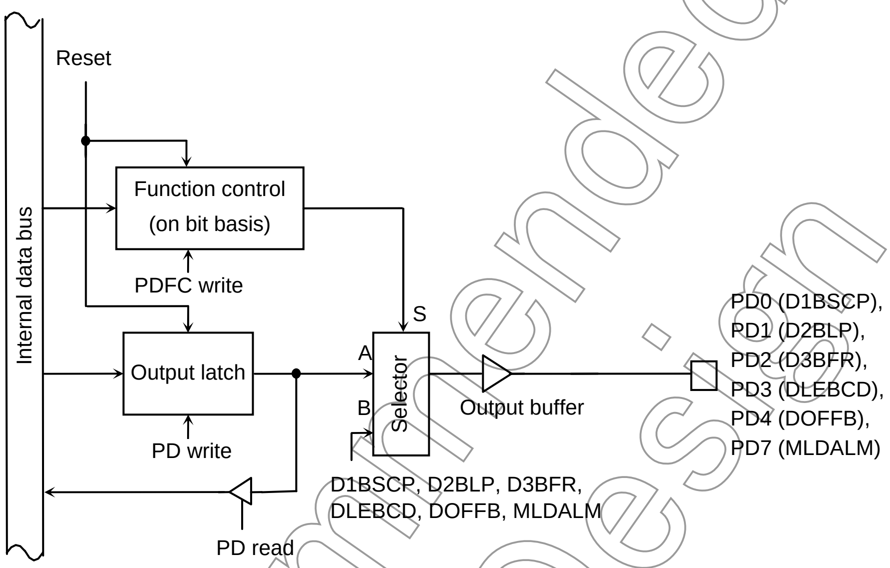


Figure 3.5.27 Port D

Port D register

		7	6	5	4	3	2	1	0
PD (0029H)	Bit symbol	PD7			PD4	PD3	PD2	PD1	PD0
	Read/Write	R/W			R/W	R/W	R/W	R/W	R/W
	After reset	1			1	1	1	1	1

Port D function register

		7	6	5	4	3	2	1	0
PDFC (002AH)	Bit symbol	PD7F			PD4F	PD3F	PD2F	PD1F	PD0F
	Read/Write	W			W	W	W	W	W
	After reset	0			0	0	0	0	0
	Function	0: Port 1: MLDALM			0: Port 1: DOFFB	0: Port 1: DLEBCD	0: Port 1: D3BFR	0: Port 1: D2BLP	0: Port 1: D1BSCP

Note: Read-modify-write is prohibited for the registers PDFC.

Figure 3.5.28 Registers for Port D

3.6 Chip Select/Wait Controller

On the TM91C025, four user-specifiable address areas (CS0 to CS3) can be set. The data bus width and the number of waits can be set independently for each address area (CS0 to CS3 and others).

The pins $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ (which can also function as port pins P60 to P63) are the respective output pins for the areas CS0 to CS3. When the CPU specifies an address in one of these areas, the corresponding $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ pin outputs the chip select signal for the specified address area (in ROM or SRAM). However, in order for the chip select signal to be output, the port 6 function register P6FC must be set.

$\overline{\text{CS2A}}$ to $\overline{\text{CS2C}}$ (CS pin except $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$) are made by MMU.

These pins is $\overline{\text{CS}}$ pin that area and BANK value is fixed without concern in setting of CS/WAIT controller.

The areas CS0 to CS3 are defined by the values in the memory start address registers MSAR0 to MSAR3 and the memory address mask registers MAMR0 to MAMR3.

The chip select/wait control registers B0CS to B3CS and BEXCS should be used to specify the master enable/disable status the data bus width and the number of waits for each address area.

The input pin controlling these states is the bus wait request pin ($\overline{\text{WAIT}}$).

3.6.1 Specifying an Address Area

The CS0 to CS3 address areas are specified using the start address registers (MSAR0 to MSAR3) and memory address mask registers (MAMR0 to MAMR3).

At each bus cycle, a compare operation is performed to determine if the address on the specified a location in the CS0 to CS3 area. If the result of the comparison is a match, this indicates an access to the corresponding CS area. In this case, the $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ pin outputs the chip select signal and the bus cycle operates in accordance with the settings in chip select/wait control register B0CS to B3CS. (See 3.6.2, Chip Select/Wait Control Registers.)

(1) Memory start address registers

Figure 3.6.1 shows the memory start address registers. The memory start address registers MSAR0 to MSAR3 set the start addresses for the CS0 to CS3 areas. Set the upper 8 bits (A23 to A16) of the start address in <S23:16>. The lower 16 bits of the start address (A15 to A0) are permanently set to 0. Accordingly, the start address can only be set in 64-Kbyte increments, starting from 000000H. Figure 3.6.2 shows the relationship between the start address and the start address register value.

Memory Start Address Registers (for areas CS0 to CS3)

MSAR0 (00C8H) / MSAR1 (00CAH)
MSAR2 (00CCH) / MSAR3 (00CEH)

	7	6	5	4	3	2	1	0
Bit symbol	S23	S22	S21	S20	S19	S18	S17	S16
Read/Write	R/W							
After reset	1	1	1	1	1	1	1	1
Function	Determines A23 to A16 of start address.							

Sets start addresses for areas CS0 to CS3.

Figure 3.6.1 Memory Start Address Register

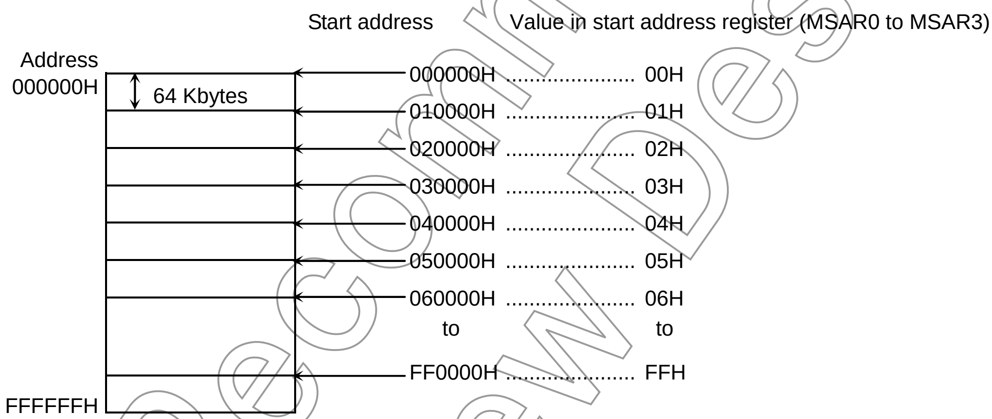


Figure 3.6.2 Relationship between Start Address and Start Address Register Value

(2) Memory address mask registers

Figure 3.6.3 shows the memory address mask registers. Memory address mask registers MAMR0 to MAMR3 are used to set the size of the CS0 to CS3 areas by specifying a mask for each bit of the start address set in memory start address registers MAMR0 to MAMR3. The compare operation used to determine if an address is in the CS0 to CS3 areas is only performed for bus address bits corresponding to bits set to 0 in these registers. Also, the address bits that can be masked by MAMR0 to MAMR3 differ between CS0 to CS3 areas. Accordingly, the size that can be each area is different.

Memory Address Mask Register (for CS0 area)

MAMR0 (00C9H)		7	6	5	4	3	2	1	0
	Bit symbol	V20	V19	V18	V17	V16	V15	V14 to 9	V8
	Read/Write	R/W							
	After reset	1	1	1	1	1	1	1	1
	Function	Sets size of CS0 area. 0: Used for address compare							

Range of possible settings for CS0 area size: 256 bytes to 2 Mbytes

Memory Address Mask Register (CS1)

MAMR1 (00CBH)		7	6	5	4	3	2	1	0
	Bit symbol	V21	V20	V19	V18	V17	V16	V15 to 9	V8
	Read/Write	R/W							
	After reset	1	1	1	1	1	1	1	1
	Function	Sets size of CS1 area. 0: Used for address compare							

Range of possible settings for CS1 area size: 256 bytes to 4 Mbytes.

Memory Address Mask Register (CS2, CS3)

MAMR2 (00CDH) / MAMR3 (00CFH)		7	6	5	4	3	2	1	0
	Bit symbol	V22	V21	V20	V19	V18	V17	V16	V15
	Read/Write	R/W							
	After reset	1	1	1	1	1	1	1	1
	Function	Sets size of CS2 or CS3 area. 0: Used for address compare							

Range of possible settings for CS2 and CS3 area sizes: 32 Kbytes to 8 Mbytes.

Figure 3.6.3 Memory Address Mask Registers

(3) Setting memory start addresses and address areas

Figure 3.6.4 show an example of specifying a 64-Kbyte address area starting from 010000H using the CS0 areas.

Set 01H in memory start address register MSAR0<S23:16> (Corresponding to the upper 8-bits of the start address). Next, calculate the difference between the start address and the anticipated end address (01FFFFH). Bits 20 to 8 of the result correspond to the mask value to be set for the CS0 area. Setting this value in memory address mask register MAMR0<V20:8>sets the area size this example sets 07H in MAMR0 to specify a 64-Kbyte area.

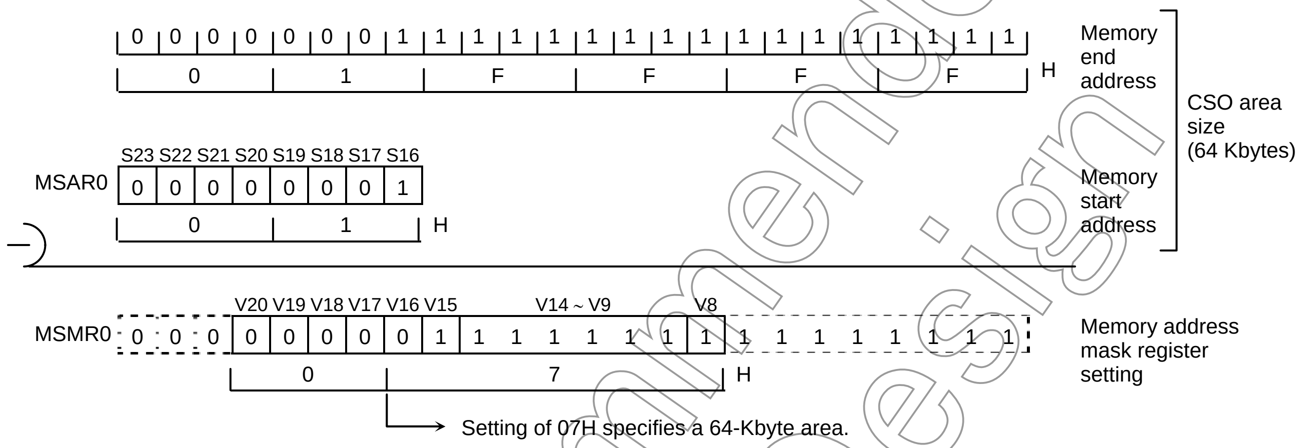


Figure 3.6.4 Example Showing How to Set the CS0 Area

After a reset, MSAR0 to MSAR3 and MAMR0 to MAMR3 are set to FFH. B0CS<B0E>, B1CS<B1E> and B3CS<B3E> are reset to 0. This disabling the CS0, CS1 and CS3 areas. However, as B2CS<B2M> to 0 and B2CS<B2E> to 1, CS2 is enabled from 000FE0H to 000FFFH and 001000H to FFFFFFH in TMP91C025. Also, the bus width and number of waits specified in BEXCS are used for accessing addresses outside the specified CS0 to CS3 area. (See 3.6.2, Chip Select/Wait Control Registers.)

(4) Address area size specification

Table 3.6.1 shows the relationship between CS area and area size. Triangle (Δ) indicates areas that cannot be set by memory start address register and address mask register combinations. When setting an area size using a combination indicated by Δ, set the start address mask register in the desired steps starting from 000000H.

If the CS2 area is set to 16 Mbytes or if two or more areas overlap, the smaller CS area number has the higher priority.

Example: To set the area size for CS0 to 128 Kbytes:

(a) Valid start addresses

000000H
128 Kbytes
020000H
128 Kbytes
040000H
128 Kbytes
060000H
⋮

Any of these addresses may be set as the start address.

(b) Invalid start addresses

000000H
64 Kbytes
010000H
128 Kbytes
030000H
128 Kbytes
050000H
⋮

← This is not an integer multiple of the desired area size setting. Hence, none of these addresses can be set as the start address.

Table 3.6.1 Valid Area Sizes for Each CS Area

CS Area \ Size (Bytes)	256	512	32 K	64 K	128 K	256 K	512 K	1 M	2 M	4 M	8 M
CS0	○	○	○	○	Δ	Δ	Δ	Δ	Δ		
CS1	○	○		○	Δ	Δ	Δ	Δ	Δ	Δ	
CS2			○	○	Δ	Δ	Δ	Δ	Δ	Δ	Δ
CS3			○	○	Δ	Δ	Δ	Δ	Δ	Δ	Δ

Note: Δ: This symbol indicates areas that cannot be set by memory start address register and address mask register combinations.

3.6.2 Chip Select/Wait Control Registers

Figure 3.6.5 lists the chip select/wait control registers.

The master enable/disable, chip select output waveform, data bus width and number of wait states for each address area (CS0 to CS3 and others) are set in their respective chip select/wait control registers, B0CS to B3CS and BEXCS.

Register		7	6	5	4	3	2	1	0
B0CS (00C0H)	Bit symbol	B0E		B0OM1	B0OM0	B0BUS	B0W2	B0W1	B0W0
	Read/Write	W		W					
	After reset	0		0	0	0	0	0	0
	Function	0: Disable 1: Enable		Chip select output waveform selection. 00: For ROM/SRAM 01: 10: Don't care 11:		Data bus width 0: 16 bits 1: 8 bits	Number of waits 000: 2 waits 001: 1 wait 010: (1 + N) waits 011: 0 waits	100: (0 + N) waits 101: 3 waits 110: 4 waits 111: 8 waits	
B1CS (00C1H)	Bit symbol	B1E		B1OM1	B1OM0	B1BUS	B1W2	B1W1	B1W0
	Read/Write	W		W					
	After reset	0		0	0	0	0	0	0
	Function	0: Disable 1: Enable		Chip select output waveform selection. 00: For ROM/SRAM 01: 10: Don't care 11:		Data bus width 0: 16 bits 1: 8 bits	Number of waits 000: 2 waits 001: 1 wait 010: (1 + N) waits 011: 0 waits	100: (0 + N) waits 101: 3 waits 110: 4 waits 111: 8 waits	
B2CS (00C2H)	Bit symbol	B2E	B2M	B2OM1	B2OM0	B2BUS	B2W2	B2W1	B2W0
	Read/Write	W							
	After reset	1	0	0	0	0	0	0	0
	Functions	0: Disable 1: Enable	CS2 area selection. 0: 16-Mbyte area 1: CS area	Chip select output waveform selection. 00: For ROM/SRAM 01: 10: Don't care 11:		Data bus width 0: 16 bits 1: 8 bits	Number of waits 000: 2 waits 001: 1 wait 010: (1 + N) waits 011: 0 waits	100: (0 + N) waits 101: 3 waits 110: 4 waits 111: 8 waits	
B3CS (00C3H)	Bit symbol	B3E		B3OM1	B3OM0	B3BUS	B3W2	B3W1	B3W0
	Read/Write	W		W					
	After reset	0		0	0	0	0	0	0
	Functions	0: Disable 1: Enable		Chip select output waveform selection. 00: For ROM/SRAM 01: 10: Don't care 11:		Data bus width 0: 16 bits 1: 8 bits	Number of waits 000: 2 waits 001: 1 wait 010: (1 + N) waits 011: 0 waits	100: (0 + N) waits 101: 3 waits 110: 4 waits 111: 8 waits	
BEXCS (00C7H)	Bit symbol					BEXBUS	BEXW2	BEXW1	BEXW0
	Read/Write					W			
	After reset					0	0	0	0
	Functions					Data bus width 0: 16 bits 1: 8 bits	Number of waits 000: 2 waits 001: 1 wait 010: (1 + N) waits 011: 0 waits	100: (0 + N) waits 101: 3 waits 110: 4 waits 111: 8 waits	

Master enable bit

0	Disable
1	Enable

CS2 area selection

0	16-Mbyte area
1	Specified address area

Chip select output waveform selection

00	For ROM/SRAM
01	Don't care
10	
11	

Number of address area waits (See 3.6.2, (3) Wait control.)

Data bus width selection

0	16-bit data bus
1	8-bit data bus

Note: Read-modify-write is prohibited for the registers B0CS, B1CS, B2CS, B3CS and BEXCS.

Figure 3.6.5 Chip Select/Wait Control Registers

(1) Master enable bits

Bit 7 (<B0E>, <B1E>, <B2E> or <B3E>) of a chip select/wait control register is the master bit which is used to enable or disable settings for the corresponding address area. Writing 1 to this bit enables the settings. Reset disables (Sets to 0)<B0E>, <B1E>, <B3E>, and enabled (sets to 1) <B2E>. This enables area CS2 only.

(2) Data bus width selection

Bit 3 (<B0BUS>, <B1BUS>, <B2BUS>, <B3BUS> or <BEXBUS>) of a chip select/wait control register specifies the width of the data bus. This bit should be set to 0 when memory is to be accessed using a 16-bit data bus and to 1 when an 8-bit data bus is to be used.

This process of changing the data bus width according to the address being accessed is known as dynamic bus sizing. For details of this bus operation see Table 3.6.2.

Table 3.6.2 Dynamic Bus Sizing

Operand Data Bus Width	Operand Start Address	Memory Data Bus Width	CPU Address	CPU Data		Control for READ Cycle							Control for WRITE Cycle						
				D15 to D8	D7 to D0	$R/\overline{W}$	$\overline{RD}$	$\overline{WR}$	$\overline{HWR}$	$\overline{SRLB}$	$\overline{SRUB}$	$\overline{SRWR}$	$R/\overline{W}$	$\overline{RD}$	$\overline{WR}$	$\overline{HWR}$	$\overline{SRLB}$	$\overline{SRUB}$	$\overline{SRWR}$
8 bits	2n + 0 (Even number)	8 bits	2n + 0	XXXX	b7-b0	H	L	H	H	L	H	H	L	H	L	H	L	H	L
		16 bits	2n + 0	XXXX	b7-b0														
	2n + 1 (Odd number)	8 bits	2n + 1	XXXX	b7-b0					L	H				L	H	L	H	
		16 bits	2n + 1	b7-b0	XXXX					H	L				H	L	H	L	
16 bits	2n + 0 (Even number)	8 bits	2n + 0 2n + 1	XXXX XXXX	b7-b0 b15-b8					L	H				L	H	L	H	
		16 bits	2n + 0	b15-b8	b7-b0					L	L				L	L	L	L	
	2n + 1 (Odd number)	8 bits	2n + 1 2n + 2	XXXX XXXX	b7-b0 b15-b8					L	H				L	H	L	H	
		16 bits	2n + 1 2n + 2	b7-b0 XXXX	XXXX b15-b8					H L	L H				H L	L H	H L	L H	
32 bits	2n + 0 (Even number)	8 bits	2n + 0 2n + 1 2n + 2 2n + 3	XXXX XXXX XXXX XXXX	b7-b0 b15-b8 b23-b16 b31-b24					L	H				L	H	L	H	
		16 bits	2n + 0 2n + 2	b15-b8 b31-b24	b7-b0 b23-b16					L	L				L	L	L	L	
	2n + 1 (Odd number)	8 bits	2n + 1 2n + 2 2n + 3 2n + 4	XXXX XXXX XXXX XXXX	b7-b0 b15-b8 b23-b16 b31-b24					L	H				L	H	L	H	
		16 bits	2n + 1 2n + 2 2n + 4	b7-b0 b23-b16 XXXX	XXXX b15-b8 b31-b24					H L L	L L H				H L L	L L H	H L L	L L H	

xxxx: Indicates that the input data from these bits are ignored during a read. During a write, indicates that the bus for these bits goes too high-impedance; also, that the write strobe signal for the bus remains inactive.

(3) Wait control

Bits 0 to 2 (<B0W0:2>, <B1W0:2>, <B2W0:2>, <B3W0:2>, <BEXW0:2>) of a chip select/wait control register specify the number of waits that are to be inserted when the corresponding memory area is accessed.

The following types of wait operation can be specified using these bits. Bit settings other than those listed in the table should not be made.

Table 3.6.3 Wait Operation Settings

<BxW2:0>	No. of Waits	Wait Operation
000	2 waits	Inserts a wait of 2 states, irrespective of the $\overline{\text{WAIT}}$ pin state.
001	1 wait	Inserts a wait of 1 state, irrespective of the $\overline{\text{WAIT}}$ pin state.
010	(1 + N) waits	Samples the state of the $\overline{\text{WAIT}}$ pin after inserting a wait of one state. If the $\overline{\text{WAIT}}$ pin is low, the waits continue and the bus cycle is extended until the pin goes high.
011	0 waits	Ends the bus cycle without a wait, regardless of the $\overline{\text{WAIT}}$ pin state.
100	(0 + N) waits	Samples the state of the $\overline{\text{WAIT}}$ pin without inserting a wait. If the $\overline{\text{WAIT}}$ pin is low, the waits continue and the bus cycle is extended until the pin goes high.
101	3 waits	Inserts a wait of 3 states, irrespective of the $\overline{\text{WAIT}}$ pin state.
110	4 waits	Inserts a wait of 4 states, irrespective of the $\overline{\text{WAIT}}$ pin state.
111	8 waits	Inserts a wait of 8 states, irrespective of the $\overline{\text{WAIT}}$ pin state.

A Reset sets these bits to 000 (2 waits).

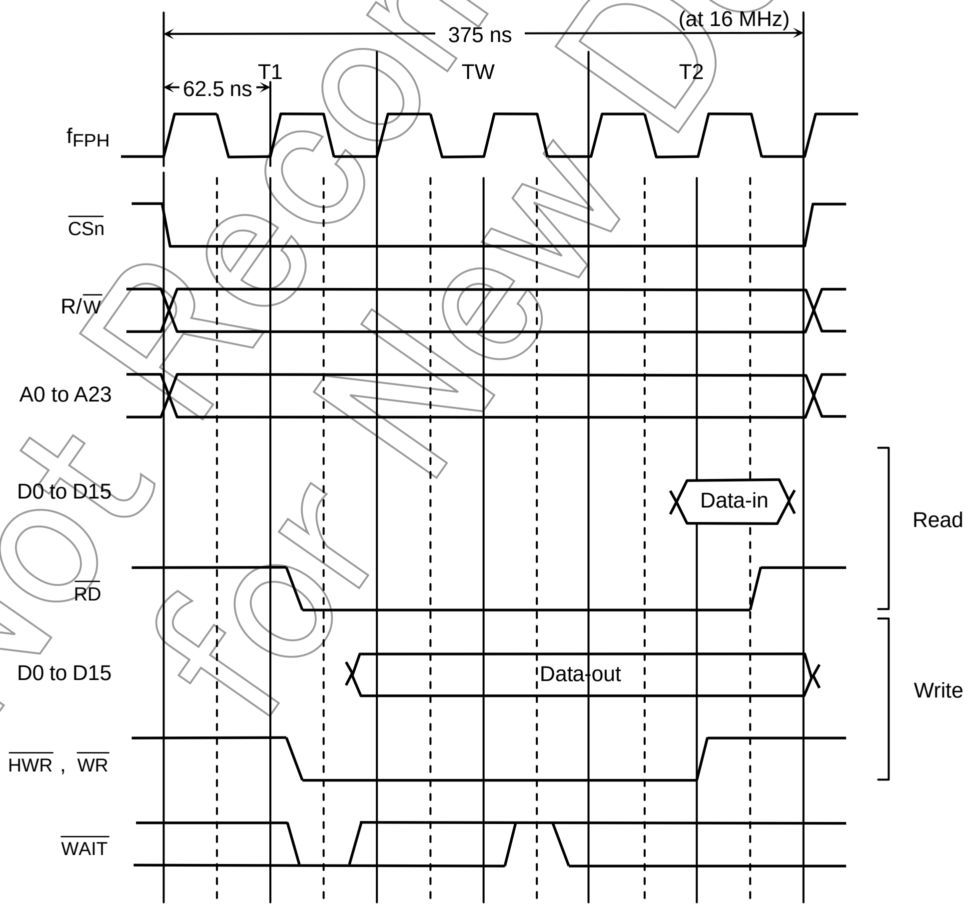


Figure 3.6.6 (0 + N) Waits Read/Write Cycle (N = 1)

(4) Bus width and wait control for an area other than CS0 to CS3

The chip select/wait control register BEXCS controls the bus width and number of waits when memory locations which are not in one of the four user-specified address areas (CS0 to CS3) are accessed. The BEXCS register settings are always enabled for areas other than CS0 to CS3.

(5) Selecting 16-Mbyte area/specified address area

Setting B2CS<B2M> (bit 6 of the chip select/wait control register for CS2) to 0 designates the 16-Mbyte area 000FE0H to 000FFFH, 003000H to FFFFFFH as the CS2 area. Setting B2CS<B2M> to 1 designates the address area specified by the start address register MSAR2 and the address mask register MAMR2 as CS2 (e.g., if B2CS<B2M> = 1, CS2 is specified in the same manner as CS0, CS1 and CS3 are).

A reset clears this bit to 0, specifying CS2 as a 16-Mbyte address area.

(6) Procedure for setting chip select/wait control

When using the chip select/wait control function, set the registers in the following order:

- Set the memory start address registers MSAR0 to MSAR3.
  Set the start addresses for CS0 to CS3.
- Set the memory address mask registers MAMR0 to MAMR3.
  Set the sizes of CS0 to CS3.
- Set the chip select/wait control registers B0CS to B3CS.
  Set the chip select output waveform, data bus width, number of waits and master enable/disable status for $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$.
  The CS0 to S3 pins can also function as pins P60 to P63. To output a chip select signal using one of these pins, set the corresponding bit in the port 6 function register P6FC to 1.
  If a CS0 to S3 address is specified which is actually an internal I/O and RAM area address, the CPU accesses the internal address area and no chip select signal is output on any of the $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ pins.

(Setting example)

In this example CS0 is set to be the 64-Kbyte area 010000H to 01FFFFH. The bus width is set to 16 bits and the number of waits is set to 0.

MSAR0 = 01H - - - - Start address: 010000H
MAMR0 = 07H - - - Address area: 64 Kbytes
B0CS = 83H - - - - - ROM/SRAM, 16-bit data bus, zero waits, CS0 area settings enabled.

3.6.3 Connecting External Memory

Figure 3.6.7 shows an example of how to connect external memory to the TMP91C025. In this example the ROM is connected using a 16-bit bus. The RAM and I/O are connected using an 8-bit bus.

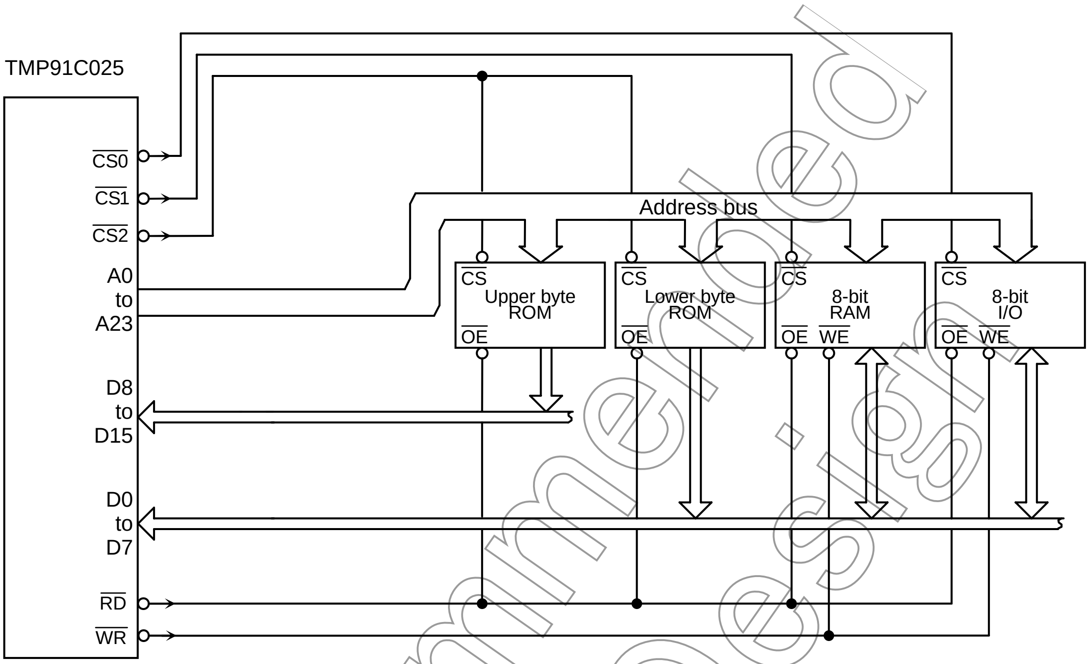


Figure 3.6.7 Example of External Memory Connection (ROM uses 16-bit bus: RAM and I/O use 8-bit bus.)

A reset clears all bits of the port 6 control register P6CR and the port 6 function register P6FC to 0 and disables output of the CS signal. To output the CS signal, the appropriate bit must be set to 1.

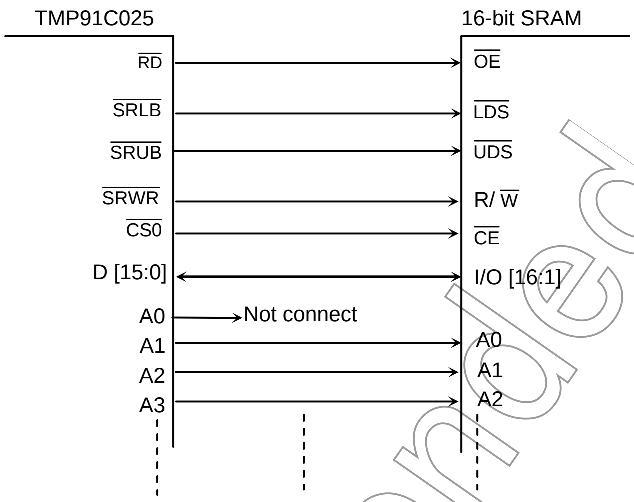


Figure 3.6.8 How to Connect to 16-Bit SRAM for TMP91C025

3.7 8-Bit Timers (TMRA)

The TMP91C025 features 4 channel (TMRA0 to TMRA3) built-in 8-bit timers.

These timers are paired into 2 modules: TMRA01 and TMRA23. Each module consists of 2 channels and can operate in any of the following 4 operating modes.

- 8-bit interval timer mode
- 16-bit interval timer mode
- 8-bit programmable square wave pulse generation output mode
  (PPG: Variable duty cycle with variable period)
- 8-bit pulse width modulation output mode
  (PWM: Variable duty cycle with constant period)

Figure 3.7.1 to Figure 3.7.2 Show block diagrams for TMRA01 and TMRA23.

Each channel consists of an 8-bit up counter, an 8-bit comparator and an 8-bit timer register. In addition, a timer flip-flop and a prescaler are provided for each pair of channels.

The operation mode and timer flip-flops are controlled by 5 bytes registers SFRs (Special-function registers).

Each of the 2 modules (TMRA01 and TMRA23) can be operated independently. All modules operate in the same manner; hence only the operation of TMRA01 is explained here.

The contents of this chapter are as follows.

3.7.1 Block Diagrams
3.7.2 Operation of Each Circuit
3.7.3 SFRs
3.7.4 Operation in Each Mode
(1) 8-bit timer mode
(2) 16-bit timer mode
(3) 8-bit PPG (Programmable pulse generation) output mode
(4) 8-bit PWM (Pulse width modulation) output mode
(5) Setting for each mode

Table 3.7.1 Registers and Pins for Each Module

Module		TMRA01	TMRA23
External pin	Input pin for external clock	TA0IN (shared with PB4)	None
	Output pin for timer flip-flop	TA1OUT (shared with PA1)	TA3OUT (shared with PA2)
SFR (address)	Timer run register	TA01RUN (0100H)	TA23RUN (0108H)
	Timer register	TA0REG (0102H) TA1REG (0103H)	TA2REG (010AH) TA3REG (010BH)
	Timer mode register	TA01MOD (0104H)	TA23MOD (010CH)
	Timer flip-flop control register	TA1FFCR (0105H)	TA3FFCR (010DH)

3.7.1 Block Diagrams

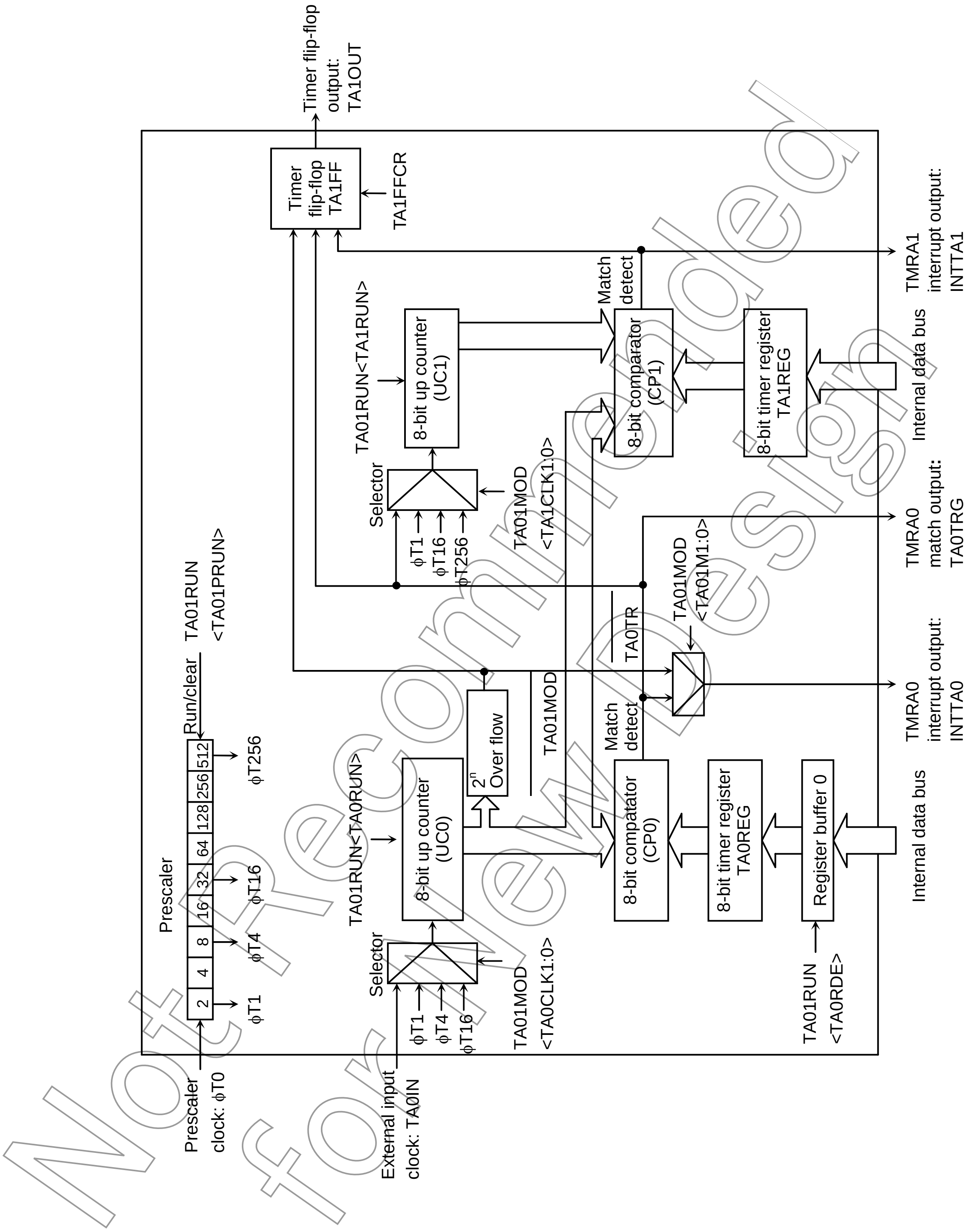


Figure 3.7.1 TMRA01 Block Diagram

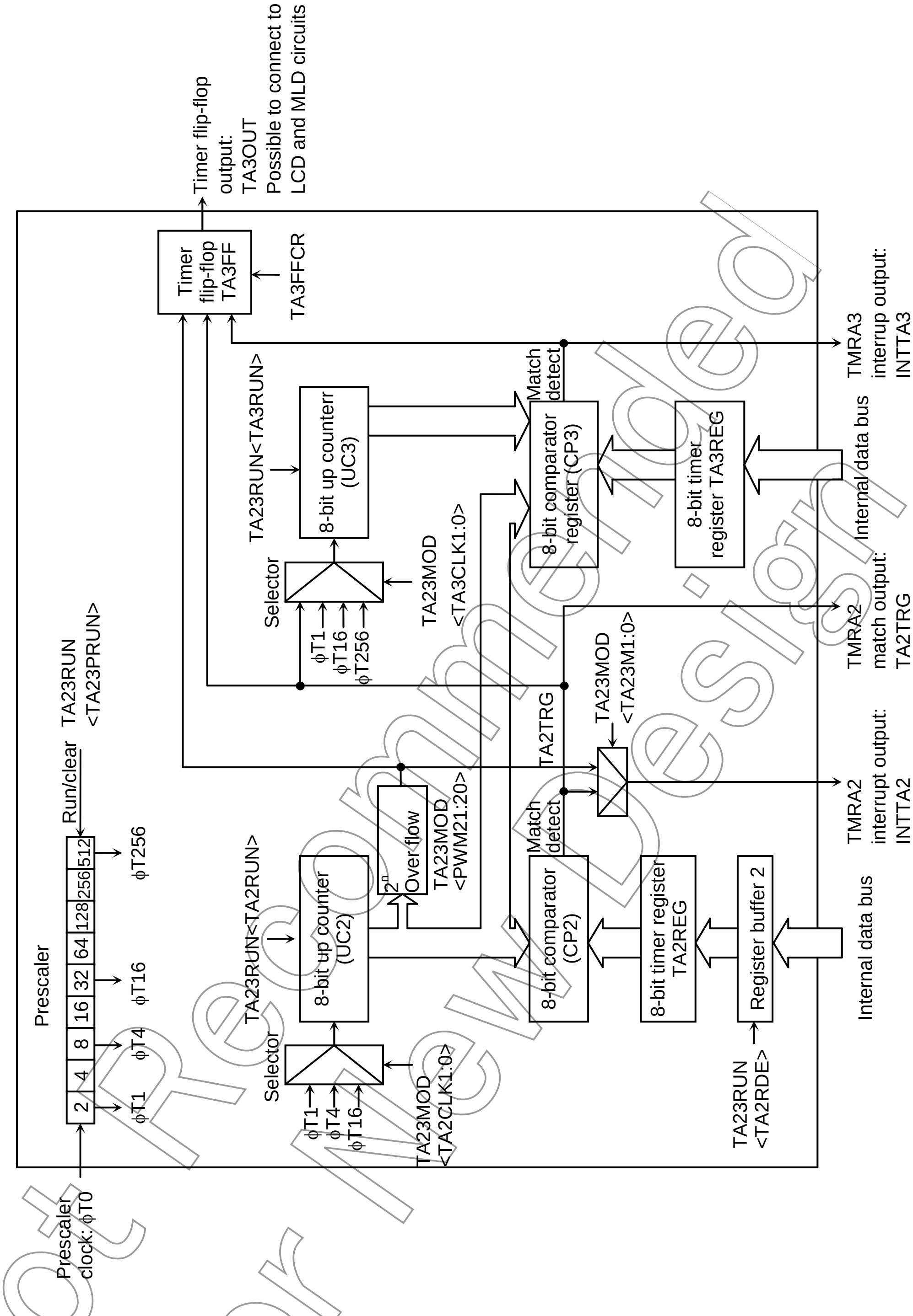


Figure 3.7.2 TMRA23 Block Diagram

3.7.2 Operation of Each Circuit

(1) Prescalers

A 9-bit prescaler generates the input clock to TMRA01.

The φT0 as the input clock to prescaler is a clock divided by 4 which selected using the prescaler clock selection register SYSCR0<PRCK1:0>.

The prescaler's operation can be controlled using TA01RUN<TA01PRUN> in the timer control register. Setting <TA01PRUN> to 1 starts the count; setting <TA01PRUN> to 0 clears the prescaler to zero and stops operation. Table 3.7.2 shows the various prescaler output clock resolutions.

Table 3.7.2 Prescaler Output Clock Resolution

at fc = 36 MHz, fs = 32.768 kHz

System Clock Selection SYSCR1 <SYSCK>	Prescaler Clock Selection SYSCR0 <PRCK1:0>	Gear Value SYSCR1 <GEAR2:0>	Prescaler Output Clock Resolution			
			φT1	φT4	φT16	φT256
1 (fs)	00 (f_{FPH})	XXX	2^{3}/fs (244 μs)	2^{5}/fs (977 μs)	2^{7}/fs (3.9 ms)	2^{11}/fs (62.5 ms)
0 (fc)		000 (fc)	2^{3}/fc (0.2 μs)	2^{5}/fc (0.9 μs)	2^{7}/fc (3.6 μs)	2^{11}/fc (56.9 μs)
		001 (fc/2)	2^{4}/fc (0.4 μs)	2^{6}/fc (1.8 μs)	2^{8}/fc (7.1 μs)	2^{12}/fc (113.8 μs)
		010 (fc/4)	2^{5}/fc (0.9 μs)	2^{7}/fc (3.6 μs)	2^{9}/fc (14.2 μs)	2^{13}/fc (227.6 μs)
		011 (fc/8)	2^{6}/fc (1.8 μs)	2^{8}/fc (7.1 μs)	2^{10}/fc (28.4 μs)	2^{14}/fc (455.1 μs)
		100 (fc/16)	2^{7}/fc (3.6 μs)	2^{9}/fc (14.2 μs)	2^{11}/fc (56.9 μs)	2^{15}/fc (910.2 μs)
	10 (fc/16 CLOCK)	XXX	2^{7}/fc (3.6 μs)	2^{9}/fc (14.2 μs)	2^{11}/fc (56.9 μs)	2^{15}/fc (910.2 μs)

xxx: Don't care

(2) Up counters (UC0 and UC1)

These are 8-bit binary counters which count up the input clock pulses for the clock specified by TA01MOD.

The input clock for UC0 is selectable and can be either the external clock input via the TA0IN pin or one of the three internal clocks φT1, φT4 or φT16. The clock setting is specified by the value set in TA01MOD<TA01CLK1:0>.

The input clock for UC1 depends on the operation mode. In 16-bit timer mode, the overflow output from UC0 is used as the input clock. In any mode other than 16-bit timer mode, the input clock is selectable and can either be one of the internal clocks φT1, φT16 or φT256, or the comparator output (The match detection signal) from TMRA0.

For each interval timer the timer operation control register bits TA01RUN<TA0RUN> and TA01RUN<TA1RUN> can be used to stop and clear the up counters and to control their count. A reset clears both up counters, stopping the timers.

(3) Timer registers (TA0REG and TA1REG)

These are 8-bit registers which can be used to set a time interval. When the value set in the timer register TA0REG or TA1REG matches the value in the corresponding up counter, the comparator match detect signal goes active. If the value set in the timer register is 00H, the signal goes active when the up counter overflows.

The TA0REG are double buffer structure, each of which makes a pair with register buffer.

The setting of the bit TA01RUN<TA0RDE> determines whether TA0REG's double buffer structure is enabled or disabled. It is disabled if <TA0RDE> = 0 and enabled if <TA0RDE> = 1.

When the double buffer is enabled, data is transferred from the register buffer to the timer register when a 2^n overflow occurs in PWM mode, or at the start of the PPG cycle in PPG mode. Hence the double buffer cannot be used in timer mode.

A reset initializes <TA0RDE> to 0, disabling the double buffer. To use the double buffer, write data to the timer register, set <TA0RDE> to 1, and write the following data to the register buffer. Figure 3.7.3 show the configuration of TA0REG.

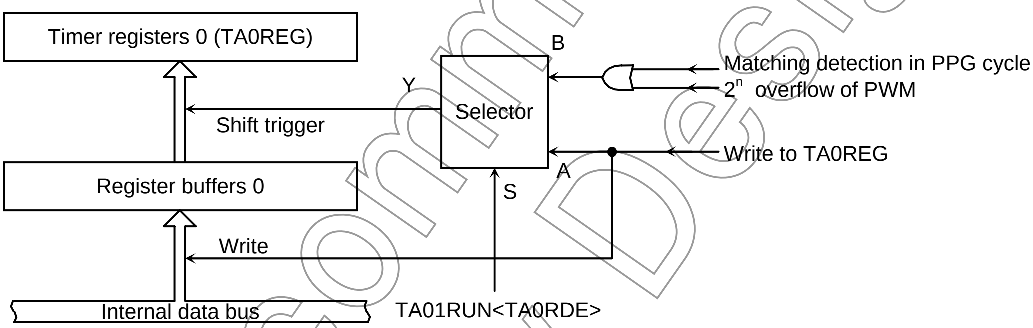


Figure 3.7.3 Configuration of TA0REG

Note: The same memory address is allocated to the timer register and the register buffer. When <TA0RDE> = 0, the same value is written to the register buffer and the timer register; when <TA0RDE> = 1, only the register buffer is written to.

The address of each timer register is as follows.

TA0REG: 000102H	TA1REG: 000103H
TA2REG: 00010AH	TA3REG: 00010BH

All these registers are write only and cannot be read.

(4) Comparator (CP0)

The comparator compares the value in an up counter with the value set in a timer register. If they match, the up counter is cleared to zero and an interrupt signal (INTTA0 or INTTA1) is generated. If timer flip-flop inversion is enabled, the timer flip-flop is inverted at the same time.

(5) Timer flip-flop (TA1FF)

The timer flip-flop (TA1FF) is a flip-flop inverted by the match detects signal (8-bit comparator output) of each interval timer.

Whether inversion is enabled or disabled is determined by the setting of the bit TA1FFCR<TA1FFIE> in the timer flip-flop control register.

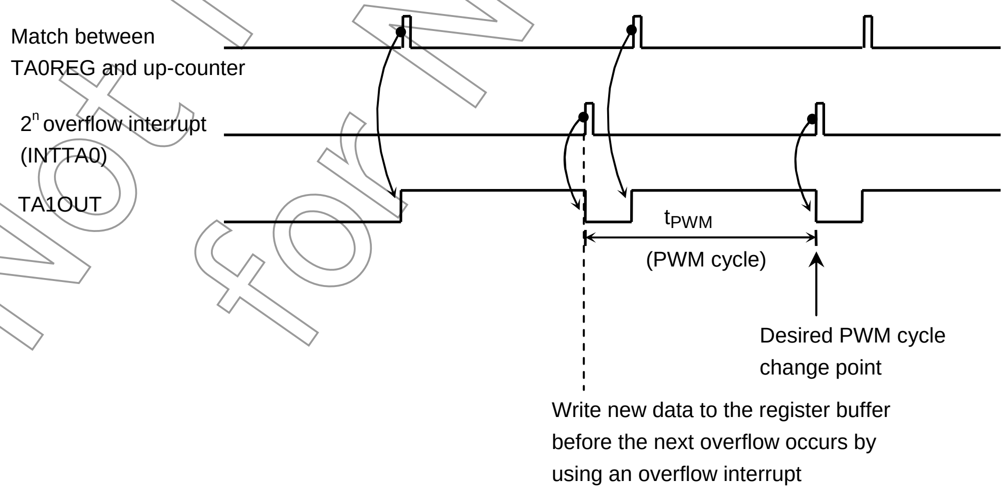
A Reset clears the value of TA1FF1 to 0.

Writing 01 or 10 to TA1FFCR<TA1FFC1:0> sets TA1FF to 0 or 1. Writing 00 to these bits inverts the value of TA1FF (This is known as software inversion).

The TA1FF signal is output via the TA1OUT pin (Concurrent with PA1). When this pin is used as the timer output, the timer flip-flop should be set beforehand using the port A function register PAFC2.

Note: When the double buffer is enabled for an 8-bit timer in PWM or PPG mode, caution is required as explained below.
If new data is written to the register buffer immediately before an overflow occurs by a match between the timer register value and the up-counter value, the timer flip-flop may output an unexpected value.
For this reason, make sure that in PWM mode new data is written to the register buffer by six cycles ($f_{SYS} \times 6$) before the next overflow occurs by using an overflow interrupt.
In the case of using PPG mode, make sure that new data is written to the register buffer by six cycles before the next cycle compare match occurs by using a cycle compare match interrupt.

Example when using PWM mode



3.7.3 SFRs

TMRA01 Run Register

TA01RUN (0100H)

	7	6	5	4	3	2	1	0
Bit symbol	TA0RDE				I2TA01	TA01PRUN	TA1RUN	TA0RUN
Read/Write	R/W				R/W			
After reset	0				0	0	0	0
Function	Double buffer 0: Disable 1: Enable				IDLE2 0: Stop 1: Operate	8-bit timer run/stop control 0: Stop and clear 1: Run (Count up)		

TA0REG double buffer control

0	Disable
1	Enable

Timer run/stop control

0	Stop and clear
1	Run (Count up)

I2TA01: Operation in IDLE2 mode
TA01PRUN: Run prescaler
TA1RUN: Run TMRA1
TA0RUN: Run TMRA0

Note: The values of bits 4, 5, 6 of TA01RUN are undefined when read.

TMRA23 Run Register

TA23RUN (0108H)

	7	6	5	4	3	2	1	0
Bit symbol	TA2RDE				I2TA23	TA23PRUN	TA3RUN	TA2RUN
Read/Write	R/W				R/W			
After reset	0				0	0	0	0
Function	Double buffer 0: Disable 1: Enable				IDLE2 0: Stop 1: Operate	8-bit timer run/stop control 0: Stop and clear 1: Run (Count up)		

TA2REG double buffer control

0	Disable
1	Enable

Timer run/stop control

0	Stop and clear
1	Run (Count up)

I2TA23: Operation in IDLE2 mode
TA23PRUN: Run prescaler
TA3RUN: Run TMRA3
TA2RUN: Run TMRA2

Note: The values of bits 4, 5, 6 of TA23RUN are undefined when read.

Figure 3.7.4 TMRA Registers

TMRA01 Mode Register

TA01MOD (0104H)

	7	6	5	4	3	2	1	0
Bit symbol	TA01M1	TA01M0	PWM01	PWM00	TA1CLK1	TA1CLK0	TA0CLK1	TA0CLK0
Read/Write	R/W							
After reset	0	0	0	0	0	0	0	0
Function	Operation mode 00: 8-bit timer mode 01: 16-bit timer mode 10: 8-bit PPG mode 11: 8-bit PWM mode		PWM cycle 00: Reserved 01: 2^6 10: 2^7 11: 2^8		Source clock for TMRA1 00: TA0TRG 01: φT1 10: φT16 11: φT256		Source clock for TMRA0 00: TA0IN pin 01: φT1 10: φT4 11: φT16	

→ TMRA0 source clock selection

00	TA0IN (External input)
01	φT1 (Prescaler)
10	φT4 (Prescaler)
11	φT16 (Prescaler)

→ TMRA1 source clock selection

	TA01MOD <TA01M1:0> ≠ 01	TA01MOD <TA01M1:0> = 01
00	Comparator output from TMRA0	Overflow output from TMRA0 (16-bit timer mode)
01	φT1	
10	φT16	
11	φT256	

→ PWM cycle selection

00	Reserved
01	2^6 × source clock
10	2^7 × source clock
11	2^8 × source clock

→ TMRA01 operation mode selection

00	Two 8-bit timers
01	16-bit timer
10	8-bit PPG
11	8-bit PWM (TMRA0) + 8-bit timer (TMRA1)

Figure 3.7.5 TMRA Registers

TMRA23 Mode Register

		7	6	5	4	3	2	1	0
TA23MOD (010CH)	Bit Symbol	TA23M1	TA23M0	PWM21	PWM20	TA3CLK1	TA3CLK0	TA2CLK1	TA2CLK0
	Read/Write	R/W							
	After reset	0	0	0	0	0	0	0	0
	Function	Operation mode 00: 8-bit timer mode 01: 16-bit timer mode 10: 8-bit PPG mode 11: 8-bit PWM mode		PWM cycle 00: Reserved 01: 2^6 10: 2^7 11: 2^8		TMRA3 clock for TMRA3 00: TA2TRG 01: ϕT1 10: ϕT16 11: ϕT256		TMRA2 clock for TMRA2 00: Reserved 01: ϕT1 10: ϕT4 11: ϕT16	

TMRA2 source clock selection

00	Do not set
01	ϕT1 (Prescaler)
10	ϕT4 (Prescaler)
11	ϕT16 (Prescaler)

TMRA3 source clock selection

	TA23MOD <TA23M1:0> $\neq$ 01	TA23MOD <TA23M1:0> $=$ 01
00	Comparator output from TMRA2	Overflow output from TMRA2
01	ϕT1	
10	ϕT16	
11	ϕT256	(16-bit timer mode)

PWM cycle selection

00	Reserved
01	$2^6 \times$ source clock
10	$2^7 \times$ source clock
11	$2^8 \times$ source clock

TMRA23 operation mode selection

00	Two 8-bit timers
01	16-bit timer
10	8-bit PPG
11	8-bit PWM (TMRA2) $+$ 8-bit timer (TMRA3)

Figure 3.7.6 TMRA Registers

TMRA1 Flip-Flop Control Register

TA1FFCR (0105H)

	7	6	5	4	3	2	1	0
Bit symbol					TA1FFC1	TA1FFC0	TA1FFIE	TA1FFIS
Read/Write					R/W		R/W	
After reset					1	1	0	0
Function					00: Invert TA1FF 01: Set TA1FF 10: Clear TA1FF 11: Don't care		TA1FF control for inversion 0: Disable 1: Enable	TA1FF inversion select 0: TMRA0 1: TMRA1

Read-modify -write instructions are prohibited.

Inverse signal for timer flop-flop 1 (TA1FF)
(Don't care except in 8-bit timer mode)

0	Inversion by TMRA0
1	Inversion by TMRA1

Inversion of TA1FF

0	Disabled
1	Enabled

Control of TA1FF

00	Inverts the value of TA1FF
01	Sets TA1FF to 1
10	Clears TA1FF to 0
11	Don't care

Figure 3.7.7 TMRA Registers

TMRA3 Flip-Flop Control Register

TA3FFCR (010DH)

	7	6	5	4	3	2	1	0
Bit symbol					TA3FFC1	TA3FFC0	TA3FFIE	TA3FFIS
Read/Write					R/W		R/W	
After reset					1	1	0	0
Function					00: Invert TA3FF 01: Set TA3FF 10: Clear TA3FF 11: Don’t care		TA3FF control for inversion 0: Disable 1: Enable	TA3FF inversion select 0: TMRA2 1: TMRA3

Read-modify -write instructions are prohibited.

Inverse signal for timer flip-flop 3 (TA3FF)
(Don’t care except in 8-bit timer mode)

0	Inversion by TMRA2
1	Inversion by TMRA3

Inversion of TA3FF

0	Disabled
1	Enabled

Control of TA3FF

00	Inverts the value of TA3FF
01	Sets TA3FF to 1
10	Clears TA3FF to 0
11	Don’t care

Figure 3.7.8 TMRA Registers

TMRA register

		7	6	5	4	3	2	1	0
TA0REG (0102H)	bit Symbol	–							
	Read/Write	W							
	After reset	Undefined							
TA1REG (0103H)	bit Symbol	–							
	Read/Write	W							
	After reset	Undefined							
TA2REG (010AH)	bit Symbol	–							
	Read/Write	W							
	After reset	Undefined							
TA3REG (010BH)	bit Symbol	–							
	Read/Write	W							
	After reset	Undefined							

Note: The above registers are prohibited read-modify-write instruction.

Figure 3.7.9 TMRA Registers

3.7.4 Operation in Each Mode

(1) 8-bit timer mode

Both TMRA0 and TMRA1 can be used independently as 8-bit interval timers. Setting its function or counter data for TMRA0 and TMRA1 after stop these registers.

a. Generating interrupts at a fixed interval (Using TMRA1)

To generate interrupts at constant intervals using TMRA1 (INTTA1), first stop TMRA1 then set the operation mode, input clock and a cycle to TA01MOD and TA1REG register, respectively. Then, enable the interrupt INTTA1 and start TMRA1 counting.

Example: To generate an INTTA1 interrupt every 8.0 μs at fc = 36 MHz, set each register as follows:

∗ Clock state: System clock: High-frequency (fc); Prescaler clock: f_{FPH}

		MSB 7	6	5	4	3	2	1	LSB 0	
TA01RUN	←	–	X	X	X	–	–	0	–	Stop TMRA1 and clear it to 0.
TA01MOD	←	0	0	X	X	0	1	X	X	Select 8-bit timer mode and select φT1 ((2^3/fc)s at fc = 36 MHz) as the input clock.
TA1REG	←	0	0	1	0	1	0	0	0	Set TA1REG to 8.0 μs ÷ φT1(2^3/fc) ≈ 40 = 28H
INTETA01	←	X	1	0	1	–	–	–	–	Enable INTTA1 and set it to level 5.
TA01RUN	←	–	X	X	X	–	1	1	–	Start TMRA1 counting.

X: Don't care, –: No change

Select the input clock using Table 3.7 2.

Note: The input clocks for TMRA0 and TMRA1 are different from as follows.
TMRA0: TA0IN input, φT1, φT4 or φT16
TMRA1: Match output of TMRA0, φT1, φT16, φT256

b. Generating a 50% duty ratio square wave pulse

The state of the timer flip-flop (TA1FF) is inverted at constant intervals and its status output via the timer output pin (TA1OUT).

Example: To output a 1.2-μs square wave pulse from the TA1OUT pin at fc = 36 MHz, use the following procedure to make the appropriate register settings. This example uses TMRA1; however, either TMRA0 or TMRA1 may be used.

∗ Clock state
- System clock: High-frequency (fc)
- Clock gear: 1 (fc)
- Prescaler clock: f_{FPH}

		7	6	5	4	3	2	1	0	
TA01RUN	←	–	X	X	X	–	–	0	–	Stop TMRA1 and clear it to 0.
TA01MOD	←	0	0	X	X	0	1	–	–	Select 8-bit timer mode and select φT1 ((2^3/fc)s at fc = 36 MHz) as the input clock.
TA1REG	←	0	0	0	0	0	0	1	1	Set the timer register to 1.2 μs ÷ φT1(2^3/fc) ÷ 2 = 3
TA1FFCR	←	X	X	X	X	1	0	1	1	Clear TA1FF to 0 and set it to invert on the match detects signal from TMRA1.
PAFC2	←	X	X	X	X	–	–	1	–	Set PA1 to function as the TA1OUT pin.
TA01RUN	←	–	X	X	X	–	1	1	–	Start TMRA1 counting.

X: Don't care, –: No change

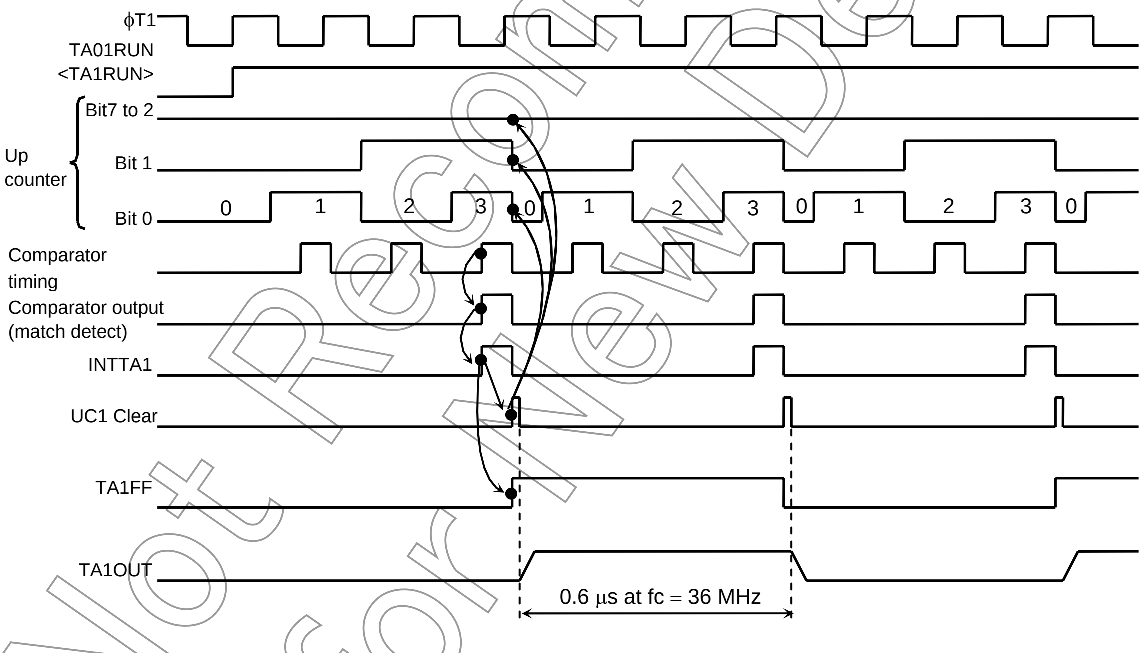


Figure 3.7.10 Square Wave Output Timing Chart (50% duty)

c. Making TMRA1 count up on the match signal from the TMRA0 comparator

Select 8-bit timer mode and set the comparator output from TMRA0 to be the input clock to TMRA1.

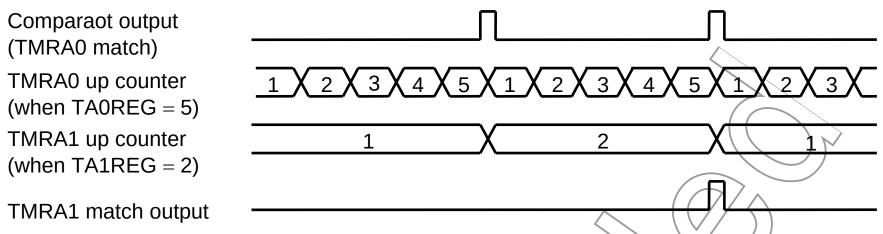


Figure 3.7.11 TMRA1 Count Up on Signal from TMRA0

(2) 16-bit timer mode

A 16-bit interval timer is configured by pairing the two 8-bit timers TMRA0 and TMRA1.

To make a 16-bit interval timer in which TMRA0 and TMRA1 are cascaded together, set TA01MOD<TA01M1:0> to 01.

In 16-bit timer mode, the overflow output from TMRA0 is used as the input clock for TMRA1, regardless of the value set in TA01MOD<TA01CLK1:0>. Table 3.7.2 shows the relationship between the timer (Interrupt) cycle and the input clock selection.

LSB 8-bit set to TA0REG and MSB 8-bit is for TA1REG. Please keep setting TA0REG first because setting data for TA0REG inhibit its compare function and setting data for TA1REG permit it.

(Setting example)

To generate an INTTA1 interrupt every 0.22 s at fc = 36 MHz, set the timer registers TA0REG and TA1REG as follows:

* Clock state
- System clock: High-frequency (fc)
- Clock gear: 1 (fc)
- Prescaler clock: f_{FPH}

If ϕT16 ((2^7/fc)s at 36 MHz) is used as the input clock for counting, set the following value in the registers: 0.22 s/(2^7/fc) μs ≈ 62500 = F424H

(i.e. set TA1REG to F4H and TA0REG to 24H).

As a result, INTTA1 interrupt can be generated every 0.23 [s].

The comparator match signal is output from TMRA0 each time the up counter UC0 matches TA0REG, though the up counter UC0 is not be cleared and also INTTA0 is not generated.

In the case of the TMRA1 comparator, the match detect signal is output on each comparator pulse on which the values in the up counter UC1 and TA1REG match. When the match detect signal is output simultaneously from both the comparators TMRA0 and TMRA1, the up counters UC0 and UC1 are cleared to 0 and the interrupt INTTA1 is generated. Also, if inversion is enabled, the value of the timer flip-flop TA1FF is inverted.

(Example)

When TA1REG = 04H and TA0REG = 80H

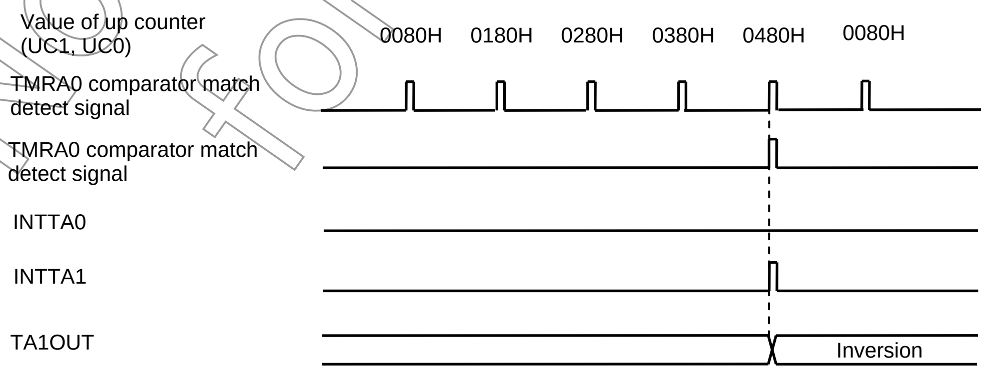


Figure 3.7.12 Timer Output by 16-Bit Timer Mode

(3) 8-bit PPG (Programmable pulse generation) output mode

Square wave pulses can be generated at any frequency and duty ratio by TMRA0. The output pulses may be active low or active high. In this mode TMRA1 cannot be used.

TMRA0 outputs pulses on the TA1OUT pin.

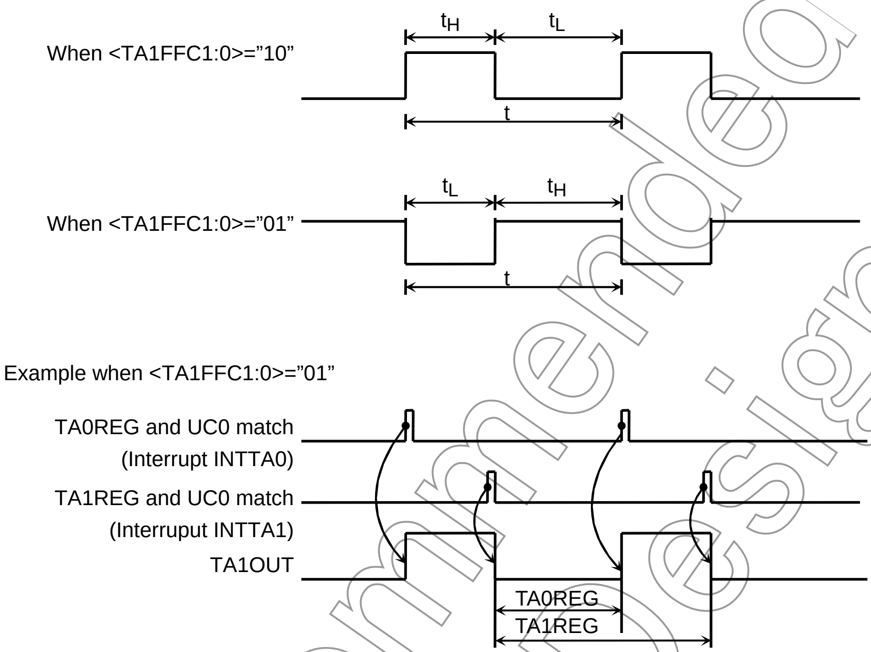


Figure 3.7.13 8-Bit PPG Output Waveforms

In this mode, a programmable square wave is generated by inverting the timer output each time the 8-bit up counter (UC0) matches the value in one of the timer registers TA0REG or TA1REG.

The value set in TA0REG must be smaller than the value set in TA1REG.

Although the up counter for TMRA1 (UC1) is not used in this mode, TA01RUN <TA1RUN> should be set to 1, so that UC1 is set for counting.

Figure 3.7.14 shows a block diagram representing this mode.

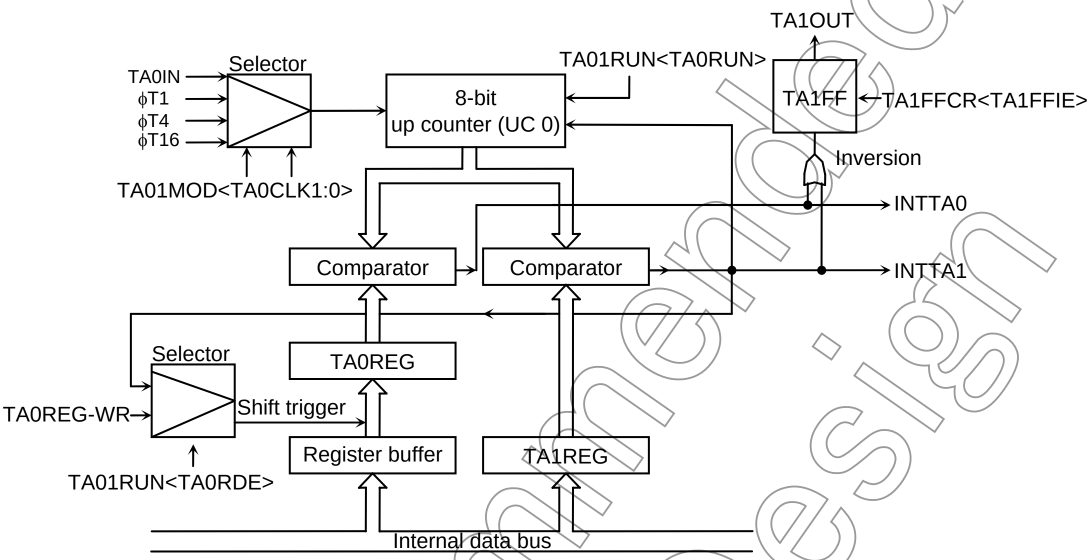


Figure 3.7.14 Block Diagram of 8-Bit PPG Output Mode

If the TA0REG double buffer is enabled in this mode, the value of the register buffer will be shifted into TA0REG each time TA1REG matches UC0.

Use of the double buffer facilitates the handling of low-duty waves (when duty is varied).

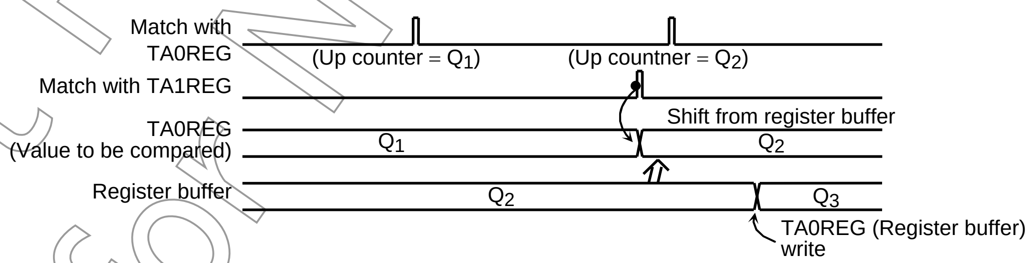
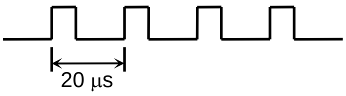


Figure 3.7.15 Operation of Register Buffer

(Example)

To generate 1/4-duty 50 kHz pulses (at fc = 36 MHz):



* Clock state
  - System clock: High-frequency (fc)
  - Clock gear: 1 (fc)
  - Prescaler clock: f_{FPH}

Calculate the value which should be set in the timer register.

To obtain a frequency of 50 kHz, the pulse cycle t should be: t = 1/50 kHz = 20 μs

$\phi T1 = (2^3/fc)s$ (at 36 MHz);

$20\ \mu s \div (2^3/fc)s \approx 90$

Therefore set TA1REG to 90 (5AH)

The duty is to be set to 1/4: $t \times 1/4 = 20\ \mu s \times 1/4 = 5\ \mu s$

$5\ \mu s \div (2^3/fc)s \approx 22$

Therefore, set TA0REG = 22 = 16H.

		7	6	5	4	3	2	1	0	
TA01RUN	←	0	X	X	X	–	0	0	0	Stop TMRA0 and TMRA0, 1 and clear it to 0.
TA01MOD	←	1	0	X	X	X	X	0	1	Set the 8-bit PPG mode, and select ϕT1 as input clock.
TA0REG	←	0	0	0	1	0	1	1	0	Write 16H
TA1REG	←	0	1	0	1	1	0	1	0	Write 5AH
TA1FFCR	←	X	X	X	X	0	1	1	X	Set TA1FF, enabling both inversion and the double buffer.
										Writing 10 provides negative logic pulse.
PAFC2	←	X	X	X	X	–	–	1	–	Set PA1 as the TA1OUT pin.
TA01RUN	←	1	X	X	X	–	1	1	1	Start TMRA0 and TMRA01 counting.

X: Don’t care, –: No change

(4) 8-bit PWM (Pulse width modulation) output mode

This mode is only valid for TMRA0. In this mode, a PWM pulse with the maximum resolution of 8 bits can be output.

When TMRA0 is used the PWM pulse is output on the TA1OUT pin (which is also used as P71). TMRA1 can also be used as an 8-bit timer.

The timer output is inverted when the up counter (UC0) matches the value set in the timer register TA0REG or when 2^n counter overflow occurs (n = 6, 7 or 8 as specified by TA01MOD<PWM01:00>). The up counter UC0 is cleared when 2^n counter overflow occurs.

The following conditions must be satisfied before this PWM mode can be used.

Value set in TA0REG < value set for 2^n counter overflow

Value set in TA0REG ≠ 0

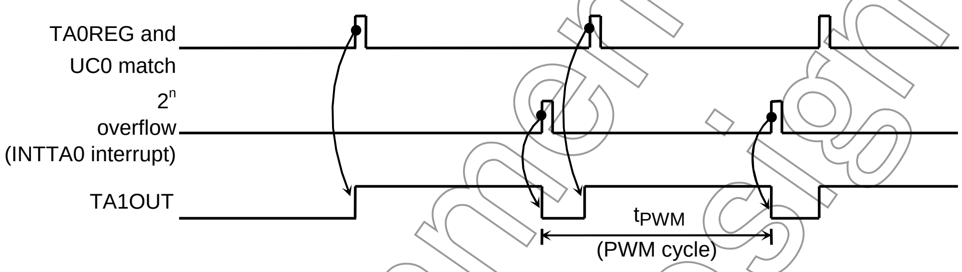


Figure 3.7.16 8-Bit PWM Waveforms

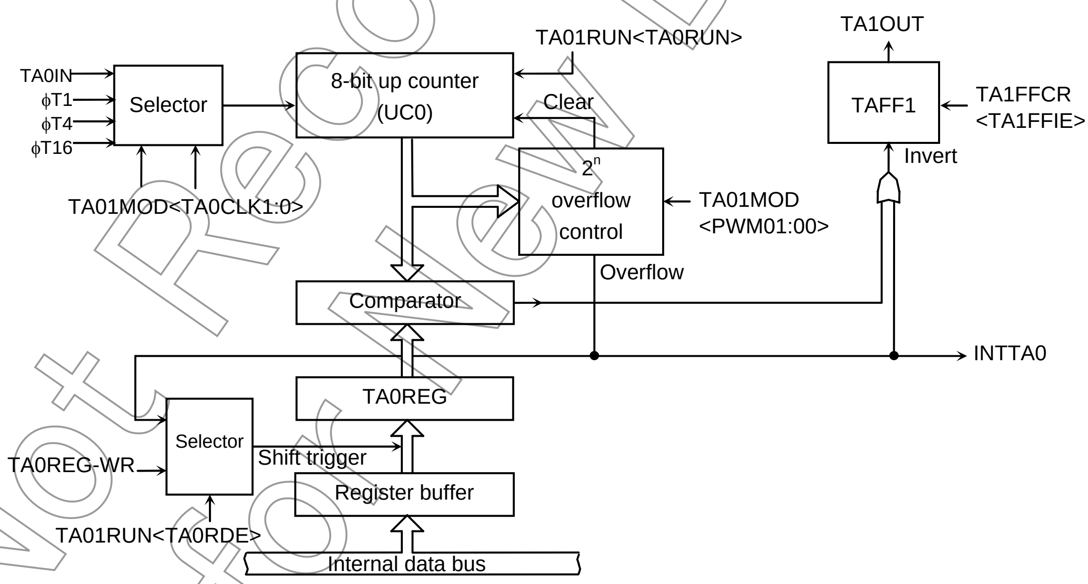


Figure 3.7.17 Block Diagram of 8-Bit PWM Mode

In this mode, the value of the register buffer will be shifted into TA0REG if 2^n overflow is detected when the TA0REG double buffer is enabled.

Use of the double buffer facilitates the handling of low duty ratio waves.

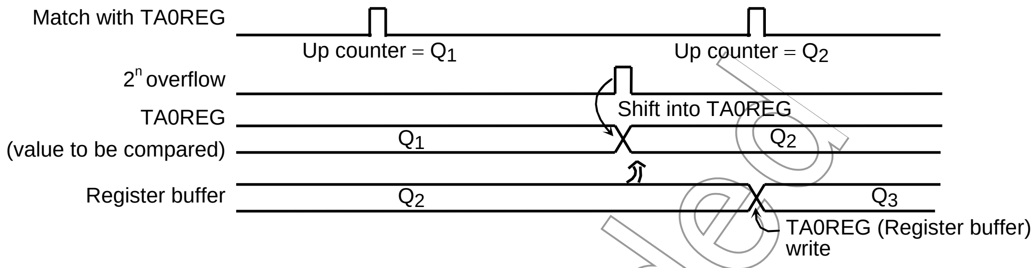
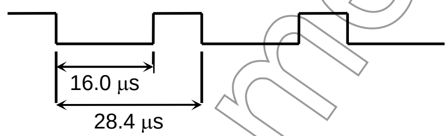


Figure 3.7.18 Register Buffer Operation

Example: To output the following PWM waves on the TA1OUT pin at fc = 16 MHz:



∗ Clock state

- System clock: High-frequency (fc)
- Clock gear: 1 (fc)
- Prescaler clock: f_{FPH}

To achieve a 64.0-μs PWM cycle by setting φT1 to $(2^3/fc)$s (at fc = 36 MHz):

$28.4\ \mu s \div (2^3/fc)s \approx 128 = 2^n$

Therefore n should be set to 7.

Since the low-level period is 16.0 μsec when φT1 = $(2^3/fc)$s,

set the following value for TA0REG:

$16.0\ \mu s \div (2^3/fc)s \approx 72 = 48H$

		MSB 7	6	5	4	3	2	1	LSB 0	
TA01RUN	←	–	X	X	X	–	–	–	0	Stop TMRA0 and clear it to 0.
TA01MOD	←	1	1	1	0	–	–	0	1	Select 8-bit PWM mode (cycle: 2^7) and select φT1 as the input clock.
TA0REG	←	0	1	0	0	1	0	0	0	Write 48H.
TA1FFCR	←	X	X	X	X	1	0	1	X	Clear TA1FF to 0, enable the inversion and double buffer.
PAFC2	←	X	X	X	X	–	–	1	–	Set PA1 and the TA1OUT pin.
TA01RUN	←	1	X	X	X	–	1	–	1	Start TMRA0 counting.

X: Don't care, –: No change

Table 3.7.3 PWM Cycle

at fc = 36 MHz, fs = 32.768 kHz

Select System Clock SYSCR1 <SYSCK>	Select Prescaler Clock SYSCR0 <PRCK1:0>	Gear Value SYSCR1 <GEAR2:0>	PWM Cycle								
			2^6			2^7			2^8		
			φT1	φT4	φT16	φT1	φT4	φT16	φT1	φT4	φT16
1 (fs)	00 (f_{FPH})	XXX	15.6 ms	62.5 ms	250 ms	31.3 ms	125 ms	500 ms	62.5 ms	250 ms	1000 ms
0 (fc)		000 (fc)	14.2 μs	56.8 μs	227 μs	28.4 μs	113 μs	455 μs	56.8 μs	227 μs	910 μs
		001 (fc/2)	28.4 μs	113 μs	455 μs	56.8 μs	227 μs	910 μs	113 μs	455 μs	1820 μs
		010 (fc/4)	56.8 μs	227 μs	910 μs	113 μs	455 μs	1820 μs	227 μs	910 μs	3640 μs
		011 (fc/8)	113 μs	455 μs	1820 μs	227 μs	910 μs	3640 μs	455 μs	1820 μs	7281 μs
		100 (fc/16)	227 μs	910 μs	3640 μs	455 μs	1820 μs	7281 μs	910 μs	3640 μs	14563 μs
	10 (fc/16 clock)	XXX	227 μs	910 μs	3640 μs	455 μs	1820 μs	7281 μs	910 μs	3640 μs	14563 μs

XXX: Don't care

(5) Settings for each mode

Table 3.7.4 shows the SFR settings for each mode.

Table 3.7.4 Timer Mode Setting Registers

Register Name	TA01MOD				TA1FFCR
<Bit Symbol>	<TA01M1:0>	<PWM01:00>	<TA1CLK1:0>	<TA0CLK1:0>	TA1FFIS
Function	Timer Mode	PWM Cycle	Upper Timer Input Clock	Lower Timer Input Clock	Timer F/F Invert Signal Select
8-bit timer × 2 channels	00	–	Lower timer match φT1, φT16, φT256 (00, 01, 10, 11)	External clock φT1, φT4, φT16 (00, 01, 10, 11)	0: Lower timer output 1: Upper timer output
16-bit timer mode	01	–	–	External clock φT1, φT4, φT16 (00, 01, 10, 11)	–
8-bit PPG × 1 channel	10	–	–	External clock φT1, φT4, φT16 (00, 01, 10, 11)	–
8-bit PWM × 1 channel	11	2^6, 2^7, 2^8 (01, 10, 11)	–	External clock φT1, φT4, φT16 (00, 01, 10, 11)	–
8-bit timer × 1 channel	11	–	φT1, φT16 , φT256 (01, 10, 11)	–	Output disabled

–: Don't care

(6) LCDC and MELODY/ALARM circuit supply mode

This function can operate only TMRA3. It can use LCDC and MELODY/ALARM source clock TA3 clock generated by TMRA3. But this function is special mode, without low clock (XTIN, XTOUT) so keep the rule under below.

Operate

a. Clock generate by timer 3

b. Clock supply start (EMCCR0 <TA3LCDE> = 1)

c. Need setup time

d. LCDC or MELODY/ALARM start to operate

STOP

e. LCDC or MELODY/ALARM stop to operate

f. Clock supply cut off (<TA3LCDE> = 0 or <TA3MLDE> = 0)

EMCCR0 (00E3H)

	7	6	5	4	3	2	1	0
Bit symbol	PROTECT	TA3LCDE	AHOLD	TA3MLDE	–	EXTIN	DRVOSCH	DRVOSCL
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	1	1
Function	Protect flag 0: Off 1: On	LCDC source CLK 0: 32 kHz 1: TA3OUT	Address hold 0: Normal 1: Enable	Melody/Alarm source clock. 0: 32 kHz 1: TA3OUT	Always write 0.	1: External clock	fc oscillator driver ability. 1: Normal 0: Weak	fs oscillator driver ability. 1: Normal 0: Weak

3.8 External Memory Extension Function (MMU)

This is MMU function which can expand program/data area to 104 Mbytes by having 4 local areas.

Address pins to external memory are 2 extended address bus pins (EA24, EA25) or 3 extended chip select pins ($\overline{CS2A}$ to $\overline{CS2C}$) in addition to 24 address bus pins (A0 to A23) which are common specification of TLCS-900 and 4 chip select pins ($\overline{CS0}$ to $\overline{CS3}$) output from CS/WAIT controller.

The feature and the recommendation setting method of two types are shown below.

In addition, AH in the table is the value which number address 23 to 16 displayed as hex.

Purpose	Item	(A): For Standard Extended Memory	(B): For Many Pieces Extended Memory
Program ROM	Maximum memory size	16 Mbytes: BANK (16 Mbytes × 1 pcs)	
	Used local area, BANK number	LOCAL2 (AH = C0 to DF: 2 Mbytes × 7 BANK)	
	Setting CS/WAIT	Setup AH = C0 to FF to CS2	Setup AH = 80 to FF to CS2
	Used $\overline{CS}$ pin	$\overline{CS2}$	$\overline{CS2A}$
Data ROM	Maximum memory size	64 Mbytes : BANK (64 Mbytes × 1 pcs)	32 Mbytes : BANK (16 Mbytes × 2 pcs)
	Used local area, BANK number	LOCAL3 (AH = 80 to BF: 4 Mbytes × 16 BANK)	LOCAL3 (AH = 80 to BF: 4 Mbytes × 8 BANK)
	Setting CS/WAIT	Setup AH = 80 to BF to CS3	Setup AH = 80 to FF to CS2
	Used $\overline{CS}$ pins	$\overline{CS3}$, EA24, EA25	$\overline{CS2B}$, $\overline{CS2C}$
Option Program ROM	Maximum memory size	16 Mbytes: BANK (16 Mbytes × 1 pcs)	
	Used local area, BANK number	LOCAL1 (AH = 40 to 5F: 2 Mbytes × 7 BANK)	
	Setting CS/WAIT	Setup AH = 40 to 7F to CS1	
	Used $\overline{CS}$ pin	$\overline{CS1}$	
Data RAM	Maximum memory size	8 Mbytes: BANK (8 Mbytes × 1 pcs)	
	Used local area, BANK number	LOCAL0 (AH = 10 to 1F: 1 Mbyte × 7 BANK)	
	Setting CS/WAIT	Setup AH = 00 to 1F to CS0	Setup AH = 00 to 1F to CS3
	Used $\overline{CS}$ pin	$\overline{CS0}$	$\overline{CS3}$
Extended memory 1	Maximum memory size		2 Mbytes (2 Mbytes × 1 pcs)
	Used local area, BANK number		None
	Setting CS/WAIT		Setup AH = 20 to 3F to CS0
	Used $\overline{CS}$ pin		$\overline{CS0}$
Total memory size		16 M + 64 M + 16 M + 8 M = 104 Mbytes	16 M + 32 M + 16 M + 8 M + 2 M = 74 Mbytes

3.8.1 Recommendable Memory Map

The recommendation logic address memory map at the time of varieties extension memory correspondence is shown in Figure 3.8.1. And a physical-address map is shown in Figure 3.8.2.

However, when memory area is less than 16 Mbytes and is not expanded, please refer to section of CS/WAIT controller. Setting of register in MMU is not necessary.

Since it is being fixed, the address of a local-area cannot be changed.

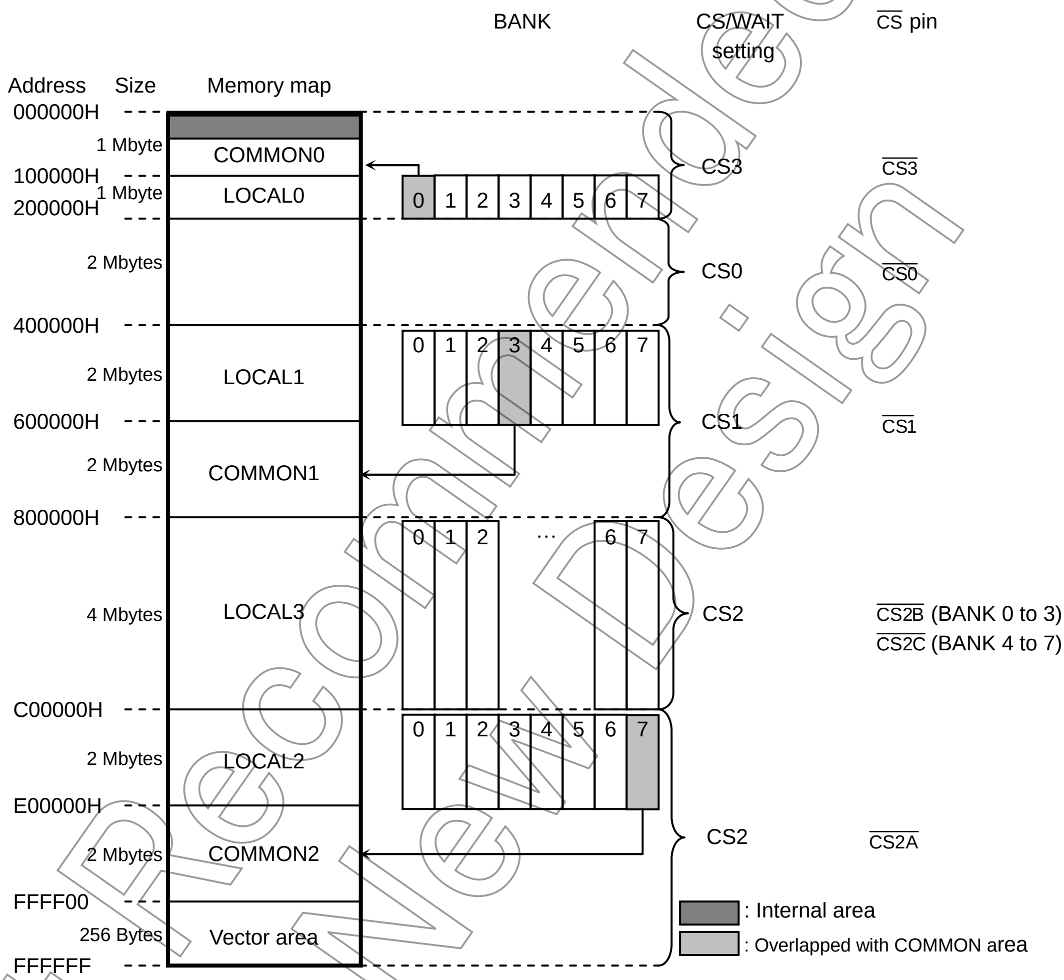


Figure 3.8.1 Logical Address Map

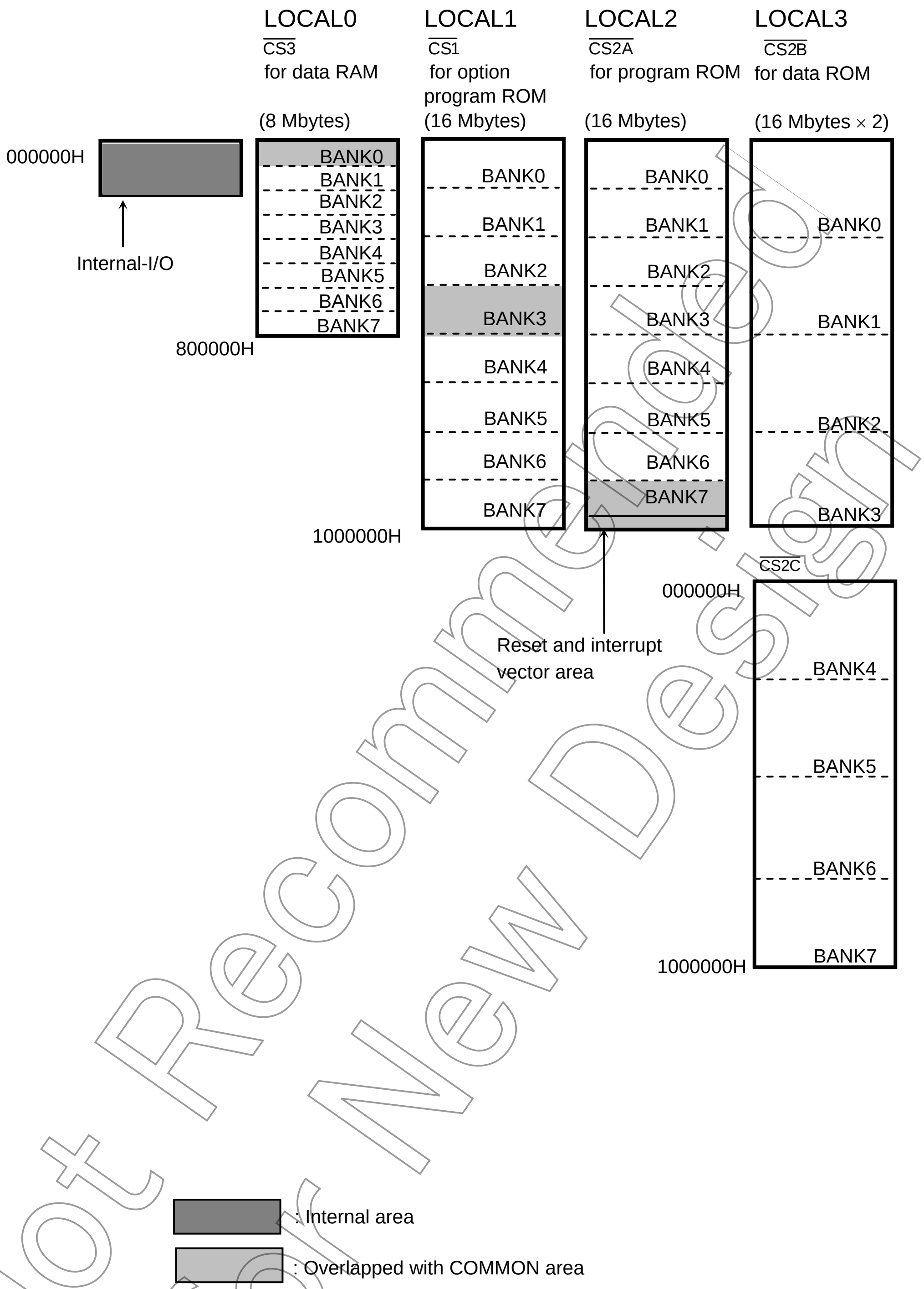


Figure 3.8.2 Physical Address Map

3.8.2 Control Registers

Set a bank setting value and bank enable/disable in each local register in the common area. At this time, also specify the pin function and mapping by the CS/WAIT controller. When the CPU outputs the logical address of the local area, the MMU outputs its physical address to the external address bus pin according to the value in the bank setting register. This enables access to external memory.

LOCAL0 Register

LOCAL0 (0350H)		7	6	5	4	3	2	1	0
	Bit symbol	L0E					L0EA22	L0EA21	L0EA20
	Read/Write	R/W					R/W		
	After reset	0					0	0	0
	Function	BANK for LOCAL0 0: Disable 1: Enable					Setting BANK number for LOCAL0 “000” setting is prohibited because it pretend COMMON 0 area		

LOCAL1 Register

LOCAL1 (0351H)		7	6	5	4	3	2	1	0
	Bit symbol	L1E					L1EA23	L1EA22	L1EA21
	Read/Write	R/W					R/W		
	After reset	0					0	0	0
	Function	BANK for LOCAL1 0: Disable 1: Enable					Setting BANK number for LOCAL1 “001” setting is prohibited because it pretend COMMON 0 area		

LOCAL2 Register

LOCAL2 (0352H)		7	6	5	4	3	2	1	0
	Bit symbol	L2E					L2EA23	L2EA22	L2EA21
	Read/Write	R/W					R/W		
	After reset	0					0	0	0
	Function	BANK for LOCAL2 0: Disable 1: Enable					Setting BANK number for LOCAL2 “111” setting is prohibited because it pretend COMMON 0 area		

LOCAL3 Register

LOCAL3 (0353H)		7	6	5	4	3	2	1	0
	Bit symbol	L3E			–	L3EA25	L3EA24	L3EA23	L3EA22
	Read/Write	R/W			R/W	R/W	R/W	R/W	R/W
	After reset	0			0	0	0	0	0
	Function	BANK for LOCAL3 0: Disable 1: Enable			Always write 0.	0000~0011: $\overline{CS2B}$ 0100~0111: $\overline{CS2C}$ 1000~1111: Set prohibition			

Figure 3.8.3 Register of MMU

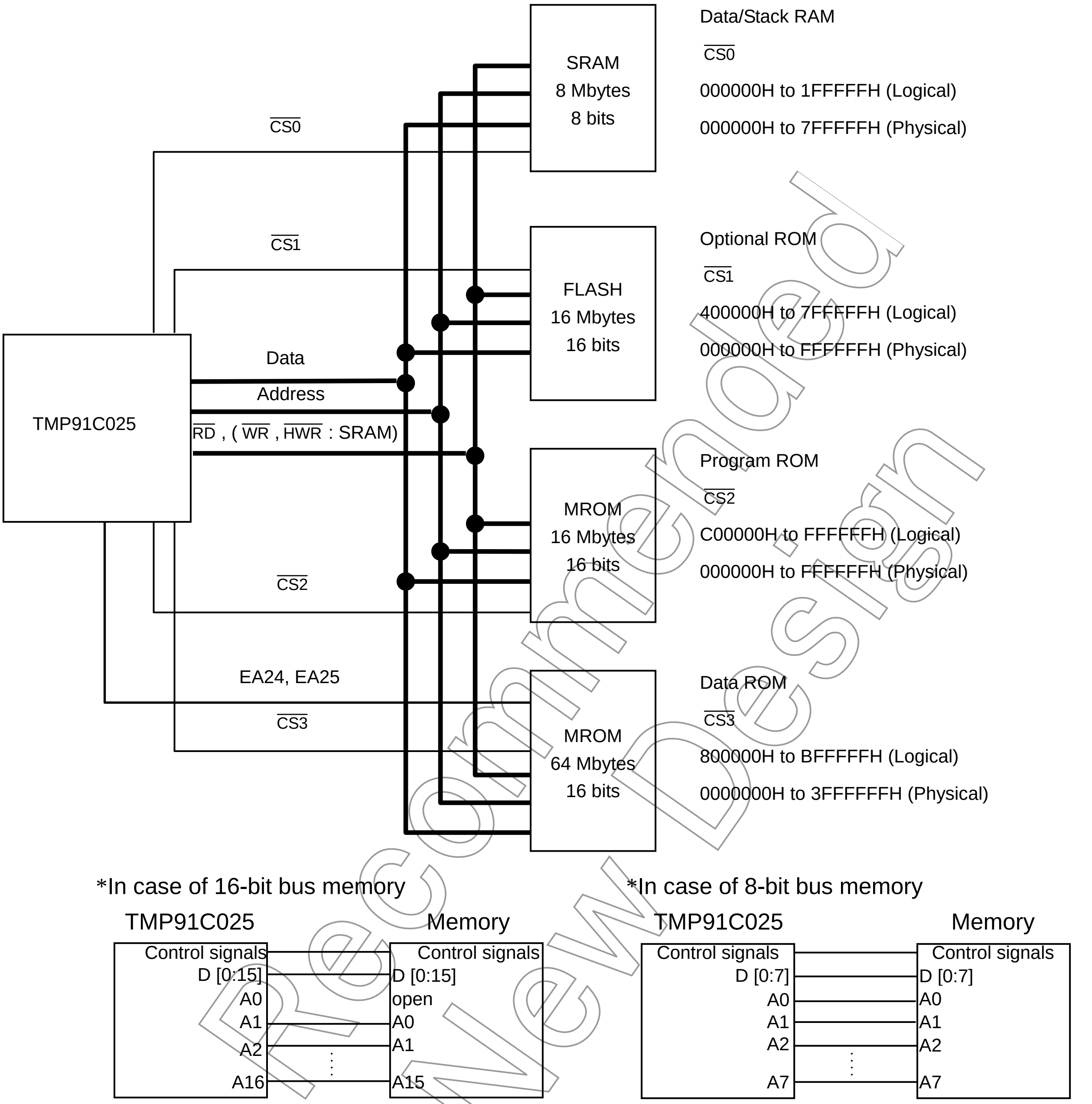


Figure 3.8.4 H/W Setting Example

At Figure 3.8.4, it shows example of connection TMP91C025 and some memories: Program ROM: MROM, 16 Mbytes, Data ROM: MROM, 64 Mbytes, Data RAM: SRAM, 8 Mbytes, 8-bit bus, Option ROM: Flash, 16 Mbytes.

In case of 16-bit bus memory connection, it need to shift 1-bit address bus from TMP91C025 and 8-bit bus case, direct connection address bus from TMP91C025.

In that figure, logical address and physical address are shown. And each memory allot each chip select signal, RAM: $\overline{\text{CS0}}$, FLASH_ROM: $\overline{\text{CS1}}$, Program MROM: $\overline{\text{CS2}}$, Data MROM: $\overline{\text{CS3}}$. In case of this example, as data MROM is 64 Mbytes, this MROM connect to EA24 and EA25.

Initial condition after reset, because TMP91C025 access from CS2 area, CS2 area allots to program ROM. It can set free setting except program ROM.

```
;Initial Setting
;CS0
        LD      (MSAR0), 00H     ; Logical address area: 000000H to 1FFFFFH
        LD      (MAMR0), FFH     ; Logical address size: 2 Mbytes
        LD      (B0CS), 89H      ; Condition: 8-bit, 1 waits (8 Mbytes, SRAM)
;CS1
        LD      (MSAR1), 40H     ; Logical address area: 400000H to 7FFFFFH
        LD      (MAMR1), FFH     ; Logical address size: 4 Mbytes
        LD      (B1CS), 80H      ; Condition: 16-bit, 2 waits (16 Mbytes, Flash ROM)
;CS2
        LD      (MSAR2), C0H     ; Logical address area: C00000H to FFFFFFH
        LD      (MAMR2), 7FH     ; Logical address size: 4 Mbytes
        LD      (B2CS), C3H      ; Condition: 16-bit, 0 waits (16 Mbytes, MROM)
;CS3
        LD      (MSAR3), 80H     ; Logical address area: 800000H to BFFFFFH
        LD      (MAMR3), 7FH     ; Logical address size: 4 Mbytes
        LD      (B3CS), 85H      ; Condition: 16-bit, 3 waits (64 Mbytes, MROM)
;CSX
        LD      (BEXCS), 00H     ; Other: 16-bit, 2 waits (Don't care)
;Port
        LD      (P6FC), 3FH      ; CS0 to CS3, EA24, EA25: port 6 setting
to
```

Figure 3.8.5 Bank Operation S/W Example 1

Secondly, Figure 3.8.5 shows example of initial setting at BANK operation S/W example1 of the above.

Because $\overline{\text{CS0}}$ connect to RAM: 8-bit bus, 8 Mbytes, it need to set 8-bit bus. At this example, it set 1-wait setting. In the same way $\overline{\text{CS1}}$ set to 16-bit bus and 2 waits, $\overline{\text{CS2}}$ set 16-bit bus and 0 waits, $\overline{\text{CS3}}$ set 16-bit bus and 3 waits.

By CS/WAIT controller, each chip selection signal's memory size, don't set actual connect memory size, need to set that logical address size: fitting to each local area. Actual physical address is set by each area's BANK register setting.

CSEX setting of CS/WAIT controller is except above CS0 to CS3's setting.

Finally pin condition is set. Port 60 to 65 set to $\overline{\text{CS0}}$, 1, 2, 3, EA24, EA25.

```
;Bank Operation
;***** /CS2 *****
ORG   000000H                  ; Program ROM: Start address at BANK0 of LOCAL2
ORG   200000H                  ; Program ROM: Start address at BANK1 of LOCAL2
ORG   400000H                  ; Program ROM: Start address at BANK2 of LOCAL2
ORG   600000H                  ; Program ROM: Start address at BANK3 of LOCAL2
ORG   800000H                  ; Program ROM: Start address at BANK4 of LOCAL2
ORG   a00000H                  ; Program ROM: Start address at BANK5 of LOCAL2
ORG   c00000H                  ; Program ROM: Start address at BANK6 of LOCAL2

ORG   E00000H                  ; Program ROM: Start address at BANK7 (= COMMON2) of LOCAL2
                               ; Logical address E00000H to FFFFFFH
                               ; Physical address 0E00000H to 0FFFFFFH
      LD    (LOCAL3), 85H      ; LOCAL3 BANK5 set 14xxxxH
      LDW   HL,(800000H)       ; Load data (5555H) form BANK5 (140000H: Physical address)
                                                           of LOCAL3 (CS3)
      LD    (LOCAL3), 88H      ; LOCAL3 BANK8 set 20xxxxH
      LDW   BC,(800000H)       ; Load data (AAAAH) form BANK8 (200000H: Physical address)
                                                           of LOCAL3 (CS3)
to
ORG   FFFFFFH                  ; Program ROM: End address at BANK7 (= COMMON2) of LOCAL2

;***** /CS3 *****
ORG   0000000H                 ; Data ROM: Start address at BANK0 of LOCAL3
ORG   0400000H                 ; Data ROM: Start address at BANK1 of LOCAL3
ORG   0800000H                 ; Data ROM: Start address at BANK2 of LOCAL3
ORG   0C00000H                 ; Data ROM: Start address at BANK3 of LOCAL3
ORG   1000000H                 ; Data ROM: Start address at BANK4 of LOCAL3
ORG   1400000H                 ; Data ROM: Start address at BANK5 of LOCAL3
      dw      5555H
to
ORG   1800000H                 ; Data ROM: Start address at BANK6 of LOCAL3
ORG   1C00000H                 ; Data ROM: Start address at BANK7 of LOCAL3
ORG   2000000H                 ; Data ROM: Start address at BANK8 of LOCAL3
      dw      AAAAH
to
ORG   2400000H                 ; Data ROM: Start address at BANK9 of LOCAL3
ORG   2800000H                 ; Data ROM: Start address at BANK10 of LOCAL3
ORG   2C00000H                 ; Data ROM: Start address at BANK11 of LOCAL3
ORG   3000000H                 ; Data ROM: Start address at BANK12 of LOCAL3
ORG   3400000H                 ; Data ROM: Start address at BANK13 of LOCAL3
ORG   3800000H                 ; Data ROM: Start address at BANK14 of LOCAL3
ORG   3C00000H                 ; Data ROM: Start address at BANK15 of LOCAL3
ORG   3FFFFFFH                 ; Data ROM: End address at BANK15 of LOCAL3
```

Figure 3.8.6 Bank Operation S/W Example 2

Figure 3.8.6 shows example of data access between one BANK and other BANK is one software example. A dot line square area shows one memory and each dot line square shows $\overline{CS2}$'s program ROM and $\overline{CS3}$'s data ROM. Program start from E00000H address, firstly, write to BANK register of LOCAL3 area upper 5-bit address of access point.

In case of this TMP91C025, because most upper address bit of physical address is EA25, most upper address bit of BANK register is meaningless. 4 bits of upper 5-bit address means 16 BANKs. After setting BANK5, accessing 800000H to BFFFFFH address: Logical local3 address, actually access to physical 1400000H to 1700000H address.

```
;Bank Operation
;***** /CS2 *****
ORG     000000H                     ; Program ROM: Start address at BANK0 of LOCAL2
ORG     200000H                     ; Program ROM: Start address at BANK1 of LOCAL2
        NOP                         ; Operation at BANK1of LOCAL2
to
        JP      E00100H             ; Jump to BANK7 (= COMMON2) of LOCAL2
ORG     400000H                     ; Program ROM: Start address at BANK2 of LOCAL2
ORG     600000H                     ; Program ROM: Start address at BANK3 of LOCAL2
        NOP                         ; Operation at BANK3 of LOCAL2
to
        JP      E00200H             ; Jump to BANK7 (= COMMON2) of LOCAL2
ORG     800000H                     ; Program ROM: Start address at BANK4 of LOCAL2
ORG     a00000H                     ; Program ROM: Start address at BANK5 of LOCAL2
ORG     c00000H                     ; Program ROM: Start address at BANK6 of LOCAL2

!!!! Program Start !!!!
ORG     E00000H                     ; Program ROM: Start address at BANK7 (= COMMON2) of LOCAL2
                                    ; Logical address E00000H to FFFFFFH
                                    ; Physical address 0E00000H to 0FFFFFFH
        LD      (LOCAL2), 81H       ; LOCAL2 BANK1 set 20xxxxH
        JP      C00000H             ; Jump to BANK1 (200000H: Physical address) of LOCAL2
to
ORG     E00100H
        LD      (LOCAL2), 83H       ; LOCAL2 BANK3 set 60xxxxH
        JP      C00000H             ; Jump to BANK3 (600000H: Physical address) of LOCAL2
to
ORG     E00200H
        LD      (LOCAL1),84H        ; LOCAL1 BANK4 set 80xxxxH
        JP      400000H             ; Jump to BANK4 (800000H: Physical address) of LOCAL1
ORG     FFFFFFH                     ; Program ROM: End address at BANK7(= COMMON2) of LOCAL2
```

```
;***** /CS1 *****
ORG     000000H                     ; Program ROM: Start address at BANK0 of LOCAL1
ORG     200000H                     ; Program ROM: Start address at BANK1 of LOCAL1
ORG     400000H                     ; Program ROM: Start address at BANK2 of LOCAL1
ORG     600000H                     ; Program ROM: Start address at BANK3 (= COMMON1) of LOCAL1
        LD      (LOCAL1),87H        ; LOCAL1 BANK7 set E0xxxxH
        JP      400000H             ; Jump to BANK7 (E00000H: Physical address) of LOCAL1
ORG     800000H                     ; Program ROM: Start address at BANK4 of LOCAL1
        NOP                         ; Operation at BANK4 of LOCAL1
to
        JP      600000H             ; Jump to BANK3 (= COMMON1) of LOCAL1
ORG     a00000H                     ; Program ROM: Start address at BANK5 of LOCAL1
ORG     c00000H                     ; Program ROM: Start address at BANK6 of LOCAL1
ORG     E00000H                     ; Program ROM: Start address at BANK7 of LOCAL1
        LD      (LOCAL1),80H        ; LOCAL1 BANK0 set 00xxxxH
        JP      400000H             ; Jump to BANK0 (000000H: Physical address) of LOCAL1

It's prohibiting to set other BANK setting in except common area Program run away.

ORG     FFFFFFH                     ; Program ROM: End address at BANK7 of LOCAL1
```

Figure 3.8.7 Bank Operation S/W Example 3

At bank operation S/W Example 3 of the above, Figure 3.8.7 shows example of program jump.

In the same way with before example, two dot line squares show each $\overline{CS2}$'s program ROM and $\overline{CS1}$'s option ROM. Program start from E00000H common address, firstly, write to BANK register of LOCAL2 area upper 3-bit address of jumping point.

After setting BANK1, jumping C00000H to DFFFFFH address: logical local2 address, actually jump to physical 2000000H to 3FFFFFH address. When return to common area, it can only jump to E00000H to FFFFFFH without writing to BANK register of LOCAL2 area.

By a way of setting of BANK register, the setting that BANK address and common address conflict with is possible. When two kinds or more logical addresses to show common area exist, management of BANK is confused. We recommends not using the BANK setting, BANK address and common address conflict with.

When it jumps to one memory from other different memory, it can set same as the last time setting. It needs to write to BANK register of LOCAL1 area upper 3-bit address of jumping point. After setting BANK4, jumping 400000H to 5FFFFFH address: logical local1 address, actually jump to physical 8000000H to 9FFFFFH address.

It is a mark paid attention to here, it needs to go by way of common area by all means when moves from a bank to a bank. In other words, it must write to BANK register only in common area and it is prohibit writing the BANK register in BANK area. If it modify the BANK register's data in BANK area, program runaway.

3.9 Serial Channels

TMP91C025 includes 2 serial I/O channels. For both channels either UART mode (Asynchronous transmission) or I/O Interface mode (Synchronous transmission) can be selected.

- I/O interface mode —— Mode 0: For transmitting and receiving I/O data using the synchronizing signal SCLK for extending I/O.
- UART mode
  - Mode 1: 7-bit data
  - Mode 2: 8-bit data
  - Mode 3: 9-bit data

In mode 1 and mode 2 a parity bit can be added. mode 3 has a wakeup function for making the master controller start slave controllers via a serial link (A multi-controller system).

Figure 3.9.2, Figure 3.9.3 are block diagrams for each channel.

Serial channels 0 and 1 can be used independently.

Both channels operate in the same fashion except for the following points; hence only the operation of channel 0 is explained below.

Table 3.9.1 Differences between Channels 0 to 1

	Channel 0	Channel 1
Pin name	TXD0 (PC0) RXD0 (PC1) $\overline{\text{CTS0}}$ /SCLK0 (PC2)	TXD1 (PC3) RXD1 (PC4) $\overline{\text{CTS1}}$/SCLK1 (PC5)
IrDA mode	Yes	No

This chapter contains the following sections:

3.9.1 Block Diagrams
3.9.2 Operation of Each Circuit
3.9.3 SFRs
3.9.4 Operation in Each Mode
3.9.5 Support for IrDA

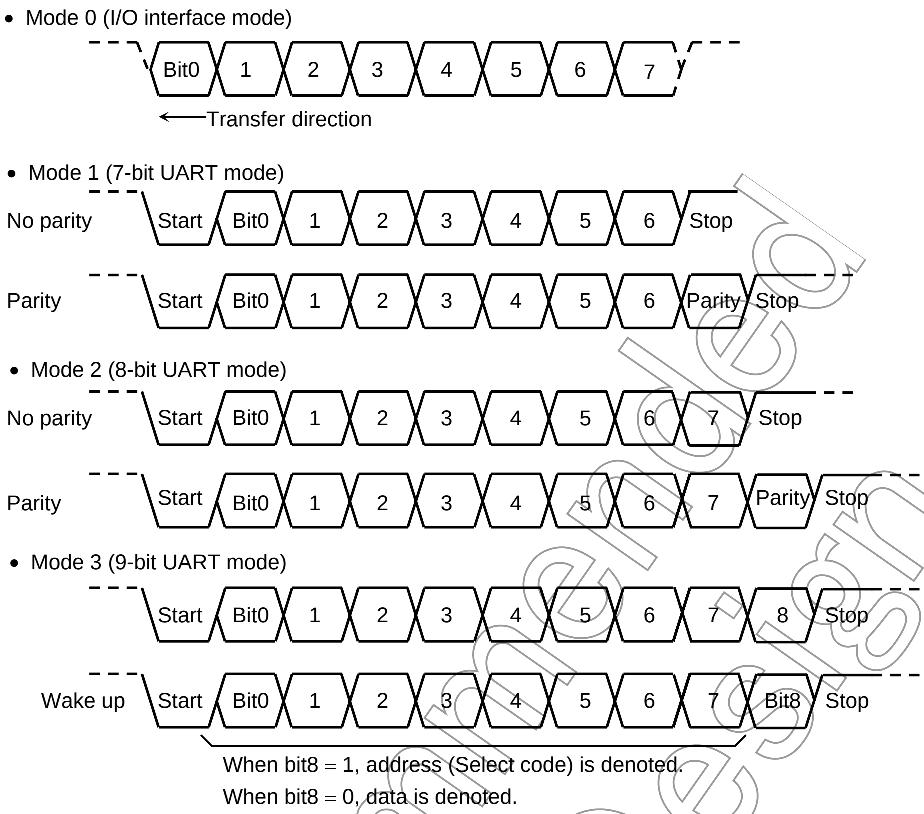


Figure 3.9.1 Data Formats

3.9.1 Block Diagrams

Figure 3.9.2 is a block diagram representing serial channel 0.

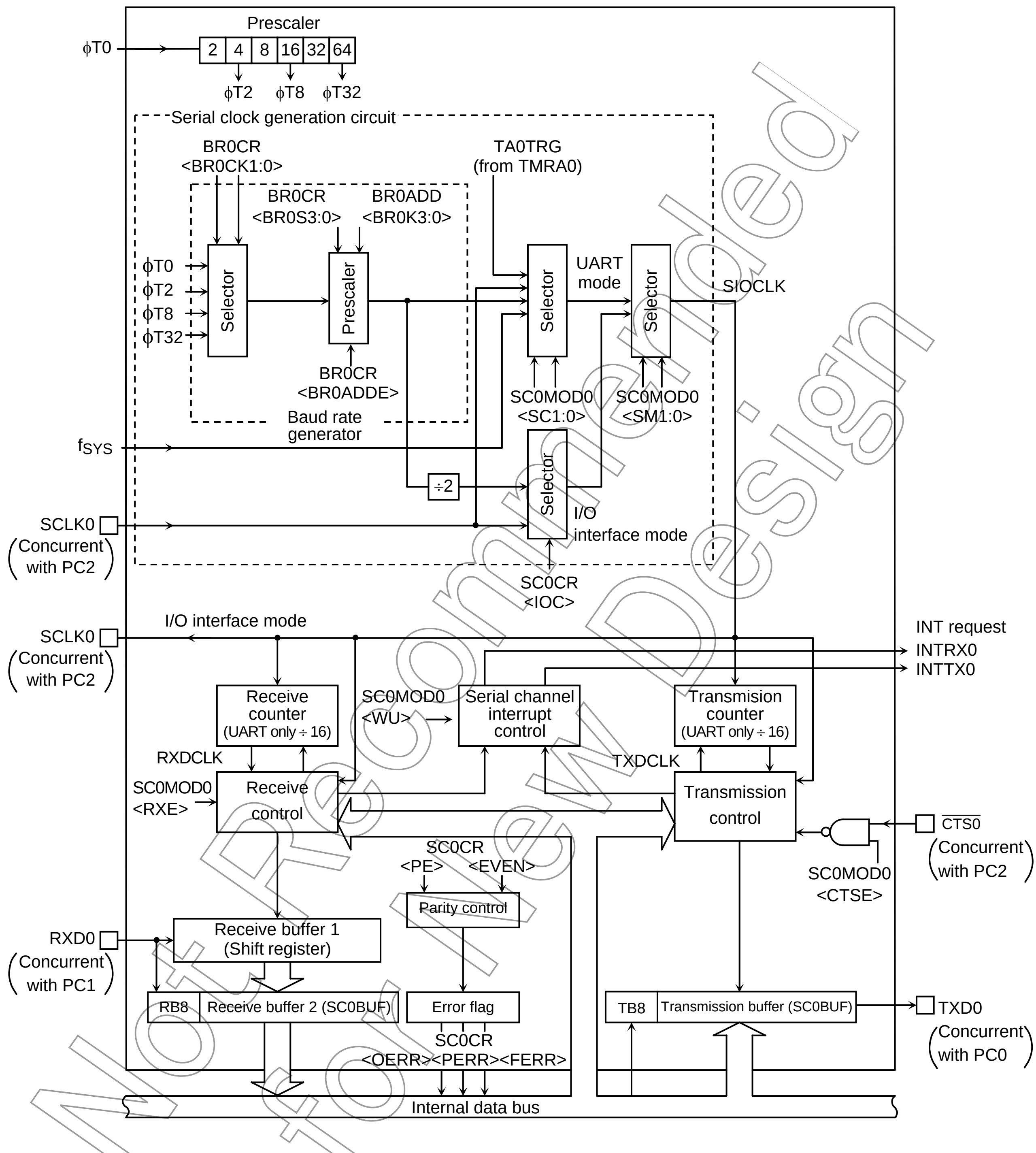


Figure 3.9.2 Block Diagram of the Serial Channel 0 (SIO0)

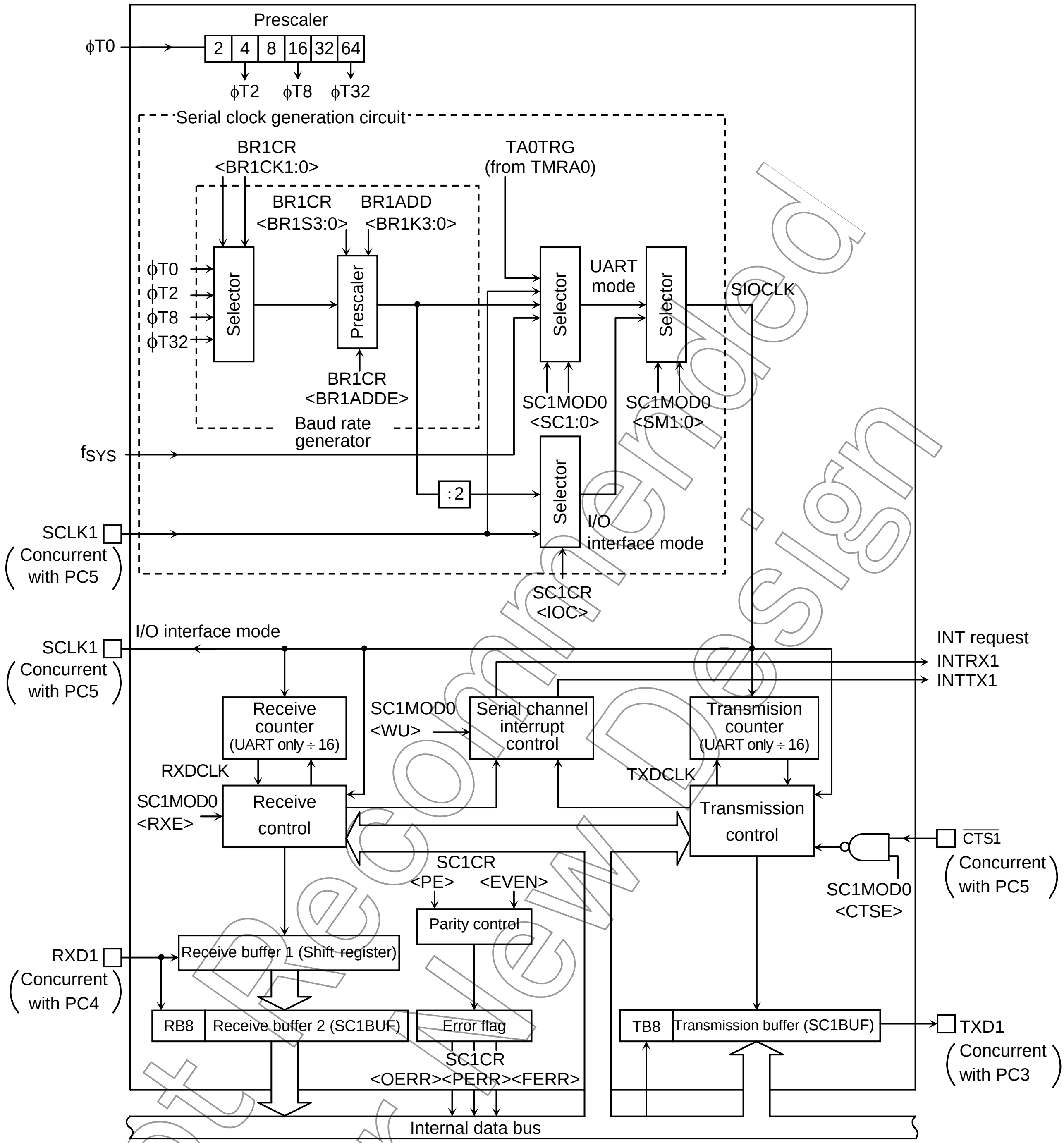


Figure 3.9.3 Block Diagram of the Serial Channel 1 (SIO1)

3.9.2 Operation of Each Circuit

(1) Prescaler

There is a 6-bit prescaler for generating a clock to SIO0. The clock selected using SYSCR<PRCK1:0> is divided by 4 and input to the prescaler as ϕT0. The prescaler can be run by selecting the baud rate generator as the serial transfer clock.

Table 3.9.2 shows prescaler clock resolution into the baud rate generator.

Table 3.9.2 Prescaler Clock Resolution to Baud Rate Generator

Select System Clock <SYSCK>	Select Prescaler Clock <PRCK1:0>	Gear Value <GEAR2:0>	Prescaler Output Clock Resolution			
			ϕT0	ϕT2	ϕT8	ϕT32
1 (fs)	00 (f_{FPH})	XXX	2^2/fs	2^4/fs	2^6/fs	2^8/fs
0 (fc)		000 (fc)	2^2/fc	2^4/fc	2^6/fc	2^8/fc
		001 (fc/2)	2^3/fc	2^5/fc	2^7/fc	2^9/fc
		010 (fc/4)	2^4/fc	2^6/fc	2^8/fc	2^{10}/fc
		011 (fc/8)	2^5/fc	2^7/fc	2^9/fc	2^{11}/fc
		100 (fc/16)	2^6/fc	2^8/fc	2^{10}/fc	2^{12}/fc
	10 (fc/16 clock)	XXX	–	2^8/fc	2^{10}/fc	2^{12}/fc

X: Don’t care, –: Cannot be used

The baud rate generator selects between 4 clock inputs: ϕT0, ϕT2, ϕT8, and ϕT32 among the prescaler outputs.

(2) Baud rate generator

The baud rate generator is a circuit which generates transmission and receiving clocks which determine the transfer rate of the serial channels.

The input clock to the baud rate generator, ϕT0, ϕT2, ϕT8 or ϕT32, is generated by the 6-bit prescaler which is shared by the timers. One of these input clocks is selected using the BR0CR<BR0CK1:0> field in the baud rate generator control register.

The baud rate generator includes a frequency divider, which divides the frequency by 1 or N + (16 – K)/16 to 16 values, determining the transfer rate.

The transfer rate is determined by the settings of BR0CR<BR0ADDE, BR0S3:0> and BR0ADD<BR0K3:0>.

- In UART mode

(1) When BR0CR<BR0ADDE> = 0

The settings BR0ADD<BR0K3:0> are ignored. The baud rate generator divides the selected prescaler clock by N, which is set in BR0CK<BR0S3:0>. (N = 1, 2, 3 ... 16)

(2) When BR0CR<BR0ADDE> = 1

The N + (16 – K)/16 division function is enabled. The baud rate generator divides the selected prescaler clock by N + (16 – K)/16 using the value of N set in BR0CR <BR0S3:0> (N = 2, 3 ... 15) and the value of K set in BR0ADD<BR0K3:0> (K = 1, 2, 3 ... 15)

Note: If N = 1 or N = 16, the N + (16 – K)/16 division function is disabled. Set BR0CR <BR0ADDE> to 0.

- In I/O interface mode

The N + (16 – K)/16 division function is not available in I/O interface mode. Set BR0CR<BR0ADDE> to 0 before dividing by N.

The method for calculating the transfer rate when the baud rate generator is used is explained below.

- In UART mode

$$\text{Baud rate} = \frac{\text{Input clock of baud rate generator}}{\text{Frequency divider for baud rate generator}} \div 16$$

- In I/O interface mode

$$\text{Baud rate} = \frac{\text{Input clock of baud rate generator}}{\text{Frequency divider for baud rate generator}} \div 2$$

- Integer divider (N divider)

  For example, when the source clock frequency (fc) = 12.288 MHz, the input clock frequency = φT2 (fc/16), the frequency divider N (BR0CR<BR0S3:0>) = 5, and BR0CR<BR0ADDE> = 0, the baud rate in UART mode is as follows:

  ∗ Clock state
  - System clock: High-frequency (fc)
  - Clock gear: 1 (fc)
  - Prescaler clock: System clock

$$\text{Baud rate} = \frac{fc/16}{5} \div 16$$

$$= 12.288 \times 10^{6} \div 16 \div 5 \div 16 = 9600 \text{ (bps)}$$

Note: The N + (16 – K)/16 division function is disabled and setting BR0ADD<BR0K3:0> is invalid.

- N + (16 – K)/16 divider (UART mode only)

  Accordingly, when the source clock frequency (fc) = 4.8 MHz, the input clock frequency = φT0, the frequency divider N (BR0CR<BR0S3:0>) = 7, K (BR0ADD<BR0K3:0>) = 3, and BR0CR<BR0ADDE> = 1, the baud rate in UART Mode is as follows:

  ∗ Clock state
  - System clock: High-frequency (fc)
  - Clock gear: 1 (fc)
  - Prescaler clock: System clock

$$\text{Baud rate} = \frac{fc/4}{7 + (16 - 3)/16} \div 16$$

$$= 4.8 \times 10^{6} \div 4 \div (7 + 13/16) \div 16 = 9600 \text{ (bps)}$$

Table 3.9.3 show examples of UART mode transfer rates.

Additionally, the external clock input is available in the serial clock. (Serial channels 0, 1). The method for calculating the baud rate is explained below:

- In UART mode

  Baud rate = External clock input frequency ÷ 16

  It is necessary to satisfy (External clock input cycle) ≥ 4/fc

- In I/O interface mode

  Baud rate = External clock input frequency

  It is necessary to satisfy (External clock input cycle) ≥ 16/fc

Table 3.9.3 Transfer Rate Selection (when baud rate generator is used and BR0CR<BR0ADDE> = 0)

Unit (kbps)

fc [MHz]	Input Clock / Frequency Divider N (BR0CR<BR0S3:0>)	ϕT0	ϕT2	ϕT8	ϕT32
9.830400	2	76.800	19.200	4.800	1.200
↑	4	38.400	9.600	2.400	0.600
↑	8	19.200	4.800	1.200	0.300
↑	0	9.600	2.400	0.600	0.150
12.288000	5	38.400	9.600	2.400	0.600
↑	A	19.200	4.800	1.200	0.300
14.745600	2	115.200	28.800	7.200	1.800
↑	3	76.800	19.200	4.800	1.200
↑	6	38.400	9.600	2.400	0.600
↑	C	19.200	4.800	1.200	0.300
19.6608	1	307.200	76.800	19.200	4.800
↑	2	153.600	38.400	93.600	2.400
↑	4	76.800	19.10	4.800	1.200
↑	8	38.400	9.600	2.400	0.600
↑	10	19.200	4.800	1.200	0.300
22.1184	3	115.200	28.800	7.200	1.800
24.576	1	384.000	96.000	24.000	6.000
↑	2	192.000	48.000	12.000	3.000
↑	4	96.000	24.000	6.000	1.500
↑	5	76.800	19.200	4.800	1.200
↑	8	48.000	12.000	3.000	0.750
↑	A	38.400	9.600	2.400	0.600
↑	10	24.000	6.000	1.500	0.375
27.0336	B	38.400	9.600	2.400	0.600
29.4912	1	460.800	115.200	28.800	7.200
↑	3	153.600	38.400	9.600	2.400
↑	4	115.200	28.800	7.200	1.800
↑	6	76.800	19.200	4.800	1.200
↑	9	51.200	12.800	3.200	1.800
↑	C	38.400	9.600	2.400	1.600
↑	F	30.720	7.680	1.920	1.480
↑	10	28.800	7.200	1.800	0.450
31.9488	D	38.400	9.600	2.400	0.600
34.4064	7	76.800	19.200	4.800	1.200

Note 1: Transfer rates in I/O interface mode are eight times faster than the values given above.

Note 2: The values in this table are calculated for when fc is selected as the system clock, the clock gear is set for fc/1 and the system clock is the prescaler clock input f_{FPH}.

Timer out clock (TA0TRG) can be used for source clock of UART mode only.

Calculation method the frequency of TA0TRG

Frequency of TA0TRG = Baud rate × 16

Note: The TMRA0 match detect signal cannot be used as the transfer clock in I/O interface mode.

(3) Serial clock generation circuit

This circuit generates the basic clock for transmitting and receiving data.

- In I/O interface mode

  In SCLK output mode with the setting SC0CR<IOC> = 0, the basic clock is generated by dividing the output of the baud rate generator by 2, as described previously.

  In SCLK input mode with the setting SC0CR<IOC> = 1, the rising edge or falling edge will be detected according to the setting of the SC0CR<SCLKS> register to generate the basic clock.

- In UART mode

  The SC0MOD0<SC1:0> setting determines whether the baud rate generator clock, the internal system clock f_{SYS}, the match detect signal from timer TMRA0 or the external clock (SCLK0) is used to generate the basic clock SIOCLK.

(4) Receiving counter

The receiving counter is a 4-bit binary counter used in UART mode which counts up the pulses of the SIOCLK clock. It takes 16 SIOCLK pulses to receive 1 bit of data; each data bit is sampled three times – on the 7th, 8th and 9th clock cycles.

The value of the data bit is determined from these three samples using the majority rule.

For example, if the data bit is sampled respectively as 1, 0 and 1 on 7th, 8th and 9th clock cycles, the received data bit is taken to be 1. A data bit sampled as 0, 0 and 1 is taken to be 0.

(5) Receiving control

- In I/O interface mode

  In SCLK output mode with the setting SC0CR<IOC> = 0, the RXD0 signal is sampled on the rising or falling edge of the shift clock which is output on the SCLK0 pin, according to the SC0CR<SCLKS> setting.

  In SCLK input mode with the setting SC0CR<IOC> = 1, the RXD0 signal is sampled on the rising or falling edge of the SCLK0 input, according to the SC0CR<SCLKS> setting.

- In UART mode

  The receiving control block has a circuit which detects a start bit using the majority rule. Received bits are sampled three times; when two or more out of three samples are 0, the bit is recognized as the start bit and the receiving operation commences.

  The values of the data bits that are received are also determined using the majority rule.

(6) The receiving buffers

To prevent overrun errors, the receiving buffers are arranged in a double-buffer structure.

Received data is stored one bit at a time in receiving buffer 1 (which is a shift register). When 7 or 8 bits of data have been stored in receiving buffer 1, the stored data is transferred to receiving buffer 2 (SC0BUF); this cause an INTRX0 interrupt to be generated. The CPU only reads receiving buffer 2 (SC0BUF). Even before the CPU reads receiving buffer 2 (SC0BUF), the received data can be stored in receiving buffer 1. However, unless receiving buffer 2 (SC0BUF) is read before all bits of the next data are received by receiving buffer 1, an overrun error occurs. If an overrun error occurs, the contents of receiving buffer 1 will be lost, although the contents of receiving buffer 2 and SC0CR<RB8> will be preserved.

SC0CR<RB8> is used to store either the parity bit – added in 8-bit UART mode – or the most significant bit (MSB) – in 9-bit UART mode.

In 9-bit UART mode the wake-up function for the slave controller is enabled by setting SC0MOD0<WU> to 1; in this mode INTRX0 interrupts occur only when the value of SC0CR<RB8> is 1.

(7) Transmission counter

The transmission counter is a 4-bit binary counter which is used in UART mode and which, like the receiving counter, counts the SIOCLK clock pulses; a TXDCLK pulse is generated every 16 SIOCLK clock pulses.

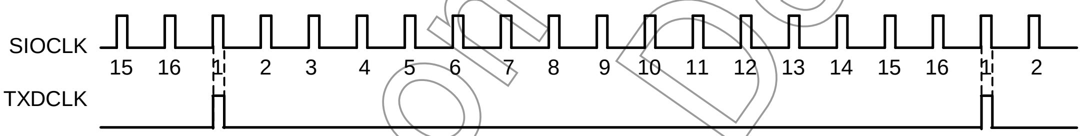


Figure 3.9.4 Generation of the Transmission Clock

(8) Transmission controller

- In I/O interface mode

  In SCLK output mode with the setting SC0CR<IOC> = 0, the data in the transmission buffer is output one bit at a time to the TXD0 pin on the rising or falling edge of the shift clock which is output on the SCLK0 pin, according to the SC0CR<SCLKS> setting.

  In SCLK input mode with the setting SC0CR<IOC> = 1, the data in the transmission buffer is output one bit at a time on the TXD0 pin on the rising or falling edge of the SCLK0 input, according to the SC0CR<SCLKS> setting.

- In UART mode

  When transmission data sent from the CPU is written to the transmission buffer, transmission starts on the rising edge of the next TXDCLK, generating a transmission shift clock TXDSFT.

Handshake function

Use of $\overline{\text{CTS}}$ pin allows data can be sent in units of one frame; thus, Overrun errors can be avoided. The handshake functions is enabled or disabled by the SC0MOD<CTSE> setting.

When the $\overline{\text{CTS0}}$ pin foes high on completion of the current data send, data transmission is halted until the $\overline{\text{CTS0}}$ pin foes low again. However, the INTTX0 interrupt is generated, it requests the next data send to the CPU. The next data is written in the transmission buffer and data sending is halted.

Though there is no $\overline{\text{RTS}}$ pin, a handshake function can be easily configured by setting any port assigned to be the $\overline{\text{RTS}}$ function. The $\overline{\text{RTS}}$ should be output high to request send data halt after data receive is completed by software in the RXD interrupt routine.

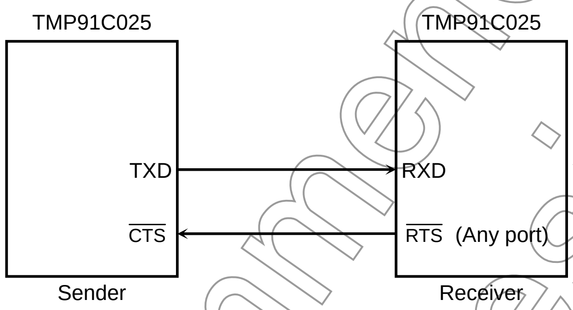
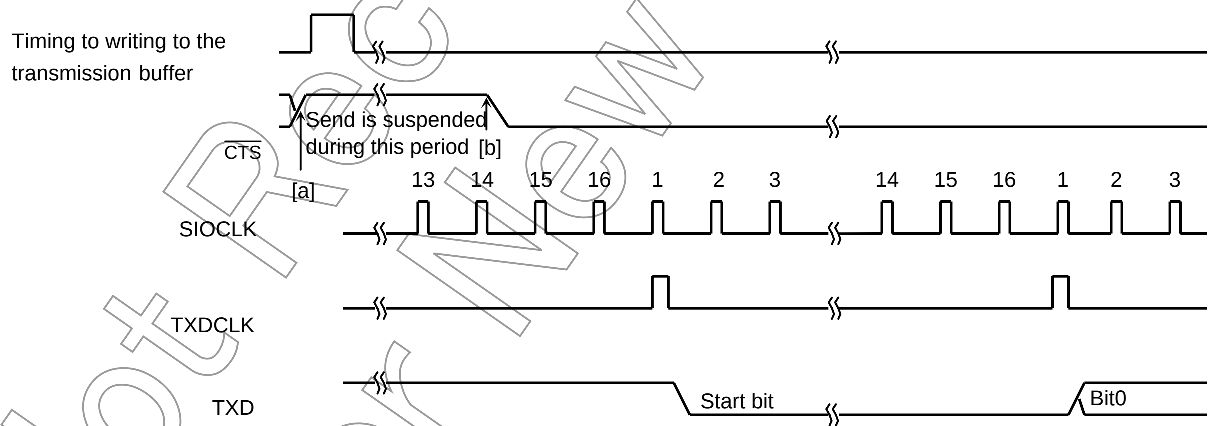


Figure 3.9.5 Handshake Function



Note 1: If the $\overline{\text{CTS}}$ signal goes high during transmission, no more data will be sent after completion of the current transmission.

Note 2: Transmission starts on the first falling edge of the TXDCLK clock after the $\overline{\text{CTS}}$ signal has fallen.

Figure 3.9.6 $\overline{\text{CTS}}$ (Clear to send) Timing

(9) Transmission buffer

The transmission buffer (SC0BUF) shifts out and sends the transmission data written from the CPU form the least significant bit (LSB) in order. When all the bits are shifted out, the transmission buffer becomes empty and generates an INTTX0 interrupt.

(10) Parity control circuit

When SC0CR<PE> in the serial channel control register is set to 1, it is possible to transmit and receive data with parity. However, parity can be added only in 7-bit UART mode or 8-bit UART mode. The SC0CR<EVEN> field in the serial channel control register allows either even or odd parity to be selected.

In the case of transmission, parity is automatically generated when data is written to the transmission buffer SC0BUF. The data is transmitted after the parity bit has been stored in SC0BUF<TB7> in 7-bit UART mode or in SC0MOD0<TB8> in 8-bit UART mode. SC0CR<PE> and SC0CR<EVEN> must be set before the transmission data is written to the transmission buffer.

In the case of receiving, data is shifted into receiving buffer 1, and the parity is added after the data has been transferred to receiving buffer 2 (SC0BUF), and then compared with SC0BUF<RB7> in 7-bit UART mode or with SC0CR<RB8> in 8-bit UART mode. If they are not equal, a parity error is generated and the SC0CR<PERR> flag is set.

(11) Error flags

Three error flags are provided to increase the reliability of data reception.

1. Overrun error <OERR>

   If all the bits of the next data item have been received in receiving buffer 1 while valid data still remains stored in receiving buffer 2 (SC0BUF), an overrun error is generated.
   The below is a recommended flow when the overrun-error is generated.

   (INTRX interrupt routine)

   1) Read receiving buffer

   2) Read error flag

   3) If <OERR> = 1

      then

      a) Set to disable receiving (Write 0 to SC0MOD0<RXE>)

      b) Wait to terminate current frame

      c) Read receiving buffer

      d) Read error flag

      e) Set to enable receiving (Write 1 to SC0MOD0<RXE>)

      f) Request to transmit again

   4) Other

2. Parity error <PERR>

   The parity generated for the data shifted into receiving buffer 2 (SC0BUF) is compared with the parity bit received via the RXD pin. If they are not equal, a Parity error is generated.

3. Framing error <FERR>

   The stop bit for the received data is sampled three times around the center. If the majority of the samples are 0, a framing error is generated.

(12) Timing generation

a. In UART mode

Receiving

Mode	9 Bits	8 Bits + Parity	8 Bits, 7 Bits + Parity, 7 Bits
Interrupt Timing	Center of last bit. (Bit8)	Center of last bit. (Parity bit)	Center of stop bit.
Framing Error Timing	Center of stop bit.	Center of stop bit.	Center of stop bit.
Parity Error Timing	−	Center of last bit. (Parity bit)	Center of stop bit.
Overrun Error Timing	Center of last bit. (Bit8)	Center of last bit. (Parity bit)	Center of stop bit.

Note: In 9-Bit and 8-Bit+Parity mode, interrupts coincide with the ninth bit pulse.Thus, when servicing the interrupt, it is necessary to wait for a 1-bit period (to allow the stop bit to be transferred) to allow checking for a framing error.

Transmitting

Mode	9 Bits	8 Bits + Parity	8 Bits, 7 Bits + Parity, 7 Bits
Interrupt Timing	Just before stop bit is transmitted.	Just before stop bit is transmitted.	Just before stop bit is transmitted.

b. I/O interface

Transmission Interrupt Timing	SCLK output mode	Immediately after last bit data. (See Figure 3.9.19.)
	SCLK input mode	Immediately after rise of last SCLK signal rising mode, or immediately after fall in falling mode. (See Figure 3.9.20.)
Receiving Interrupt Timing	SCLK output mode	Timing used to transfer received to data receive buffer 2 (SC0BUF) (e.g. immediately after last SCLK). (See Figure 3.9.21.)
	SCLK input mode	Timing used to transfer received data to receive buffer 2 (SC0BUF) (e.g. immediately after last SCLK). (See Figure 3.9.22.)

3.9.3 SFRs

		7	6	5	4	3	2	1	0
SC0MOD0 (0202H)	Bit symbol	TB8	CTSE	RXE	WU	SM1	SM0	SC1	SC0
	Read/Write	R/W							
	After reset	0	0	0	0	0	0	0	0
	Function	Transfer data bit8.	Hand shake 0: CTS disable 1: CTS enable	Receive function. 0: Receive disable 1: Receive enable	Wakeup function. 0: Disable 1: Enable	Serial transmission mode. 00: I/O interface mode 01: 7-bit UART mode 10: 8-bit UART mode 11: 9-bit UART mode		Serial transmission clock. (UART) 00: TMRA0 trigger 01: Baud rate generator 10: Internal clock f_{SYS} 11: External clcok (SCLK0 input)	

Serial transmission clock source (UART)

00	Timer TMRA0 match detect signal
01	Baud rate generator
10	Internal clock f_{SYS}
11	External clock (SCLK0 input)

Note: The clock selection for the I/O interface mode is controlled by the serial bontrol register (SC0CR).

Serial transmission mode

00	I/O interface mode	
01	UART mode	7-bit mode
10		8-bit mode
11		9-bit mode

Wakeup function

	9-bit UART	Other modes
0	Interrupt generated when data is received	Don't care
1	Interrupt generated only when SC0CR<RB8> = 1	

Receiving function

0	Receive disabled
1	Receive enabled

Handshake function ($\overline{CTS}$ pin) Enable

0	Disabled (Always transferable)
1	Enabled

Transmission data bit8

Figure 3.9.7 Serial Mode Control Register (SIO0, SC0MOD0)

SC1MOD0
(020AH)

	7	6	5	4	3	2	1	0
Bit symbol	TB8	CTSE	RXE	WU	SM1	SM0	SC1	SC0
Read/Write	R/W							
After reset	0	0	0	0	0	0	0	0
Function	Transfer data bit8.	Hand shake 0: CTS disable 1: CTS enable	Receive function. 0: Receive disable 1: Receive enable	Wakeup function. 0: Disable 1: Enable	Serial transmission mode. 00: I/O interface mode 01: 7-bit UART mode 10: 8-bit UART mode 11: 9-bit UART mode		Serial transmission clock. (UART) 00: TMRA0 trigger 01: Baud rate generator 10: Internal clock f_{SYS} 11: External clcok (SCLK1 input)	

Serial transmission clock source (for UART)

00	Timer TMRA0 match detect signal
01	Baud rate generator
10	Internal clock f_{SYS}
11	External clock (SCLK1 input)

Serial transmission mode

00	I/O Interface Mode	
01	UART mode	7-bit mode
10		8-bit mode
11		9-bit mode

Wakeup function

	9-bit UART	Other modes
0	Interrupt generated when data is received	Don’t care
1	Interrupt generated only when SC1CR<RB8> = 1	

Receiving function

0	Receive disabled
1	Receive enabled

Handshake function ($\overline{CTS}$ pin) enables

0	Disabled (Always transferable)
1	Enabled

Transmission data bit8

Figure 3.9.8 Serial Mode Control Register (SIO1, SC1MOD0)

SC0CR (0201H)		7	6	5	4	3	2	1	0
	Bit symbol	RB8	EVEN	PE	OERR	PERR	FERR	SCLKS	IOC
	Read/Write	R	R/W		R (Cleared to 0 when read.)			R/W	
	After reset	Undefined	0	0	0	0	0	0	0
	Function	Received data bit8.	Parity 0: Odd 1: Even	Parity addition. 0: Disable 1: Enable	1: Error Overrun	1: Error Parity	1: Error Framing	0: SCLK0 1: SCLK0	0: Baud rate generator 1: SCLK0 pin input

I/O interface input clock selection

0	Baud rate generator
1	SCLK0 pin input

Edge selection for SCLK pin (I/O mode)

0	Transmits and receivers data on rising edge of SCLK0.
1	Transmits and receivers data on falling edge SCLK0.

Framing error flag
Parity error flag
Overrun error flag
} Cleared to 0 when read

Parity addition enables

0	Disabled
1	Enabled

Even parity addition/check

0	Odd parity
1	Even parity

Received data bit8

Note: As all error flags are cleared after reading do not test only a single bit with a bit testing instruction.

Figure 3.9.9 Serial Control Register (SIO0, SC0CR)

SC1CR
(0209H)

	7	6	5	4	3	2	1	0
Bit symbol	RB8	EVEN	PE	OERR	PERR	FERR	SCLKS	IOC
Read/Write	R	R/W		R (Cleared to 0 when read.)			R/W	
After reset	Undefined	0	0	0	0	0	0	0
Function	Received data bit8.	Parity 0: Odd 1: Even	Parity addition. 0: Disable 1: Enable	1: Error Overrun	1: Error Parity	1: Error Framing	0: SCLK1 1: SCLK1	0: Baud rate generator 1: SCLK1 pin input

I/O interface input clock select

0	Baud rate generator
1	SCLK1 pin input

Edge selection for SCLK pin (I/O mode)

0	Transmits and receive data on rising edge of SCLK1.
1	Transmits and receive data on falling edge of SCLK1.

Framing error flag
Parity error flag
Overrun error flag
} Cleared to 0 when read

Parity addition enables

0	Disabled
1	Enabled

Even parity addition/check

0	Odd parity
1	Even parity

Received data bit8

Note: As all error flags are cleared after reading do not test only a single bit with a bit testing instruction.

Figure 3.9.10 Serial Control Register (SIO1, SC1CR)

BR0CR (0203H)

	7	6	5	4	3	2	1	0
Bit symbol	−	BR0ADDE	BR0CK1	BR0CK0	BR0S3	BR0S2	BR0S1	BR0S0
Read/Write	R/W							
After reset	0	0	0	0	0	0	0	0
Function	Always write 0.	+(16 − K)/16 division. 0: Disable 1: Enable	00: ϕT0 01: ϕT2 10: ϕT8 11: ϕT32		Setting the divided frequency “N”. (0 to F)			

+(16 − K)/16 division enable

0	Disable
1	Enable

Setting the input clock of baud rate generator

00	Internal clock ϕT0
01	Internal clock ϕT2
10	Internal clock ϕT8
11	Internal clock ϕT32

BR0ADD (0204H)

	7	6	5	4	3	2	1	0
Bit symbol					BR0K3	BR0K2	BR0K1	BR0K0
Read/Write					R/W			
After reset					0	0	0	0
Function					Sets frequency divisor “K”. (Divided by N + (16 − K)/16)			

Sets baud rate generator frequency divisor

BR0ADD <BR0K3:0> \ BR0CR <BR0S3:0>	BR0CR<BR0ADDE> = 1		BR0CR<BR0ADDE> = 0
	0000 (N = 16) or 0001 (N = 1)	0010 (N = 2) to 1111 (N = 15)	0001 (N = 1) (UART only) to 1111 (N = 15) 0000 (N = 16)
0000	Disable	Disable	Divided by N
0001 (K = 1) to 1111 (K = 15)	Disable	Divided by N + (16 − K)/16	

Note1:Availability of +(16-K)/16 division function

N	UART mode	I/O mode
2 to 15	○	×
1 , 16	×	×

The baud rate generator can be set “1” in UART mode and disable +(16-K)/16 division function.Don’t use in I/O interface mode.

Note2:Set BR0CR <BR0ADDE> to 1 after setting K (K = 1 to 15) to BR0ADD<BR0K3:0> when +(16-K)/16 division function is used. Writes to unused bits in the BR0ADD register do not affext operation, and undefined data is read from these unused bits.

Figure 3.9.11 Baud Rate Generator Control (SIO0, BR0CR, BR0ADD)

BR1CR (020BH)

	7	6	5	4	3	2	1	0
Bit symbol	−	BR1ADDE	BR1CK1	BR1CK0	BR1S3	BR1S2	BR1S1	BR1S0
Read/Write	R/W							
After reset	0	0	0	0	0	0	0	0
Function	Always write 0.	+(16 − K)/16 division. 0: Disable 1: Enable	00: φT0 01: φT2 10: φT8 11: φT32		Setting the divided frequency "N". (0 to F)			

+(16 − K)/16 division enable

0	Disabled
1	Enabled

Input clock selection for baud rate generator

00	Internal clock φT0
01	Internal clock φT2
10	Internal clock φT8
11	Internal clock φT32

BR1ADD (020CH)

	7	6	5	4	3	2	1	0
Bit symbol					BR1K3	BR1K2	BR1K1	BR1K0
Read/Write					R/W			
After reset					0	0	0	0
Function					Sets frequency divisor "K". (Divided by N + (16 − K)/16)			

Baud rate generator frequency divisor setting

BR1ADD <BR1K3:0> \ BR0CR <BR1S3:0>	BR1CR<BR1ADDE> = 1		BR1CR<BR1ADDE> = 0
	0000 (N = 16) or 0001 (N = 1)	0010 (N = 2) to 1111 (N = 15)	0001 (N = 1) (UART only) to 1111 (N = 15) 0000 (N = 16)
0000	Disable	Disable	Divided by N
0001 (K = 1) to 1111 (K = 15)	Disable	Disabled by N + (16 − K)/16	

Note1:Availability of +(16-K)/16 division function

N	UART mode	I/O mode
2 to 15	○	×
1 , 16	×	×

The baud rate generator can be set "1" in UART mode and disable +(16-K)/16 division function.Don't use in I/O interface mode.

Note2:Set BR1CR <BR1ADDE> to 1 after setting K (K = 1 to 15) to BR10ADD<BR1K3:0> when +(16-K)/16 division function is used. Writes to unused bits in the BR1ADD register do not affext operation, and undefined data is read from these unused bits.

Figure 3.9.12 Baud Rate Generator Control (SIO1, BR1CR, BR1ADD)

SC0BUF (0200H)

	7	6	5	4	3	2	1	0	
	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0	(Transmission)
	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	(Receiving)

Note: Prohibit read-modify-write for SC0BUF.

Figure 3.9.13 Serial Transmission/Receiving Buffer Registers (SIO0, SC0BUF)

SC0MOD1 (0205H)

	7	6	5	4	3	2	1	0
Bit symbol	I2S0	FDPX0						
Read/Write	R/W	R/W						
After reset	0	0						
Function	IDLE2 0: Stop 1: Run	Duplex 0: Half 1: Full						

Figure 3.9.14 Serial Mode Control Register 1 (SIO0, SC0MOD1)

SC1BUF (0208H)

	7	6	5	4	3	2	1	0	
	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0	(Transmission)
	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	(Receiving)

Note: Prohibit read-modify-write for SC1BUF.

Figure 3.9.15 Serial Transmission/Receiving Buffer Registers (SIO1, SC1BUF)

SC1MOD1 (020DH)

	7	6	5	4	3	2	1	0
Bit symbol	I2S1	FDPX1						
Read/Write	R/W	R/W						
After reset	0	0						
Function	IDLE2 0: Stop 1: Run	Duplex 0: Half 1: Full						

Figure 3.9.16 Serial Mode Control Register 1 (SIO1, SC1MOD1)

3.9.4 Operation in Each Mode

(1) Mode 0 (I/O interface mode)

This mode allows an increase in the number of I/O pins available for transmitting data to or receiving data from an external shift register.

This mode includes the SCLK output mode to output synchronous clock SCLK and SCLK input mode to input external synchronous clock SCLK.

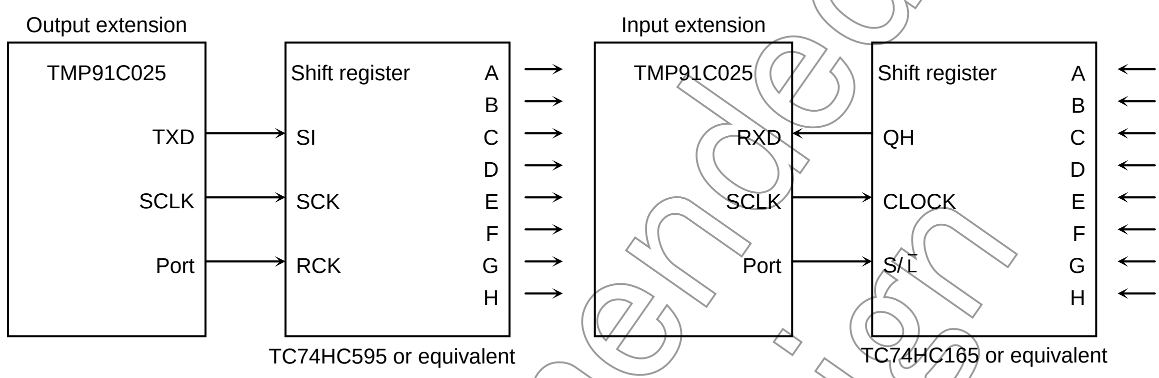


Figure 3.9.17 SCLK Output Mode Connection Example

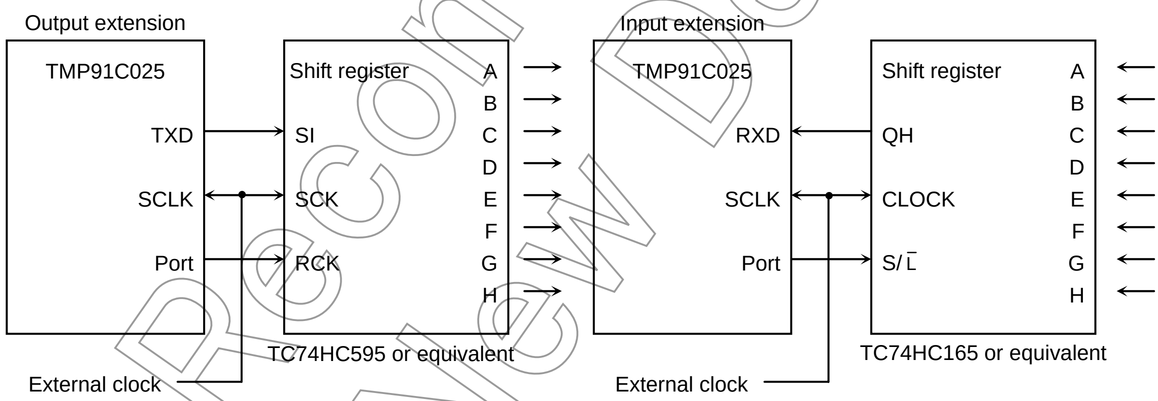


Figure 3.9.18 SCLK Input Mode Connection Example

a. Transmission

In SCLK output mode 8-bit data and a synchronous clock are output on the TXD0 and SCLK0 pins respectively each time the CPU writes the data to the transmission buffer. When all data is output, INTES0<ITX0C> will be set to generate the INTTX0 interrupt.

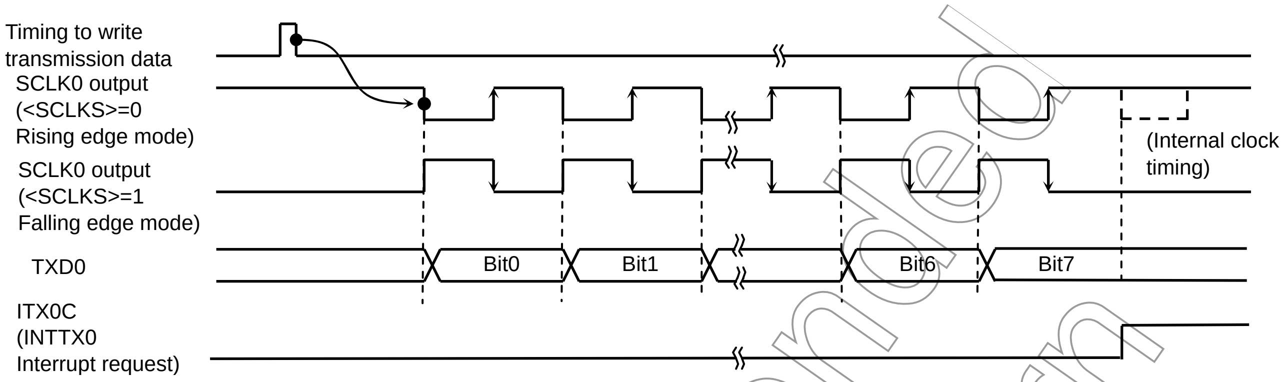


Figure 3.9.19 Transmitting Operation in I/O Interface Mode (SCLK0 output mode)

In SCLK input mode, 8-bit data is output on the TXD0 pin when the SCLK0 input becomes active after the data has been written to the transmission buffer by the CPU.

When all data is output, INTES0<ITX0C> will be set to generate INTTX0 interrupt.

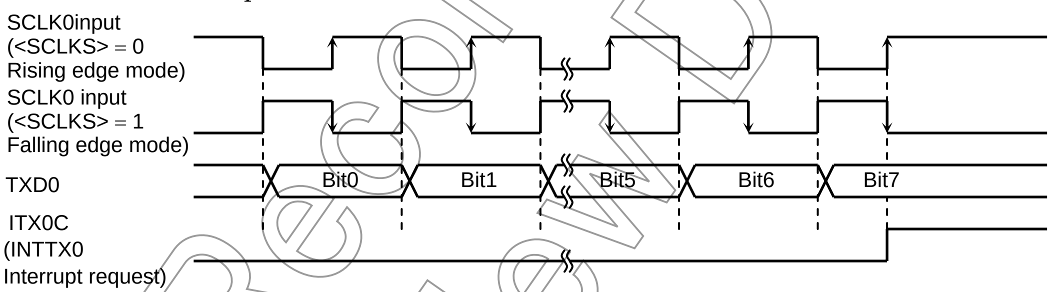


Figure 3.9.20 Transmitting Operation in I/O Interface Mode (SCLK0 input mode)

b. Receiving

In SCLK output mode, the synchronous clock is outputted from SCLK0 pin and the data is shifted to receiving buffer 1. This starts when the receive interrupt flag INTES0<IRX0C> is cleared by reading the received data. When 8-bit data are received, the data will be transferred to receiving buffer 2 (SC0BUF according to the timing shown below) and INTES0<IRX0C> will be set to generate INTRX0 interrupt.

The outputting for the first SCLK0 starts by setting SC0MOD0<RXE> to 1.

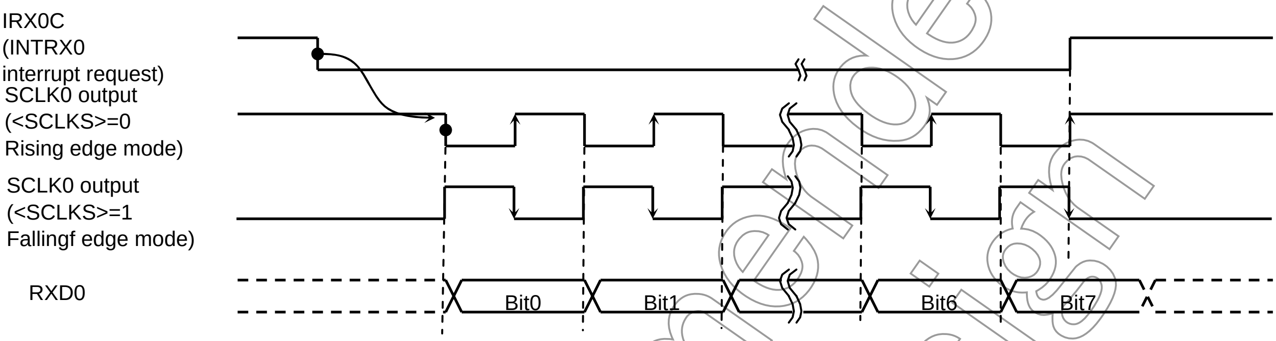


Figure 3.9.21 Receiving Operation in I/O Interface Mode (SCLK0 output mode)

In SCLK input mode, the data is shifted to receiving buffer 1 when the SCLK input becomes active after the receive interrupt flag INTES0<IRX0C> is cleared by reading the received data. When 8-bit data is received, the data will be shifted to receiving buffer 2 (SC0BUF according to the timing shown below) and INTES0<IRX0C> will be set again to be generate INTRX0 interrupt.

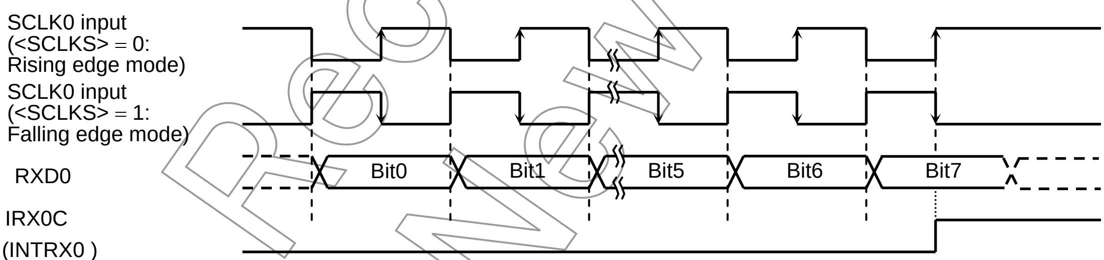


Figure 3.9.22 Receiving Operation in I/O Interface Mode (SCLK0 input mode)

Note: The system must be put in the receive enable state (SCMOD0<RXE> = 1) before data can be received.

c. Transmission and receiving (Full duplex mode)

When the full duplex mode is used, set the level of receive interrupt to 0 and set enable the interrupt level (1 to 6) to the transfer interrupt. In the transfer interrupt program, the receiving operation should be done like the above example before setting the next transfer data.

(Example)

Channel 0, SCLK output

Baud rate = 9600 bps

fc = 14.7456 MHz

System clock: High-frequency (fc)

Clock gear: 1 (fc)

Prescaler clock: f_{FPH}

Main routine

	7	6	5	4	3	2	1	0	
INTES0	0	0	0	1	0	0	0	0	Set the INTTX0 level to 1. Set the INTRX0 level to 0.
PCCR	–	–	–	–	–	1	0	1	Set PC0, PC1 and PC2 to function as the TXD0, RXD0 and SCLK0 pins respectively.
PCFC	–	–	–	–	–	1	–	1	
SC0MOD0	0	0	0	0	0	0	0	0	Select I/O interface Mode.
SC0MOD1	1	1	X	X	X	X	X	X	Select full duplex Mode.
SC0CR	0	0	0	0	0	0	0	0	SCLK output, transmit on negative edge, receive on positive edge
BR0CR	0	0	1	1	0	0	1	1	Baud rate = 9600 bps
SC0MOD0	0	0	1	0	0	0	0	0	Enable receiving
SC0BUF	*	*	*	*	*	*	*	*	Set the transmit data and start.

INTTX0 interrupt routine

Acc SC0BUF									Read the receiving buffer.
SC0BUF	*	*	*	*	*	*	*	*	Set the next transmit data.

X: Don’t care, –: No change

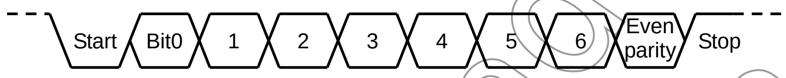
(2) Mode 1 (7-bit UART mode)

7-bit UART mode is selected by setting serial channel mode register SC0MOD0 <SM1:0> to 01.

In this mode, a parity bit can be added. Use of a parity bit is enabled or disabled by the setting of the serial channel control register SC0CR<PE> bit; whether even parity or odd parity will be used is determined by the SC0CR<EVEN> setting when SC0CR<PE> is set to 1 (Enabled).

(Setting example)

When transmitting data of the following format, the control registers should be set as described below. This explanation applies to channel 0.



← Transmission direction (transmission rate: 2400 bps at fc = 12.288 MHz)

∗ Clock state
- System clock: High-frequency (fc)
- Clock gear: 1 (fc)
- Prescaler clock: f_{FPH}

	7	6	5	4	3	2	1	0	
P9CR	← –	–	–	–	–	–	–	1	Set PC0 to function as the TXD0 pin.
P9FC	← –	–	–	–	–	–	–	1	
SC0MOD	← X	0	–	X	0	1	0	1	Select 7-bit UART mode.
SC0CR	← X	1	1	X	X	X	0	0	Add even parity.
BR0CR	← 0	0	1	0	0	1	0	1	Set the transfer rate to 2400 bps.
INTES0	← 1	1	0	0	–	–	–	–	Enable the INTTX0 interrupt and set it to interrupt level 4.
SC0BUF	← *	*	*	*	*	*	*	*	Set data for transmission.

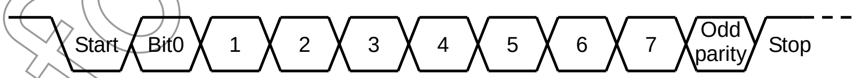
X: Don't care, –: No change

(3) Mode 2 (8-bit UART mode)

8-bit UART mode is selected by setting SC0MOD0<SM1:0> to 10. In this mode, a parity bit can be added (Use of a parity bit is enabled or disabled by the setting of SC0CR<PE>); whether even parity or odd parity will be used is determined by the SC0CR<EVEN> setting when SC0CR<PE> is set to 1 (Enabled).

(Setting example)

When receiving data of the following format, the control registers should be set as described below.



← Transmission direction (transmission rate: 9600 bps at fc = 12.288 MHz)

∗ Clock state
- System clock: High-frequency (fc)
- Clock gear: 1 (fc)
- Prescaler clock: f_{FPH}

Main settings

		7	6	5	4	3	2	1	0	
PCCR	←	–	–	–	–	–	–	0	–	Set PC1 to function as the RXD0 pin.
SC0MOD	←	–	0	1	X	1	0	0	1	Enable receiving in 8-bit UART mode.
SC0CR	←	X	0	1	X	X	X	0	0	Add even parity.
BR0CR	←	0	0	0	1	0	1	0	1	Set the transfer rate to 9600 bps.
INTES0	←	–	–	–	–	1	1	0	0	Enable the INTRX0 interrupt and set it to interrupt level 4.

Interrupt processing

Acc	←	SC0CR AND 00011100	Check for errors.
if Acc	≠	0 then ERROR	
Acc	←	SC0BUF	Read the received data.

X: Don’t care, –: No change

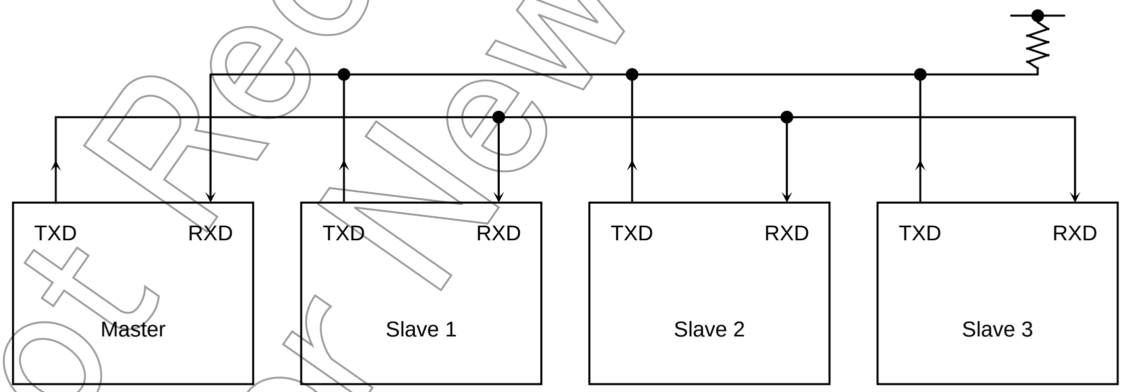
(4) Mode 3 (9-bit UART mode)

9-bit UART mode is selected by setting SC0MOD0<SM1:0> to 11. In this mode parity bit cannot be added.

In the case of transmission the MSB (9th bit) is written to SC0MOD0<TB8>. In the case of receiving it is stored in SC0CR<RB8>. When the buffer is written and read, the MSB is read or written first, before the rest of the SC0BUF data.

Wakeup function

In 9-bit UART mode, the wakeup function for slave controllers is enabled by setting SC0MOD0<WU> to 1. The interrupt INTRX0 occurs only when<RB8> = 1.



Note: The TXD pin of each slave controller must be in open-drain output mode.

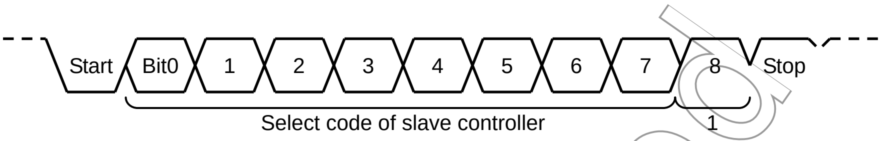
Figure 3.9.23 Serial Link Using Wakeup Function

Protocol

a. Select 9-bit UART mode on the master and slave controllers.

b. Set the SC0MOD0<WU> bit on each slave controller to 1 to enable data receiving.

c. The master controller transmits one-frame data including the 8-bit select code for the slave controllers. The MSB (bit8)<TB8> is set to 1.



d. Each slave controller receives the above frame. Each controller checks the above select code against its own select code. The controller whose code matches clears its WU bit to 0.

e. The master controller transmits data to the specified slave controller whose SC0MOD<WU> bit is cleared to 0. The MSB (bit8) <TB8> is cleared to 0.

f. The other slave controllers (whose <WU> bits remain at 1) ignore the received data because their MSBs (Bit8 or <RB8>) are set to 0, disabling INTRX0 interrupts.
The slave controller (WU bit = 0) can transmit data to the master controller, and it is possible to indicate the end of data receiving to the master controller by this transmission.

(Setting example)

To link two slave controllers serially with the master controller using the internal clock f_{SYS} as the transfer clock.

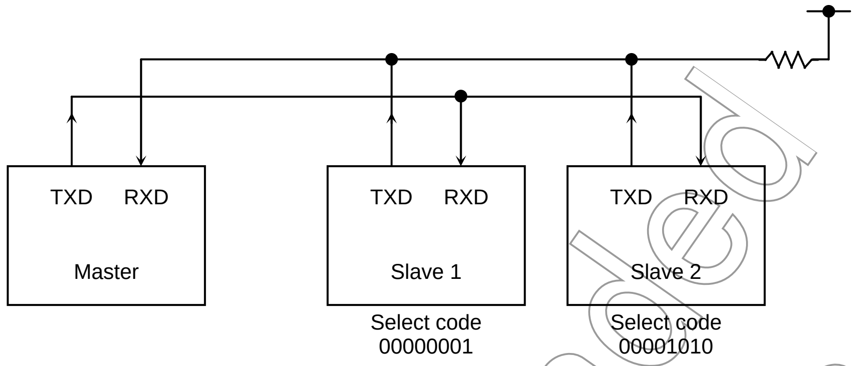


Figure 3.9.24 UART Block Connection

Since serial channels 0 and 1 operate in exactly the same way, channel 0 only is used for the purposes of this explanation.

- Setting the master controller

Main

PCCR	← – – – – – – 0 1	Set PC0 and PC1 to function as the TXD0 and RXD0 pins respectively.
PCFC	← X X – X – – X 1	
INTES0	← 1 1 0 0 1 1 0 1	Enable the INTTX0 interrupt and set it to interrupt level 4. Enable the INTRX0 interrupt and set it to interrupt level 5.
SC0MOD0	← 1 0 1 0 1 1 1 0	Set f_{SYS} as the transmission clock for 9-bit UART mode.
SC0BUF	← 0 0 0 0 0 0 0 1	Set the select code for slave controller 1.

INTTX0 interrupt

SC0MOD0	← 0 – – – – – – –	Set TB8 to 0.
SC0BUF	← * * * * * * * *	Set data for transmission.

- Setting the slave controller

Main

PCCR	← – – – – – – 0 1	Set PC1 to RXD and PC0 to TXD0 (Open-drain output).
PCFC	← X X – X – – X 1	
PCODE	← X X X X – X X 1	
INTES0	← 1 1 0 1 1 1 1 0	Enable INTRX0 and INTTX0.
SC0MOD0	← 0 0 1 1 1 1 1 0	Set <WU> to 1 in 9-bit UART transmission mode using f_{SYS} as the transfer clock.

INTRX0 interrupt

Acc ← SC0BUF

if Acc = Select code

Then SC0MOD0 ← – – – 0 – – – –   Clear <WU> to 0.

3.9.5 Support for IrDA

SIO0 includes support for the IrDA 1.0 infrared data communication specification. Figure 3.9.25 shows the block diagram.

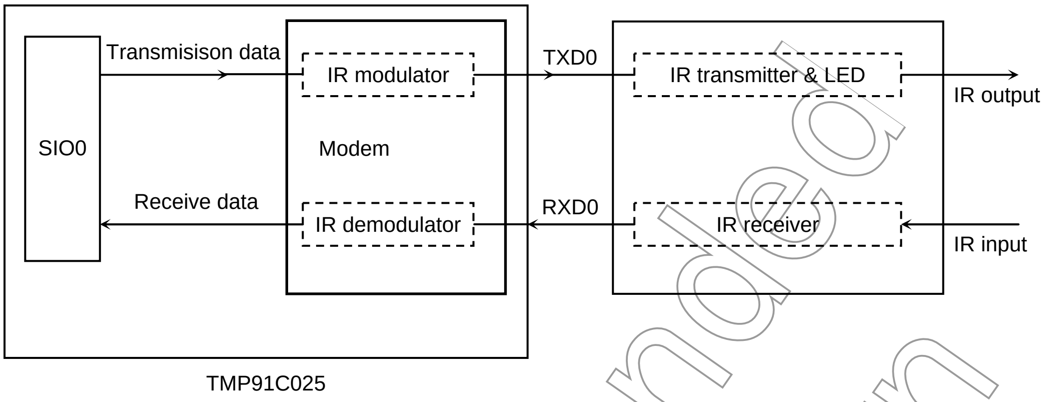


Figure 3.9.25 IrDA Block Diagram

(1) Modulation of the transmission data

When the transfer data is 0, the modem outputs 1 to TXD0 pin with either 3/16 or 1/16 times for width of baud-rate. The pulse width is selected by the SIRCR<PLSEL>. When the transfer data is 1, the modem outputs 0.

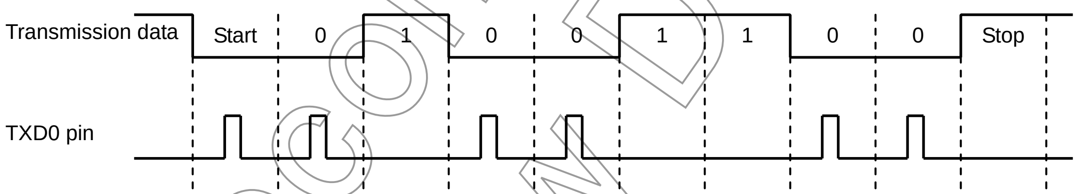


Figure 3.9.26 Modulation Example of Transfer Data

(2) Demodulation of the receive data

When the receive data has the effective high-level pulse width (Software selectable), the modem outputs 0 to SIO0. Otherwise the modem outputs 1 to SIO0. The receive pulse logic is also selectable by SIRCR<RXSEL>.

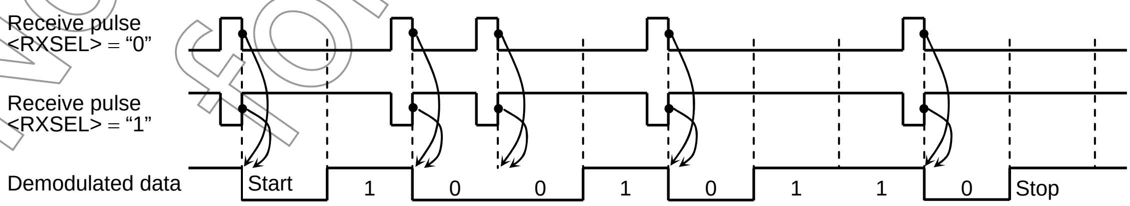


Figure 3.9.27 Demodulation Example of Receive Data

(3) Data format

The data format is fixed as follows:

- Data length: 8 bits
- Parity bits: None
- Stop bits: 1

Any other settings don't guarantee the normal operation.

(4) SFR

Figure 3.9.28 shows the control register SIRCR. Set the data SIRCR during SIO0 is inhibited (Both TXEN and RXEN of this register should be set to 0).

Any changing for this register during transmission or receiving operation doesn't guarantee the normal operation.

The following example describes how to set this register:

1) SIO setting ; Set the SIO to UART mode.
↓
2) LD (SIRCR), 07H ; Set the receive data pulse width to 16×.
3) LD (SIRCR), 37H ; TXEN, RXEN enable the transmission and receiving of SIO.
↓
4) Start transmission and receiving for SIO0 ; The modem operates as follows:
- SIO0 starts transmitting.
- IR receiver starts receiving.

(5) Notes

1) Baud rate generator for IrDA
To generate baud-rate for IrDA, use baud-rate generator in SIO0 by setting 01 to SC0MOD0<SC1:0>. To use another source (TA0TRG, f_{SYS} and SCLK0 input) are not allowed.

2) As the IrDA 1.0 physical layer specification, the data transfer speed and infra red pulse width is specified.

Table 3.9.4 Baud Rate and Pulse Width Specifications

Baud Rate	Modulation	Rate Tolerance (% of rate)	Pulse Width (Min)	Pulse Width (Typ.)	Pulse width (Max)
2.4 kbps	RZI	±0.87	1.41 µs	78.13 µs	88.55 µs
9.6 kbps	RZI	±0.87	1.41 µs	19.53 µs	22.13 µs
19.2 kbps	RZI	±0.87	1.41 µs	9.77 µs	11.07 µs
38.4 kbps	RZI	±0.87	1.41 µs	4.88 µs	5.96 µs
57.6 kbps	RZI	±0.87	1.41 µs	3.26 µs	4.34 µs
115.2 kbps	RZI	±0.87	1.41 µs	1.63 µs	2.23 µs

The infra red pulse width is specified either baud rate T x 3/16 or 1.6 µs (1.6 µs is equal to 3/16 pulse width when baud rate is 115.2 kbps).

The TMP91C025 has the function selects the pulse width on the transmission either 3/16 or 1/16. But 1/16 pulse width can be selected when the baud rate is equal or less than 38.4 kbps only. When 38.4 kbps and 115.2 kbps, the output pulse width should not be set to T x 1/16.

As the same reason, + (16 – K)/16 division functions in the baud rate generator of SIO0 can not be used to generate 115.2 kbps baud-rate.

Also when the 38.4 kbps and 1/16 pulse width, + (16 – K)/16 divisions function can not be used. Table 3.9.5 shows “Baud-rate and Pulse Width for (16 – K)/16 Division Function”.

Table 3.9.5 Baud-rate and Pulse Width for (16 – K)/16 Division Function

Pulse Width	Baud-rate					
	115.2 kbps	57.6 kbps	38.4 kbps	19.2 kbps	9.6 kbps	2.4 kbps
T × 3/16	×	○	○	○	○	○
T × 1/16	–	–	×	○	○	○

○: Can be used (16 – K)/16 division function
×: Can not be used (16 – K)/16 division function
–: Can not be set to 1/16 pulse width

SIRCR (0207H)

	7	6	5	4	3	2	1	0
Bit symbol	PLSEL	RXSEL	TXEN	RXEN	SIRWD3	SIRWD2	SIRWD1	SIRWD0
Read/Write	R/W							
After reset	0	0	0	0	0	0	0	0
Function	Select transmit pulse width. 0:3/16 1:1/16	Receive data. 0: H pulse 1: L pulse	Transmit 0: Disable 1: Enable	Receive 0: Disable 1: Enable	Select receive pulse width Set effective pulse width for equal or more than $2x \times (\text{value} + 1) + 100\text{ns}$ Can be set: 1 to 14 Can not be set: 0, 15.			

Select receive pulse width

Formula:

Effective pulse width $\geq 2x \times (\text{value} + 1) + 100\text{ns}$

$x = 1/f_{FPH}$

0000	Cannot be set
0001	Equal or more than 4x + 100nS
to	
1110	Equal or more than 30x + 100nS
1111	Can not be set

Receive operation

0	Disabled
1	Enabled

Transmit operation

0	Disabled
1	Enabled

Select transmit pulse width

0	3/16
1	1/16

Figure 3.9.28 IrDA Control Register

3.10 Touch Screen Interface (TSI)

The TMP91C025 has an interface for 4-terminal resistor network touch-screen.

This interface supports two procedures: an X/Y position measurement and touch detection.

Each procedure can be performed by setting the TSI control register (TSICR0 and TSICR1) and using an internal AD converter.

3.10.1 Touch Screen Interface Module Internal/External Connection

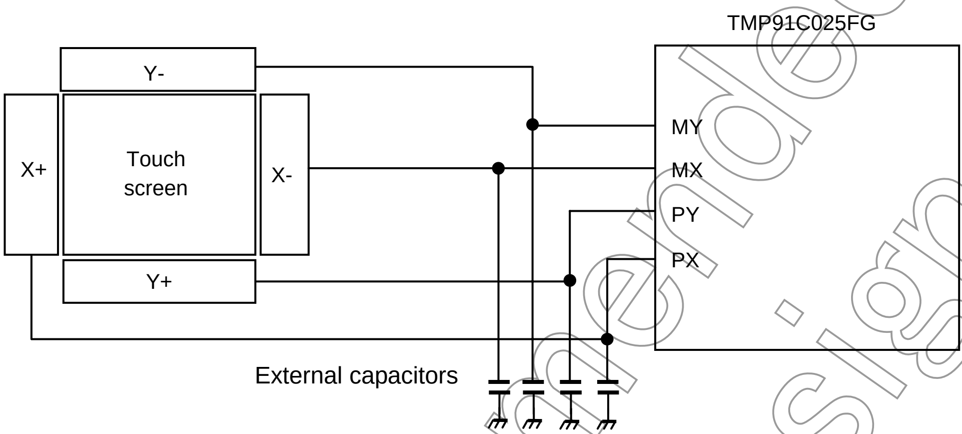


Figure 3.10.1 External Connection of TSI (A)

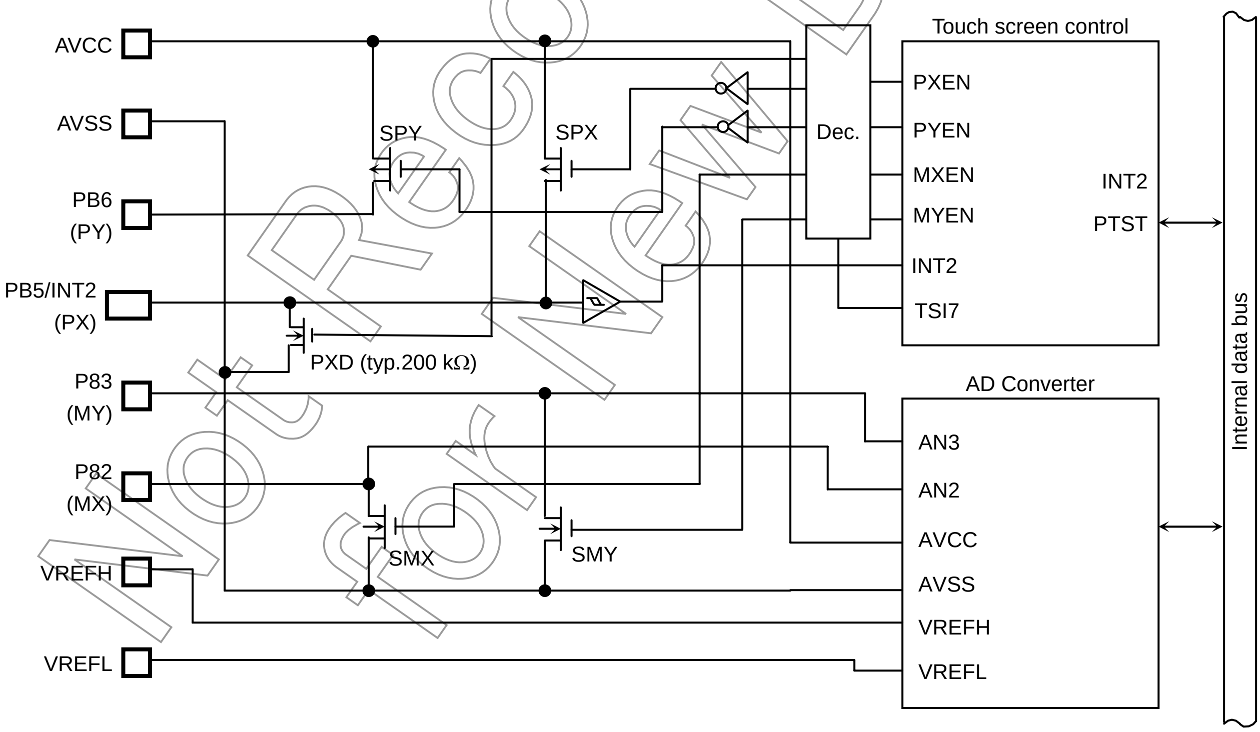


Figure 3.10.2 Internal Block Diagram of TSI (B)

3.10.2 Touch Screen Interface (TSI) Control Register

TSI Control Register

TSICR0 (002BH)

	7	6	5	4	3	2	1	0
Bit symbol	TSI7		PTST	TWIEN	PYEN	PXEN	MYEN	MXEN
Read/Write	R/W		R	R/W	R/W	R/W	R/W	R/W
After reset	0		0	0	0	0	0	0
Function	0: Disable 1: Enable		Detection condition 0: no touch 1: touch	INT2 interrupt control 0: Disable 1: Enable	SPY 0 : OFF 1 : ON	SPX 0 : OFF 1 : ON	SMY 0 : OFF 1 : ON	SMX 0 : OFF 1 : ON

Bit5 monitors whether the screen was touched or not.
The bit is 1 while the screen has been touched.

PXD (Internal Pull-down resistor) ON/OFF setting

<TSI7> \ <PXEN>	0	1
0	OFF	OFF
1	ON	OFF

De-bounce Time Setting Register

TSICR1 (002CH)

	7	6	5	4	3	2	1	0
Bit symbol	DBC7	DB1024	DB256	DB64	DB8	DB4	DB2	DB1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0
Function	0: Disable 1: Enable	1024	256	64	8	4	2	1
		De-bounce time is set by "($N \times 64 - 16$)/f_{SYS}" – formula. "N" is sum of number which is set to 1 in bit6 to bit0.						

3.10.3 Touch Detection Procedure

A touch detection procedure is a preparing procedure till a pen touches to the screen.

When the waiting state, ON only SPY-switch and OFF other 3-switch (SMY, SPX and SMX).

During this waiting state, PB5/INT2/PX pin's level is L because of the internal resistors between X and Y directions in the touch screen are not connected and INT2 isn't generated.

If the pen touches, PB5/INT2/PX pin's level is H because of the internal pull-down register (PXD) between X and Y direction in the touch screen are connected and INT2 will be generated.

And the de-bounce circuit like following diagram is prepared to avoid some number's interrupt generation though one time touch.

This can ignore the pulse under the time which is set to TSICR1 register.

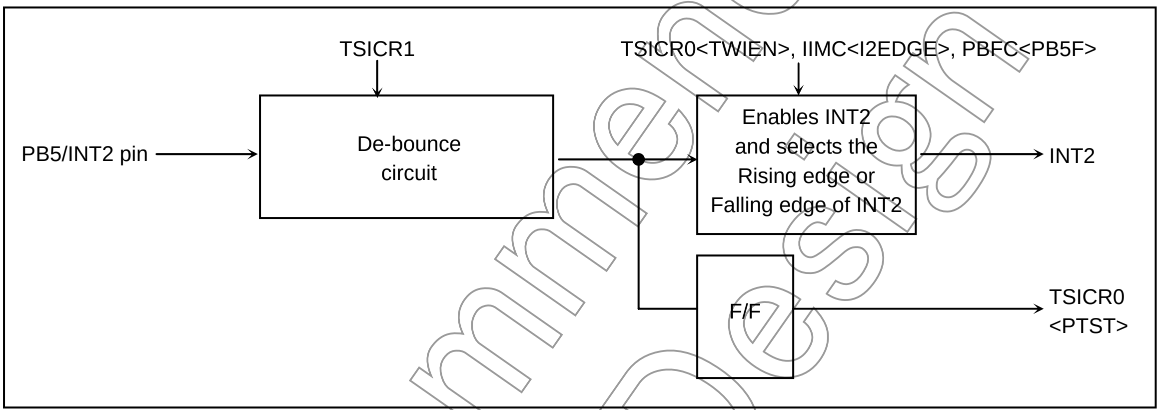


Figure 3.10.3 Block Diagram of De-bounce Circuit

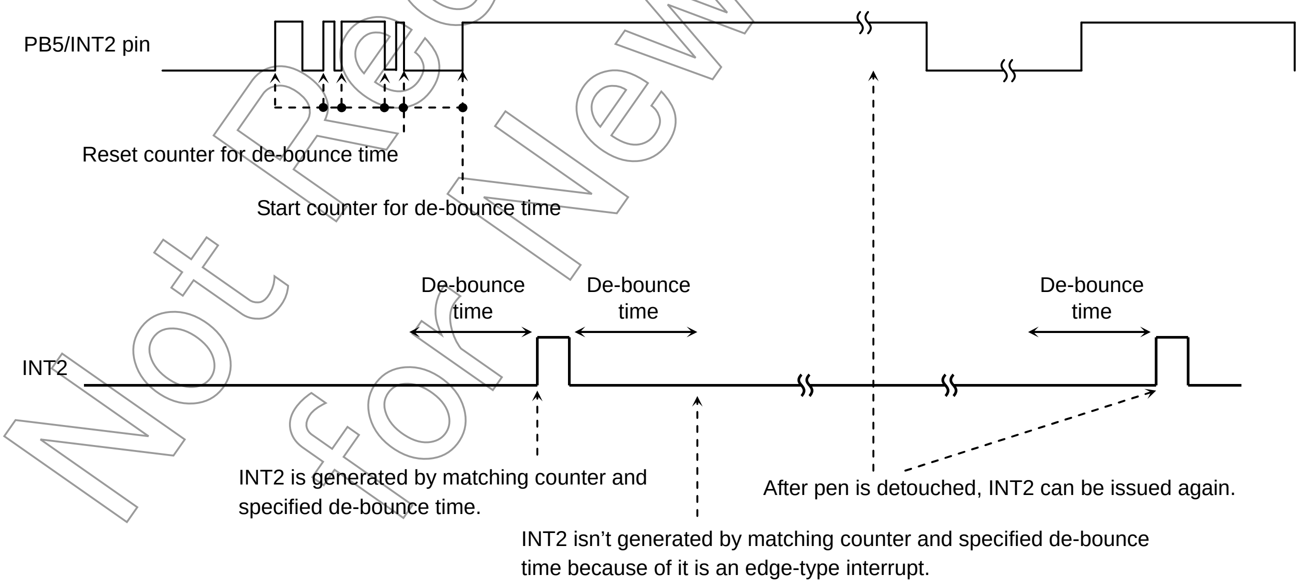


Figure 3.10.4 Timing Diagram of De-bounce Circuit

3.10.4 X/Y Position Measuring Procedure

In the INT2 routine, execute an X/Y position measuring procedure like below.

<X position measurement>

At first, ON both SPX and SMX-switches and OFF SPY, SMY-switches.

By this setting, analog-voltage which shows the X position will be inputted to P83/MY/AN3 pin. The X position can be measured by converting this voltage to digital code with AD converter.

<Y position measurement>

Next, ON both SPY and SMY-switches and OFF SPX, SMX-switches.

By this setting, analog voltage which shows the Y position will be inputted to P82/MX/AN2 pin. The Y position can be measured by converting this voltage to digital code with AD converter.

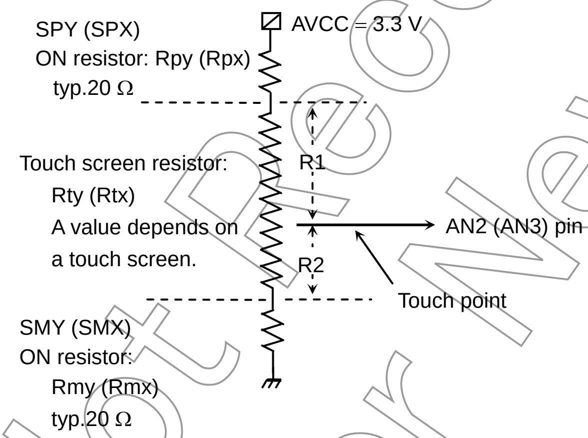
The above analog voltage which is inputted to AN3 or AN2 pin can be calculated.

It is a ratio between resistance value in TMP91C025FG and resistance value in touch screen shown in Figure 3.10.5.

Therefore, if the pen touches a corner area on touch screen, analog-voltage will not be to 3.3 V or 0.0 V.

As a notice, since each resistor has an uneven, consider about it.

And it is recommended that an average code among a few times AD conversion will be adopted as a correct code.



[Formula to calculate analog voltage (E1) to AN2 or AN3 pin]

E1 = ((R2 + Rmy)/(Rpy + Rty + Rmy)) × AVCC [V]

(Example) The case of AVCC = 3.3 V, Rpy = Rmy = 20 Ω,
R1 = 400 Ω and R2 = 100 Ω
E1 = ((100 + 20)/(20 + 400 + 100 + 20) × 3.3
= 0.733 V

Note 1: An X position can be calculated in the same way though above formula is for Y position.

Note 2: Rty = R1 + R2.

Figure 3.10.5 Calculation Analog Voltage

3.10.5 Flow Chart for TSI

(1) Touch detection procedure

(2) X/Y position measurement procedure

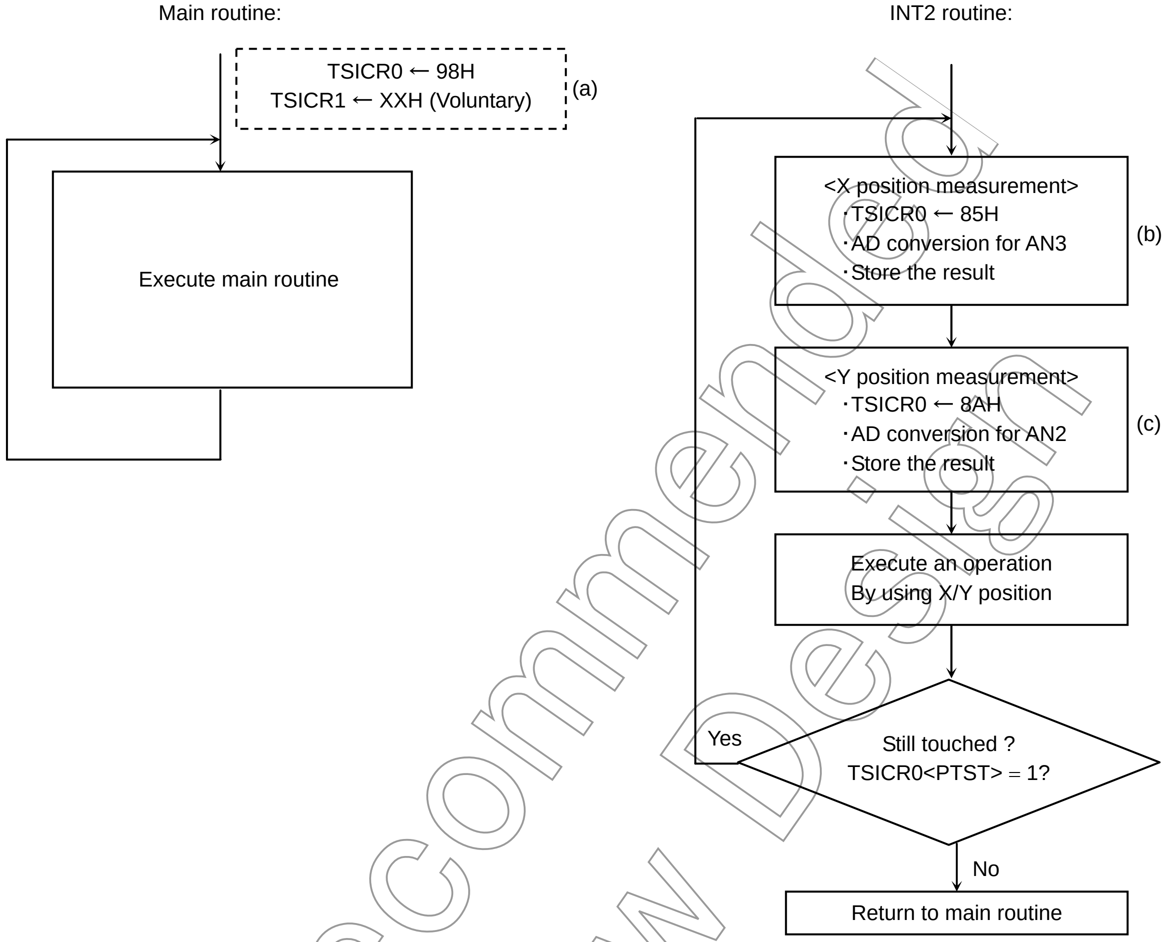
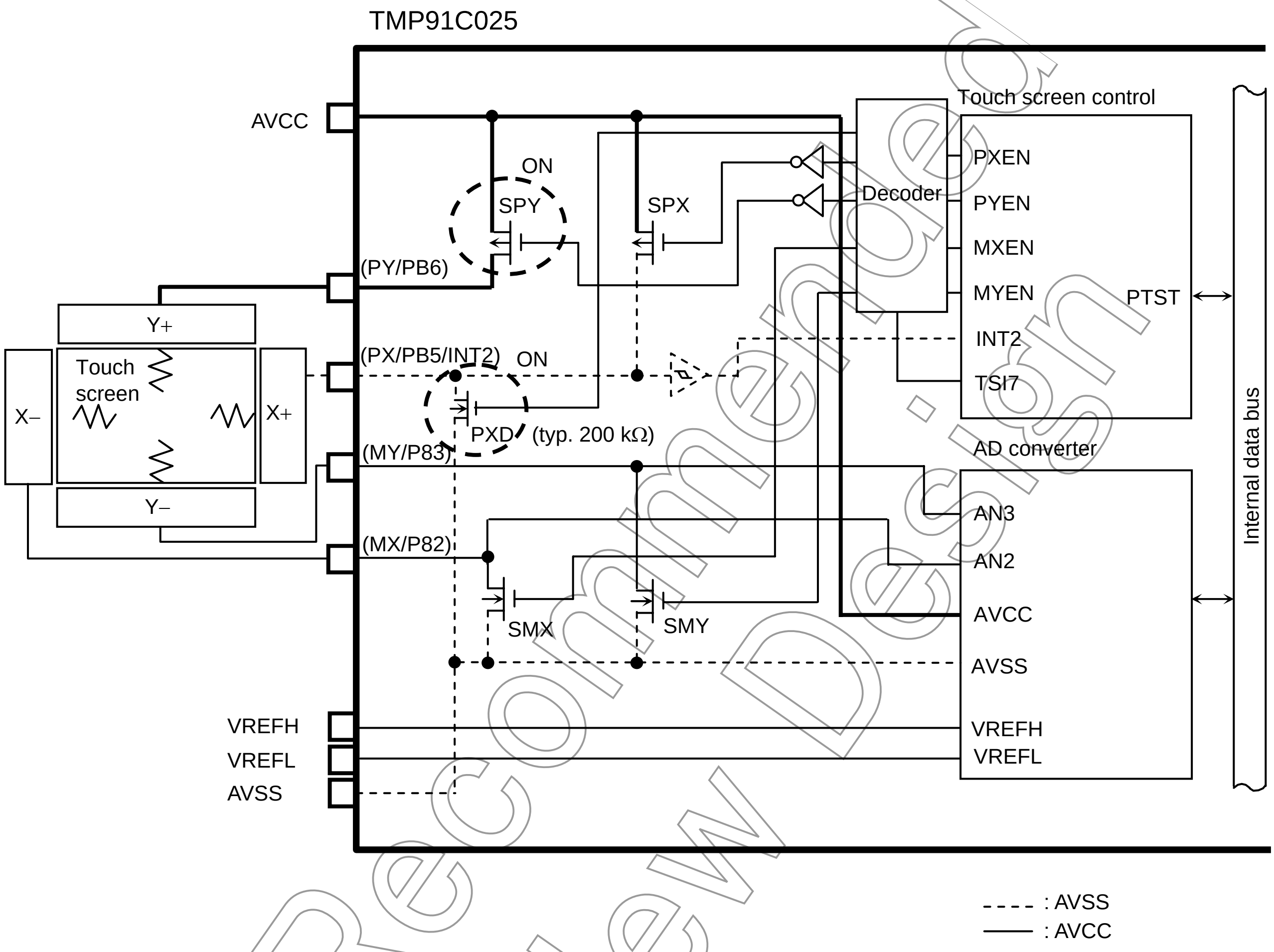


Figure 3.10.6 Flow Chart for TSI

It shows the circuit for each statement (a), (b) and (c) in the next page.

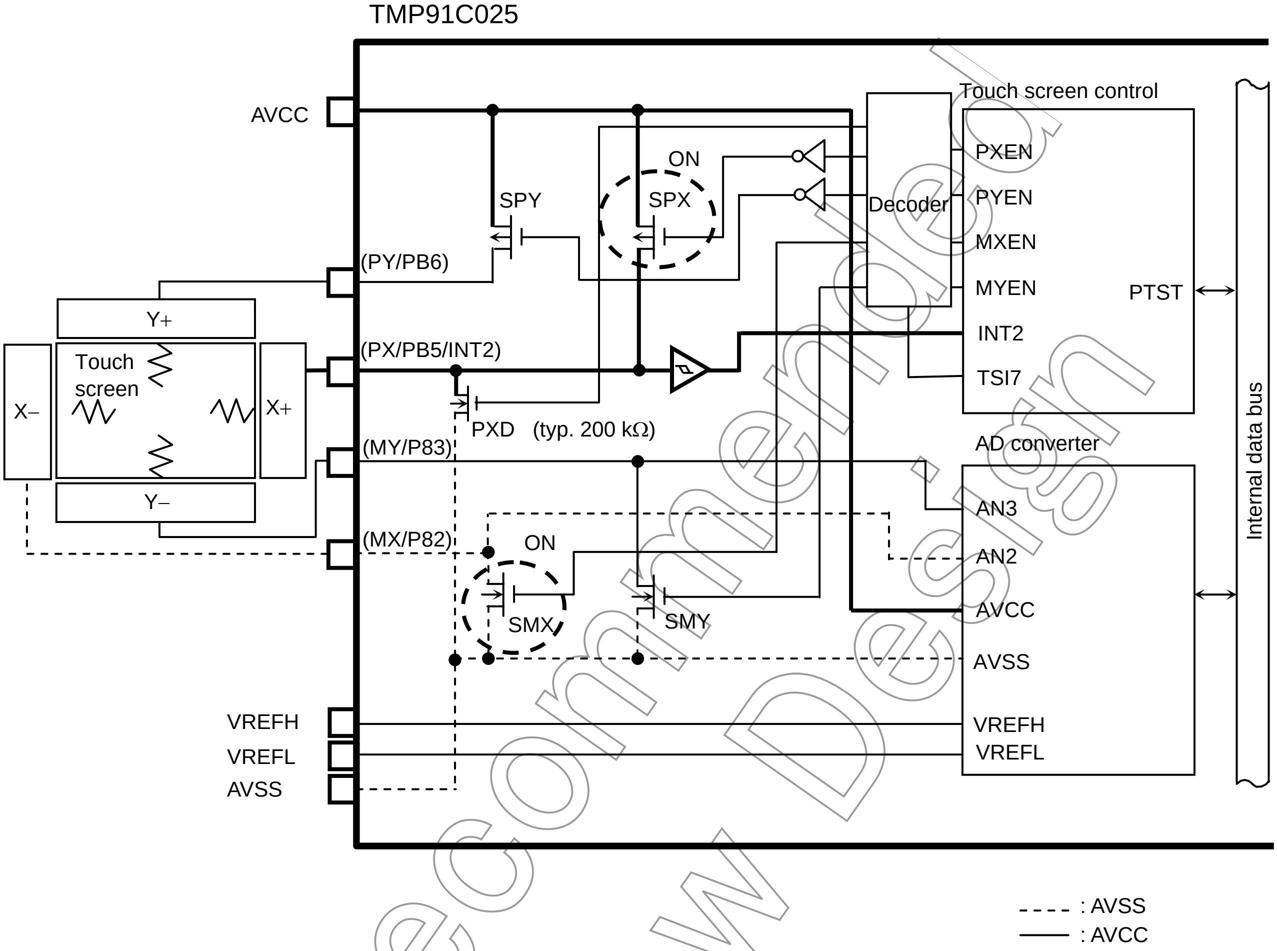
(a) Main routine : Waiting for INT2 interrupt

(pbfc)<PB5F>, <PB6F> = "1"	:	Set PB5 to int2/PX, set PB6 to PY
(inte12)	:	Set interrupt level of INT2
(tsicr0) = 98h	:	Pull-down resistor on, SPY on, Interrupt set<TWIEN>
ei	:	Enable interrupt



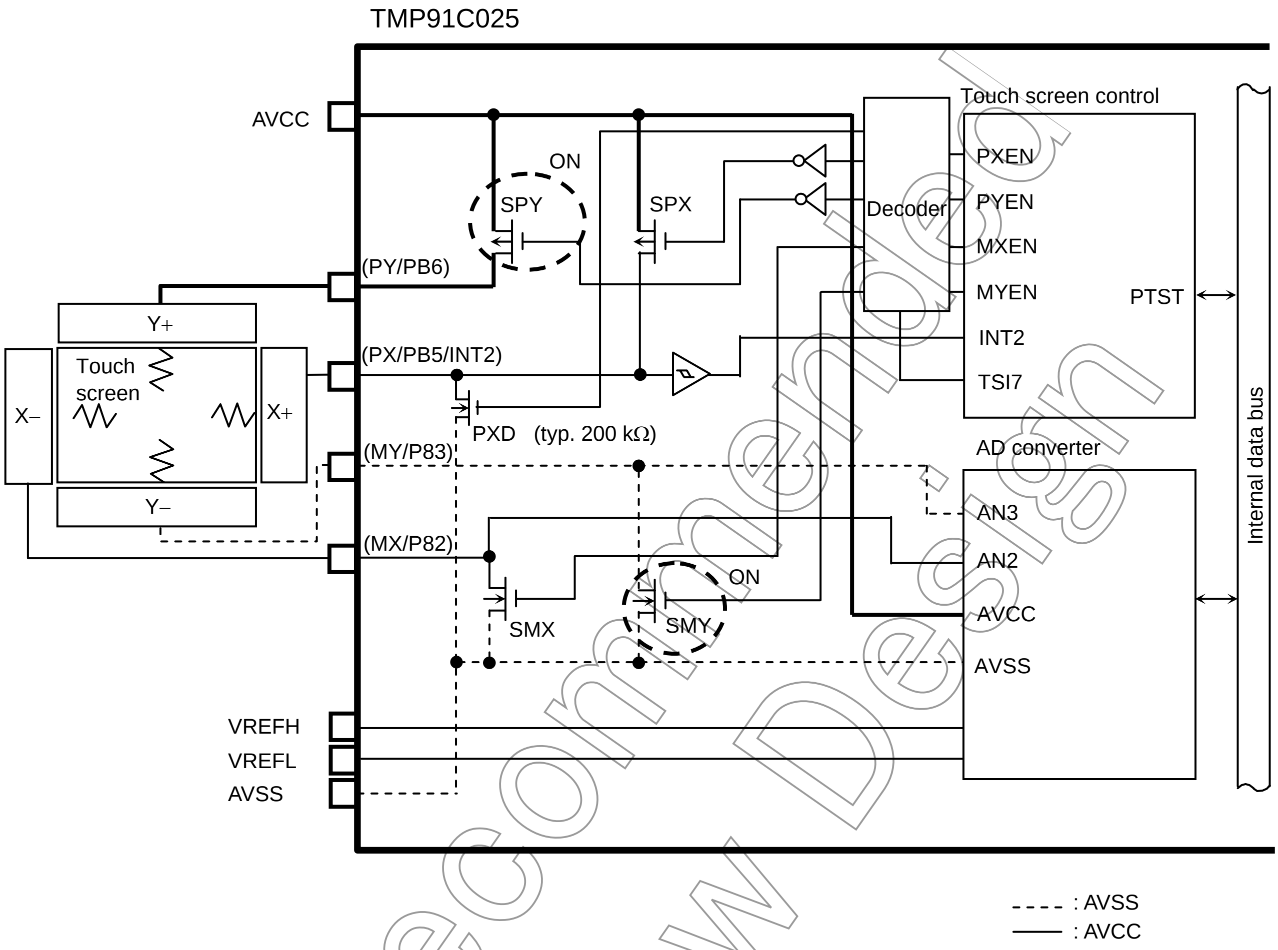
(b) INT2 routine: X position measurement (AD conversion start)

(tsicr0) = 85h : Set SMX, SPX to ON.
(admod1) = 83h : Set to AN3.
(admod0) = 01h : Start AD conversion.



(c) INT2 routine: Y position measurement (AD conversion start)

(tsicr0) = 8ah	:	Set SMX, SPX to ON.
(admod1) = 82h	:	Set to AN2.
(admod0) = 01h	:	Start AD conversion.



3.11 Analog/Digital Converter

The TMP91C025 incorporates a 10-bit successive approximation type analog/digital converter (AD converter) with 4-channel analog input.

Figure 3.11.1 is a block diagram of the AD converter. The 4-channel analog input pins (AN0 to AN3) are shared with the input only port 4 and can thus be used as an input port.

Note: When IDLE2, IDLE1 or STOP mode is selected, so as to reduce the power, with some timings the system may enter a standby mode even though the internal comparator is still enabled. Therefore be sure to check that AD converter operations are halted before a HALT instruction is executed.

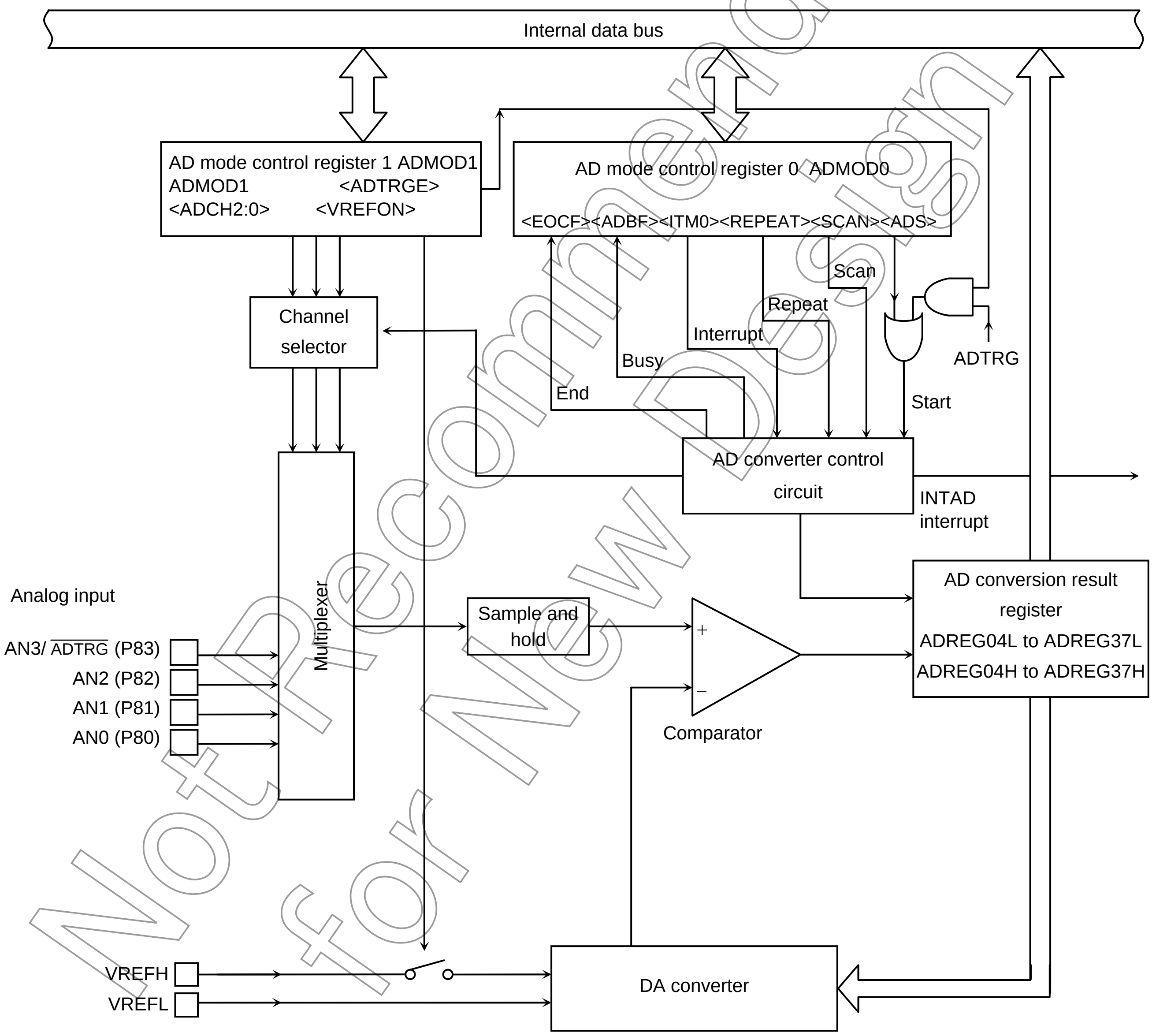


Figure 3.11.1 Block Diagram of AD Converter

3.11.1 Analog/Digital Converter Registers

The AD converter is controlled by the two AD mode control registers: ADMOD0 and ADMOD1. The AD conversion results are stored in 8 kinds of AD conversion data upper and lower registers: ADREG04H/L, ADREG15H/L, ADREG26H/L and ADREG37H/L.

Figure 3.11.2 shows the registers related to the AD converter.

AD Mode Control Register 0

ADMOD0 (02B0H)

	7	6	5	4	3	2	1	0
Bit symbol	EOCF	ADBF	–	–	ITM0	REPEAT	SCAN	ADS
Read/Write	R		R/W					
After reset	0	0	0	0	0	0	0	0
Function	AD conversion end flag. 0: Conversion in progress 1: Conversion complete	AD conversion busy flag. 0: Conversion stopped 1: Conversion in progress	Always write 0.	Always write 0.	Interrupt specification in conversion channel fixed repeat mode. 0: Every conversion 1: Every fourth conversion	Repeat mode specification. 0: Single conversion 1: Repeat conversion mode	Scan mode specification. 0: Conversion channel fixed mode 1: Conversion channel scan mode	Decoder AD conversion start. 0: Don't care 1: Start conversion Note: Always 0 when read.

AD conversion start

0	Don't care
1	Start AD conversion

Note: Always read as 0.

AD scan mode setting

0	AD conversion channel fixed mode
1	AD conversion channel scan mode

AD repeat mode setting

0	AD single conversion mode
1	AD repeat conversion mode

Specify AD conversion interrupt for channel fixed repeat conversion mode.

	Channel fixed repeat conversion mode <SCAN> = 0, <REPEAT> = 1
0	Generates interrupt every conversion
1	Generates interrupt every fourth conversion

AD conversion busy flag

0	AD conversion stopped
1	AD conversion in progress

AD conversion end flag

0	Before or during AD conversion
1	AD conversion complete

Figure 3.11.2 AD Converter Related Register

AD Mode Control Register 1

ADMOD1 (02B1H)		7	6	5	4	3	2	1	0
	Bit symbol	VREFON	I2AD			ADTRGE	ADCH2	ADCH1	ADCH0
	Read/Write	R/W	R/W			R/W			
	After reset	0	0			0	0	0	0
	Function	VREF application control. 0: Off 1: On	IDLE2 0: Stop 1: Operate			AD external trigger start control. 0: Disable 1: Enable	Analog input channel selection.		

Analog input channel selection.

<ADCH2:0> \ <SCAN>	0 (Channel fixed)	1 (Channel scanned)
000	AN0	AN0
001	AN1	AN0 → AN1
010	AN2	AN0 → AN1 → AN2
011 (Note)	AN3	AN0 → AN1 → AN2 → AN3
100 to 111	–	Use prohibition

AD conversion starts control by external trigger. ($\overline{\text{ADTRG}}$ input)

0	Disabled
1	Enabled

IDLE2 control

0	Stopped
1	In operation

Control of application of reference voltage to AD converter.

0	Off
1	On

Before starting conversion (Before writing 1 to ADMOD0<ADS>), set the <VREFON> bit to 1.

Note: As pin AN3 also functions as the $\overline{\text{ADTRG}}$ input pin, do not set <ADCH2:0> = 011 when using $\overline{\text{ADTRG}}$ with < ADTRGE> = 0.

Figure 3.11.3 AD Converter Related Registers

AD Conversion Data Lower Register 0/4

ADREG04L (02A0H)		7	6	5	4	3	2	1	0
	Bit symbol	ADR01	ADR00						ADR0RF
	Read/Write	R							R
	After reset	Undefined							0
	Function	Stores lower 2 bits of AD conversion result.							AD conversion data storage flag. 1: Conversion result stored

AD Conversion Data Upper Register 0/4

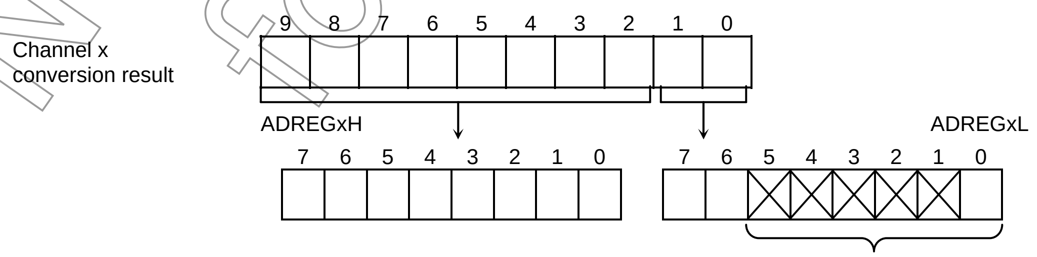
ADREG04H (02A1H)		7	6	5	4	3	2	1	0
	Bit symbol	ADR09	ADR08	ADR07	ADR06	ADR05	ADR04	ADR03	ADR02
	Read/Write	R							
	After reset	Undefined							
	Function	Stores upper 8 bits AD conversion result.							

AD Conversion Data Lower Register 1/5

ADREG15L (02A2H)		7	6	5	4	3	2	1	0
	Bit symbol	ADR11	ADR10						ADR1RF
	Read/Write	R							R
	After reset	Undefined							0
	Function	Stores lower 2 bits of AD conversion result.							AD conversion result flag. 1: Conversion result stored

AD Conversion Data Upper Register 1/5

ADREG15H (02A3H)		7	6	5	4	3	2	1	0
	Bit symbol	ADR19	ADR18	ADR17	ADR16	ADR15	ADR14	ADR13	ADR12
	Read/Write	R							
	After reset	Undefined							
	Function	Stores upper 8 bits of AD conversion result.							



- Bits 5 to 1 are always read as 1.
- Bit0 is the AD conversion data storage flag <ADRxRF>. When the AD conversion result is stored, the flag is set to 1. When either of the registers (ADREGxH, ADREGxL) is read, the flag is cleared to 0.

Figure 3.11.4 AD Converter Related Registers

AD Conversion Result Lower Register 2/6

ADREG26L (02A4H)

	7	6	5	4	3	2	1	0
Bit symbol	ADR21	ADR20						ADR2RF
Read/Write	R							R
After reset	Undefined							0
Function	Stores lower 2 bits of AD conversion result.							AD conversion data storage flag. 1: Conversion result stored

AD Conversion Data Upper Register 2/6

ADREG26H (02A5H)

	7	6	5	4	3	2	1	0
Bit symbol	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24	ADR23	ADR22
Read/Write	R							
After reset	Undefined							
Function	Stores upper 8 bits of AD conversion result.							

AD Conversion Data Lower Register 3/7

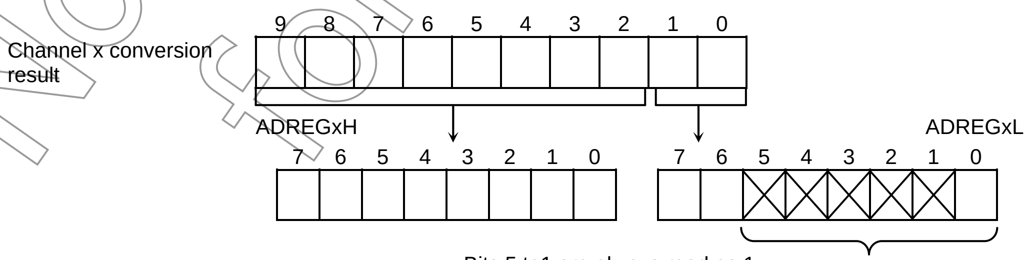
ADREG37L (02A6H)

	7	6	5	4	3	2	1	0
Bit symbol	ADR31	ADR30						ADR3RF
Read/Write	R							R
After reset	Undefined							0
Function	Stores lower 2 bits of AD conversion result.							AD conversion data storage flag. 1: Conversion result stored

AD Conversion Result Upper Register 3/7

ADREG37H (02A7H)

	7	6	5	4	3	2	1	0
Bit symbol	ADR39	ADR38	ADR37	ADR36	ADR35	ADR34	ADR33	ADR32
Read/Write	R							
After reset	Undefined							
Function	Stores upper 8 bits of AD conversion result.							



- Bits 5 to1 are always read as 1.
- Bit0 is the AD conversion data storage flag <ADRxRF>. When the AD conversion result is stored, the flag is set to 1. When either of the registers (ADREGxH, ADREGxL) is read, the flag is cleared to 0.

Figure 3.11.5 AD Converter Related Registers

3.11.2 Description of Operation

(1) Analog reference voltage

A high-level analog reference voltage is applied to the VREFH pin; a low-level analog reference voltage is applied to the VREFL pin. To perform AD conversion, the reference voltage as the difference between VREFH and VREFL, is divided by 1024 using string resistance. The result of the division is then compared with the analog input voltage.

To turn off the switch between VREFH and VREFL, write 0 to ADMOD1<VREFON> in AD mode control register 1. To start AD conversion in the off state, first write 1 to ADMOD1<VREFON>, wait 3 μs until the internal reference voltage stabilizes (this is not related to fc), then set ADMOD0<ADS> to 1.

(2) Analog input channel selection

The analog input channel selection varies depends on the operation mode of the AD converter.

- In analog input channel fixed mode (ADMOD0<SCAN> = 0)
  Setting ADMOD1<ADCH2:0> selects one of the input pins AN0 to AN3 as the input channel.
- In analog input channel scan mode (ADMOD0<SCAN> = 1)
  Setting ADMOD1<ADCH2:0> selects one of the 4 scan modes.

Table 3.11.1 illustrates analog input channel selection in each operation mode.

After reset, ADMOD0<SCAN> = 0 and ADMOD1<ADCH2:0> = 000. Thus pin AN0 is selected as the fixed input channel. Pins not used as analog input channels can be used as standard input port pins.

Table 3.11.1 Analog Input Channel Selection

<ADCH2:0>	Channel Fixed <SCAN> = 0	Channel Scan <SCAN> = 1
000	AN0	AN0
001	AN1	AN0 → AN1
010	AN2	AN0 → AN1 → AN2
011	AN3	AN0 → AN1 → AN2 → AN3
100-111	Use prohibition	Use prohibition

(3) Starting AD conversion

To start AD conversion, write 1 to ADMOD0<ADS> in AD mode control register 0, or ADMOD1<ADTRGE> in AD mode control register 1 and input falling edge on $\overline{\text{ADTRG}}$ pin. When AD conversion starts, the AD conversion busy flag ADMOD0<ADBF> will be set to 1, indicating that AD conversion is in progress.

Writing 1 to ADMOD0<ADS> during AD conversion restarts conversion. At that time, to determine whether the AD conversion results have been preserved, check the value of the conversion data storage flag ADREGxL<ADRxRF>.

During AD conversion, a falling edge input on the $\overline{\text{ADTRG}}$ pin will be ignored.

(4) AD conversion modes and the AD conversion end interrupt

The 4 AD conversion modes are:

- Channel fixed single conversion mode
- Channel scan single conversion mode
- Channel fixed repeat conversion mode
- Channel scan repeat conversion mode

The ADMOD0<REPEAT> and ADMOD0<SCAN> settings in AD mode control register 0 determine the AD mode setting.

Completion of AD conversion triggers an INTAD AD conversion end interrupt request. Also, ADMOD0<EOCF> will be set to 1 to indicate that AD conversion has been completed.

(a) Channel fixed single conversion mode

Setting ADMOD0<REPEAT> and ADMOD0<SCAN> to 00 selects channel fixed single conversion mode.

In this mode, data on one specified channel is converted once only. When the conversion has been completed, the ADMOD0<EOCF> flag is set to 1, ADMOD0 <ADBF> is cleared to 0, and an INTAD interrupt request is generated.

(b) Channel scan single conversion mode

Setting ADMOD0<REPEAT> and ADMOD0<SCAN> to 01 selects channel scan single conversion mode.

In this mode, data on the specified scan channels is converted once only. When scan conversion has been completed, ADMOD0<EOCF> is set to 1, ADMOD0<ADBF> is cleared to 0, and an INTAD interrupt request is generated.

(c) Channel fixed repeat conversion mode

Setting ADMOD0<REPEAT> and ADMOD0<SCAN> to 10 selects channel fixed repeat conversion mode.

In this mode, data on one specified channel is converted repeatedly. When conversion has been completed, ADMOD0<EOCF> is set to 1 and ADMOD0<ADBF> is not cleared to 0 but held 1. INTAD interrupt request generation timing is determined by the setting of ADMOD0<ITM0>.

Setting <ITM0> to 0 generates an interrupt request every time an AD conversion is completed.

Setting <ITM0> to 1 generates an interrupt request on completion of every fourth conversion.

(d) Channel scan repeat conversion mode

Setting ADMOD0<REPEAT> and ADMOD0<SCAN> to 11 selects channel scan repeat conversion mode.

In this mode, data on the specified scan channels is converted repeatedly. When each scan conversion has been completed, ADMOD0<EOCF> is set to 1 and an INTAD interrupt request is generated. ADMOD0<ADBF> is not cleared to 0 but held 1.

To stop conversion in a repeat conversion mode (e.g., in cases (C) and (d)), write 0 to ADMOD0<REPEAT>. After the current conversion has been completed, the repeat conversion mode terminates and ADMOD0<ADBF> is cleared to 0.
Switching to a halt state (IDLE2 mode with ADMOD1<I2AD> cleared to 0, IDLE1 mode or STOP mode) immediately stops operation of the AD converter even when AD conversion is still in progress. In repeat conversion modes (e.g., in cases (C) and (d)), when the halt is released, conversion restarts from the beginning. In single conversion modes (e.g., in cases (a) and (b)), conversion does not restart when the halt is released (the converter remains stopped).

Table 3.11.2 shows the relationship between the AD conversion modes and interrupt requests.

Table 3.11.2 Relationship between AD Conversion Modes and Interrupt Requests

Mode	Interrupt Request Generation	ADMOD0		
		<ITM0>	<REPEAT>	<SCAN>
Channel fixed single conversion mode	After completion of conversion	X	0	0
Channel scan single conversion mode	After completion of scan conversion	X	0	1
Channel fixed repeat conversion mode	Every conversion	0	1	0
	Every forth conversion	1		
Channel scan repeat conversion mode	After completion of every scan conversion	X	1	1

X: Don't care

(e) AD conversion time

84 states (4.7 μs at f_{FPH} = 36 MHz) are required for the AD conversion for one channel.

(f) Storing and reading the results of AD conversion

The AD conversion data upper and lower registers (ADREG04H/L to ADREG37H/L) store the AD conversion results. (ADREG04H/L to ADREG37H/L are read-only registers.)

In channel fixed repeat conversion mode, the conversion results are stored successively in registers ADREG04H/L to ADREG37H/L. In other modes, the AN0, AN1, AN2 and AN3 conversion results are stored in ADREG04H/L, ADREG15H/L, ADREG26H/L and ADREG37H/L respectively.

Table 3.11.3 shows the correspondence between the analog input channels and the registers which are used to hold the results of AD conversion.

Table 3.11.3 Correspondence between Analog Input Channels and AD Conversion Result Registers

Analog Input Channel (Port A)	AD Conversion Result Register	
	Conversion Modes Other than at Right	Channel Fixed Repeat Conversion Mode (<ITM0>=1)
AN0	ADREG04H/L	ADREG04H/L
AN1	ADREG15H/L	ADREG15H/L
AN2	ADREG26H/L	ADREG26H/L
AN3	ADREG37H/L	ADREG37H/L

<ADRxRF>, bit0 of the AD conversion data lower register, is used as the AD conversion data storage flag. The storage flag indicates whether the AD conversion result register has been read or not. When a conversion result is stored in the AD conversion result register, the flag is set to 1. When either of the AD conversion result registers (ADREGxH or ADREGxL) is read, the flag is cleared to 0.

Reading the AD conversion result also clears the AD conversion end flag ADMOD0<EOCF> to 0.

(Setting example)

a. Convert the analog input voltage on the AN3 pin and write the result, to memory address 0800H using the AD interrupt (INTAD) processing routine.

Main routine:

		7	6	5	4	3	2	1	0	
INTE0AD	←	X	1	0	0	–	–	–	–	Enable INTAD and set it to interrupt level 4.
ADMOD1	←	1	1	X	X	0	0	1	1	Set pin AN3 to be the analog input channel.
ADMOD0	←	X	X	0	0	0	0	0	1	Start conversion in channel fixed single conversion mode.

Interrupt routine processing example:

WA	←	ADREG37	Read value of ADREG37L and ADREG37H into 16-bit general-purpose register WA.
WA	> > 6		Shift contents read into WA six times to right and zero-fill upper bits.
(0800H)	←	WA	Write contents of WA to memory address 0800H.

b. This example repeatedly converts the analog input voltages on the three pins AN0, AN1 and AN2, using channel scan repeat conversion mode.

INTE0AD	←	X	0	0	0	–	–	–	–	Disable INTAD.
ADMOD1	←	1	1	X	X	0	0	1	0	Set pins AN0 to AN2 to be the analog input channels.
ADMOD0	←	X	X	0	0	0	1	1	1	Start conversion in channel scan repeat conversion mode.

X: Don’t care, –: No change

3.12 Watchdog Timer (Runaway detection timer)

The TMP91C025 features a watchdog timer for detecting runaway.

The watchdog timer (WDT) is used to return the CPU to normal state when it detects that the CPU has started to malfunction (Runaway) due to causes such as noise.

When the watchdog timer detects a malfunction, it generates a non-maskable interrupt INTWD to notify the CPU. Connecting the watchdog timer output to the Reset pin internally forces a reset. (The level of external $\overline{\text{RESET}}$ pin is not changed.)

3.12.1 Configuration

Figure 3.12.1 is a block diagram of he watchdog timer (WDT).

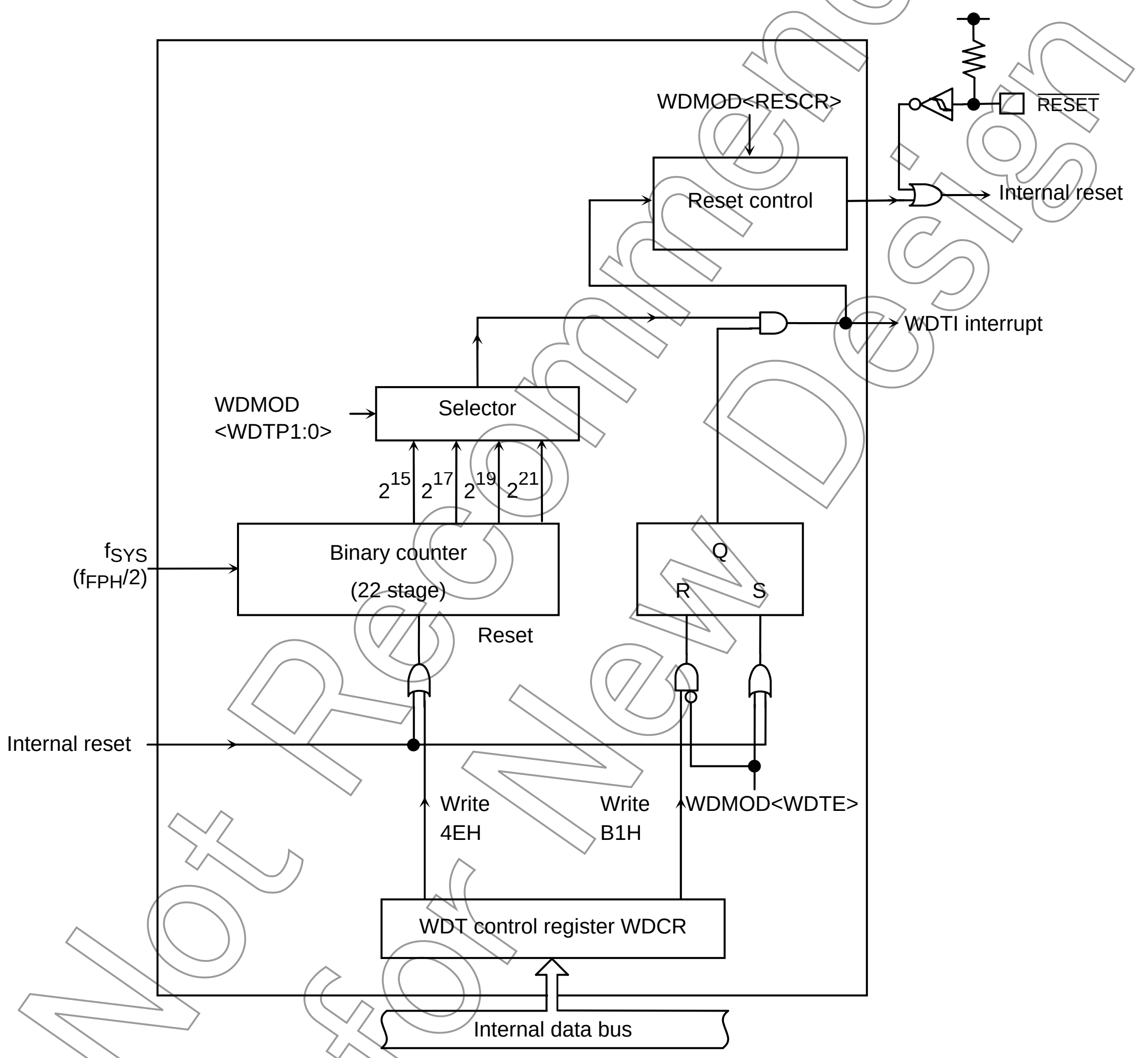


Figure 3.12.1 Block Diagram of Watchdog Timer

Note: It needs to care designing the total machine set, because Watchdog timer can’t operate completely by external noise.

3.12.2 Operation

The watchdog timer generates an INTWD interrupt when the detection time set in the WDMOD<WDTP1:0> has elapsed. The watchdog timer must be cleared 0 by software before an INTWD interrupt will be generated. If the CPU malfunctions (e.g. if runaway occurs) due to causes such as noise, but does not execute the instruction used to clear the binary counter, the binary counter will overflow and an INTWD interrupt will be generated. The CPU will detect malfunction (Runaway) due to the INTWD interrupt and in this case it is possible to return to the CPU to normal operation by means of an anti-malfunction program.

The watchdog timer works immediately after reset.

The watchdog timer does not operate in IDLE1 or STOP mode, as the binary counter continues counting during bus release (When $\overline{\text{BUSAK}}$ goes low).

When the device is in IDLE2 mode, the operation of WDT depends on the WDMOD <I2WDT> setting. Ensure that WDMOD<I2WDT> is set before the device enters IDLE2 mode.

The watchdog timer consists of a 22-stage binary counter which uses the system clock (f_{SYS}) as the input clock. The binary counter can output $f_{SYS}/2^{15}$, $f_{SYS}/2^{17}$, $f_{SYS}/2^{19}$ and $f_{SYS}/2^{21}$.

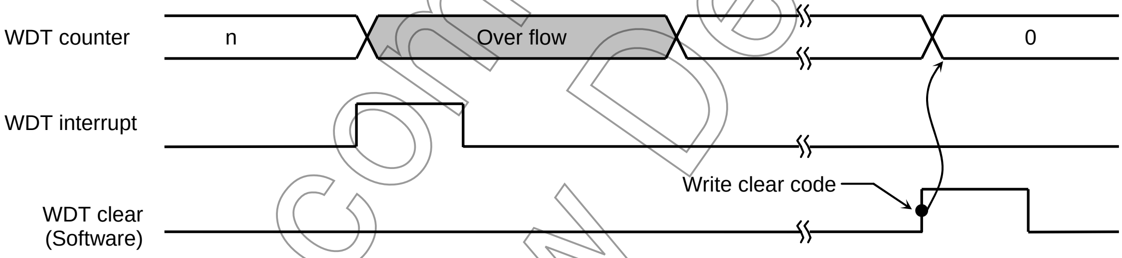


Figure 3.12.2 Normal Mode

The runaway is detected when an overflow occurs, and the watchdog timer can reset device. In this case, the reset time will be between 22 and 29 states (19.6 to 25.8 μs at f_{FPH} = 36MHz, f_{OSCH} = 2.25 state)is $f_{FPH}/2$, where f_{FPH} is generated by dividing the high-speed oscillator clock (f_{OSCH}) by sixteen through the clock gear function.

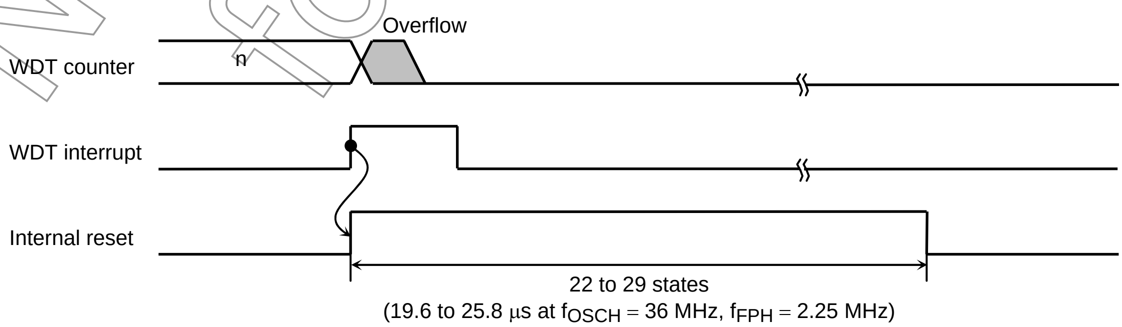


Figure 3.12.3 Reset Mode

3.12.3 Control Registers

The watchdog timer WDT is controlled by two control registers WDMOD and WDCR.

(1) Watchdog timer mode register (WDMOD)

a. Setting the detection time for the watchdog timer in <WDTP1:0>

This 2-bit register is used for setting the watchdog timer interrupt time used when detecting runaway. After reset, this register is initialized to WDMOD<WDTP1:0> = 00.

The detection times for WDT are shown in Figure 3.12.4.

b. Watchdog timer enable/disable control register <WDTE>

After reset, WDMOD<WDTE> is initialized to 1, enabling the watchdog timer. To disable the watchdog timer, it is necessary to set this bit to 0 and to write the disable code (B1H) to the watchdog timer control register WDCR. This makes it difficult for the watchdog timer to be disabled by runaway.

However, it is possible to return the watchdog timer from the disabled state to the enabled state merely by setting <WDTE> to 1.

c. Watchdog timer out reset connection <RESCR>

This register is used to connect the output of the watchdog timer with the RESET terminal internally. Since WDMOD<RESCR>is initialized to 0 on reset, a reset by the watchdog timer will not be performed.

(2) Watchdog timer control register (WDCR)

This register is used to disable and clear the binary counter for the watchdog timer.

Disable control the watchdog timer can be disabled by clearing WDMOD<WDTE> to 0 and then writing the disable code (B1H) to the WDCR register.

```
WDCR    ← 0 1 0 0 1 1 1 0    Write the clear code (4EH).
WDMOD   ← 0 – – X X – – 0    Clear WDMOD<WDTE> to 0.
WDCR    ← 1 0 1 1 0 0 0 1    Write the disable code (B1H).
```

- Enable control

  Set WDMOD<WDTE> to 1.

- Watchdog timer clear control

  To clear the binary counter and cause counting to resume, write the clear code (4EH) to the WDCR register.

```
WDCR    ← 0 1 0 0 1 1 1 0    Write the clear code (4EH).
```

Note1: If it is used disable control, set the disable code (B1H) to WDCR after write the clear code (4EH) once. (Please refer to setting example.)

Note2: If it is changed Watchdog timer setting, change setting after set to disable condition once.

WDMOD (0300H)

	7	6	5	4	3	2	1	0
Bit symbol	WDTE	WDTP1	WDTP0			I2WDT	RESCR	–
Read/Write	R/W	R/W				R/W		R/W
After reset	1	0	0			0	0	0
Function	WDT control 1: Enable	Select detecting time. 00: $2^{15}/f_{SYS}$ 01: $2^{17}/f_{SYS}$ 10: $2^{19}/f_{SYS}$ 11: $2^{21}/f_{SYS}$				IDLE2 0: Stop 1: Operate	1: Internally connects WDT out to the reset pin	Always write 0.

Watchdog timer out control

0	–
1	Connects WDT out to a reset

IDLE2 Control

0	Stop
1	Operation

Watchdog timer detection time

at fc = 36 MHz, fs = 32.768 kHz

SYSCR1 System Clock Selection <SYSCK>	SYSCR1 Gear Value <GEAR2:0>	Watchdog Timer Detection Time WDMOD<WDTP1:0> 00	01	10	11
1 (fs)	XXX	2.0 s	8.0 s	32.0 s	128.0 s
0 (fc)	000 (fc)	1.82 ms	7.28 ms	29.13 ms	116.51 ms
	001 (fc/2)	3.64 ms	14.56 ms	58.25 ms	233.02 ms
	010 (fc/4)	7.28 ms	29.13 ms	116.51 ms	466.03 ms
	011 (fc/8)	14.56 ms	58.25 ms	233.02 ms	932.07 ms
	100 (fc/16)	29.13 ms	116.51 ms	466.03 ms	1864.14 ms

Watchdog timer enable/disable control

0	Disabled
1	Enabled

Figure 3.12.4 Watchdog Timer Mode Register

		7	6	5	4	3	2	1	0
WDCR	Bit symbol	–							
(0301H)	Read/Write	W							
	After reset	–							
Read-modify -write instructions are prohibited.	Function	B1H: WDT disable code 4EH: WDT clear code							

Disable/clear WDT

B1H	Disable code
4EH	Clear code
Others	Don’t care

Figure 3.12.5 Watchdog Timer Control Register

3.13 Real Time Clock (RTC)

3.13.1 Function Description for RTC

1) Clock function (hour, minute, second)
2) Calendar function (month and day, day of the week, and leap year)
3) 24- or 12-hour (AM/PM) clock function
4) ± 30 second adjustment function (by software)
5) Alarm function (Alarm output
6) Alarm interrupt generate

3.13.2 Block Diagram

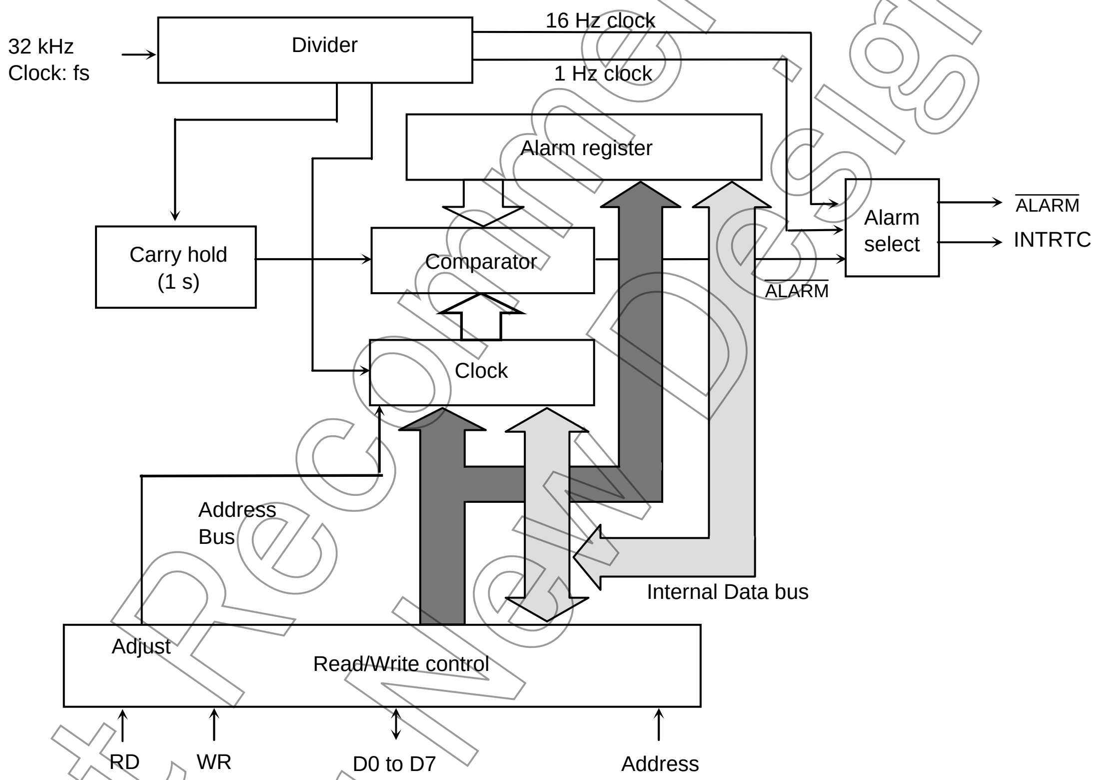


Figure 3.13.1 Block Diagram

Note 1: The Christian era year column:

This product has year column toward only lower two columns. Therefore the next year in 99 works as 00 years. In system to use it, please manage upper two columns with the system side when handle year column in the christian era.

Note 2: Leap year:

A leap year is the year which is divisible with 4, but the year which there is exception, and is divisible with 100 is not a leap year. However, the year which is divisible with 400 is a leap year. But there is not this product for the correspondence to the above exception. Because there are only with the year which is divisible with 4 as a leap year, please cope with the system side if this function is problem.

3.13.3 Control Registers

Table 3.13.1 PAGE 0 (Clock function) Registers

Symbol	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Read/Write
SECR	0320H		40 s	20 s	10 s	8 s	4 s	2 s	1 s	Second column	R/W
MINR	0321H		40 min.	20 min.	10 min.	8 min.	4 min.	2 min.	1 min.	Minute column	R/W
HOURR	0322H			20 /PM/AM	10 hours	8 hours	4 hours	2 hours	1 hour	Hour column	R/W
DAYR	0323H						W2	W1	W0	Day of the week column	R/W
DATER	0324H			Day 20	Day 10	Day 8	Day 4	Day 2	Day 1	Day column	R/W
MONTHR	0325H				Oct.	Aug.	Apr.	Feb.	Jan.	Month column	R/W
YEARR	0326H	Year 80	Year 40	Year 20	Year 10	Year 8	Year 4	Year 2	Year 1	Year column (Lower two columns)	R/W
PAGER	0327H	Interrupt enable			Adjust -ment function	Clock enable	Alarm enable		PAGE setting	PAGE register	W, R/W
RESTR	0328H	1Hz enable	16Hz enable	Clock reset	Alarm reset	Always write "0"				Reset register	W only

Note: As for SECR, MINR, HOURR, DAYR, MONTHR, YEARR of PAGE0, current state is read when read it.

Table 3.13.2 PAGE 1 (Alarm function) Registers

Symbol	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Read/Write
SECR	0320H										R/W
MINR	0321H		40 min.	20 min.	10 min.	8 min.	4 min.	2 min.	1 min.	Minute column for alarm	R/W
HOURR	0322H			20 /PM/AM	10 hours	8 hours	4 hours	2 hours	1 hour	Hour column for alarm	R/W
DAYR	0323H						W2	W1	W0	Day of the week column for alarm	R/W
DATER	0324H			Day 20	Day 10	Day 8	Day 4	Day 2	Day 1	Day column for alarm	R/W
MONTHR	0325H								24/12	24-hour clock mode	R/W
YEARR	0326H							Leap-year setting		Leap-year mode	R/W
PAGER	0327H	Interrupt enable			Adjust -ment function	Clock enable	Alarm enable		PAGE setting	PAGE register	W, R/W
RESTR	0328H	1Hz enable	16Hz enable	Clock reset	Alarm reset	Always write "0"				Reset register	W only

Note: As for MINR, HOURR, DAYR, MONTHR, YEARR of PAGE1, current state is read when read it.

3.13.4 Detailed Explanation of Control Register

RTC is not initialized by reset.
Therefore, all registers must be initialized at the beginning of the program.

(1) Second column register (for PAGE0 only)

SECR (0320H)

		7	6	5	4	3	2	1	0
SECR (0320H)	Bit symbol		SE6	SE5	SE4	SE3	SE2	SE1	SE0
	Read/Write		R/W						
	After reset		Undefined						
	Function	"0" is read.	40 sec. column	20 sec. column	10 sec. column	8 sec. column	4 sec. column	2 sec. column	1 sec. column

0	0	0	0	0	0	0	0 sec
0	0	0	0	0	0	1	1 sec
0	0	0	0	0	1	0	2 sec
0	0	0	0	0	1	1	3 sec
0	0	0	0	1	0	0	4 sec
0	0	0	0	1	0	1	5 sec
0	0	0	0	1	1	0	6 sec
0	0	0	0	1	1	1	7 sec
0	0	0	1	0	0	0	8 sec
0	0	0	1	0	0	1	9 sec
0	0	1	0	0	0	0	10 sec
			:				
0	0	1	1	0	0	1	19 sec
0	1	0	0	0	0	0	20 sec
			:				
0	1	0	1	0	0	1	29 sec
0	1	1	0	0	0	0	30 sec
			:				
0	1	1	1	0	0	1	39 sec
1	0	0	0	0	0	0	40 sec
			:				
1	0	0	1	0	0	1	49 sec
1	0	1	0	0	0	0	50 sec
			:				
1	0	1	1	0	0	1	59 sec

Note: Do not set the data other than showing above.

(2) Minute column register (for PAGE0/1)

MINR
(0321H)

	7	6	5	4	3	2	1	0
Bit symbol		MI6	MI5	MI4	MI3	MI2	MI1	MI0
Read/Write		R/W						
After reset		Undefined						
Function	"0" is read.	40 min, column	20 min, column	10 min, column	8 min, column	4 min, column	2 min, column	1 min, column

0	0	0	0	0	0	0	0 min.
0	0	0	0	0	0	1	1 min.
0	0	0	0	0	1	0	2 min.
0	0	0	0	0	1	1	3 min.
0	0	0	0	1	0	0	4 min.
0	0	0	0	1	0	1	5 min.
0	0	0	0	1	1	0	6 min.
0	0	0	0	1	1	1	7 min.
0	0	0	1	0	0	0	8 min.
0	0	0	1	0	0	1	9 min.
0	0	1	0	0	0	0	10 min.
			:				
0	0	1	1	0	0	1	19 min.
0	1	0	0	0	0	0	20 min.
			:				
0	1	0	1	0	0	1	29 min.
0	1	1	0	0	0	0	30 min.
			:				
0	1	1	1	0	0	1	39 min.
1	0	0	0	0	0	0	40 min.
			:				
1	0	0	1	0	0	1	49 min.
1	0	1	0	0	0	0	50 min.
			:				
1	0	1	1	0	0	1	59 min.

Note: Do not set the data other than showing above.

(3) Hour column register (for PAGE0/1)

a. In case of 24-hour clock mode (MONTHR<MO0> = 1) of PAGE1

		7	6	5	4	3	2	1	0
HOURR (0322H)	Bit symbol			HO5	HO4	HO3	HO2	HO1	HO0
	Read/Write			R/W					
	After reset			Undefined					
	Function	"0" is read.		20 hour column	10 hour column	8 hour column	4 hour column	2 hour column	1 hour column

0	0	0	0	0	0	0 o’clock
0	0	0	0	0	1	1 o’clock
0	0	0	0	1	0	2 o’clock
			:			
0	0	1	0	0	0	8 o’clock
0	0	1	0	0	1	9 o’clock
0	1	0	0	0	0	10 o’clock
			:			
0	1	1	0	0	1	19 o’clock
1	0	0	0	0	0	20 o’clock
			:			
1	0	0	0	1	1	23 o’clock

Note: Do not set the data other than showing above.

b. In case of 12-hour clock mode (MONTHR<MO0> = 0) of PAGE1

		7	6	5	4	3	2	1	0
HOURR (0322H)	Bit symbol			HO5	HO4	HO3	HO2	HO1	HO0
	Read/Write			R/W					
	After reset			Undefined					
	Function	"0" is read.		PM/AM	10 hour column	8 hour column	4 hour column	2 hour column	1 hour column

0	0	0	0	0	0	0 o’clock (AM)
0	0	0	0	0	1	1 o’clock
0	0	0	0	1	0	2 o’clock
			:			
0	0	1	0	0	1	9 o’clock
0	1	0	0	0	0	10 o’clock
0	1	0	0	0	1	11 o’clock
1	0	0	0	0	0	0 o’clock (PM)
1	0	0	0	0	1	1 o’clock

Note: Do not set the data other than showing above.

(4) Day of the week column register (for PAGE0/1)

DAYR (0323H)		7	6	5	4	3	2	1	0
	Bit symbol						WE2	WE1	WE0
	Read/Write						R/W		
	After reset						Undefined		
	Function	"0" is read.					W2	W1	W0

0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

Note: Do not set the data other than showing above.

(5) Day column register (for PAGE0/1)

DATER (0324H)		7	6	5	4	3	2	1	0
	Bit symbol			DA5	DA4	DA3	DA2	DA1	DA0
	Read/Write			R/W					
	After reset			Undefined					
	Function	"0" is read.		Day 20	Day 10	Day 8	Day 4	Day 2	Day 1

0	0	0	0	0	0	0
0	0	0	0	0	1	1st day
0	0	0	0	1	0	2nd day
0	0	0	0	1	1	3rd day
0	0	0	1	0	0	4th day
			:			
0	0	1	0	0	1	9th day
0	1	0	0	0	0	10th day
0	1	0	0	0	1	11th day
			:			
0	1	1	0	0	1	19th day
1	0	0	0	0	0	20th day
			:			
1	0	1	0	0	1	29th day
1	1	0	0	0	0	30th day
1	1	0	0	0	1	31st day

Note1: Do not set the data other than showing above.

Note2: Do not set the day which is not existed. (ex: 30th Feb)

(6) Month column register (for PAGE0 only)

		7	6	5	4	3	2	1	0
MONTHR (0325H)	Bit symbol				MO4	MO4	MO2	MO1	MO0
	Read/Write				R/W				
	After reset				Undefined				
	Function	"0" is read.			10 months	8 months	4 months	2 months	1 month

0	0	0	0	1	January
0	0	0	1	0	February
0	0	0	1	1	March
0	0	1	0	0	April
0	0	1	0	1	May
0	0	1	1	0	June
0	0	1	1	1	July
0	1	0	0	0	August
0	1	0	0	1	September
1	0	0	0	0	October
1	0	0	0	1	November
1	0	0	1	0	December

Note: Do not set the data other than showing above.

(7) Select 24-hour clock or 12-hour clock (for PAGE1 only)

		7	6	5	4	3	2	1	0
MONTHR (0325H)	Bit symbol								MO0
	Read/Write								R/W
	After reset								Undefined
	Function	"0" is read.							0: 12-hour 1: 24-hour

(8) Year column register (for PAGE0 only)

YEARR (0326H)

	7	6	5	4	3	2	1	0
Bit symbol	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0
Read/Write	R/W							
After reset	Undefined							
Function	80 Years	40 Years	20 Years	10 Years	8 Years	4 Years	2 Years	1 Year

0	0	0	0	0	0	0	0	00 years
0	0	0	0	0	0	0	1	01 years
0	0	0	0	0	0	1	0	02 years
0	0	0	0	0	0	1	1	03 years
0	0	0	0	0	1	0	0	04 years
0	0	0	0	0	1	0	1	05 years
				:				
1	0	0	1	1	0	0	1	99 years

Note: Do not set the data other than showing above.

(9) Leap-year register (for PAGE1 only)

YEARR (0326H)

	7	6	5	4	3	2	1	0
Bit symbol							LEAP1	LEAP0
Read/Write							R/W	
After reset							不定	
Function							00: Leap-year 01: One year leap year 10: Two years leap year 11: Three years leap year	

0	0	Current year is leap year
0	1	Present is next year of a leap year
1	0	Present is two years after a leap year
1	1	Present is three years after leap year

(10) PAGE register setting (for PAGE0/1)

		7	6	5	4	3	2	1	0
PAGER (0327H)	Bit symbol	INTENA			ADJUST	ENATMR	ENAALM		PAGE
Read-modify write instruction are prohibited	Read/Write	R/W			W	R/W			R/W
	After reset	0			Undefined	Undefined			Undefined
	Function	INTRTC 1: Enable 0: Disable	"0" is read.		0:Don't care 1:Adjust	Clock 1: Enable 0: Disable	ALARM 1: Enable 0: Disable	"0" is read.	PAGE selection

Note: Please keep the setting order below of <ENATMR>, <ENAAML> and <INTENA>. Set different times for Clock/Alarm setting and interrupt setting

(Example) Clock setting/Alarm setting

```
ld    (pager), 0ch    :    Clock, Alarm enable

ld    (pager), 8ch    :    Interrupt enable
```

PAGE	0	Select Page0
	1	Select Page1

ADJUST	0	Don't care
	1	Adjust sec. counter. When set this bit is set to "1" the sec. counter becomes to "0" when the value of the sec. counter is 0 – 29.When the value of sec. counter is 30-59, the min. counter is carried and sec. counter becomes "0". Output Adjust signal during 1 cycle of f_{SYS}. After being adjusted once, Adjust is released automatically. (PAGE0 only)

(11) Reset register setting (for PAGE0/1)

		7	6	5	4	3	2	1	0
RESTR (1328H)	Bit symbol	DIS1Hz	DIS16Hz	RSTTMR	RSTALM	RE3	RE2	RE1	RE0
Read-modify write instruction are prohibited	Read/Write	W							
	After reset	Undefined							
	Function	1Hz 0: Enable 1: Disable	16Hz 0: Enable 1: Disable	1: Clock reset	1: Alarm reset	Always write "0"			

RSTALM	0	Unused
	1	Reset alarm register

RSTTMR	0	Unused
	1	Reset Counter

<DIS1HZ>	<DIS1HZ>	PAGER<ENAALM>	Source signal
1	1	1	Alarm
0	1	0	1Hz
1	0	0	16Hz
Others			Output "0"

3.13.5 Operational description

(1) Reading clock data

1. Using 1Hz interrupt

1Hz interrupt and the count up of internal data synchronize. Therefore, data can read correctly if reading data after 1Hz interrupt occurred.

2. Using two times reading

There is a possibility of incorrect clock data reading when the internal counter carries over. To ensure correct data reading, please read twice, as follows:

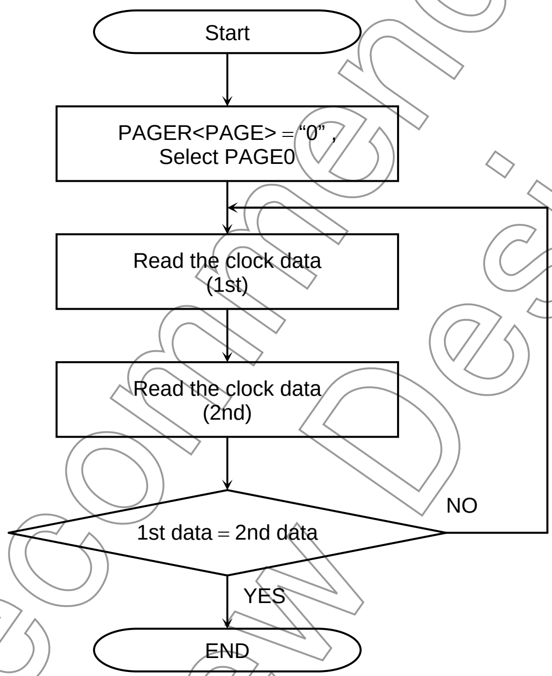


Figure 3.13.2 Flowchart of clock data read

(2) Writing clock data

When a carry over occurs during a write operation, the data cannot be written correctly. Please use the following method to ensure data is written correctly.

1. Using 1Hz interrupt

   1Hz interrupt and the count up of internal data synchronize. Therefore, data can write correctly if writing data after 1Hz interrupt occurred.

2. Resets counter

   There are 15-stage counter inside the RTC, which generates a 1Hz clock from 32,768 KHz. The data is written after reset this counter.

   However, if clearing the counter, it is counted up only first writing at half of the setting time, first writing only. Therefore, if setting the clock counter correctly, after clearing the counter, set the 1Hz-interrupt to enable. And set the time after the first interrupt (occurs at 0.5Hz) is occurred.

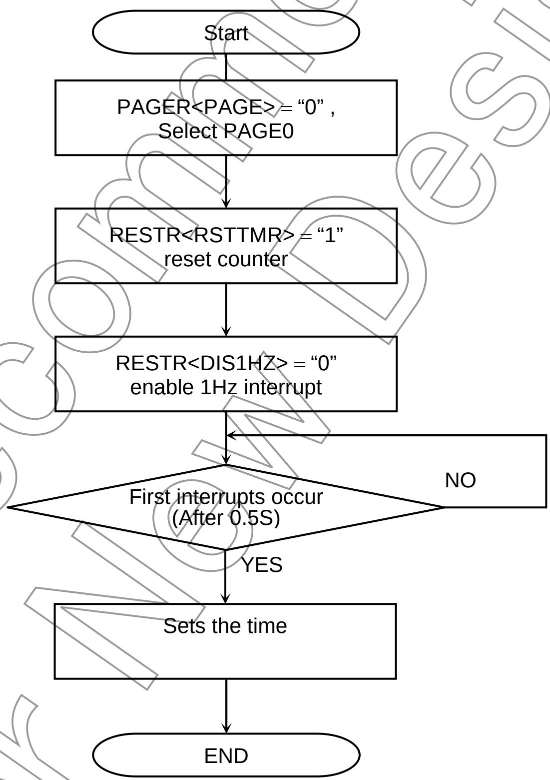


Figure 3.13.3 Flowchart of data write

3. Disabling the clock

A clock carry over is prohibited when "0" is written to PAGER<ENATMR> in order to prevent malfunction caused by the Carry hold circuit. While the clock is prohibited, the Carry hold circuit holds a one sec. carry signal from a divider. When the clock becomes enabled, the carry signal is output to the clock, the time is revised and operation continues. However, the clock is delayed when clock-disabled state continues for one second or more. Note that at this time system power is down while the clock is disabled. In this case the clock is stopped and clock is delayed.

During clock disabling, pay attention with system power is downed. In this case the clock is stopped and time is delayed.

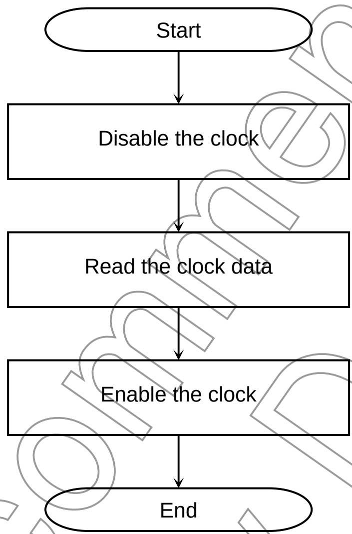


Figure 3.13.4 Flowchart of Clock disable

3.13.6 Explanation of the interrupt signal and alarm signal

The alarm function used by setting the PAGE1 register and outputting either of the following three signals from $\overline{\text{ALARM}}$ pin as follows by write writing “1” to PAGER<PAGE>. INTRTC outputs a 1-shot pulse when the falling edge is detected. RTC is not initializes initialized by RESET. Therefore, when the clock or alarm function is used, clear interrupt request flag in INTC (interrupt controller).

(1) When the alarm register and the timer clock correspond, output “0”.

(2) 1Hz Output clock of 1Hz.

(3) 16Hz Output clock of 16Hz.

(1) In accordance with alarm register and a clock, output “0”.

When value of a clock of PAGE0 accorded with alarm register of PAGE1 with a state of PAGER<ENAALM>= “1”, output “0” to $\overline{\text{ALARM}}$ pin and occur INTRTC.

Follows are ways using alarm.

Initialization of alarm is done by writing in “1” at RESTR<RSTALM>, setting value of all alarm becomes don’t care. In this case, always accorded with value of a clock and request INTRTC interrupt if PAGER<ENAALM> is “1”.

Setting alarm min., alarm hour, alarm day and alarm the day week are done by writing in data at each register of PAGE1.

When all setting contents accorded, RTC generates INTRTC interrupt, if PAGER<INTENA><ENAALM> is “1”. However, contents (don't care state) which does not set it up is considered to always accord.

The contents, which set it up once, cannot be returned to don't care state in independence. Initialization of alarm and resetting of alarm register set to “Don’t care”.

The following is an example program for outputting alarm from $\overline{\text{ALARM}}$ -pin at noon (PM12:00) every day.

```
  LD    (PAGER), 09H     ;  Alarm disable, setting PAGE1
  LD    (RESTR), D0H     ;  Alarm initialize
  LD    (DAYR), 01H      ;  W0
  LD    (DATAR),01H         1 day
  LD    (HOURR), 12H     ;  Setting 12 o’clock
  LD    (MINR), 00H      ;  Setting 00 min
                         ;  Set up time 31 μs (Note)
  LD    (PAGER), 0CH     ;  Alarm enable
( LD    (PAGER), 8CH     ;  Interrupt enable )
```

When CPU is operated by high frequency oscillation, it may take a maximum of one clock at 32 kHz (about 30μs) for the time register setting to become valid. In the above example, it is necessary to set 31μs of set up time between setting the time register and enabling the alarm register.

Note: This set up time is unnecessary when you use only internal interruption.

(2) With 1Hz output clock

RTC outputs clock of 1Hz to $\overline{\text{ALARM}}$ pin by setting up PAGER<ENAALM> = “0”, RESTR<DIS1HZ> = “0”, <DIS16HZ>= “1”. RTC also generates an INTRTC interrupt of the falling edge of the clock.

(3) With 16Hz output clock

RTC outputs clock of 16Hz to $\overline{\text{ALARM}}$ pin by setting up PAGER<ENAALM> = “0”, RESTR<DIS1HZ> = “1”, <DIS16HZ> = “0”. RTC also generates INTRTC an interrupt on the falling edge of the clock.

3.14 LCD Driver Controller (LCDC)

The TMP91C025 incorporates two types liquid crystal display driving circuit for controlling LCD driver LSI.

One circuit handles a RAM build-in type LCD driver that can store display data in the LCD driver in itself, and the other circuit handles a shift-register type LCD driver that must serially transfer the display data to LCD driver for each display picture.

- Shift-register type LCD driver control mode (SR mode)

  Set the mode of operation, start address of source data save memory and LCD size to control register before setting start register.

  After set start register LCDC outputs bus release request to CPU and read data from source memory. After that LCDC transmits data of volume of LCD size to external LCD driver through data bus.

  At this time, control signals (D1BSCP etc.) connected LCD driver output specified waveform synchronizes with data transmission.

  After finish data transmission, LCDC cancels the bus release request and CPU will restart.

- RAM built-in type LCD driver control mode (RAM mode)

  Data transmission to LCD driver is executed by move instruction of CPU.

  After setting mode of operation to control register, when move instruction of CPU is executed LCDC outputs chip select signal to LCD driver connected to the outside from control pin. (D1BSCP etc.)

  Therefore control of data transmission numbers corresponding to LCD size is controlled by instruction of CPU.

- Special mode

  It is assigned <TA3LCDE> at bit6 and <TA3MLDE> at bit4, of EMCCR0 register (00E3hex). These bits are used when you want to operate LCDD and MELODY circuit without low frequency clock (XT1, XT2). After reset these two bits are set to "0" and low clock is supplied each LCDD and MELODY circuit. If you write these bits to 1, TA3OUT (Generate by timer 3) is supplied each LCDD and MELODY circuit. In this case, you should set 32 kHz timer 3 frequency. For detail, look AC specification characteristics.

This section is constituted as follows.

3.14.1 Feature of LCDC of Each Mode
3.14.2 Block Diagram
3.14.3 Control Registers
3.14.4 Shift-register Type LCD Driver Control Mode (SR type)
  3.14.4.1 Settlement of Frame Frequency Function
  3.14.4.2 Timer Out LCDCK
  3.14.4.3 Transfer Time by Data Bus Width
  3.14.4.4 LCDC Operation in HALT Mode
3.14.5 RAM Built-in Type LCD Driver Control Mode (RAM Type)

3.14.1 Feature of LCDC of Each Mode

Each feature and operation of pin is as follows.

Table 3.14.1 Feature of LCDC of Each Mode

		Shift-register Type LCD Driver Control Mode	RAM Built-in Type LCD Driver Control Mode
The number of picture elements can be handled		Common (row): 64, 68, 80, 100, 120, 128, 144, 160, 200, 240 Segment (column): 32, 64, 80, 120, 128, 160, 240, 320, 360	There is not a limitation
Receiver data bus width		8 bits, 16 bits selectable	8 bit, 16 bit, selectable (depend on CPU command)
Transfer data bus width		8 bits, 4 bits selectable	8-bit fixed
Transfer rate (at f_{FPH} = 16 MHz)		250 ns/1 byte at Byte mode 375 ns/1 byte at Nibble mode	Equal to memory cycle
External pins	Data Bus: (D7 to D0)	Data bus: Connect with DI pin of column driver. Upper 7 pins do not use in byte mode and upper 4 pins do not use in nibble mode.	Data bus: Connect with DB pin of column/row driver.
	Write Strobe: ($\overline{WR}$)	not used	Write strobe: Connect with /WR pin of column/row driver.
	Address Bus: (A0)	not used	Address 0: Connect with D/I pin of column driver. When A0 = 1 data bus value means display data, when A0 = 0 data bus means instruction data.
	Shift Clock Pulse: (D1BSCP)	Shift clock pulse: Connect with SCP pin of column driver. LCD driver latches data bus value by falling edge of this pin.	Chip enable for column driver 1: Connect with $\overline{CE}$ pin of column driver 1.
	Latch Pulse: (D2BLP)	Latch pulse output: Connect with LP/EIO1 pin of column/row driver. Display data is latched in output buffer in LCD driver by rising edge of this pin.	Chip enable for column driver 2: Connect with $\overline{CE}$ pin of column driver 2.
	Frame: (D3BFR)	LCD frame output: Connect with FR pin of column/row driver.	Chip enable for column driver 3: Connect with/ $\overline{CE}$ pin of column driver 3.
	Cascade Pulse: (DLEBCD)	Cascade pulse output: Connect with DIO1 pin of row driver. This pin outputs 1 shot pulse by every D3BFR pin changes.	Chip enable for row driver: Connect with $\overline{LE}$ pin of row driver.
	Display Off: ($\overline{DOFF}$)	Display off output: Connect with /DSPOF terminal of column/row driver. L means display off and H means display on.	

3.14.2 Block Diagram

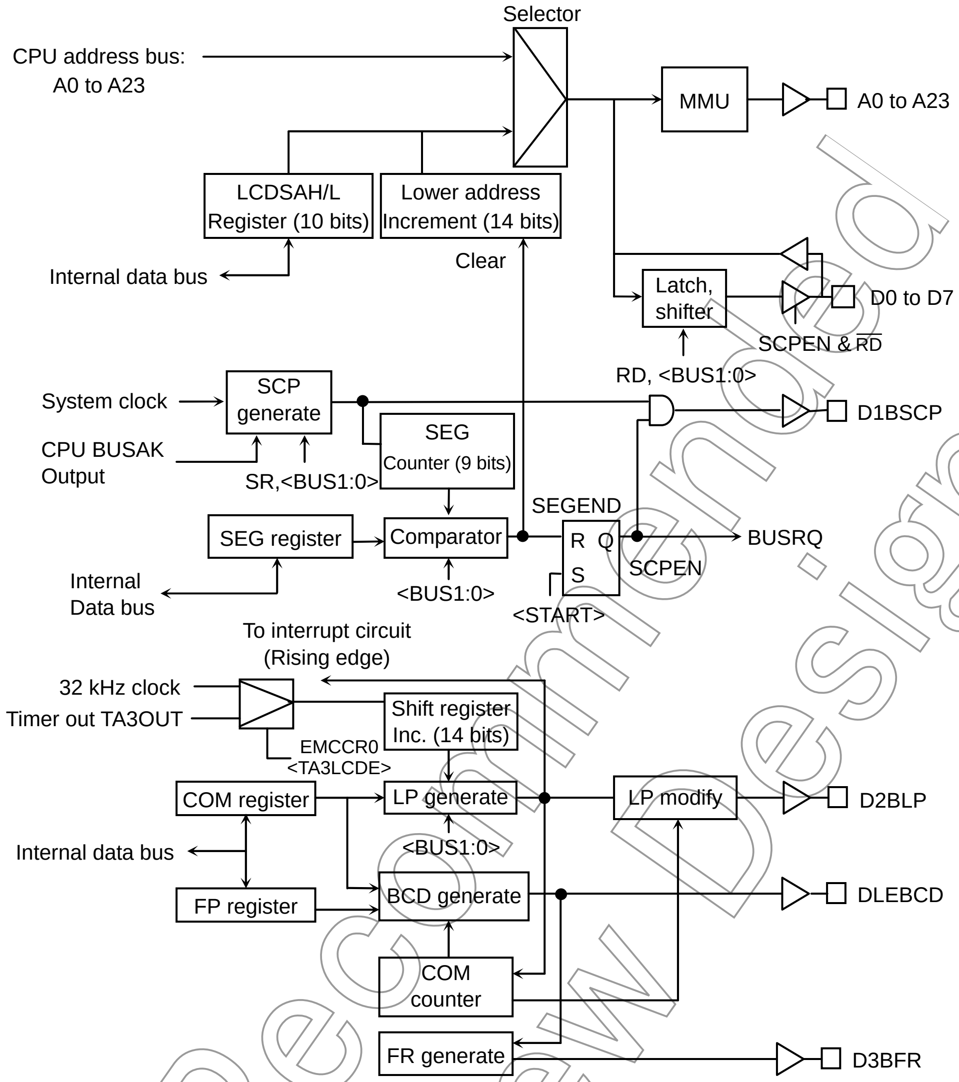


Figure 3.14.1 LCDC Block Diagram

3.14.3 Control Registers

LCDSAL Register

		7	6	5	4	3	2	1	0
LCDSAL (0360H)	Bit symbol	SAL15	SAL14	SAL13	SAL12		−	−	MODE
	Read/Write	R/W	R/W	R/W	R/W		R/W	R/W	R/W
	After reset	0	0	0	0		0	0	0
	Function	SR mode Display memory address. (Low: A15 to A12)					Always write 0.	Always write 0.	Mode select 0: RAM 1: SR

LCDSAH Register

		7	6	5	4	3	2	1	0
LCDSAH (0361H)	Bit symbol	SAL23	SAL22	SAL21	SAL20	SAL19	SAL18	SAL17	SAL16
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	After reset	0	0	0	0	0	0	0	0
	Function	SR mode Display memory address. (High: A23 to A16)							

LCDSIZE Register

		7	6	5	4	3	2	1	0
LCDSIZE (0362H)	Bit symbol	COM3	COM2	COM1	COM0	SEG3	SEG2	SEG1	SEG0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	After reset	0	0	0	0	0	0	0	0
	Function	LCD common number. (SR mode) 0000: 64 0101: 128 0001: 68 0110: 144 0010: 80 0111: 160 0011: 100 1000: 200 0100: 120 1001: 240 Other: Reserved				LCD segment number. (SR mode) 0000: 32 0101: 160 0001: 64 0110: 240 0010: 80 0111: 320 0011: 120 1000: 360 0100: 128 Other: Reserved			

LCDCTL Register

		7	6	5	4	3	2	1	0
LCDCTL (0363H)	Bit symbol	LCDON	−	−	BUS1	BUS0	MMULCD	FP8	START
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	After reset	0	0	0	0	0	0	0	0
	Function	$\overline{\text{DOFF}}$ (SR,RAM mode) 0: Off 1: On	Always write 0.	Always write 0.	Data bus width. (SR mode) 00: 8 bits (Byte mode) 01: 4 bits (Nibble mode) 10: Reserved 11: Reserved		Type selection LCDD (build in RAM). 0: Sequential 1: Random	Setting bit8 for f_{FP}.	Start control. (SR mode) 0: Stop 1: Start

Note 1: There is a limitation about to set LCDSAH and LCDSAL start address.
It prohibit to set A13 carry to A14 by all 1-frame data transmitting.
e.g. In case 240 (Row) × 360 (Column): 2a30 bytes
Start address of LCDC: SAL15 to SAL12 = 0000 or 0001;

Note 2: Initial incrementer's address (LSB 14 bits) for LCDC DMA is 0000 (hex).

LCDFFP Register

LCDFFP (0364H)		7	6	5	4	3	2	1	0
	Bit symbol	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
	Read/Write	R/W							
	After reset	0	0	0	0	0	0	0	0
	Function	Setting bit7 to bit0 for f_{FP}.							

LCDCTR2 Register

LCDCTL2 (0366H)		7	6	5	4	3	2	1	0
	Bit symbol	–	–	–			RAMBUS	AC1	AC0
	Read/Write	R/W	R/W	R/W			R/W	R/W	R/W
	After reset	0	0	0			0	0	0
	Function	Always write to “111”.					0: Byte 1: Word	00: Type A 01: Type B 10: Type C 11: Reserved	

Note: Please write bit7:5 to “111”, even if you use <RAMBUS>, <AC1> and <AC0> as initial setting.

LCDC1L/LCDC1H/LCDC2L/LCDC2H/LCDC3L/LCDC3H/LCDR1L/LCDR1H Register

	7	6	5	4	3	2	1	0
Bit symbol	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write	Depend on the specification of external LCD driver.							
After reset	Depend on the specification of external LCD driver.							
Function	Depend on the specification of external LCD driver.							

These registers do not exist on TMP91C025. These are image for instruction registers and display registers of external RAM built-in sequential access type (Note) LCD driver.

Address as Table 3.14.2 is assigned to these registers, and the following chip enable pin becomes active when accesses corresponding address.

And, the area of these address is external area, so $\overline{RD}$, $\overline{WR}$ terminal becomes active by external access. Table 3.14.3 shows the address map in the case of controlling RAM built-in random access type (Note) LCD driver.

The explanation part of MMU circuit also explains this. This setup is performed by LCDCTL<MMULCD>.

Table 3.14.2 Memory Mapping for Direct Addressed Built-in RAM Type

Register	Address	Purpose Sequential Access Type		Chip Enable Terminal	A0 Terminal
LCDC1L	0FE0H	RAM built-in type column driver 1	Instruction	D1BSCP	0
LCDC1H	0FE1H		Display data		1
LCDC2L	0FE2H	RAM built-in type column driver 2	Instruction	D2BLP	0
LCDC2H	0FE3H		Display data		1
LCDC3L	0FE4H	RAM built-in type column driver 3	Instruction	D3BFR	0
LCDC3H	0FE5H		Display data		1
LCDR1L	0FE6H	RAM built-in type row driver	Instruction	DLEBCD	0
LCDR1H	0FE7H		Display data		1

Table 3.14.3 Memory Mapping for Built-in RAM Random Access Type

Address	Purpose Random Access Type	Chip Enable Terminal
3C0000H to 3CFFFFH	RAM built-in type driver 1	D1BSCP
3D0000H to 3DFFFFH	RAM built-in type driver 2	D2BLP
3E0000H to 3EFFFFH	RAM built-in type driver 3	D3BFR
3F0000H to 3FFFFFH	RAM built-in type driver 4	DLEBCD

Note: We call built-in RAM sequential access type LCD driver that use register to access to display-ram without address. (e.g., T6B65A,T6C84 etc: mar/2000)

We call built-in RAM random access type LCD driver that is same method to access to SRAM. (e.g., T6C23, T6K01 etc: mar/2000)

3.14.4 Shift-register Type LCD Driver Control Mode (SR type)

Set the mode of operation, start address of source data save memory and LCD size to control registers before setting start register.

After set start register LCDC outputs bus release request to CPU and read data from source memory.

After that LCDC transmits data of volume of LCD size to external LCD driver through data bus.

At this time, control signals (D1BSCP etc.) connected LCD driver output specified waveform synchronizes with data transmission.

After finish data transmission, LCDC cancels the bus release request and CPU will re-start.

LCDC timing figure in the case of 240 seg × 120 com and BYTE mode is shown in Figure 3.14.2, Figure 3.14.3.

The table of t_{LP} (D2BLP pin cycle) by the number of segments and the common number and CPU stop time/stop ratio are shown in Table 3.14.4. And, f_{FP} (Frame frequency) by the common number is shown in Table 3.14.5.

Moreover, the example of a 240 seg × 120 com LCD driver connection circuit is shown in Figure 3.14.5.

3.14.4.1 Settlement of Frame Frequency Function

TMP91C025 defines so-called frame period (Refresh interval for LCD panel) by the value set in f_{FP} [8:0]. DLEBCD pin outputs pulse every frame period. DLEBFR pin usually outputs the signal inverts polarity every frame period.

Basic frame period: DLEBCD signal, is made according to the resister f_{FP} [8:0] setting mentioned before. However this f_{FP} [8:0] setting is generally equal to common number, frame period can be corrected by increasing f_{FP} [8:0] with ease.

The equation can calculate frame period.

Frame period = LCDCK/ (D x f_{FP}) [Hz] D: Constant for each common (Table 3.14.5)
f_{FP}: Setting of f_{FP} [8:0] resister
LCDCK: Source clock of LCD
(Low clock is usually selected)

Please select the value of f_{FP} [8:0] as the frame period you want to set in the Table 3.14.5.

Note: Please make the value set to f_{FP} [8:0] into the following range.
COM (Common number) ≤ FR ≤ 320

Example: In the case where frame period is set to 72.10 Hz by 240 coms.
f_{FP} = 240 (COM) + 63 = 303 = 12FH (by Table 3.14.5)
Therefore, LCDCTL<FP8> = 1 and LCDFFP<FP7:0> = 2FH are setup.

LCDCTL Register

LCDCTL (0363H)		7	6	5	4	3	2	1	0
	Bit symbol	LCDON	–	–	BUS1	BUS0	MMULCD	FP8	START
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	After reset	0	0	0	0	0	0	0	0
	Function	$\overline{\text{DOFF}}$ (SR, RAM mode) 0: Off 1: On	Always write 0.	Always write 0.	Data bus width. (SR mode) 00: 8 bits (Byte mode) 01: 4 bits (Nibble mode) 10: Reserve 11: Reserve		TYPE selection LCDD (Build in RAM). 0:Sequential 1:Random	Setting bit 8 for f_{FP}.	Start control. (SR mode) 0: Stop 1: Start

LCDFFP Register

LCDFFP (0364H)		7	6	5	4	3	2	1	0
	Bit symbol	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
	Read/Write	R/W							
	After reset	0	0	0	0	0	0	0	0
	Function	Setting bit7 to bit0 for f_{FP}.							

3.14.4.2 Timer Out LCDCK

LCD source clock (LCDCK) can select low frequency (XT1, XT2: 32.768 [kHz]) or timer out (TA3OUT) outputs from internal TMRA23.

Example: Here indicates the method that frame period is set 70 [Hz] by selecting TA3OUT for source clock of LCD (fc = 6 [MHz], 120 COM).

The next equation calculates frame period.

Frame period = $1/(t_{LP} \times f_{FP})$ [Hz] t_{LP}: The period of D2BLP

Source clock for LCDC defines as XT [Hz] and then this t_{LP} represents

t_{LP} = D/XT D: The value is 3.5 at 120 COM

Therefore if you set the frame period at 70 [Hz] under 120 COM,

$XT = 120 \times 3.5 \times 70$

$= 29400$ [Hz]

XT should be above value.

In order to make XT = 29400 [Hz] under fc = 6 [MHz] with ϕT1 of timer3,

$1/XT = T3 \times 2 \times 8/fc$ [s] T3: the value of timer resister (TA3REG)

in short, $XT = fc/(T3 \times 2 \times 8)$ [Hz]

However T3 = (TA3REG) is 12.75 after calculate, it's impossible to set the value under a decimal point.

So if (TA3REG) is set 0CH, XT = 31250 [Hz]. And because of D = 3.5,

Frame period = $31250/(120 \times 3.5)$

$= 74.404$ [Hz]

Further if f_{FP} is 127 (COM + 7) with correction,

Frame period = $31250/(127 \times 3.5)$

$= 70.30$ ... [Hz]

Reference: To maintain quality for display, please refer to following value for each gray scale.
(You have to use settlement of frame frequency function, frame invert adjustment function and timer out LCDCK.)
Monochrome: Frame period = 70 [Hz]

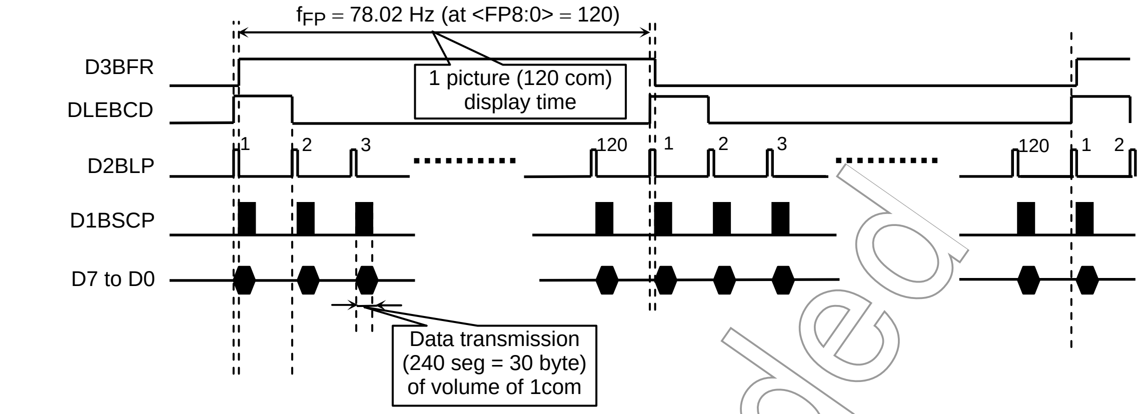


Figure 3.14.2 Timing Diagram for SR Mode

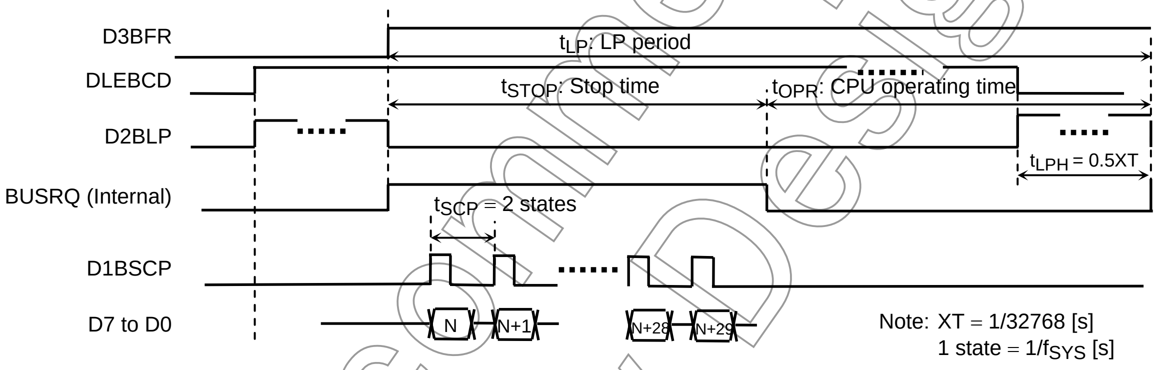


Figure 3.14.3 Timing Diagram for SR Mode (Detail)

Table 3.14.4 Performance Listing for Each Segment and Common Number

		64 com	68 com	80 com	100 com	120 com	128 com	144 com	160 com	200 com	240 com	Unit
XT number of counts for t_{LP} making: D		6.5	6	5	4	3.5	3	2.5	2.5	2	1.5	---
t_{LP}		198.4	183.1	152.6	122.1	106.8	91.6	76.3	76.3	61.0	45.8	μs
32 seg	t_{STOP}	0.4										μs
	CPU stop rate	0.2	0.2	0.3	0.4	0.4	0.5	0.6	0.6	0.7	1.0	%
64 seg	t_{STOP}	0.9										μs
	CPU stop rate	0.4	0.5	0.6	0.7	0.8	1.0	1.2	1.2	1.5	1.9	%
80 seg	t_{STOP}	1.1										μs
	CPU stop rate	0.6	0.6	0.7	0.9	1.0	1.2	1.5	1.5	1.8	2.4	%
120 seg	t_{STOP}	1.7										μs
	CPU stop rate	0.8	0.9	1.1	1.4	1.6	1.8	2.2	2.2	2.7	3.6	%
128 seg	t_{STOP}	1.8										μs
	CPU stop rate	0.9	1.0	1.2	1.5	1.7	1.9	2.3	2.3	2.9	3.9	%
160 seg	t_{STOP}	2.2										μs
	CPU stop rate	1.1	1.2	1.5	1.8	2.1	2.4	2.9	2.9	3.6	4.9	%
240 seg	t_{STOP}	3.3										μs
	CPU stop rate	1.7	1.8	2.2	2.7	3.1	3.6	4.4	4.4	5.5	7.3	%
320 seg	t_{STOP}	4.4										μs
	CPU stop rate	2.2	2.4	2.9	3.6	4.2	4.9	5.8	5.8	7.3	9.7	%
360 seg	t_{STOP}	5.0										μs
	CPU stop rate	2.5	2.7	3.3	4.1	4.7	5.5	6.6	6.6	8.2	10.9	%

Note 1: The above value is at f_{FPH} = 36 [MHz].

Note 2: CPU stop time t_{STOP}: A value is value when reading a transmitting memory by 0 waits in the BYTE write/BYTE read mode. The value becomes x1.5 in NIBBLE write mode. Details, see the “state/cycle” is each type timing table. The time required to the transmission start accompanied by bus opening demand is not included in the above-mentioned numerical value.

Note 3: The following equation can calculate t_{LP} listed below.

$$t_{LP} = D/32768 \text{ [s]}$$

(e.g.) If the row is 240 and D = 1.5 by the above table

$$t_{LP} = 1.5/32768 = 45.8 \text{ [μs]}$$

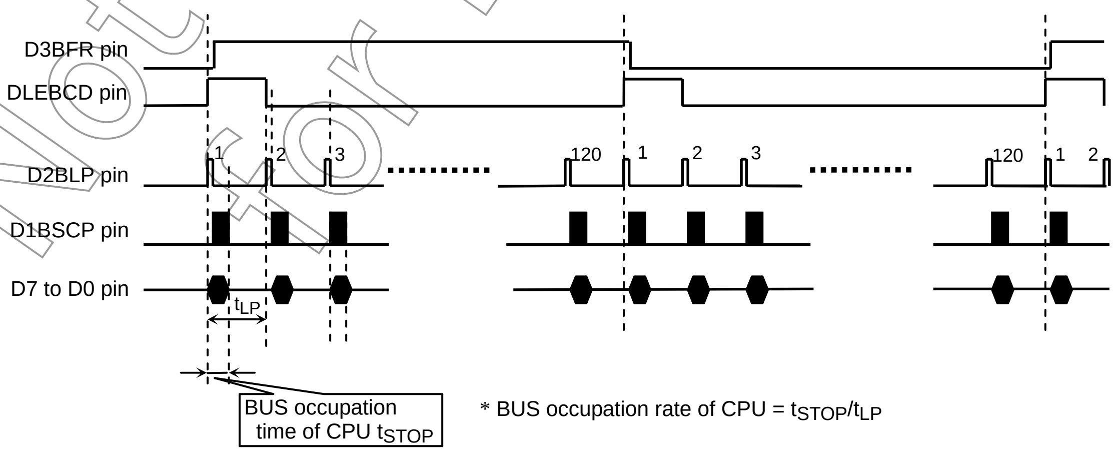


Figure 3.14.4 Stop Time and BUS Occupation Rate of CPU

Table 3.14.5 f_{FP} Table for Each Common Number (1/2)

D	6.5	6	5	4	3.5	3	2.5	2.5	2	1.5
COM	64	68	80	100	120	128	144	160	200	240
COM+0	78.77	80.31	81.92	81.92	78.02	85.33	91.02	81.92	81.92	91.02
COM+1	77.56	79.15	80.91	81.11	77.37	84.67	90.39	81.41	81.51	90.64
COM	76.38	78.02	79.92	80.31	76.74	84.02	89.78	80.91	81.11	90.27
COM	75.24	76.92	78.96	79.53	76.12	83.38	89.16	80.41	80.71	89.90
COM	74.14	75.85	78.02	78.77	75.50	82.75	88.56	79.92	80.31	89.53
COM	73.06	74.81	77.10	78.02	74.90	82.13	87.97	79.44	79.92	89.16
COM	72.02	73.80	76.20	77.28	74.30	81.51	87.38	78.96	79.53	88.80
COM	71.00	72.82	75.33	76.56	73.72	80.91	86.80	78.49	79.15	88.44
COM	70.02	71.86	74.47	75.85	73.14	80.31	86.23	78.02	78.77	88.09
COM	69.06	70.93	73.64	75.16	72.58	79.73	85.67	77.56	78.39	87.73
COM + 10	68.12	70.02	72.82	74.47	72.02	79.15	85.11	77.10	78.02	87.38
COM	67.22	69.13	72.02	73.80	71.47	78.58	84.56	76.65	77.65	87.03
COM	66.33	68.27	71.23	73.14	70.93	78.02	84.02	76.20	77.28	86.69
COM	65.47	67.42	70.47	72.50	70.39	77.47	83.49	75.76	76.92	86.35
COM	64.63	66.60	69.72	71.86	69.87	76.92	82.96	75.33	76.56	86.01
COM	63.81	65.80	68.99	71.23	69.35	76.38	82.44	74.90	76.20	85.67
COM	63.02	65.02	68.27	70.62	68.84	75.85	81.92	74.47	75.85	85.33
COM	62.24	64.25	67.56	70.02	68.34	75.33	81.41	74.05	75.50	85.00
COM	61.48	63.50	66.87	69.42	67.84	74.81	80.91	73.64	75.16	84.67
COM	60.74	62.77	66.20	68.84	67.35	74.30	80.41	73.22	74.81	84.34
COM + 20	60.01	62.06	65.54	68.27	66.87	73.80	79.92	72.82	74.47	84.02
COM	59.31	61.36	64.89	67.70	66.40	73.31	79.44	72.42	74.14	83.70
COM	58.62	60.68	64.25	67.15	65.93	72.82	78.96	72.02	73.80	83.38
COM	57.95	60.01	63.63	66.60	65.47	72.34	78.49	71.62	73.47	83.06
COM	57.29	59.36	63.02	66.06	65.02	71.86	78.02	71.23	73.14	82.75
COM	56.64	58.72	62.42	65.54	64.57	71.39	77.56	70.85	72.82	82.44
COM	56.01	58.10	61.83	65.02	64.13	70.93	77.10	70.47	72.50	82.13
COM	55.40	57.49	61.25	64.50	63.69	70.47	76.65	70.09	72.18	81.82
COM	54.80	56.89	60.68	64.00	63.26	70.02	76.20	69.72	71.86	81.51
COM	54.21	56.30	60.12	63.50	62.83	69.57	75.76	69.35	71.55	81.21
COM + 30	53.63	55.73	59.58	63.02	62.42	69.13	75.33	68.99	71.23	80.91
COM	53.07	55.16	59.04	62.53	62.00	68.70	74.90	68.62	70.93	80.61
COM	52.51	54.61	58.51	62.06	61.59	68.27	74.47	68.27	70.62	80.31
COM	51.97	54.07	58.00	61.59	61.19	67.84	74.05	67.91	70.32	80.02
COM	51.44	53.54	57.49	61.13	60.79	67.42	73.64	67.56	70.02	79.73
COM	50.92	53.02	56.99	60.68	60.40	67.01	73.22	67.22	69.72	79.44
COM	50.41	52.51	56.50	60.24	60.01	66.60	72.82	66.87	69.42	79.15
COM	49.91	52.01	56.01	59.80	59.63	66.20	72.42	66.53	69.13	78.86
COM	49.42	51.52	55.54	59.36	59.25	65.80	72.02	66.20	68.84	78.58
COM + 39	48.94	51.04	55.07	58.94	58.88	65.41	71.62	65.87	68.55	78.30

Note 1: f_{FP} can be calculated in the following formulas.

$f_{FP} = 32768/(D \times FP)$ [Hz]

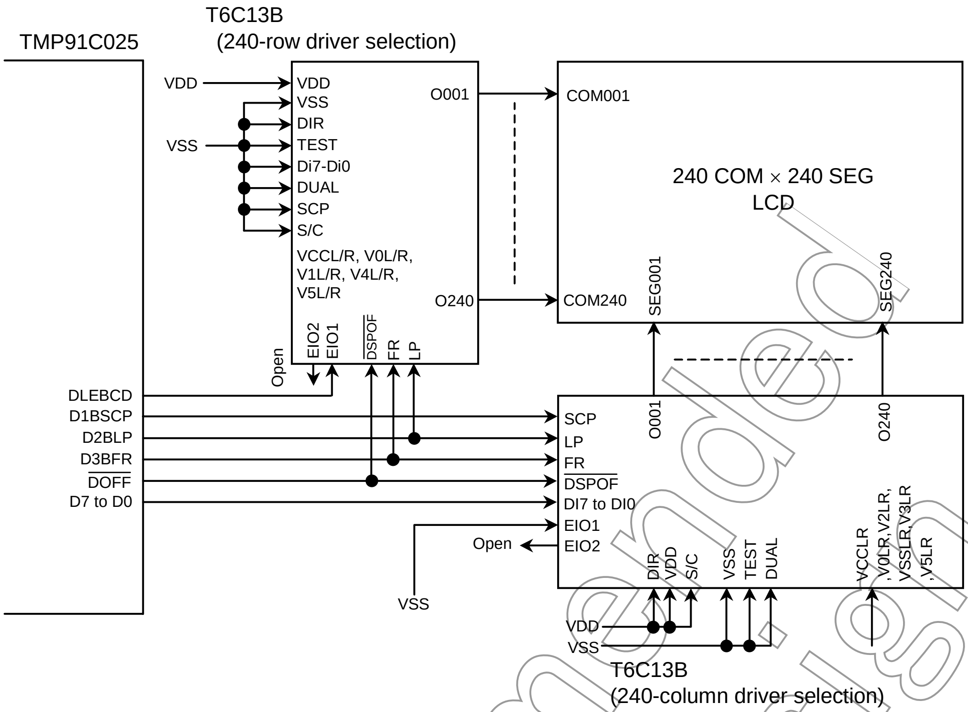
Example: In case of 120 com, <FP8:0> = 131,

$f_{FP} = 32768/(3.5 \times 131) = 71.5$ [Hz]

Note 2: The above is at fs = 32 [kHz].

Table 3.14.6 f_{FP} Table for Each Common Number (2/2)

D	6.5	6	5	4	3.5	3	2.5	2.5	2	1.5
COM	64	68	80	100	120	128	144	160	200	240
COM + 40	48.47	50.57	54.61	58.51	58.51	65.02	71.23	65.54	68.27	78.02
COM	48.01	50.10	54.16	58.10	58.15	64.63	70.85	65.21	67.98	77.74
COM	47.56	49.65	53.72	57.69	57.79	64.25	70.47	64.89	67.70	77.47
COM	47.11	49.20	53.28	57.29	57.44	63.88	70.09	64.57	67.42	77.19
COM	46.68	48.76	52.85	56.89	57.09	63.50	69.72	64.25	67.15	76.92
COM	46.25	48.33	52.43	56.50	56.74	63.14	69.35	63.94	66.87	76.65
COM	45.83	47.91	52.01	56.11	56.40	62.77	68.99	63.63	66.60	76.38
COM	45.42	47.49	51.60	55.73	56.06	62.42	68.62	63.32	66.33	76.12
COM	45.01	47.08	51.20	55.35	55.73	62.06	68.27	63.02	66.06	75.85
COM	44.61	46.68	50.80	54.98	55.40	61.71	67.91	62.71	65.80	75.59
COM + 50	44.22	46.28	50.41	54.61	55.07	61.36	67.56	62.42	65.54	75.33
COM	43.84	45.89	50.03	54.25	54.75	61.02	67.22	62.12	65.27	75.07
COM	43.46	45.51	49.65	53.89	54.43	60.68	66.87	61.83	65.02	74.81
COM	43.09	45.13	49.28	53.54	54.12	60.35	66.53	61.54	64.76	74.56
COM	42.72	44.77	48.91	53.19	53.81	60.01	66.20	61.25	64.50	74.30
COM	42.36	44.40	48.55	52.85	53.50	59.69	65.87	60.96	64.25	74.05
COM	42.01	44.04	48.19	52.51	53.19	59.36	65.54	60.68	64.00	73.80
COM	41.66	43.69	47.84	52.18	52.89	59.04	65.21	60.40	63.75	73.55
COM	41.32	43.34	47.49	51.85	52.60	58.72	64.89	60.12	63.50	73.31
COM	40.99	43.00	47.15	51.52	52.30	58.41	64.57	59.85	63.26	73.06
COM + 60	40.66	42.67	46.81	51.20	52.01	58.10	64.25	59.58	63.02	72.82
COM	40.33	42.34	46.48	50.88	51.73	57.79	63.94	59.31	62.77	72.58
COM	40.01	42.01	46.15	50.57	51.44	57.49	63.63	59.04	62.53	72.34
COM	39.69	41.69	45.83	50.26	51.16	57.19	63.32	58.78	62.30	72.10
COM	39.38	41.37	45.51	49.95	50.88	56.89	63.02	58.51	62.06	71.86
COM	39.08	41.06	45.20	49.65	50.61	56.59	62.71	58.25	61.83	71.62
COM	38.78	40.76	44.89	49.35	50.33	56.30	62.42	58.00	61.59	71.39
COM	38.48	40.45	44.58	49.05	50.07	56.01	62.12	57.74	61.36	71.16
COM	38.19	40.16	44.28	48.76	49.80	55.73	61.83	57.49	61.13	70.93
COM	37.90	39.86	43.98	48.47	49.54	55.45	61.54	57.24	60.91	70.70
COM + 70	37.62	39.57	43.69	48.19	49.28	55.16	61.25	56.99	60.68	70.47
COM	37.34	39.29	43.40	47.91	49.02	54.89	60.96	56.74	60.46	70.24
COM	37.07	39.01	43.12	47.63	48.76	54.61	60.68	56.50	60.24	70.02
COM	36.80	38.73	42.83	47.35	48.51	54.34	60.40	56.25	60.01	69.79
COM	36.53	38.46	42.56	47.08	48.26	54.07	60.12	56.01	59.80	69.57
COM	36.27	38.19	42.28	46.81	48.01	53.81	59.85	55.78	59.58	69.35
COM	36.01	37.93	42.01	46.55	47.77	53.54	59.58	55.54	59.36	69.13
COM	35.75	37.66	41.74	46.28	47.52	53.28	59.31	55.30	59.15	68.91
COM	35.50	37.41	41.48	46.02	47.28	53.02	59.04	55.07	58.94	68.70
COM	35.25	37.15	41.22	45.77	47.05	52.77	58.78	54.84	58.72	68.48
COM + 80	35.01	36.90	40.96	45.51	46.81	52.51	58.51	54.61	58.51	68.27



Note: Other circuit is necessary for LCD drive power supply for LCD driver display.

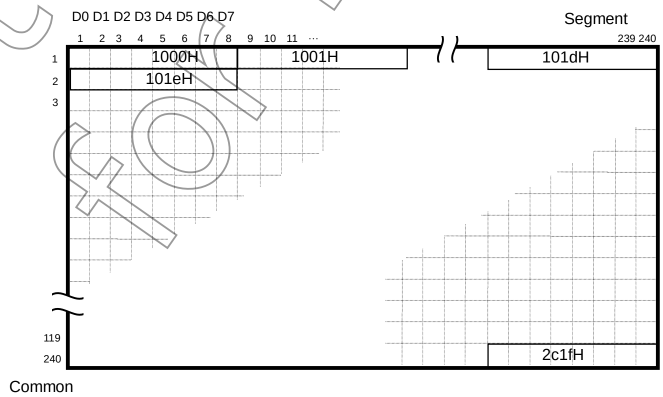
Figure 3.14.5 Interface Example for Shift Register Type LCD Driver

(Setting example)

In case of use 240 SEG × 240 COM, 8bit bus width LCD driver.

In case of store 7200 bytes transfer data to LCD driver in built-in RAM (1000H to 2c1FH).

```
LD      (PDCR), 1FH        ; Setting control terminal
LD      (LCDSAL), 11H      ; Select SR mode
LD      (LCDSAH), 00H      ; Source start address = 1000H
LD      (LCDSIZE), 96H     ; 240SEG × 240COM
LD      (LCDFFP), 308      ; fFP = 70.93 Hz
LD      (LCDCTL), 81H      ; BYTE mode fFP = 70.93 Hz,
                           ; LCDON, Transfer start
```



Relation Display Panel and Display Memory (In case of above setting)

3.14.4.3 Transfer Time by Data Bus Width

Data bus width of LCD driver can be selected either of BYTE/NIBBLE by LCDCTL<BUS1:0>. And that cycle is selectable, type A, type B and type C. Each type has each timing, for detail, look for timing table.

Readout bus width of source is selectable 8 bits or 16 bits, without concern to bus width of LCD driver.

WAIT number of the read cycle is 0 waits in case of built-in RAM and works by setting value of CS/WAIT controller in case of external RAM

3.14.4.4 LCDC Operation in HALT Mode

When LCDC is working, CPU executes HALT instruction and changes in HALT mode, LCDC continue operation if CPU in IDLE2 mode. But LCDC stops in case of IDLE1, STOP mode.

Note: It need to set the same bus width setting of display RAM, CS/WAIT controller and LCDCTL2<RAMBUS>

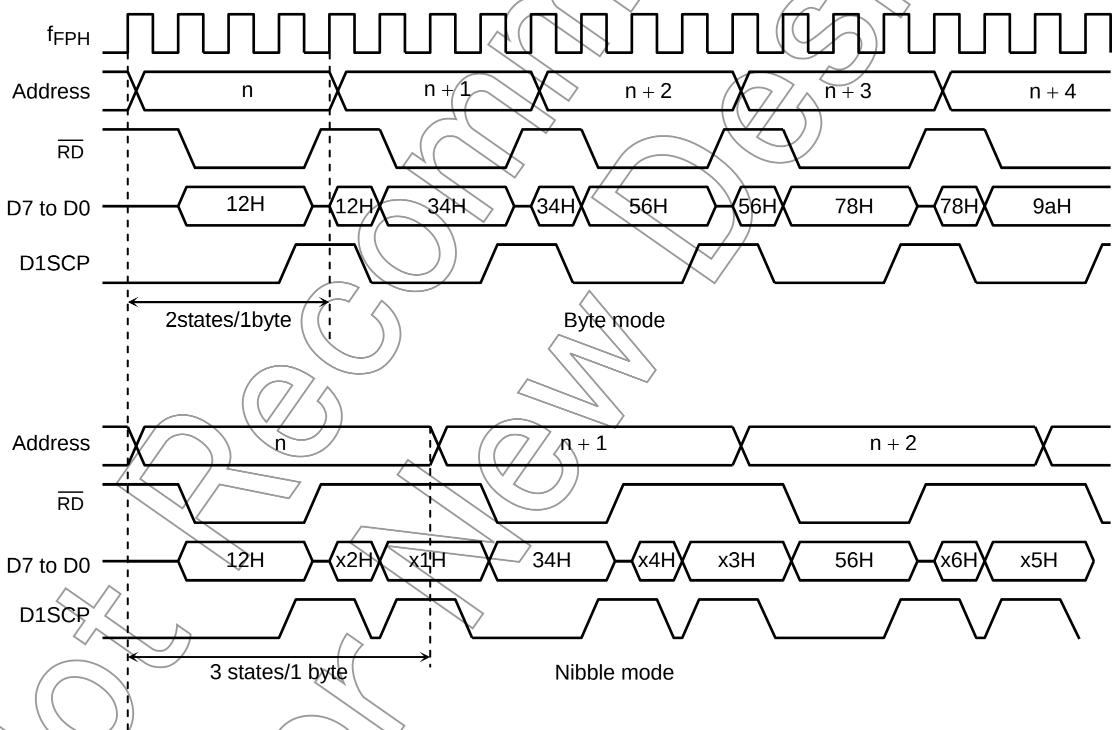


Figure 3.14.6 Bus Width Timing (No-wait external RAM)

Table 3.14.7 Each Type Timing Table

Read Bus Width	Type	Write Mode	Setup Time	Hold Time	D1BSCP Pulse Width	D1BSCP Cycle	State/ Cycle
Byte	A	Byte	0.5x	1.0x	1.5x	4.0x	4.0x
		Nibble	0.5x	1.0x	1.0x	2.0x	6.0x
	B	Byte	1.0x	0.5x	2.0x	4.0x	4.0x
		Nibble	1.0x	0.5x	1.0x	2.0x	6.0x
	C	Byte	1.0x	2.5x	1.5x	6.0x	6.0x
		Nibble	1.0x	1.5x	2.5x	5.0x	10.0x
Word	A	Byte	0.5x	1.0x	1.0x	2.0x	6.0x
		Nibble	0.5x	1.0x	1.0x	2.0x	10.0x
	B	Byte	1.0x	0.5x	1.0x	2.0x	6.0x
		Nibble	1.0x	0.5x	1.0x	2.0x	10.0x
	C	Byte	1.0x	1.5x	1.5x	3.0x	8.0x
		Nibble	1.0x	1.5x	2.5x	5.0x	20.0x

Note: Number in above Table shows f_{FPH} clock cycle, for example, in case of 27 MHz frequency Xin-Xout, 1.00 equal 37 ns.

Above table don't show to guarantee the time, it shows outline. For details, look for AC timing at after page.

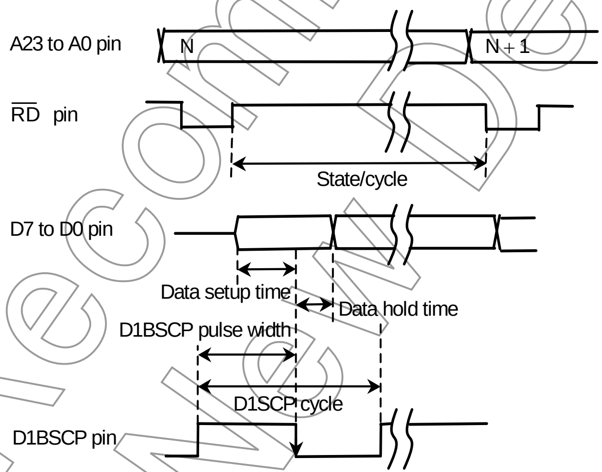
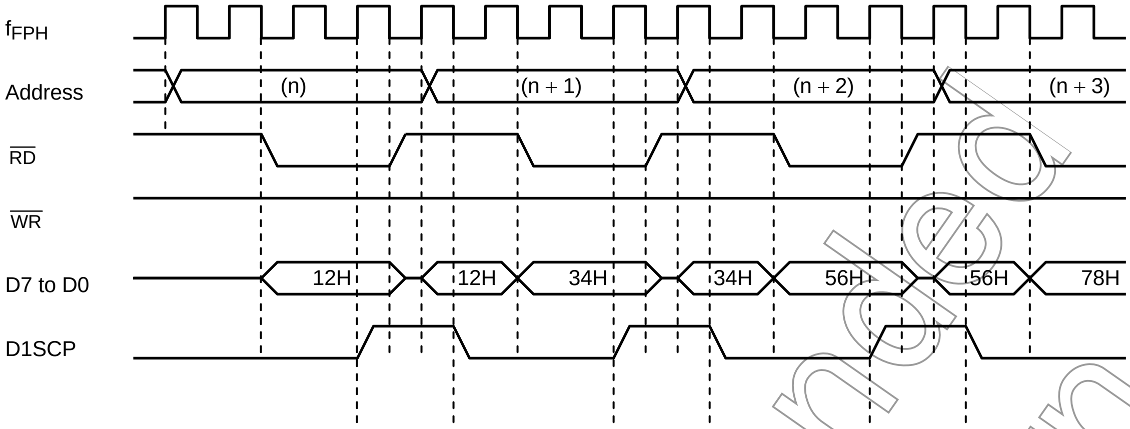
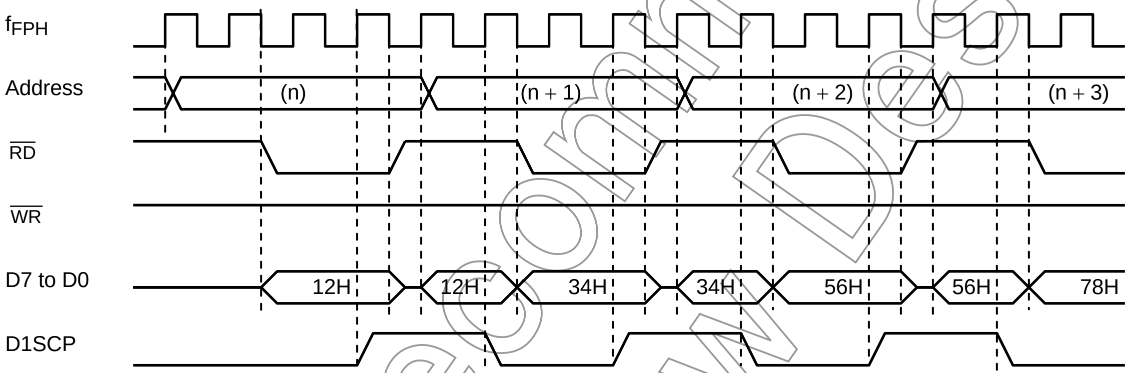


Figure 3.14.7 Definition of Specification

Type	Read	Trance	RAM
A	8 bits	8 bits	SRAM



Type	Read	Trance	RAM
B	8 bits	8 bits	SRAM



Type	Read	Trance	RAM
C	8 bits	8 bits	SRAM

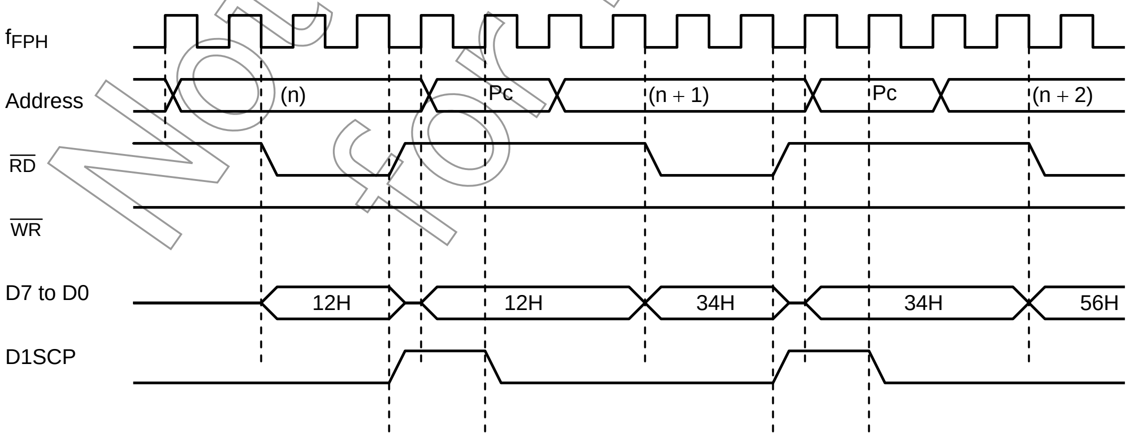
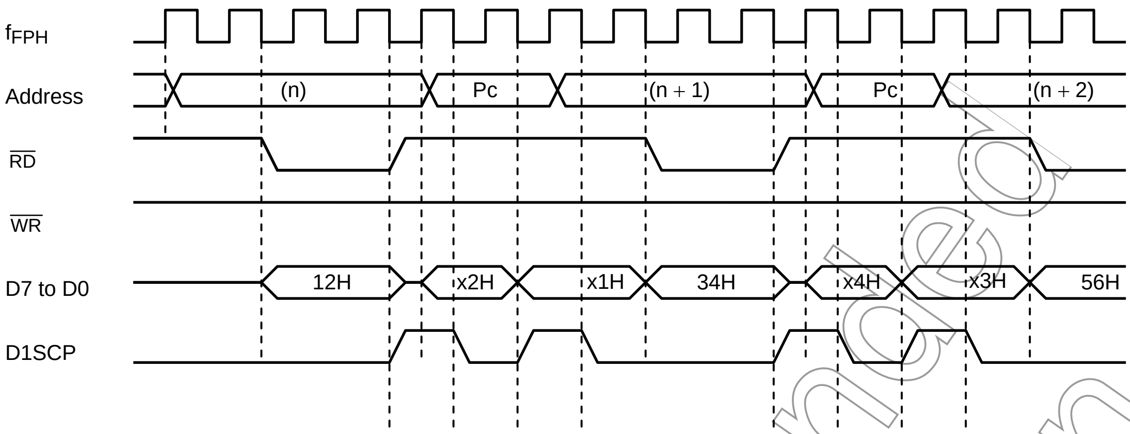
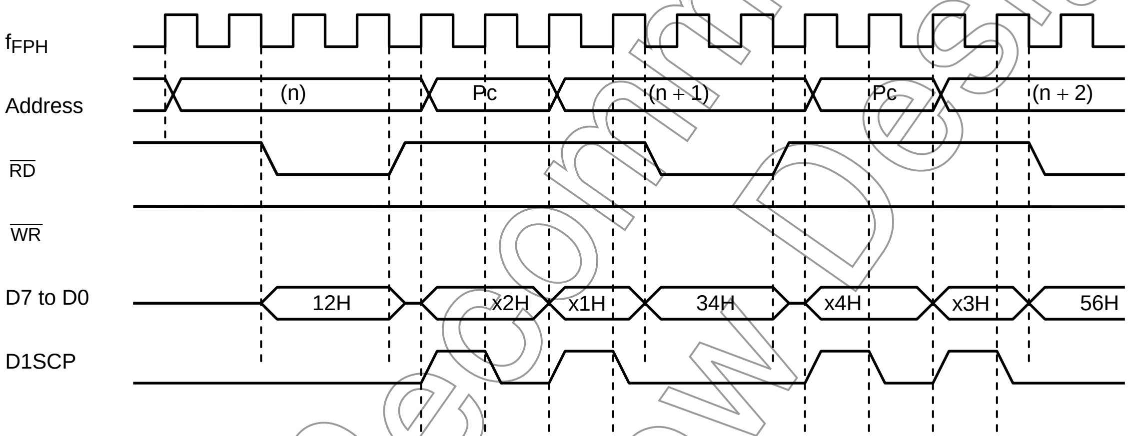


Figure 3.14.8 Byte Read and Byte Write Timing

Type	Read	Trance	RAM
A	8 bits	4 bits	SRAM



Type	Read	Trance	RAM
B	8 bits	4 bits	SRAM



Type	Read	Trance	RAM
C	8 bits	4 bits	SRAM

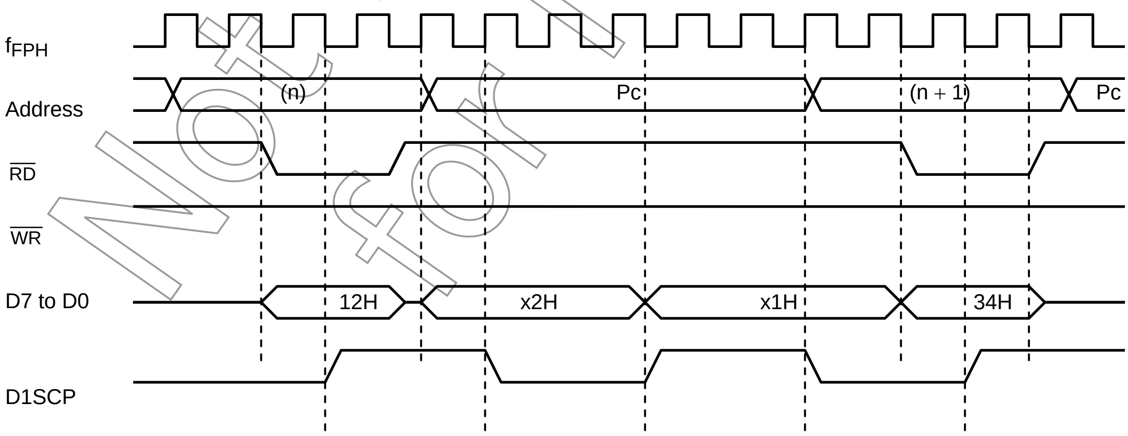
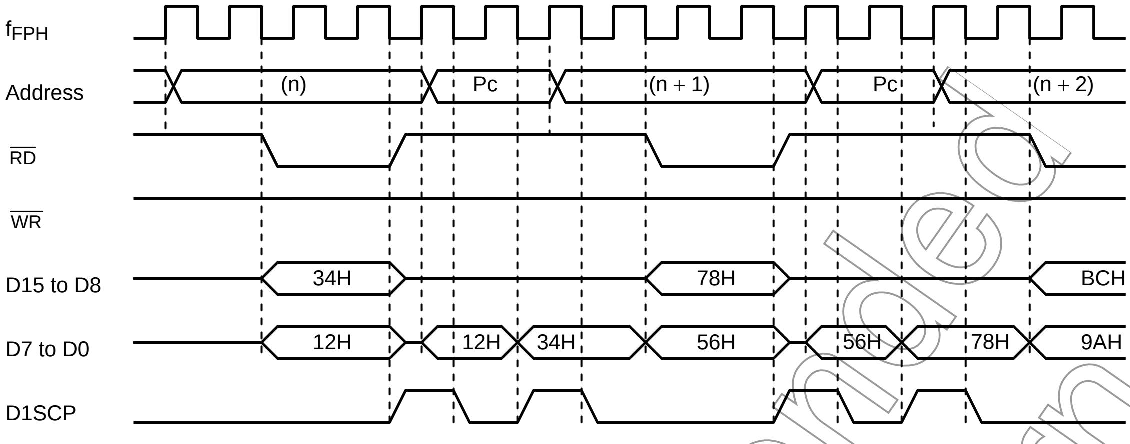
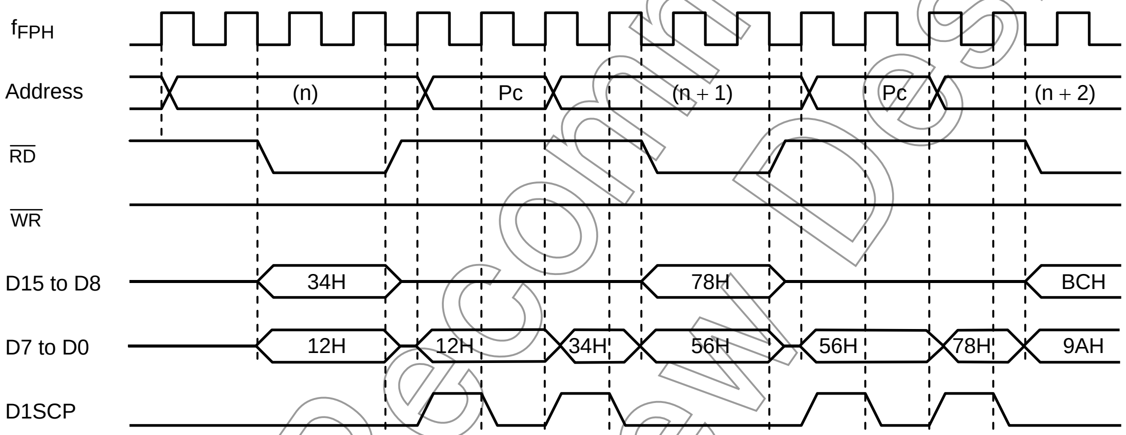


Figure 3.14.9 Byte Read and Nibble Write Timing

Type	Read	Trance	RAM
A	8 bits	4 bits	SRAM



Type	Read	Trance	RAM
B	16 bits	8 bits	SRAM



Type	Read	Trance	RAM
C	16 bits	8 bits	SRAM

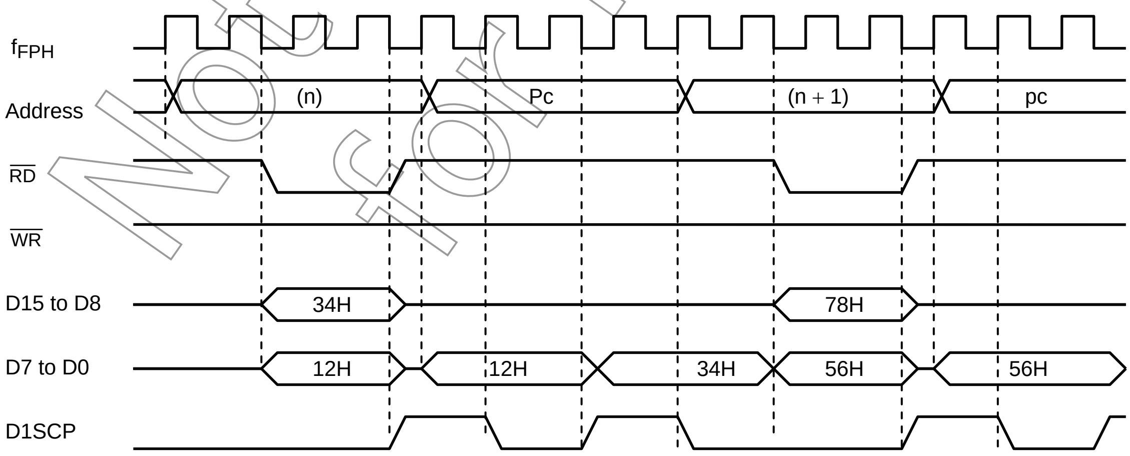
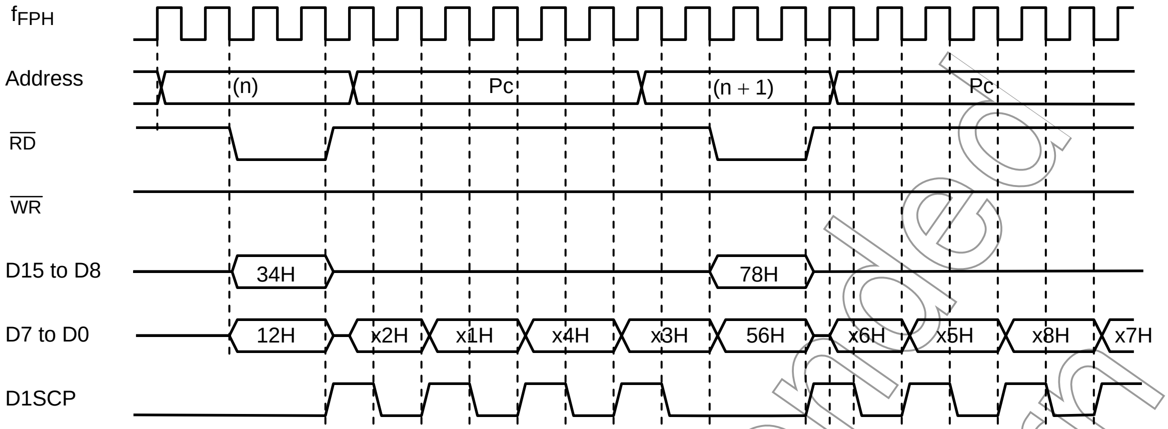
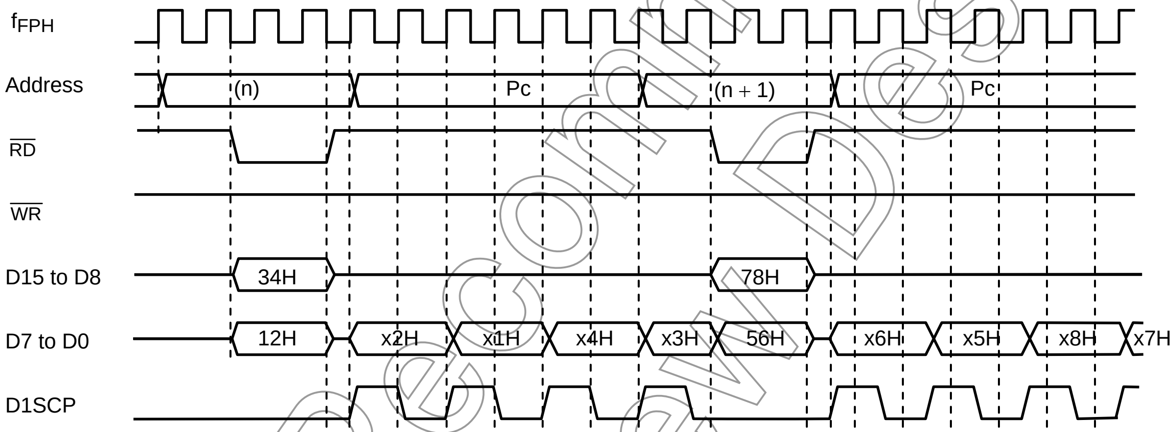


Figure 3.14.10 Word Read and Byte Write Timing

Type	Read	Trance	RAM
A	16 bits	4 bits	SRAM



Type	Read	Trance	RAM
B	16 bits	4 bits	SRAM



Type	Read	Trance	RAM
C	16 bits	4 bits	SRAM

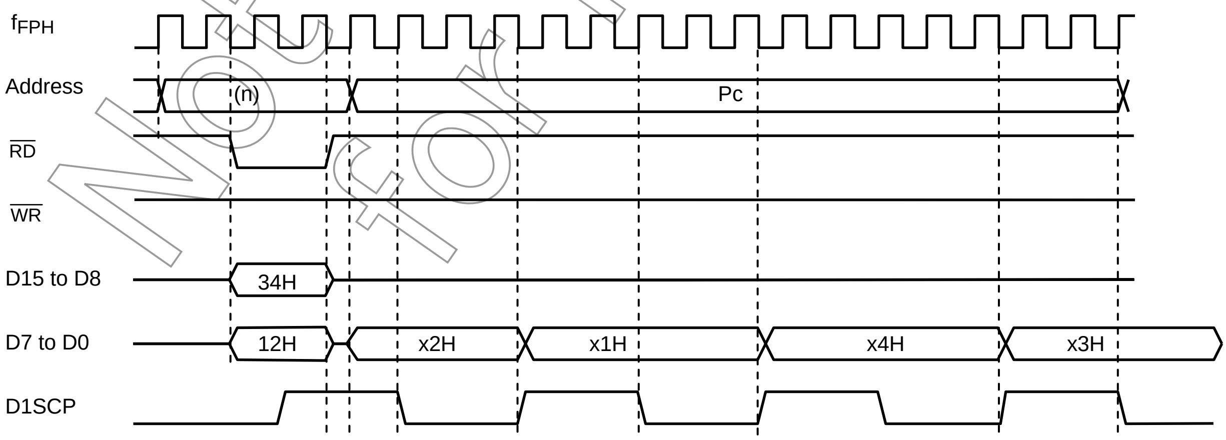


Figure 3.14.11 Word Read and Nibble Write Timing

3.14.5 RAM Built-in Type LCD Driver Control Mode (RAM Type)

Data transmission to LCD driver is executed by move instruction of CPU.

After setting mode of operation to control register, when move instruction of CPU is executed LCDC outputs chip select signal to LCD driver connected to the outside from control pin. (D1BSCP etc.)

Therefore control of data transmission numbers corresponding to LCD size is controlled by instruction of CPU. There are 2 kinds of addresses of LCD driver in this case, and which is chosen determines by LCDCTL<MMULCD> register.

It corresponds to LCD driver which has every 1 byte of instruction register and display data register in LCD driver at the time of <MMULCD> = 0. Please make the transmission place address at this time into either of FE0H to FE7H. (Table 3.14.2 references)

It corresponds to address direct writing type LCD driver at the time of <MMULCD> = 1. The transmission place address at this time can also assign the memory area of 3C0000H to 3FFFFFH to four areas for every 64 Kbytes. (Table 3.14.3 references)

The example of a setting is shown as follows and connection example is shown in Figure 3.14.12 at the time below. [<MMULCD> = 0]

(Setting example)

In case of use 80 SEG × 65 COM LCD driver.

Assign external column driver to LCDC0 and row driver to LCDR0.

This example used LD instruction in setting of instruction and used burst function of micro DMA by soft start in setting of display data.

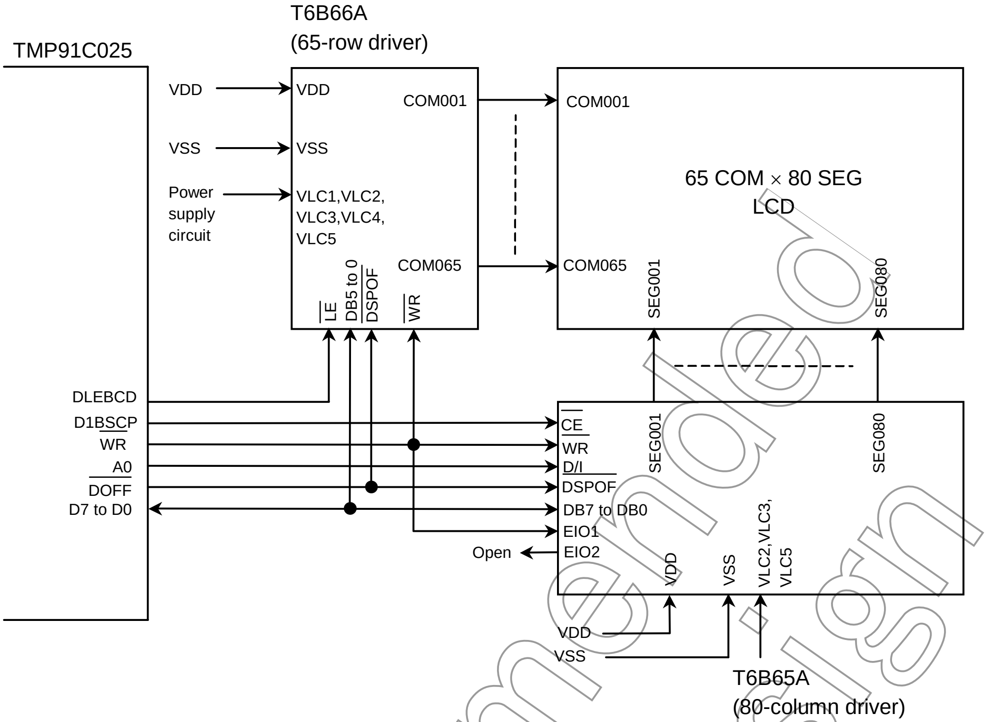
In case of store 650 bytes transfer data to LCD driver in built-in RAM (1000H to 1289H).

```
; Setting external terminal
        LD    (PDCR), 19H        ; CE for LCDC1: D1BSCP,
                                 ; LE for LCDR1: DLEBCD,
                                 ; Setting for/DOFF

; Setting for LCDC
        LD    (LCDSAL), 00H      ; Select RAM mode
        LD    (LCDCTL), 80H      ; LCDON

; Setting for mode of LCDC1/LCDR1
        LD    (LCDC1L), XX       ; Setting instruction for LCDC1
        LD    (LCDR1L), XX       ; Setting instruction for LCDR1

; Setting for micro DMA and INTTC (ch0)
        LD    A, 08H             ; Source address INC mode
        LDC   DMAM0, A           ;
        LD    WA, 650            ; count = 650
        LDC   DMAC0, WA          ;
        LD    XWA, 1000H         ; Source address = 1000H
        LDC   DMAS0, XWA         ;
        LD    XWA, 0FE1H         ; Destination address = FE1H (LCDC0H)
        LDC   DMAD0, XWA         ;
        LD    (INTETC01), 06H    ; INTTC0 level = 6
        EI    6                  ;
        LD    (DMAB), 01H        ; Burst mode
        LD    (DMAR), 01H        ; Soft start
```



Note: Other circuit is necessary for LCD drive power supply for LCD driver display.

Figure 3.14.12 Interface Example for RAM Built-in Type LCD Driver

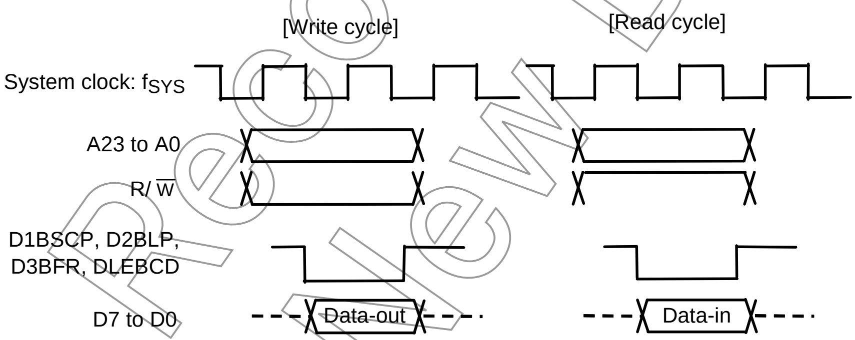


Figure 3.14.13 Example of Access Timing for RAM Built-in Type LCD Driver (Wait = 0)

3.15 Melody/Alarm Generator

TMP91C025 incorporates melody function and alarm function, both of which are output from the MLDALM pin. 5 kinds of fixed cycle interrupts are generated by the 15-bit free-run counter which is used for alarm generator.

Features are as follows.

- Melody generator

  The melody function generates signals of any frequency (4 Hz to 5461 Hz) based on low-speed clock (32.768 kHz) and outputs several signals from the MLDALM pin.

  By connecting a loud speaker outside, melody tone can sound easily.

- Alarm generator

  The alarm function generates 8 kinds of alarm waveform having a modulation frequency (4096 Hz) determined by the low-speed clock (32.768 kHz). And this waveform is able to invert by setting a value to a register.

  By connecting a loud speaker outside, Alarm tone can sound easily.

  And also 5 kinds of fixed cycle (1 Hz, 2 Hz, 64 Hz, 512 Hz, and 8192 Hz) interrupts are generated by the free-run counter which is used for alarm generator.

- Special mode

  It is assigned <TA3LCDE> at bit0 and <TA3MLDE> at bit1, of EMCCR0 register (00E3hex). These bits are used when you want to operate LCDD and MELODY circuit without low-frequency clock (XTIN, XTOUT). After reset these two bits set to "0" and low clock is supplied each LCDD and MELODY circuit. If you write these bits to "1", TA3 (Generate by timer3) is supplied each LCDD and MELODY circuit. In this case, you should set 32 kHz timer3 frequency. For detail, look AC specification characteristics.

This section is constituted as follows.

3.15.1 Block Diagram

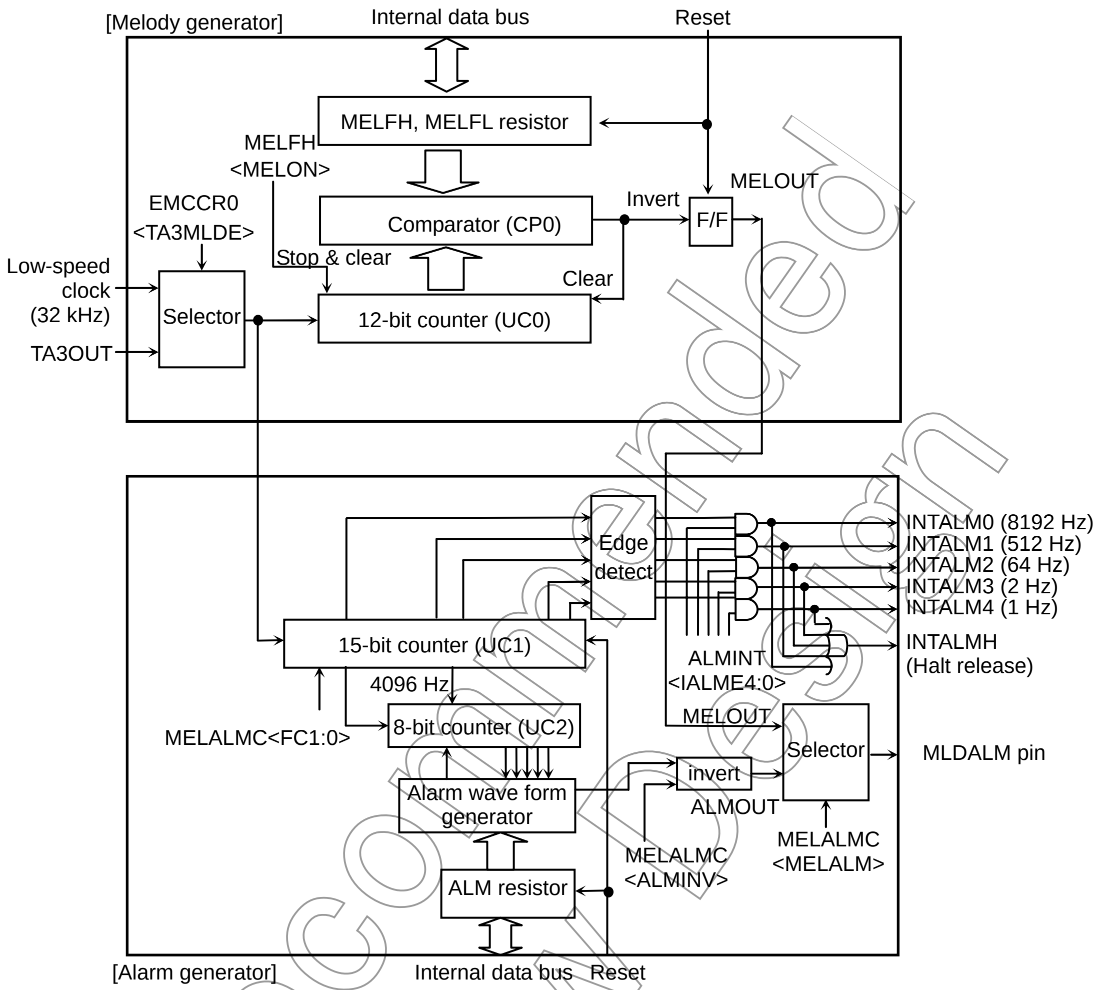


Figure 3.15.1 MLD Block Diagram

3.15.2 Control Registers

ALM Register

ALM (0330H)

	7	6	5	4	3	2	1	0
Bit symbol	AL8	AL7	AL6	AL5	AL4	AL3	AL2	AL1
Read/Write	R/W							
After reset	0	0	0	0	0	0	0	0
Function	Setting alarm pattern.							

MELALMC Register

MELALMC (0331H)

	7	6	5	4	3	2	1	0
Bit symbol	FC1	FC0	ALMINV	–	–	–	–	MELALM
Read/Write	R/W		R/W					
After reset	0	0	0	0	0	0	0	0
Function	Free-run counter control. 00: Hold 01: Restart 10: Clear 11: Clear & start		Alarm waveform invert. 1: INVERT	Always write 0.				Output waveform select. 0: Alarm 1: Melody

Note 1: MELALMEC<FC1> is read always 0.

Note 2: When setting MELALMC register except <FC1:0> during the free-run counter is running, <FC1:0> is kept 01.

MELFL Register

MELFL (0332H)

	7	6	5	4	3	2	1	0
Bit symbol	ML7	ML6	ML5	ML4	ML3	ML2	ML1	ML0
Read/Write	R/W							
After reset	0	0	0	0	0	0	0	0
Function	Setting melody frequency (Lower 8 bits).							

MELFH Register

MELFH (0333H)

	7	6	5	4	3	2	1	0
Bit symbol	MELON				ML11	ML10	ML9	ML8
Read/Write	R/W				R/W			
After reset	0				0	0	0	0
Function	Control melody counter. 0: Stop & clear 1: Start				Setting melody frequency (Upper 4 bits).			

ALMINT Register

ALMINT (0334H)

	7	6	5	4	3	2	1	0
Bit symbol			–	IALM4E	IALM3E	IALM2E	IALM1E	IALM0E
Read/Write			R/W					
After reset			0	0	0	0	0	0
Function			Always write 0.	1: Interrupt enable for INTALM4 to INTALM0.				

3.15.3 Operational Description

3.15.3.1 Melody Generator

The melody function generates signals of any frequency (4 Hz to 5461 Hz) based on low-speed clock (32.768 kHz) and outputs the signals from the MLDALM pin.

By connecting a loud speaker outside, melody tone can sound easily.

(Operation)

At first, MELALMC<MELALM> have to be set as 1 in order to select melody waveform as output waveform from MLDALM. Then melody output frequency has to be set to 12-bit register MELFH, MELFL.

Followings are setting example and calculation of melody output frequency.

(Formula for calculating of melody waveform frequency)

at fs = 32.768 [kHz]

melody output waveform f_{MLD} [Hz] = 32768/(2 × N + 4)

setting value for melody N = (16384/f_{MLD}) − 2

(Note: N = 1 to 4095 (001H to FFFH), 0 is not acceptable)

(Example program)

In case of outputting La musical scale (440 Hz)

```
LD    (MELALMC), 11X00001B    ; Select melody waveform
LD    (MELFL), 23H            ; N = 16384/440 – 2 = 35.2 = 023H
LD    (MELFH), 80H            ; Start to generate waveform
```

(Refer to basic musical scale setting table)

Scale	Frequency [Hz]	Register Value: N
C	264	03CH
D	297	035H
E	330	030H
F	352	02DH
G	396	027H
A	440	023H
B	495	01FH
C	528	01DH

3.15.3.2 Alarm Generator

The Alarm function generates 8 kinds of alarm waveform having a modulation frequency 4096 Hz determined by the low-speed clock (32.768 kHz). And this waveform is reversible by setting a value to a register.

By connecting a loud speaker outside, Alarm tone can sound easily.

5 kinds of fixed cycle (1 Hz, 2 Hz, 64 Hz, 512 Hz, 8192 Hz) interrupts are generate by the free-run counter which is used for alarm generator.

(Operation)

At first, MELALMC<MELALM> have to be set as 0 in order to select alarm waveform as output waveform from MLDALM. Then "10" be set on MELALMC<FC1:0> register, and clear internal counter. Finally alarm pattern has to be set on 8-bit register of ALM. If it is inverted output-data, set <ALMINV> as invert.

Followings are example program, setting value of alarm pattern and waveform of each setting value.

(Setting value of alarm pattern)

Setting Value for ALM Register	Alarm Waveform
00H	0 fixed
01H	AL1 pattern
02H	AL2 pattern
04H	AL3 pattern
08H	AL4 pattern
10H	AL5 pattern
20H	AL6pattern
40H	AL7 pattern
80H	AL8 pattern
Other	Undefined (do not set)

(Example program)

In case of outputting AL2 pattern (31.25 ms/8 times/1 s)

```
LD      (MELALMC), C0H          ; Set output alarm waveform
                                ; Free-run counter start
LD      (ALM), 02H              ; Set AL2 pattern, start
```

(Example)

Waveform of alarm pattern for each setting value: Not invert

3.16 Hardware Standby Function

TMP91C025 have hardware standby circuit that is able to save the power consumption and protect from program runaway by supplying power voltage down. Especially, it’s useful in case of battery using.

It can be shifted to “PS condition” by fixing $\overline{PS}$ pin to “Low” level.

Figure 3.16.1 shows timing diagram of transition of PS condition below.

PS mode can be released only by external RESET.

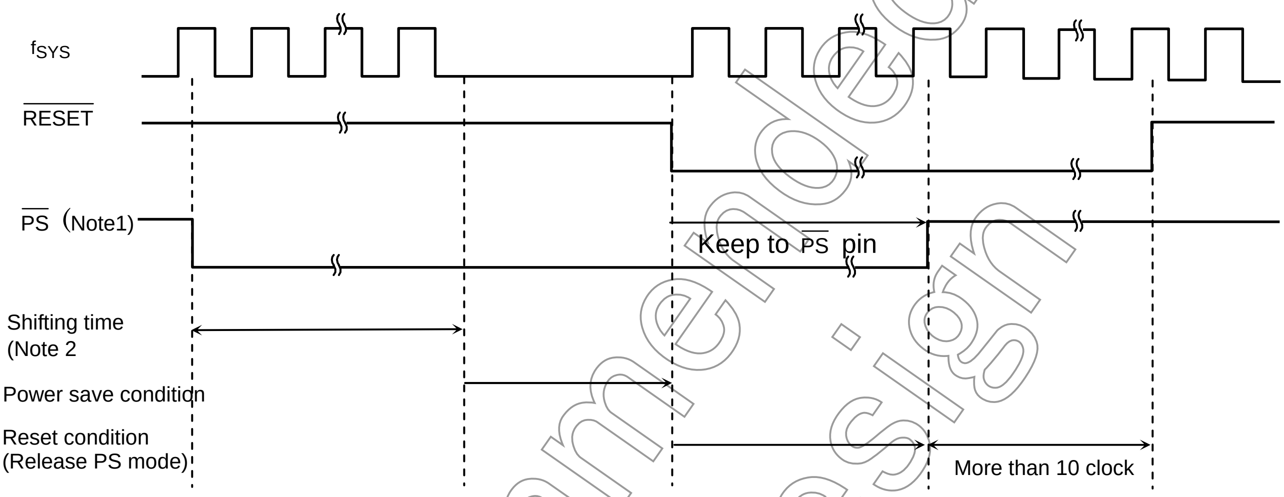


Figure 3.16.1 Hardware Standby Timing Diagram

Note 1: $\overline{PS}$ pin is effective after RESET because SYSCR2<PSENV> to 0. If you use as INT0 pin, please write SYSCR2<PSENV> to 1.

Note 2: Shifting time is 2 to 10 clock times of f_{SYS}.

Table 3.16.1 Power Save Conditions of Each HALT Mode

HALT Mode Setting	IDLE2	IDLE1	STOP
PS condition	IDLE1 mode + High-frequency stop	IDLE1 mode + High-frequency stop	STOP mode

Note: Settings of SYSCR2<DRVE> and <SELDRV> at HALT mode are effective as well as PS condition.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	Vcc	−0.5 to 4.0	V
Input voltage	VIN	−0.5 to Vcc + 0.5	V
Output current	IOL	2	mA
Output Current (MX, MY pin)	IOL	15	mA
Output current	IOH	−2	mA
Output Current (PX, PY pin)	IOH	−15	mA
Output current (Total)	ΣIOL	80	mA
Output current (Total)	ΣIOH	−80	mA
Power dissipation (Ta = 85°C)	PD	600	mW
Soldering temperature (10 s)	TSOLDER	260	°C
Storage temperature	TSTG	−65 to 150	°C
Operating temperature	TOPR	−40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, the device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Solderability of lead lead-free products

Test parameter	Test condition	Note
Solderability	(1) Use of Sn-637Pb solder Bath Solder bath temperature =230°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux	Pass: solderability rate until forming ≥ 95%
	(2) Use of Sn-3.0Ag-0.5Cu solder bath Solder bath temperature =245°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux (use of lead lead-free)	

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition		Min	Typ.	Max	Unit
Power supply voltage (AVCC = DVCC) (AVSS = DVSS = 0 V)		VCC	fc = 4 to 36 MHz	fs = 30 to 34 kHz	3.0	–	3.6	V
			fc = 4 to 27 MHz		2.7			
			fc = 4 to 16 MHz		2.4			
Input low voltage	D0 to D15	VIL	Vcc ≥ 2.7 V		−0.3	–	0.6	V
			Vcc < 2.7 V				0.2 Vcc	
	PZ2 to PD7 (Except $\overline{\text{RESET}}$, PB3, PB5, PB6, P9)	VIL1	Vcc ≥ 2.7 V			–	0.3 Vcc	
			Vcc < 2.7 V				0.2 Vcc	
	$\overline{\text{RESET}}$, PB3, PB5, PB6, P9	VIL2	Vcc ≥ 2.7 V			–	0.25 Vcc	
			Vcc < 2.7 V				0.15 Vcc	
	AM0 to AM1	VIL3	Vcc ≥ 2.7 V			–	0.3	
			Vcc < 2.7 V				0.3	
	X1	VIL4	Vcc ≥ 2.7 V			–	0.2 Vcc	
			Vcc < 2.7 V				0.1 Vcc	
Input high voltage	D0 to D15	VIH	3.6 V ≥ Vcc ≥ 2.7 V		2.4	–	Vcc + 0.3	
			3.3 V > Vcc ≥ 2.7 V		2.0			
			0.7 < Vcc		0.7 Vcc			
	PZ2 to PD7 (Except $\overline{\text{RESET}}$, PB3, PB5, PB6, P9)	VIH1	Vcc ≥ 2.7 V		0.7 Vcc	–		
			Vcc < 2.7 V		0.8 Vcc			
	$\overline{\text{RESET}}$, PB3, PB5, PB6, P9	VIH2	Vcc ≥ 2.7 V		0.75 Vcc	–		
			Vcc < 2.7 V		0.85 Vcc			
	AM0 to AM1	VIH3	Vcc ≥ 2.7 V		Vcc − 0.3	–		
			Vcc < 2.7 V		Vcc − 0.3			
	X1	VIH4	Vcc ≥ 2.7 V		0.8 Vcc	–		
			Vcc < 2.7 V		0.9 Vcc			
Output low voltage		VOL1	IOL = 1.6 mA	Vcc ≥ 2.7 V	–	–	0.45	V
			IOL = 0.4 mA	Vcc < 2.7 V			0.15 Vcc	
Output high voltage		VOH2	IOH = −400 μA	Vcc ≥ 2.7 V	Vcc − 0.3	–	–	
			IOH = 200 μA	Vcc < 2.7 V	0.8 Vcc			

Note: Typical values are for when Ta = 25°C and Vcc = 3.3 V uncles otherwise noted.

DC Characteristics (2/2)

Parameter	Symbol	Condition		Min	Typ.(Note 1)	Max	Unit
Internal resistor (ON) MX, MY pins	IMon	VOL = 0.2V	Vcc ≥ 2.7 V			30	Ω
		VOL = 0.07 Vcc	Vcc < 2.7 V			25	
Internal resistor (ON) PX, PY pins	IMon	VOH = Vcc − 0.2V	Vcc ≥ 2.7 V			30	
		VOH = 0.94 Vcc	Vcc < 2.7 V			25	
Input leak current	ILI	0.0 ≤ VIN ≤ Vcc		–	0.02	±5	μA
Output leak current	ILO	0.2 ≤ VIN ≤ Vcc − 0.2		–	0.05	±10	
$\overline{\text{RESET}}$ pull-up resistor	RRST	3.6 V ≥ Vcc ≥ 2.7 V		80		400	kΩ
Pin capacitance	CIO	fc = 1 MHz		–	–	10	pF
Schmitt width $\overline{\text{RESET}}$, INT0, KI0 to KI7, INT2, INT3	VTH	Vcc ≥ 2.7 V		0.4	1.0	–	V
		Vcc < 2.7 V		0.3	0.8		
Programmable pull-up resistor	RKH	3.6 V ≥ Vcc ≥ 2.7 V		80	–	400	kΩ
NORMAL (Note 2)	Icc	3.6 V ≥ Vcc ≥ 3.0 V fc = 36 MHz		–	16	21	mA
IDLE2				–	5.0	7	
IDLE1				–	1.5	3.2	
SLOW (Note 2)		3.6 V ≥ Vcc ≥ 2.7 V fs = 32.768 kHz		–	12	30	μA
IDLE2				–	8	25	
IDLE1				–	4	20	
STOP		3.6 V ≥ Vcc ≥ 2.7 V		–	0.2	15	

Note 1: Typical values are for when Ta = 25°C and Vcc = 3.3 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL, SLOW):
All functions are operational; output pins are open and input pins are fixed. Data and address bus CL = 30 pF loaded.

4.3 AC Characteristics

Vcc = 2.7 to 3.6 V case of f_{FPH} = 27 MHz

(1) Vcc = 2.7 V to 3.6 V   Vcc = 3.0 to 3.6 V case of f_{FPH} = 36 MHz

No.	Symbol	Parameter	Variable		27 MHz		36 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{FPH}	f_{FPH} period (= x)	27.7	31250	37.0		27.7		ns
2	t_{AC}	A0 to 23 valid → $\overline{RD}$ / $\overline{WR}$ fall	x – 23		14		4		ns
3	t_{CAR}	$\overline{RD}$ rise → A0 to A23 hold	0.5x – 13		5		0		ns
4	t_{CAW}	$\overline{WR}$ rise → A0 to A23 hold	x – 13		24		14		ns
5	t_{AD}	A0 to A23 valid → D0 to D15 input		3.5x – 24		105		73	ns
6	t_{RD}	$\overline{RD}$ fall → D0 to D15 input		2.5x – 24		68		45	ns
7	t_{RR}	$\overline{RD}$ low width	2.5x – 15		77		54		ns
8	t_{HR}	$\overline{RD}$ rise → D0 to A15 hold	0		0		0		ns
9	t_{WW}	$\overline{WR}$ low width	2.0x – 15		59		40		ns
10	t_{DW}	D0 to D15 valid → $\overline{WR}$ rise	1.5x – 35		20		6		ns
11	t_{WD}	$\overline{WR}$ rise → D0 to D15 hold	x – 25		12		2		ns
12	t_{SBA}	Data byte control access time for SRAM		3x – 24		87		59	ns
13	t_{SWP}	Write pulse width for SRAM	2x – 15		59		40		ns
14	t_{SBW}	Data byte control to end of write for SRAM	3x – 15		96		68		ns
15	t_{SAS}	Address setup time for SRAM	1.5x – 35		20		6		ns
16	t_{SWR}	Write recovery time for SRAM	0.5x – 13		5		0		ns
17	t_{SDS}	Data setup time for SRAM	2x – 35		39		20		ns
18	t_{SDH}	Data hold time for SRAM	0.5x – 13		3		0		ns
19	t_{AW}	A0 to A23 valid → $\overline{WAIT}$ input (1 + N) waits mode		3.5x – 60		69		37	ns
20	t_{CW}	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold (1 + N) waits mode	2.5x + 0		92		69		ns
21	t_{APH}	A0 to A23 valid → Port input		3.5x – 89		40		8	ns
22	t_{APH2}	A0 to A23 valid → Port hold	3.5x		129		96		ns
23	t_{APO}	A0 to A23 valid → Port valid		3.5x + 80		209		176	ns

AC measuring conditions

- Output level: High = 0.7 Vcc, Low = 0.3 Vcc, CL = 50 pF
- Input level: High = 0.9 Vcc, Low = 0.1 Vcc

Note: Symbol "x" in the above table means the period of clock "f_{FPH}", it's half period of the system clock "f_{SYS}" for CPU core. The period of f_{FPH} depends on the clock gear setting or selection of high/low oscillator frequency.

(2) Vcc = 2.4 V to 3.6 V

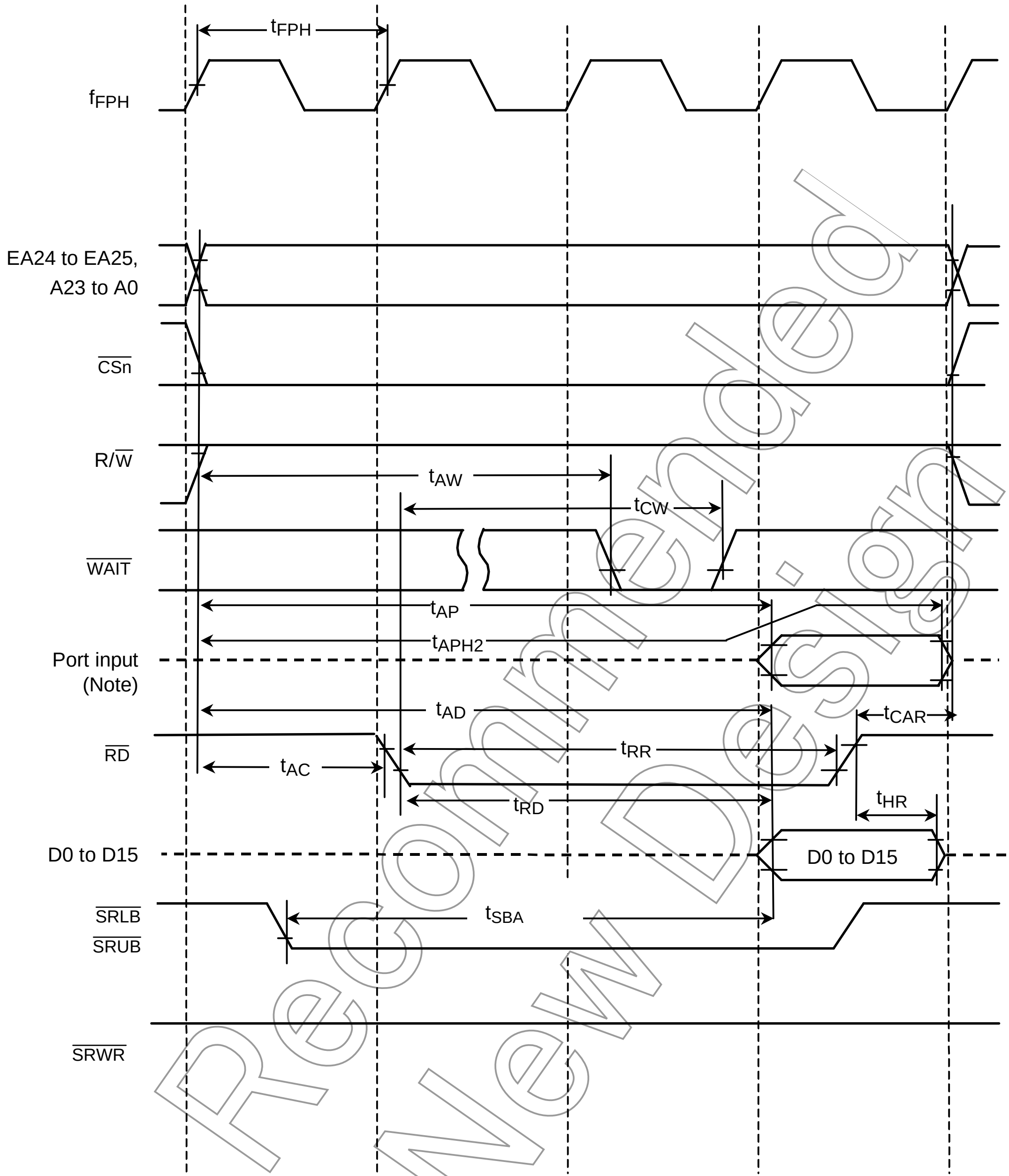
No.	Symbol	Parameter	Variable		16 MHz		Unit
			Min	Max	Min	Max	
1	t_{FPH}	f_{FPH} period (= x)	62.5	31250	62.5		ns
2	t_{AC}	A0 to 23 valid → $\overline{RD}$ / $\overline{WR}$ fall	x – 23		39		ns
3	t_{CAR}	$\overline{RD}$ rise → A0 to A23 hold	0.5x – 23		8		ns
4	t_{CAW}	$\overline{WR}$ rise → A0 to A23 hold	x – 13		49		ns
5	t_{AD}	A0 to A23 valid → D0 to D15 input		3.5x – 38		180	ns
6	t_{RD}	$\overline{RD}$ fall → D0 to D15 input		2.5x – 30		126	ns
7	t_{RR}	$\overline{RD}$ low width	2.5x – 15		141		ns
8	t_{HR}	$\overline{RD}$ rise → D0 to A15 hold	0		0		ns
9	t_{WW}	$\overline{WR}$ low width	2.0x – 15		110		ns
10	t_{DW}	D0 to D15 valid → $\overline{WR}$ rise	1.5x – 35		58		ns
11	t_{WD}	$\overline{WR}$ rise → D0 to D15 hold	x – 25		37		ns
12	t_{SBA}	Data byte control access time for SRAM		3x – 39		148	ns
13	t_{SWP}	Write pulse width for SRAM	2x – 15		110		ns
14	t_{SBW}	Data byte control to end of write for SRAM	3x – 25		162		ns
15	t_{SAS}	Address setup time for SRAM	1.5x – 35		58		ns
16	t_{SWR}	Write recovery time for SRAM	0.5x – 22		9		ns
17	t_{SDS}	Data setup time for SRAM	2x – 35		90		ns
18	t_{SDH}	Data hold time for SRAM	0.5x – 18		13		ns
19	t_{AW}	A0 to A23 valid → $\overline{WAIT}$ input (1 + N) waits mode		3.5x – 60		158	ns
20	t_{CW}	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold (1 + N) waits mode	2.5x + 0		156		ns
21	t_{APH}	A0 to A23 valid → Port input		3.5x – 89		129	ns
22	t_{APH2}	A0 to A23 valid → Port hold	3.5x		218		ns
23	t_{APO}	A0 to A23 valid → Port valid		3.5x + 80		298	ns

AC measuring conditions

- Output level: High = 0.7 Vcc, Low = 0.3 Vcc, CL = 50 pF
- Input level: High = 0.9 Vcc, Low = 0.1 Vcc

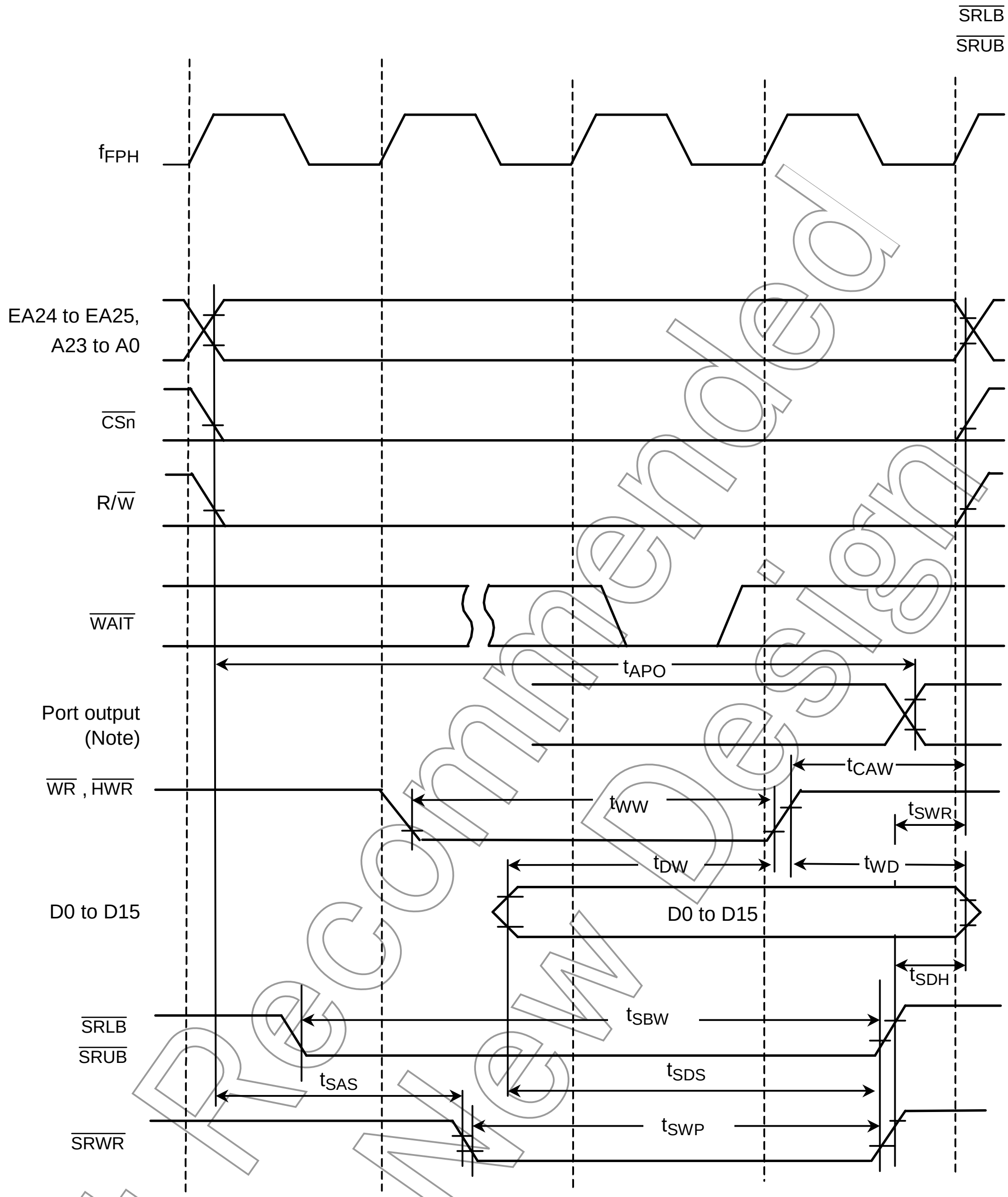
Note: Symbol “x” in the above table means the period of clock “f_{FPH}”, it’s half period of the system clock “f_{SYS}” for CPU core. The period of f_{FPH} depends on the clock gear setting or selection of high/low oscillator frequency.

(3) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(4) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 AD Conversion Characteristics

AVcc = Vcc, AVss = Vss

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
VREFH	Analog reference voltage (+)	3.6 V ≥ Vcc ≥ 2.7 V	Vcc − 0.2 V	Vcc	Vcc	V
		2.7 V ≥ Vcc ≥ 2.4 V	Vcc	Vcc	Vcc	
VREFL	Analog reference voltage (−)	3.6 V ≥ Vcc ≥ 2.7 V	Vss	Vss	Vss + 0.2 V	
		2.7 V ≥ Vcc ≥ 2.4 V	Vss	Vss	Vss	
VAIN	Analog input voltage range		VREFL		VREFH	
IREF (VREFL = 0 V)	Analog current for analog reference voltage<VREFON> = 1	3.6 V ≥ Vcc ≥ 2.7 V		1.04	1.2	mA
		2.7 V ≥ Vcc ≥ 2.4 V		0.75	0.90	
	<VREFON> = 0	3.6 V ≥ Vcc ≥ 2.4 V		0.03	10.0	μA
—	Error (Not including quantizing errors)	3.6 V ≥ Vcc ≥ 2.4 V		±1.0	±4.0	LSB

Note 1: 1 LSB = (VREFH − VREFL)/1024 [V]

Note 2: The operation above is guaranteed for f_{FPH} ≥ 4 MHz.

Note 3: The value of I_{CC} includes the current which flows through the AV_{CC} pin.

4.5 Serial Channel Timing (I/O internal mode)

Vcc = 2.7 to 3.6 V case of f_{FPH} = 27 MHz
Vcc = 3.0 to 3.6 V case of f_{FPH} = 36 MHz

(1) SCLK input mode

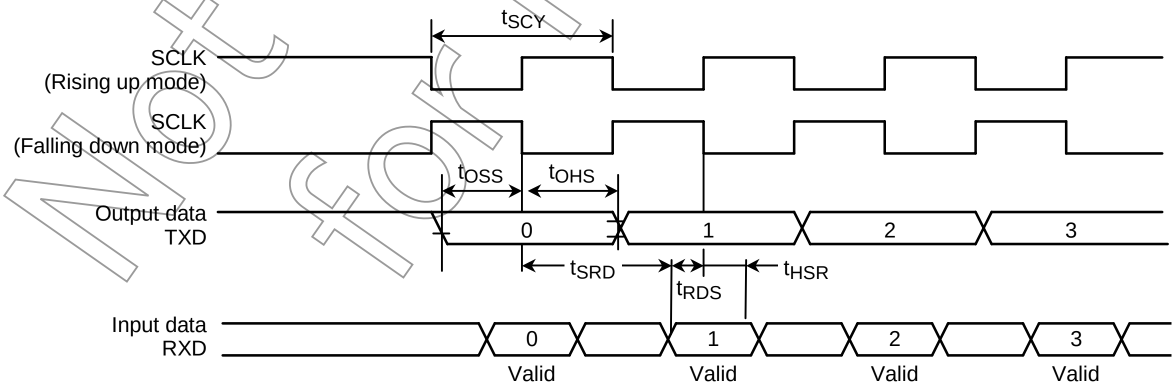
Symbol	Parameter	Variable		27 MHz		36 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK period	16X		0.59		0.44		μs
t_{OSS}	Output data → SCLK rising /Falling edge*	t_{SCY}/2 – 4X – 110		38		0		ns
t_{OHS}	SCLK rising /Falling edge*→ Output data hold	t_{SCY}/2 + 2X + 0		370		277		ns
t_{HSR}	SCLK rising /Falling edge*→ Input data hold	3X + 10		121		93		ns
t_{SRD}	SCLK rising /Falling edge*→ Valid data input		t_{SCY} – 0		592		443	ns
t_{RDS}	SCLK rising /Falling edge*→ Valid data input	0		0		0		ns

(2) SCLK output mode

Symbol	Parameter	Variable		27 MHz		36 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK period	16X	8192X	0.59	303	0.44	227	μs
t_{OSS}	Output data → SCLK rising /Falling edge*	t_{SCY}/2 – 40		256		181		ns
t_{OHS}	SCLK rising /Falling edge*→ Output data hold	t_{SCY}/2 – 40		256		181		ns
t_{HSR}	SCLK rising /Falling edge*→ Input data Hold	0		0		0		ns
t_{SRD}	SCLK rising /Falling edge*→ Valid data input		t_{SCY} – 1X – 180		375		235	ns
t_{RDS}	SCLK rising /Falling edge*→ Valid data input	1X + 180		217		207		ns

*) SCLK rising/Falling edge: The rising edge is used in SCLK Rising mode.
The Falling edge is used in SCLK Falling mode.

Note: Above table's data values at 27 MHz and 36 MHz, are caliculated from t_{SCY} = 16x base.



4.6 Event Counter (TA0IN)

Symbol	Parameter	Variable		27 MHz (V_{CC} = 2.7 to 3.6 V)		36 MHz (V_{CC} = 3.0 to 3.6 V)		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock period	8X + 100		396		321		ns
t_{VCKL}	Clock low level width	4X + 40		188		151		ns
t_{VCKH}	Clock high level width	4X + 40		188		151		ns

4.7 Interrupt, Capture

(1) $\overline{NMI}$, INT0 to INT3 interrupts

Symbol	Parameter	Variable		27 MHz (V_{CC} = 2.7 to 3.6 V)		36 MHz (V_{CC} = 3.0 to 3.6 V)		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 to INT3 low level width	4X + 40		188		151		ns
t_{INTAH}	$\overline{NMI}$, INT0 to INT3 high level width	4X + 40		188		151		ns

4.8 SCOUT pin AC Characteristics

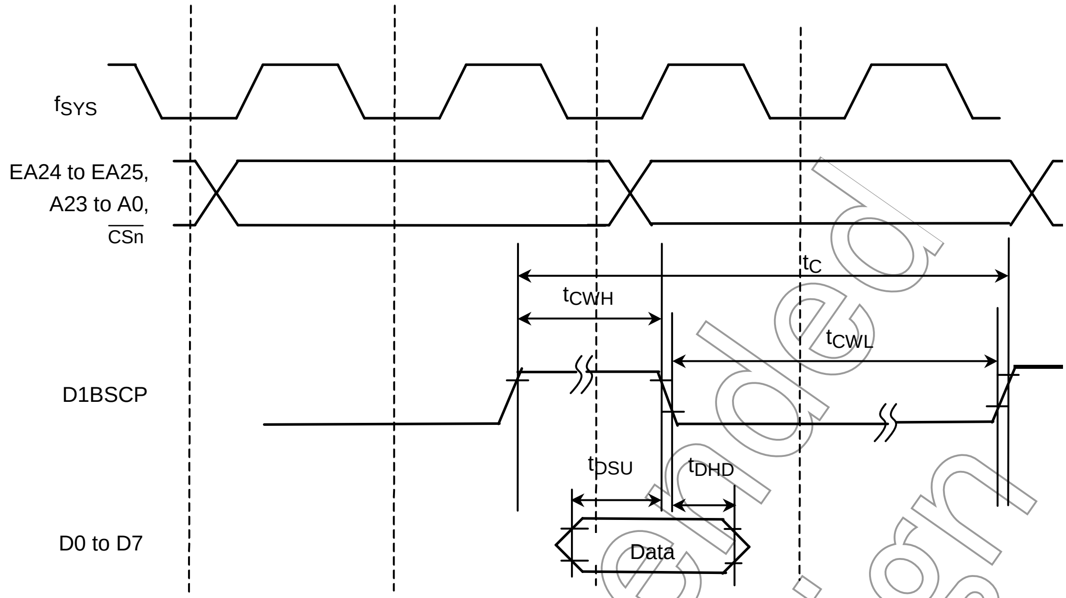
Symbol	Parameter	Variable		27 MHz		36 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCH}	Clock low level width	0.5T − 10		8		3		ns
t_{SCL}	Clock high level width	0.5T − 10		8		3		ns

Note: T = Period of SCOUT

Measuring condition

- Output level: High 0.7Vcc/Low 0.3 Vcc, CL = 10 pF

4.9 LCD Controller (SR mode)



Read Bus Width	TYPE	Write Mode	Setup Time (t_{DSU})	Hold Time (t_{DHD})	Clock High Width (t_{CWH})	Cycle (tc)	State/ Cycle
Byte	A	Byte	0.5x – α	1.0x – β	1.5x – γ	4.0x	4.0x
		Nibble	0.5x – α	1.0x – β	1.0x – γ	2.0x	6.0x
	B	Byte	1.0x – α	0.5x – β	2.0x – γ	4.0x	4.0x
		Nibble	1.0x – α	0.5x – β	1.0x – γ	2.0x	6.0x
	C	Byte	1.0x – α	2.5x – β	1.5x – γ	6.0x	6.0x
		Nibble	1.0x – α	1.5x – β	2.5x – γ	5.0x	10.0x
Word	A	Byte	0.5x – α	1.0x – β	1.0x – γ	2.0x	6.0x
		Nibble	0.5x – α	1.0x – β	1.0x – γ	2.0x	10.0x
	B	Byte	1.0x – α	0.5x – β	1.0x – γ	2.0x	6.0x
		Nibble	1.0x – α	0.5x – β	1.0x – γ	2.0x	10.0x
	C	Byte	1.0x – α	1.5x – β	1.5x – γ	3.0x	8.0x
		Nibble	1.0x – α	1.5x – β	2.5x – γ	5.0x	20.0x

Note: Value of alpha, beta and gamma are showed next page.

No.	Symbol	Parameter	Variable		27 MHz		36 MHz		Condition	Unit
			Min	Max	Min	Max	Min	Max		
1	t_{DSU}	D1BSCP rising → Data setup time	0.5x – 8		10		5		3.6 V ≥ Vcc ≥ 2.7 V	ns
			1.0x – 8		29		19			
2	t_{DHD}	D1BSCP falling → Data hold time	0.5x – 8		10		5			
			1.0x – 8		29		19			
			1.5x – 8		47		33			
			2.5x – 8		84		61			
3	t_{CWH}	D1BSCP high width	1.0x – 12		25		15			
			1.5x – 12		43		29			
			2.0x – 12		62		43			
			2.5x – 12		80		57			
4	t_C	D1BSCP clock cycle	2.0x		74		55			
			3.0x		111		83			
			4.0x		148		110			
			5.0x		185		138			
			6.0x		222		166			

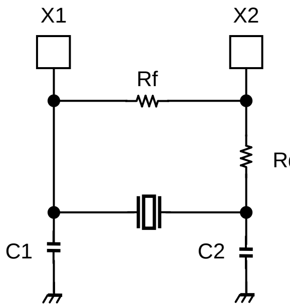
Note: The reading characteristics of display data from the memory which does not define above table, is same as 4.3 AC electrical

4.10 Recommended Crystal Oscillation Circuit

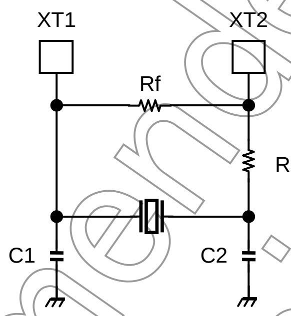
TMP91C025 is evaluated by below oscillator vender. When selecting external parts, make use of this information.

Note: Total loads value of oscillator is sum of external loads (C1 and C2) and floating loads of actual assemble board. There is a possibility of miss-operating using C1 and C2 value in below table. When designing board, it should design minimum length pattern around oscillator. And we recommend that oscillator evaluation try on your actual using board.

(1) Connection example



High-Frequency Oscillator



Low-Frequency Oscillator

(2) TMP91C025 recommended ceramic oscillator: Murata Manufacturing Co., LTD; JAPAN

MCU	Frequency [MHz]	Item of Oscillator	Parameter of Elements				Running Condition	
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]	Voltage of Power [V]	T_C [°C]
TMP91C025FG	9.0	CSTLS9M00G56-B0	(47)	(47)	Open	0	2.7~3.6	−20~80

- The values enclosed in blackest in the C1 and C2 columns apply to the condenser built-in type.
- The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL:

  http://www.murata.co.jp/search/index.html

5. Table of SFR

The SFRs (Special function registers) include the I/O ports and peripheral control registers allocated to the 4-Kbyte address space from 000000H to 000FFFH.

(1) I/O port

(2) I/O port control

(3) Interrupt control

(4) Chip select/wait control

(5) Clock gear

(6) DFM (Clock doubler)

(7) 8-bit timer

(8) UART/serial channel

(9) AD converter

(10) Watchdog timer

(11) Real-time clock

(12) Melody/alarm generator

(13) MMU

(14) LCD control

(15) Touch screen interface

Table layout

Note: Prohibit RMW in the table means that you cannot use RMW instructions on these register.

Example: When setting bit0 only of the register PxCR, the instruction SET 0, (PxCR) cannot be used. The LD (transfer) instruction must be used to write all eight bits.

Read/Write

R/W: Both read and write are possible.

R: Only read is possible.

W: Only write is possible.

W*: Both read and write are possible (when this bit is read as1)

Prohibit RMW: Read-modify-write instructions are prohibited. (The EX, ADD, ADC, BUS, SBC, INC, DEC, AND, OR, XOR, STCF, RES, SET, CHG, TSET, RLC, RRC, RL, RR, SLA, SRA, SLL, SRL, RLD and RRD instruction are read-modify-write instructions.)

R/W*: Read-modify-write instructions are prohibited when controlling the pull-up resistor.

Table 5.1 Address Map SFRs

[1], [2] Port

Address	Name
0000H	
1H	P1
2H	
3H	
4H	P1CR
5H	
6H	P2
7H	
8H	
9H	P2FC
AH	
BH	
CH	
DH	P5
EH	
FH	

Address	Name
0010H	P5CR
1H	
2H	P6
3H	
4H	
5H	P6FC
6H	
7H	
8H	P8
9H	P9
AH	
BH	P6FC2
CH	
DH	P9FC
EH	PA
FH	

Address	Name
0020H	PAFC2
1H	PAFC
2H	PB
3H	PC
4H	PBCR
5H	PBFC
6H	PCCR
7H	PCFC
8H	PCODE
9H	PD
AH	PDFC
BH	TSICR0
CH	TSICR1
DH	
EH	
FH	

Address	Name
0070H	
1H	
2H	
3H	
4H	
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	
DH	PZ
EH	PZCR
FH	PZFC

[3] INTC

Address	Name
0080H	DMA0V
1H	DMA1V
2H	DMA2V
3H	DMA3V
4H	
5H	
6H	
7H	
8H	INTCLR
9H	DMAR
AH	DMAB
BH	
CH	IIMC
DH	
EH	
FH	

Address	Name
0090H	INTE0AD
1H	INTE12
2H	INTE3ALM4
3H	INTEALM01
4H	INTEALM23
5H	INTETA01
6H	INTETA23
7H	INTERTCKEY
8H	INTES0
9H	INTES1
AH	INTELCD
BH	INTETC01
CH	INTETC23
DH	INTEP01
EH	
FH	

[4] CS/WAIT

Address	Name
00C0H	B0CS
1H	B1CS
2H	B2CS
3H	B3CS
4H	
5H	
6H	
7H	BEXCS
8H	MSAR0
9H	MAMR0
AH	MSAR1
BH	MAMR1
CH	MSAR2
DH	MAMR2
EH	MSAR3
FH	MAMR3

[5], [6] CGEAR, DFM

Address	Name
00E0H	SYSCR0
1H	SYSCR1
2H	SYSCR2
3H	EMCCR0
4H	EMCCR1
5H	EMCCR2
6H	EMCCR3
7H	
8H	DFMCR0
9H	DFMCR1
AH	
BH	
CH	
DH	
EH	
FH	

[7] TMRA

Address	Name
0100H	TA01RUN
1H	
2H	TA0REG
3H	TA1REG
4H	TA01MOD
5H	TA1FFCR
6H	
7H	
8H	TA23RUN
9H	
AH	TA2REG
BH	TA3REG
CH	TA23MOD
DH	TA3FFCR
EH	
FH	

[8] UART/serial channel

Address	Name
0200H	SC0BUF
1H	SC0CR
2H	SC0MOD0
3H	BR0CR
4H	BR0ADD
5H	SCMOD1
6H	
7H	SIRCR
8H	SC1BUF
9H	SC1CR
AH	SC1MOD0
BH	BR1CR
CH	BR1ADD
DH	SC1MOD1
EH	
FH	

[9] 10-bit ADC

Address	Name
02A0H	ADREG04L
1H	ADREG04H
2H	ADREG15L
3H	ADREG15H
4H	ADREG26L
5H	ADREG26H
6H	ADREG37L
7H	ADREG37H
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

Address	Name
02B0H	ADMOD0
1H	ADMOD1
2H	
3H	
4H	
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

Note: Do not access to the unnamed addresses, e.g., addresses to which no register has been allocated.

[10] WDT

Address	Name
0300H	WDMOD
1H	WDCR
2H	
3H	
4H	
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

[11] RTC

Address	Name
0320H	SECR
1H	MINR
2H	HOURR
3H	DAYR
4H	DATER
5H	MONTHR
6H	YEARR
7H	PAGER
8H	RESTR
9H	
AH	
BH	
CH	
DH	
EH	
FH	

[12] MLD

Address	Name
0330H	ALM
1H	MELALMC
2H	MELFL
3H	MELFH
4H	ALMINT
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

[13] MMU

Address	Name
0350H	LOCAL0
1H	LOCAL1
2H	LOCAL2
3H	LOCAL3
4H	
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

[14] LCD controller

Address	Name
0360H	LCDSAL
1H	LCDSAH
2H	LCDSIZE
3H	LCDCTL
4H	LCDFFP
5H	
6H	LCDCTL2
7H	
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

Note: Do not access to the unnamed addresses, e.g., addresses to which no register has been allocated.

(1) I/O ports

Symbol	Name	Address	7	6	5	4	3	2	1	0
P1	Port 1	01H	P17	P16	P15	P14	P13	P12	P11	P10
			R/W							
			Data from external port (Output latch register is cleared to 0).							
P2	Port 2	06H	P27	P26	P25	P24	P23	P22	P21	P20
			R/W							
			1	1	1	1	1	1	1	1
P5	Port 5	0DH		P56						
				R/W						
				Data from external port (Output latch register is set to 1).						
				0 (Output latch register) : Pull-up resistor OFF 1(Output latch register) : Pull-up resistor ON						
P6	Port 6	12H			P65	P64	P63	P62	P61	P60
					R/W					
					1	1	1	0	1	1
P8	Port 8	18H					P83	P82	P81	P80
							R			
							Data from external port.			
P9	Port 9	19H	P97	P96	P95	P94	P93	P92	P91	P90
			R							
			Data from external port.							
PA	Port A	1EH					PA3	PA2	PA1	PA0
							R/W			
							1	1	1	1
PB	Port B	22H		PB6	PB5	PB4	PB3			
				R/W						
				1	1	1	1			
				Data from external port (Output latch register is set to 1).						
PC	Port C	23H			PC5	PC4	PC3	PC2	PC1	PC0
					R/W					
					Data from external port (Output latch register is set to 1).					
PD	Port D	29H	PD7			PD4	PD3	PD2	PD1	PD0
			R/W			R/W				
			1			1	1	1	1	1
PZ	Port Z	7DH					PZ3	PZ2		
							R/W			
							Data from external port (Output latch register is set to 1”			
							0 (Output latch register) : Pull-up resistor OFF 1(Output latch register) : Pull-up resistor ON			

(2) I/O ports control (1/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
P1CR	Port 1 control	04H (Prohibit RMW)	P17C	P16C	P15C	P14C	P13C	P12C	P11C	P10C
			W							
			0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
			0: Input 1: Output							
P2FC	Port 2 function	09H (Prohibit RMW)	P27F	P26F	P25F	P24F	P23F	P22F	P21F	P20F
			W							
			1	1	1	1	1	1	1	1
			0: Port, 1:Address bus (A23 to A16)							
PZCR	Port Z control	7EH (Prohibit RMW)					PZ3C	PZ2C		
							W			
							0	0		
							0: Input 1: Output			
PZFC	Port Z function	7FH (Prohibit RMW)					PZ3F	PZ2F		
							W			
							0	0		
							0: Port 1: R/$\overline{W}$, $\overline{SRWR}$	0: Port 1: $\overline{HWR}$		
P5CR	Port 5 control	10H (Prohibit RMW)		P56C						
				W						
				0						
				0: Input 1: Output						
P6FC	Port 6 function	15H (Prohibit RMW)			P65F	P64F	P63F	P62F	P61F	P60F
					W					
					0	0	0	0	0	0
					0: Port 1: EA25	0: Port 1: EA24	0: Port 1: $\overline{CS3}$	0: Port 1: $\overline{CS2}$	0: Port 1: $\overline{CS1}$	0: Port 1: $\overline{CS0}$
P6FC2	Port 6 function2	1BH (Prohibit RMW)			P65F2	P64F2	–	P62F2	–	–
					W		W	W	W	W
					0	0	0	0	0	0
					0: <P65F> 1: $\overline{CS2C}$	0: <P64F> 1: $\overline{CS2B}$	Always write 0.	0: <P62F> 1: $\overline{CS2A}$	Always write 0.	
P9FC	Port 9 function	1DH (Prohibit RMW)	P97F	P96F	P95F	P94F	P93F	P92F	P91F	P90F
			W							
			0	0	0	0	0	0	0	0
			0: KEY-IN DISABLE , 1: KEY-IN ENABLE							
PAFC	Port A function	21H (Prohibit RMW)					PA3F	PA2F	PA1F	PA0F
							W			
							0	0	0	0
							0: CMOS output , 1: Open-drain output			
PAFC2	Port A function 2	20H (Prohibit RMW)					PA3F2	PA2F2	PA1F2	PA0F2
							W			
							0	0	0	0
							0: Port 1: SCOUT	0: Port 1: TA3OUT	0: Port 1: TA1OUT	0: Port 1: $\overline{ALARM}$ at <PA0>=1 1: $\overline{MLDALM}$ at <PA0>=0

I/O ports control (2/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
PBCR	Port B control	24H (Prohibit RMW)				PB4C	PB3C			
						W				
						0	0			
						0: Input 1: Output				
PBFC	Port B function	25H (Prohibit RMW)		PB6F	PB5F	PB4F	PB3F			
				W						
				0	0	0	0			
				0: Port 1: INT3	0: Port 1: INT2	0: Port 1: INT1	0: Port 1: INT0			
PCCR	Port C control	26H (Prohibit RMW)			PC5C	PC4C	PC3C	PC2C	PC1C	PC0C
					W					
					0	0	0	0	0	0
					0: Input 1: Output					
PCFC	Port C function	27H (Prohibit RMW)			PC5F		PC3F	PC2F		PC0F
					W		W	W		W
					0		0	0		0
					0: Port 1: SCLK1		0: Port 1: TXD1	0: Port 1: SCLK0		0: Port 1: TXD0
PCODE	Port C open-drain	28H (Prohibit RMW)					ODEPC3			ODEPC0
							W			W
							0			0
							0: CMOS 1: Open-drain			0: CMOS 1: Open-drain
PDFC	Port D function	2AH (Prohibit RMW)	PD7F			PD4F	PD3F	PD2F	PD1F	PD0F
			W			W	W	W	W	W
			0			0	0	0	0	0
			0: Port 1: MLDALM			0: Port 1: DOFFB	0: Port 1: DLEBCD	0: Port 1:D3BFR	0: Port 1: D2BLP	0: Port 1: D1BSCP

(3) Interrupt control (1/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
INTE0AD	INT0 and INTAD enable	90H	INTAD				INT0			
			IADC	IADM2	IADM1	IADM0	I0C	I0M2	I0M1	I0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
			1: INTAD	Interrupt level			1: INT0	Interrupt level		
INTE12	INT1 and INT2 enable	91H	INT2				INT1			
			I2C	I2M2	I2M1	I2M0	I1C	I1M2	I1M1	I1M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
			1: INT2	Interrupt level			1: INT1	Interrupt level		
INTE3ALM4	INT3 and INTALM4 enable	92H	INTALM4				INT3			
			IA4C	IA4M2	IA4M1	IA4M0	I3C	I3M2	I3M1	I3M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
			1: INTALM4	Interrupt level			1: INT3	Interrupt level		
INTEALM01	INTALM0 and INTALM1 enable	93H	INTALM1				INTALM0			
			IA1C	IA1M2	IA1M1	IA1M0	IA0C	IA0M2	IA0M1	IA0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
			1: INTALM1	Interrupt level			1: INTALM0	Interrupt level		
INTEALM23	INTALM2 and INTALM3 enable	94H	INTALM3				INTALM2			
			IA3C	IA3M2	IA3M1	IA3M0	IA2C	IA2M2	IA2M1	IA2M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
			1: INTALM3	Interrupt level			1: INTALM2	Interrupt level		
INTETA01	INTTA0 and INTTA1 enable	95H	INTTA1 (TMRA1)				INTTA0 (TMRA0)			
			ITA1C	ITA1M2	ITA1M1	ITA1M0	ITA0C	ITA0M2	ITA0M1	ITA0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
			1: INTTA1	Interrupt level			1: INTTA0	Interrupt level		
INTETA23	INTTA2 and INTTA3 enable	96H	INTTA3 (TMRA3)				INTTA2 (TMRA2)			
			ITA3C	ITA3M2	ITA3M1	ITA3M0	ITA2C	ITA2M2	ITA2M1	ITA2M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
			1: INTTA3	Interrupt level			1: INTTA2	Interrupt level		
INTERTCKEY	INTRTC0 and INTKEY enable	97H	INTKEY				INTRTC			
			IKC	IKM2	IKM1	IKM0	IRC	IRM2	IRM1	IRM0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
			1: INTKEY	Interrupt level			1: INTRTC	Interrupt level		
INTES0	INTRX0 and INTTX0 enable	98H	INTTX0				INTRX0			
			ITX0C	ITX0M2	ITX0M1	ITX0M0	IRX0C	IRX0M2	IRX0M1	IRX0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
			1: INTTX0	Interrupt level			1: INTRX0	Interrupt level		
INTES1	INTRX1 and INTTX1 enable	99H	INTTX1				INTRX1			
			ITX1C	ITX1M2	ITX1M1	ITX1M0	IRX1C	IRX1M2	IRX1M1	IRX1M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
			1: INTTX1	Interrupt level			1: INTRX1	Interrupt level		

Interrupt control (2/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
INTLCD	INTLCD enable	9AH	INTLCD				–			
			ILCD2C	ILCDM2	ILCDM1	ILCDM0	–	–	–	–
			R	R/W			–	–		
			0	0	0	0	–	–	–	–
			1: INTLCD	Interrupt level			Always write 0			
INTETC01	INTTC0 and INTTC1 enable	9BH	INTTC1				INTTC0			
			ITC1C	ITC1M2	ITC1M1	ITC1M0	ITC0C	ITC0M2	ITC0M1	ITC0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTETC23	INTTC2 and INTTC3 enable	9CH	INTTC3				INTTC0			
			ITC3C	ITC3M2	ITC3M1	ITC3M0	ITC2C	ITC2M2	ITC2M1	ITC2M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
INTEP01	INTP0 and INTP1 enable	9DH	INTP1				INTP0			
			IP1C	IP1M2	IP1M1	IP1M0	IP0C	IP0M2	IP0M1	IP0M0
			R	R/W			R	R/W		
			0	0	0	0	0	0	0	0
DMA0V	DMA 0 request vector	80H			DMA0V5	DMA0V4	DMA0V3	DMA0V2	DMA0V1	DMA0V0
					R/W					
					0	0	0	0	0	0
					DMA0 Start vector.					
DMA1V	DMA 1 request vector	81H			DMA1V5	DMA1V4	DMA1V3	DMA1V2	DMA1V1	DMA1V0
					R/W					
					0	0	0	0	0	0
					DMA1 Start vector.					
DMA2V	DMA 2 request vector	82H			DMA2V5	DMA2V4	DMA2V3	DMA2V2	DMA2V1	DMA2V0
					R/W					
					0	0	0	0	0	0
					DMA2 Start vector.					
DMA3V	DMA 3 request vector	83H			DMA3V5	DMA3V4	DMA3V3	DMA3V2	DMA3V1	DMA3V0
					R/W					
					0	0	0	0	0	0
					DMA3 Start vector.					
INTCLR	Interrupt clear control	88H (Prohibit RMW)			CLRV5	CLRV4	CLRV3	CLRV2	CLRV1	CLRV0
					W					
					0	0	0	0	0	0
					Clears interrupt request flag by writing to DMA start vector.					
DMAR	DMA software request register	89H (Prohibit RMW)					DMAR3	DMAR2	DMAR1	DMAR0
							R/W	R/W	R/W	R/W
							0	0	0	0
							1: DMA request in software			
DMAB	DMA burst request register	8AH					DMAB3	DMAB2	DMAB1	DMAB0
							R/W	R/W	R/W	R/W
							0	0	0	0
							1 : DMA request on Burst Mode			
IIMC	Interrupt input mode control	8CH (Prohibit RMW)	–	–	I3EDGE	I2EDGE	I1EDGE	I0EDGE	I0LE	–
			W	W	W	W	W	W	W	W
			0	0	0	0	0	0	0	0
			Always write 0.	Always write 0.	INT3 edge 0: Rising 1: Falling	INT2 edge 0: Rising 1: Falling	INT1 edge 0: Rising 1: Falling	INT0 edge 0: Rising 1: Falling	INT0 0: edge 1:level	Always write 0.

(4) Chip select/wait control (1/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
B0CS	Block 0 CS/WAIT control register	C0H (Prohibit RMW)	B0E		B0OM1	B0OM0	B0BUS	B0W2	B0W1	B0W0
			W		W	W	W	W	W	W
			0		0	0	0	0	0	0
			0: Disable 1: Enable		00: ROM/SRAM 01: 10: Reserved 11:		Data bus width. 0: 16 bits 1: 8 bits	000: 2 waits 001: 1 wait 010: (1 + N) waits 011: 0 waits 100: (0 + N) waits 101: 3 waits 110: 4 waits 111: 8 waits		
B1CS	Block 1 CS/WAIT control register	C1H (Prohibit RMW)	B1E		B1OM1	B1OM0	B1BUS	B1W2	B1W1	B1W0
			W		W	W	W	W	W	W
			0		0	0	0	0	0	0
			0: Disable 1: Enable		00: ROM/SRAM 01: 10: Reserved 11:		Data bus width. 0: 16 bits 1: 8 bits	000: 2 waits 001: 1 wait 010: (1 + N) waits 011: 0 waits 100: (0 + N) waits 101: 3 waits 110: 4 waits 111: 8 waits		
B2CS	Block 2 CS/WAIT control register	C2H (Prohibit RMW)	B2E	B2M	B2OM1	B2OM0	B2BUS	B2W2	B2W1	B2W0
			W	W	W	W	W	W	W	W
			1	0	0	0	0	0	0	0
			0: Disable 1: Enable	0: 16 M area 1: Area set	00: ROM/SRAM 01: 10: Reserved 11:		Data bus width. 0: 16 bits 1: 8 bits	000: 2 waits 001: 1 wait 010: (1 + N) waits 011: 0 waits 100: (0 + N) waits 101: 3 waits 110: 4 waits 111: 8 waits		
B3CS	Block 3 CS/WAIT control register	C3H (Prohibit RMW)	B3E		B3OM1	B3OM0	B3BUS	B3W2	B3W1	B3W0
			W		W	W	W	W	W	W
			0		0	0	0	0	0	0
			0: Disable 1: Enable		00: ROM/SRAM 01: 10: Reserved 11:		Data bus width. 0: 16 bits 1: 8 bits	000: 2 waits 001: 1 wait 010: (1 + N) waits 011: 0 waits 100: (0 + N) waits 101: 3 waits 110: 4 waits 111: 8 waits		
BEXCS	External CS/WAIT control register	C7H (Prohibit RMW)					BEXBUS	BEXW2	BEXW1	BEXW0
							W	W	W	W
							0	0	0	0
							Data bus width. 0: 16 bits 1: 8 bits	000: 2 waits 001: 1 wait 010: (1 + N) waits 011: 0 waits 100: (0 + N) waits 101: 3 waits 110: 4 waits 111: 8 waits		
MSAR0	Memory start address register 0	C8H	S23	S22	S21	S20	S19	S18	S17	S16
			R/W							
			1	1	1	1	1	1	1	1
			Start address A23 to A16.							
MAMR0	Memory address mask register 0	C9H	V20	V19	V18	V17	V16	V15	V14 to 9	V8
			R/W							
			1	1	1	1	1	1	1	1
			CS0 area size 0: Enable to address comparison							
MSAR1	Memory start address register 1	CAH	S23	S22	S21	S20	S19	S18	S17	S16
			R/W							
			1	1	1	1	1	1	1	1
			Start address A23 to A16.							
MAMR1	Memory address mask register 1	CBH	V21	V20	V19	V18	V17	V16	V15 to 9	V8
			R/W							
			1	1	1	1	1	1	1	
			CS1 area size 0: Enable to address comparison							

Interrupt control (2/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
MSAR2	Memory start address register 2	CCH	S23	S22	S21	S20	S19	S18	S17	S16
			R/W							
			1	1	1	1	1	1	1	1
			Start address A23 to A16.							
MAMR2	Memory address mask register 2	CDH	V22	V21	V20	V19	V18	V17	V16	V15
			R/W							
			1	1	1	1	1	1	1	1
			CS2 area size 0: Enable to address comparison							
MSAR3	Memory start address register 3	CEH	S23	S22	S21	S20	S19	S18	S17	S16
			R/W							
			1	1	1	1	1	1	1	1
			Start address A23 to A16.							
MAMR3	Memory address mask register 3	CFH	V22	V21	V20	V19	V18	V17	V16	V15
			R/W							
			1	1	1	1	1	1	1	1
			CS3 area size 0: Enable to address comparison							

(5) Clock gear (1/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
SYSCR0	System clock control register 0	E0H	XEN	XTEN	RXEN	RXTEN	RSYSCK	WUEF	PRCK1	PRCK0
			R/W							
			1	1	1	0	0	0	0	0
			High-frequency oscillator. (fc) 0: Stopped 1: Oscillation	Low-frequency oscillator. (fs) 0: Stopped 1: Oscillation	High-frequency oscillator (fc) after release of STOP Mode. 0: Stopped 1: Oscillation	Low-frequency oscillator (fs) after release of STOP Mode. 0: Stopped 1: Oscillation	Select clock after release of STOP Mode. 0: fc 1: fs	Warm-up timer 0 write: Don't care 1 write: start timer 0 read: end warm-up 1 read: not end warm up	Select prescaler clock. 00: f_{FPH} 01: reserved 10: fc/16 11: Reserved	
SYSCR1	System clock control register 1	E1H					SYSCK	GEAR2	GEAR1	GEAR0
							R/W			
							0	1	0	0
							System clock selection 0: fc 1: fs	High-frequency gear value selection. (fc) 000: fc 001: fc/2 010: fc/4 011: fc/8 100: fc/16 101: (Reserved) 110: (Reserved) 111: (Reserved)		
SYSCR2	System clock control register 2	E2H	PSENV		WUPTM1	WUPTM0	HALTM1	HALTM0	SELDRV	DRVE
			R/W		R/W	R/W	R/W	R/W	R/W	R/W
			0		1	0	1	1	0	0
			0: Power save mode enable 1: Disable		Warm-up time 00: Reserved 01: 2^8/input frequency 10: 2^{14} 11: 2^{16}		00: Reserved 01: STOP mode 10: IDLE1 mode 11: IDLE2 mode		<Drive> mode select 0: IDLE1 1: STOP	1: Drive the pin in STOP/ IDLE1mode

Clock gear (1/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
EMCCR0	EMC control register 0	E3H	PROTECT	TA3LCDE	AHOLD	TA3MLDE	–	EXTIN	DRVOSCH	DRVOSCL
			R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	1	1
			Protection flag 0: Off 1: On	LCDC Source clock 0: 32 kHz 1: TA3OUT	Address hold 0: Normal 1: Hold	MLD source clock 0: 32 kHz 1: TA3OUT	Always write 0.	1: fc is external clock.	fc oscillator drivability 1: Normal 0: Weak	fs oscillator drivebility 1: Normal 0: Weak
EMCCR1	EMC control register 1	E4H	Switching the protect ON/OFF by write to following 1st-KEY, 2nd-KEY 1st-KEY: EMCCR1 = 5AH, EMCCR2 = A5H in succession write 2nd-KEY: EMCCR1 = A5H, EMCCR2 = 5AH in succession write							
EMCCR2	EMC control register 2	E5H								
EMCCR3	EMC control register 3	E6H		ENFROM	ENDROM	ENPROM		FFLAG	DFLAG	PFLAG
				R/W	R/W	R/W		R/W	R/W	R/W
				0	0	0		0	0	0
				CS1A area detect enable 0: Disable 1: Enable	CS2B-2C area detect enable 0: Disable 1: Enable	CS2A area detect enable 0: Disable 1: Enable		CS1A write operation flag	CS2B-2C write operation flag	CS2A write operation flag
								When reading 0: Not written 1: Written		When writing 0: Clear flag

(6) DFM (clock doubler)

Symbol	Name	Address	7	6	5	4	3	2	1	0
DFMCR0	DFM control register 0	E8H	ACT1	ACT0	DLUPFG	DLUPTM				
			R/W	R/W	R	R/W				
			0	0	0	0				
			(ACT1, ACT0) / DFM / LUP / f_{FPH} 00 / STOP / STOP / f_{OSCH} 01 / RUN / RUN / f_{OSCH} 10 / RUN / STOP / f_{DFM} 11 / RUN / STOP / f_{OSCH}		Lockup falg 0: End LUP 1: Not end	Lockup time 0: $2^{12}/f_{OSCH}$ 1: $2^{10}/f_{OSCH}$				
DFMCR1	DFM control register 1	E9H	D7	D6	D5	D4	D3	D2	D1	D0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	1	0	0	1	1
			DFM correction Input frequency 4 to 9 MHz (at 3.0 to 3.6 V): Write 0BH Input frequency 4 to 6.75 MHz (at 2.7 to 3.6 V): Write 0BH							

(7) 8-bit timer

(7–1) TMRA01

Symbol	Name	Address	7	6	5	4	3	2	1	0
TA01RUN	8-bit timer RUN register	100H	TA0RDE				I2TA01	TA01PRUN	TA1RUN	TA0RUN
			R/W				R/W	R/W	R/W	R/W
			0				0	0	0	0
			Double Buffer 0: Disable 1: Enable				IDLE2 0: Stop 1: Operate	8-bit timer run/stop control 0: Stop and clear 1: Run (Count up)		
TA0REG	8-bit timer register 0	102H (Prohibit RMW)	–							
			W							
			Undefined							
TA1REG	8-bit timer register 1	103H (Prohibit RMW)	–							
			W							
			Undefined							
TA01MOD	8-bit timer source CLK and MODE	104H	TA01M1	TA01M0	PWM01	PWM00	TA1CLK1	TA1CLK0	TA0CLK1	TA0CLK0
			R/W							
			0	0	0	0	0	0	0	0
			00: 8-bit timer 01: 16-bit timer 10: 8-bit PPG 11: 8-bit PWM		00: Reserved 01: 2^6 PWM cycle 10: 2^7 11: 2^8		00: TA0TRG 01: ϕT1 10: ϕT16 11: ϕT256		00: TA0IN pin 01: ϕT1 10: ϕT4 11: ϕT16	
TA1FFCR	8-bit timer flip-flop control	105H (Prohibit RMW)					TA1FFC1	TA1FFC0	TA1FFIE	TA1FFIS
							R/W		R/W	
							1	1	0	0
							00: Invert TA1FF 01: Set TA1FF 10: Clear TA1FF 11: Don't care		1: TA1FF invert enable	0: TMRA0 1: TMRA1 inversion

(7–2) TMRA23

Symbol	Name	Address	7	6	5	4	3	2	1	0
TA23RUN	8-bit timer RUN register	108H	TA2RDE				I2TA23	TA23PRUN	TA3RUN	TA2RUN
			R/W				R/W	R/W	R/W	R/W
			0				0	0	0	0
			Double buffer 0: Disable 1: Enable				IDLE2 0: Stop 1: Operate	8-bit timer run/stop control 0: Stop and clear 1: Run (Count up)		
TA2REG	8-bit timer register 0	10AH (Prohibit RMW)	–							
			W							
			Undefined							
TA3REG	8-bit timer register 1	10BH (Prohibit RMW)	–							
			W							
			Undefined							
TA23MOD	8-bit timer source CLK and MODE	10CH	TA23M1	TA23M0	PWM21	PWM20	TA3CLK1	TA3CLK0	TA2CLK1	TA2CLK0
			R/W							
			0	0	0	0	0	0	0	0
			00: 8-bit timer 01: 16-bit timer 10: 8-bit PPG 11: 8-bit PWM		00: Reserved 01: 2^6 PWM cycle 10: 2^7 11: 2^8		00: TA2TRG 01: ϕT1 10: ϕT16 11: ϕT256		00: Reserved 01: ϕT1 10: ϕT4 11: ϕT16	
TA3FFCR	8-bit timer flip-flop control	10DH (Prohibit RMW)					TA3FFC1	TA3FFC0	TA3FFIE	TA3FFIS
							R/W		R/W	
							1	1	0	0
							00: Invert TA3FF 01: Set TA3FF 10: Clear TA3FF 11: Don't care		1: TA3FF invert enable	0: TMRA2 1: TMRA3 inversion

(8) UART/serial channel (1/2)

(8-1) UART/SIO channel 0

Symbol	Name	Address	7	6	5	4	3	2	1	0
SC0BUF	Serial channel 0 buffer	200H (Prohibit RMW)	RB7/TB7	RB6/TB6	RB5/TB5	RB4/TB4	RB3/TB3	RB2/TB2	RB1/TB1	RB0/TB0
			R (Receiving)/W (Transmission)							
			Undefined							
SC0CR	Serial channel 0 control	201H	RB8	EVEN	PE	OERR	PERR	FERR	SCLKS	IOC
			R	R/W		R (Cleared to 0 by reading.)			R/W	
			Undefined	0	0	0	0	0	0	0
			Receiving data bit8.	Parity 0: Odd 1: Even	Parity enable.	1: Error			0:SCLK0↑ 1:SCLK0↓	1: Input SCLK0 pin
						Over Run	Parity	Framing		
SC0MOD0	Serial channel 0 mode0	202H	TB8	CTSE	RXE	WU	SM1	SM0	SC1	SC0
			R/W							
			0	0	0	0	0	0	0	0
			Transfer data bit8.	1: CTS enable	1: Receive enable	1: Wakeup enable	00: I/O Interface 01: UART 7 bits 10: UART 8 bits 11: UART 9 bits		00: TA0TRG 01: Baud rate generator 10: Internal clock f_{SYS} 11: External clock SCLK0	
BR0CR	Baud rate control	203H	–	BR0ADDE	BR0CK1	BR0CK0	BR0S3	BR0S2	BR0S1	BR0S0
			R/W							
			0	0	0	0	0	0	0	0
			Always write 0.	1: (16-K)/16 divided enable	00: ϕT0 01: ϕT2 10: ϕT8 11: ϕT32		Setting the divided frequency "N" (0 to F)			
BR0ADD	Serial channel0 K setting register	204H					BR0K3	BR0K2	BR0K1	BR0K0
							R/W			
							0	0	0	0
							Sets frequency divisor "K" (Divided by N+(16-K)/16)			
SC0MOD1	Serial channel 0 mode1	205H	I2S0	FDPX0						
			R/W	R/W						
			0	0						
			IDLE2 0: Stop 1: Operate	Duplex 0: Half 1: Full						

(8-2) IrDA

Symbol	Name	Address	7	6	5	4	3	2	1	0
SIRCR	IrDA control register	207H	PLSEL	RXSEL	TXEN	RXEN	SIRWD3	SIRWD2	SIRWD1	SIRWD0
			R/W	R/W	R/W	R/W	R/W			
			0	0	0	0	0	0	0	0
			Transmission pulse width. 0: 3/16 1: 1/16	Receiving data. 0: H pulse 1: L pulse	Transmission 0: Disable 1: Enable	Receiving 0: Disable 1: Enable	Set the effective SIRRxD pulse width Pulse width more than 2x × (set value + 1) + 100ns Possible: 1 to 14 Not possible: 0, 15			

Clock gear (2/2)

(8-3) UART/SIO channel 0

Symbol	Name	Address	7	6	5	4	3	2	1	0
SC1BUF	Serial channel 1 buffer	208H (Prohibit RMW)	RB7/TB7	RB6/TB6	RB5/TB5	RB4/TB4	RB3/TB3	RB2/TB2	RB1/TB1	RB0/TB0
			R (Receiving)/W (Transmission)							
			Undefined							
SC1CR	Serial channel 1 control	209H	RB8	EVEN	PE	OERR	PERR	FERR	SCLKS	IOC
			R	R/W		R (Cleared to 0 by reading.)			R/W	
			Undefined	0	0	0	0	0	0	0
			Receiving data bit8.	Parity 0: Odd 1: Even	1:Parity enable	1: Error			0: SCLK1↑ 1: SCLK1↓	1: Input SCLK1 pin
						Over run	Parity	Framing		
SC1MOD0	Serial channel 1 mode	20AH	TB8	CTSE	RXE	WU	SM1	SM0	SC1	SC0
			R/W							
			0	0	0	0	0	0	0	0
			Trans-mission data bit8.	1: CTS enable	1: Receive enable	1: Wakeup enable	00: I/O interface 01: UART 7 bits 10: UART 8 bits 11: UART 9 bits		00: TA0TRG 01: Baud rate generater 10: Internal clock f_{SYS} 11: External clock SCLK1	
BR1CR	Baud rate control	20BH	–	BR1ADDE	BR1CK1	BR1CK0	BR1S3	BR1S2	BR1S1	BR1S0
			R/W							
			0	0	0	0	0	0	0	0
			Always write 0.	1: (16 – K)/16 divided enable	00: ϕT0 01: ϕT2 10: ϕT8 11: ϕT32		Setting the divided frequency “N” (0 to F)			
BR1ADD	Serial channel 1 K setting register	20CH					BR1K3	BR1K2	BR1K1	BR1K0
							R/W			
							0	0	0	0
							Sets frequency divisor “K” (Divided by N+(16-K)/16)			
SC1MOD1	Serial channel 1 mode1	20DH	I2S1	FDPX1						
			R/W	R/W						
			0	0						
			IDLE2 0: Stop 1: Operate	Duplex 0: Half 1: Full						

(9) AD converter

Symbol	Name	Address	7	6	5	4	3	2	1	0
ADMOD0	AD MODE register 0	2B0H	EOCF	ADBF	–	–	ITM0	REPEAT	SCAN	ADS
			R		R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			AD conversion end flag 1: End	AD conversion end flag 1: busy	Always write 0.	Always write 0.	Interrupt in Repeat Mode.	Repeat mode specification 1: Repeat	Scan mode specification 1: Scan	AD conversion start 1: Start
ADMOD1	AD MODE register 1	2B1H	VREFON	I2AD			ADTRGE	ADCH2	ADCH1	ADCH0
			R/W	R/W			R/W	R/W		
			0	0			0	0	0	0
			VREF control 1: VREF on	IDLE2 0: Abort 1: Operate			AD control 1: Enable for external start	Input channel 000: AN0 AN0 001: AN1 AN0 → AN1 010: AN2 AN0 → AN1 → AN2 011: AN3 AN0 → AN1 → AN2 → AN3 100-111: Reserved		
ADREG04L	AD result register 0/4 low	2A0H	ADR01	ADR00						ADR0RF
			R							R
			Undefined							0
ADREG04H	AD result register 0/4 high	2A1H	ADR09	ADR08	ADR07	ADR06	ADR05	ADR04	ADR03	ADR02
			R							
			Undefined							
ADREG15L	AD result register 1/5 low	2A2H	ADR11	ADR10						ADR1RF
			R							R
			Undefined							0
ADREG15H	AD result register 1/5 high	2A3H	ADR19	ADR18	ADR17	ADR16	ADR15	ADR14	ADR13	ADR12
			R							
			Undefined							
ADREG26L	AD result register 2/6 low	2A4H	ADR21	ADR20						ADR2RF
			R							R
			Undefined							0
ADREG26H	AD result register 2/6 high	2A5H	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24	ADR23	ADR22
			R							
			Undefined							
ADREG37L	AD result register 3/7 low	2A6H	ADR31	ADR30						ADR3RF
			R							R
			Undefined							0
ADREG37H	AD result register 3/7 high	2A7H	ADR39	ADR38	ADR37	ADR36	ADR35	ADR34	ADR33	ADR32
			R							
			Undefined							

(10) Watchdog timer

Symbol	Name	Address	7	6	5	4	3	2	1	0
WDMOD	WDT MODE register	300H	WDTE	WDTP1	WDTP0			I2WDT	RESCR	–
			R/W	R/W	R/W			R/W	R/W	R/W
			1	0	0			0	0	0
			1: WDT enable	00: 2^{15}/fsys 01: 2^{17}/fsys 10: 2^{19}/fsys 11: 2^{21}/fsys				IDLE2 0: Abort 1: Operate	1: RESET connect internally WDT out to reset pin	Always write 0.
WDCR	WDT control	301H (Prohibit RMW)	–							
			W							
			–							
			B1H: WDT disable 4EH: WDT clear							

(11) RTC (Real-time clock)

Symbol	Name	Address	7	6	5	4	3	2	1	0
SECR	Second register	320H		SE6	SE5	SE4	SE3	SE2	SE1	SE0
				R/W						
				Undefined						
			0 is read.	40 s	20 s	10 s	8 s	4 s	2 s	1 s
MINR	Minute register	321H		MI6	MI5	MI4	MI3	MI2	MI1	MI0
				R/W						
				Undefined						
			0 is read.	40 min	20 min	10 min	8 min	4 min	2 min	1min
HOURR	Hour register	322H			HO5	HO4	HO3	HO2	HO1	HO0
					R/W					
					Undefined					
			0 is read.		20 hour (PM/AM)	10 hour	8 hour	4 hour	2 hour	1 hour
DAYR	Day register	323H						W2	W1	W0
								R/W		
								Undefined		
			0 is read					W2	W1	W0
DATER	Date register	324H			DA5	DA4	DA3	DA2	DA1	DA0
					R/W					
					Undefined					
			0 is read.		20 day	10 day	8 day	4 day	2 day	1 day
MONTHR	Month register	325H				MO4	MO3	MO2	MO1	MO0
						R/W				
						Undefined				
		Page0	0 is read.			10 month	8 month	4 month	2 month	1 month
		Page1	0 is read.							0: Indicator for 12 hours 1: Indicator for 24 hours
YEARR	Year register	326H	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0
			R/W							
			Undefined							
		Page0	80 year	40 year	20 year	10 year	8 year	4 year	2 year	1 year
		Page1	0 is read.						Leap year setting.	
PAGER	Page register	327H (Prohibit RMW)	INTRTC			ADJUST	ENATMR	ENAALM		PAGE
			R/W			W	R/W			R/W
			0			Undefined	Undefined			Undefined
			INTRTC 0: Disable 1: Enable	0 is read.		0: Don’t care 1: Adjust	Clock 0: Disable 1: Enable	Alarm 0: Disable 1: Enable	0 is read.	PAGE setting
RESTR	Reset register	328H (Prohibit RMW)	DIS1HZ	DIS16HZ	RSTTMR	RSTALM	–	–	–	–
			W							
			Undefined							
			1Hz 0: Enable 1: Disable	16Hz 0: Enable 1: Disable	1: Clock reset	1: Alarm reset	Always write 0.			

(12) Melody/alarm generator

Symbol	Name	Address	7	6	5	4	3	2	1	0
ALM	Alarm-pattern register	330H	AL8	AL7	AL6	AL5	AL4	AL3	AL2	AL1
			R/W							
			0	0	0	0	0	0	0	0
			Alarm-pattern set.							
MELALMC	Melody/ alarm control register	331H	FC1	FC0	ALMINV	–	–	–	–	MELALM
			R/W		R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			Free-run counter Control. 00: Hold 01: Restart 10: Clear 11: Clear and start		Alarm frequency invert. 1: Invert	Always write 0.				Output frequency 0: Alarm 1: Melody
MELFL	Melody frequency L- register	332H	ML7	ML6	ML5	ML4	ML3	ML2	ML1	ML0
			R/W							
			0	0	0	0	0	0	0	0
			Melody frequency set. (Low 8 bits)							
MELFH	Melody frequency H- register	333H	MELON				ML11	ML10	ML9	ML8
			R/W				R/W			
			0				0	0	0	0
			Melody counter control. 0: Stop and clear 1: Start				Melody frequency set. (High 4 bits)			
ALMINT	Alarm interrupt enable register	334H			–	IALM4E	IALM3E	IALM2E	IALM1E	IALM0E
					R/W	R/W				
					0	0	0	0	0	0
					Always write 0.	INTALM4 to INTALM0 alarm interrupt enable.				

(13) MMU

Symbol	Name	Address	7	6	5	4	3	2	1	0
LOCAL0	LOCAL0 control register	350H	L0E					L0EA22	L0EA21	L0EA20
			R/W					R/W		
			0					0	0	0
			BANK for LOCAL0 0: Disable 1: Enable					LOCAL0 area BANK set. “000” setting is prohibited because it pretend COMMON0 area		
LOCAL1	LOCAL1 control register	351H	L1E					L1EA23	L1EA22	L1EA21
			R/W					R/W		
			0					0	0	0
			BANK for LOCAL1 0: Disable 1: Enable					LOCAL1 area BANK set. “001” setting is prohibited because it pretend COMMON0 area		
LOCAL2	LOCAL2 control register	352H	L2E					L2EA23	L2EA22	L2EA21
			R/W					R/W		
			0					0	0	0
			BANK for LOCAL2 0: Disable 1: Enable					LOCAL2 area BANK set. “111” setting is prohibited because it pretend COMMON0 area		
LOCAL3	LOCAL3 control register	353H	L3E			–	L3EA25	L3EA24	L3EA23	L3EA22
			R/W			R/W	R/W			
			0			0	0	0	0	0
			BANK for LOCAL3 0: Disable 1: Enable			Always write 0.	0000~0011: $\overline{CS2B}$ 0100~0111: $\overline{CS2C}$ 1000~1111: Set prohibition			

(14) LCD controllers

Symbol	Name	Address	7	6	5	4	3	2	1	0
LCDSAL	LCD start address register low	360H	SAL15	SAL14	SAL13	SAL12		–	–	MODE
			R/W					R/W	R/W	R/W
			0	0	0	0		0	0	0
			SR mode: Start address A15 to A12.					Always write 0.	Always write 0.	Mode select 0: RAM 1: SR
LCDSAH	LCD start address register high	361H	SAL23	SAL22	SAL21	SAL20	SAL19	SAL18	SAL17	SAL16
			R/W							
			0	0	0	0	0	0	0	0
			SR mode: Start Address A23 to A16.							
LCDSIZE	LCD size register	362H	COM3	COM2	COM1	COM0	SEG3	SEG2	SEG1	SEG0
			R/W							
			0	0	0	0	0	0	0	0
			SR mode :LCD common 0000: 64, 0101: 128 0001: 68, 0110: 144 0010: 80, 0111: 160 0011: 100, 1000: 200 0100: 120, 1001: 240 Other: Reserved				SR mode LCD Segment 0000: 32, 0101: 160 0001: 64, 0110: 240 0010: 80, 0111: 320 0011: 120, 1000: 360 0100: 128, Other: Reserved			
LCDCTL	LCD control register	363H	LCDON	–	–	BUS1	BUS0	MMULCD	FP8	START
			R/W							
			0	0	0	0	0	0	0	0
			$\overline{\text{DOFF}}$ pin 0: Off 1: On	Always write 0.	Always write 0.	SR mode: Data-bus width select. 00: 8 bits Byte 01: 4 bits Nibble 10: Reserved 11: Reserved		Type selection LCDD (build in RAM) 0: Sequential 1: Random	Set bit8 for f_{FP}	SR mode: Start address. 1: START
LCDFFP	LCD frame frequency register	364H	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
			R/W							
			0	0	0	0	0	0	0	0
			Set bit7 to bit0 for f_{FP}							
LCDCTL2	LCD control register 2	366H	–	–	–			RAMBUS	AC1	AC0
			R/W	R/W	R/W			R/W	R/W	R/W
			0	0	0			0	0	0
			Always write to “111”.					0: Byte 1: Word	00: Type A 01: Type B 10: Type C 11: Reserved	

(15) Touch screen interface

Symbol	Name	Address	7	6	5	4	3	2	1	0
TSICR0	Touch-screen control register	2BH	TSI7		PTST	TWIEN	PYEN	PXEN	MYEN	MXEN
			R/W		R	R/W	R/W	R/W	R/W	R/W
			0		0	0	0	0	0	0
			0: Disable 1: Enable		Detection condition 0: No touch 1: touch	INT2 interrupt control 0: Disable 1: Enable	SPY 0: OFF 1: ON	SPX 0: OFF 1: ON	SMY 0: OFF 1: ON	SMX 0: OFF 1: ON
TSICR1	Debounce-circuit control register	2CH	DBC7	DB1024	DB256	DB64	DB8	DB4	DB2	DB1
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			0: Disable 1: Enable	1024	256	64	8	4	2	1
				De-bounce time is set by “($N \times 64 - 16)/f_{SYS}$” – formula “N” is sum of number which is set to 1 in bit6 to bit0						

6. Points of Note and Restrictions

(1) Notation

a. The notation for built-in I/O registers is as follows register symbol <Bit symbol>

e.g.) TA01RUN<TA0RUN> denotes bit TA0RUN of register TA01RUN.

b. Read-modify-write instructions

An instruction in which the CPU reads data from memory and writes the data to the same memory location in one instruction.

Example 1: SET 3, (TA01RUN) ... Set bit 3 of TA01RUN.

Example 2: INC 1, (100H) ... Increment the data at 100H.

- Examples of read-modify-write instructions on the TLCS-900

Exchange instruction

EX (mem), R

Arithmetic operations

ADD	(mem), R/#	ADC	(mem), R/#
SUB	(mem), R/#	SBC	(mem), R/#
INC	#3, (mem)	DEC	#3, (mem)

Logic operations

AND	(mem), R/#	OR	(mem), R/#
XOR	(mem), R/#		

Bit manipulation operations

STCF	#3/A, (mem)	RES	#3, (mem)
SET	#3, (mem)	CHG	#3, (mem)
TSET	#3, (mem)		

Rotate and shift operations

RLC	(mem)	RRC	(mem)
RL	(mem)	RR	(mem)
SLA	(mem)	SRA	(mem)
SLL	(mem)	SRL	(mem)
RLD	(mem)	RRD	(mem)

c. fc, fs, f_{FPH}, f_{SYS} and one state

The clock frequency input on pins X1 and 2 is called f_{OSCH}. The clock selected by DFMCR0<ACT1:0> is called fc.

The clock selected by SYSCR1<SYSCK> is called f_{FPH}. The clock frequency give by f_{FPH} divided by 2 is called f_{SYS}.

One cycle of f_{SYS} is referred to as one state.

(2) Points to note

a. AM0 and AM1 pins

This pin is connected to the VCC or the VSS pin. Do not alter the level when the pin is active.

b. EMU0 and EMU1

Open pins.

c. Warm-up counter

The warm-up counter operates when STOP mode is released, even if the system is using an external oscillator. As a result a time equivalent to the warm-up time elapses between input of the release request and output of the system clock.

d. Programmable pull-up resistance

The programmable pull-up resistor can be turned on/off by a program when the ports are set for use as input ports. When the ports are set for use as output ports, they cannot be turned on/off by a program.

The data registers (e.g., Px) are used to turn the pull-up/pull-down resistors on/off. Consequently Read-Modify-write instructions are prohibited.

e. Watchdog timer

The watchdog timer starts operation immediately after a Reset is released. When the watchdog timer is not to be used, disable it.

f. AD converter

The string resistor between the VREFH and VREFL pins can be cut by a program so as to reduce power consumption. When STOP mode is used, disable the resistor using the program before the HALT instruction is executed.

g. CPU (micro DMA)

Only the LDC cr, r and LDC r, cr instructions can be used to access the control registers in the CPU (e.g., The transfer source address register (DMASn)).

h. Undefined SFR

The value of an undefined bit in an SFR is undefined when read.

i. POP SR instruction

Please execute the POP SR instruction during DI condition.

j. Releasing the HALT mode by requesting an interruption

Usually, interrupts can release all halts status. However, the interrupts (INT0 to INT3, INTKEY, INTRTC, INTALM0 to INTALM4) which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficulty. The priority of this interrupt is compared with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

7. Package Dimensions

P-LQFP100-1414-0.50F

Unit: mm