

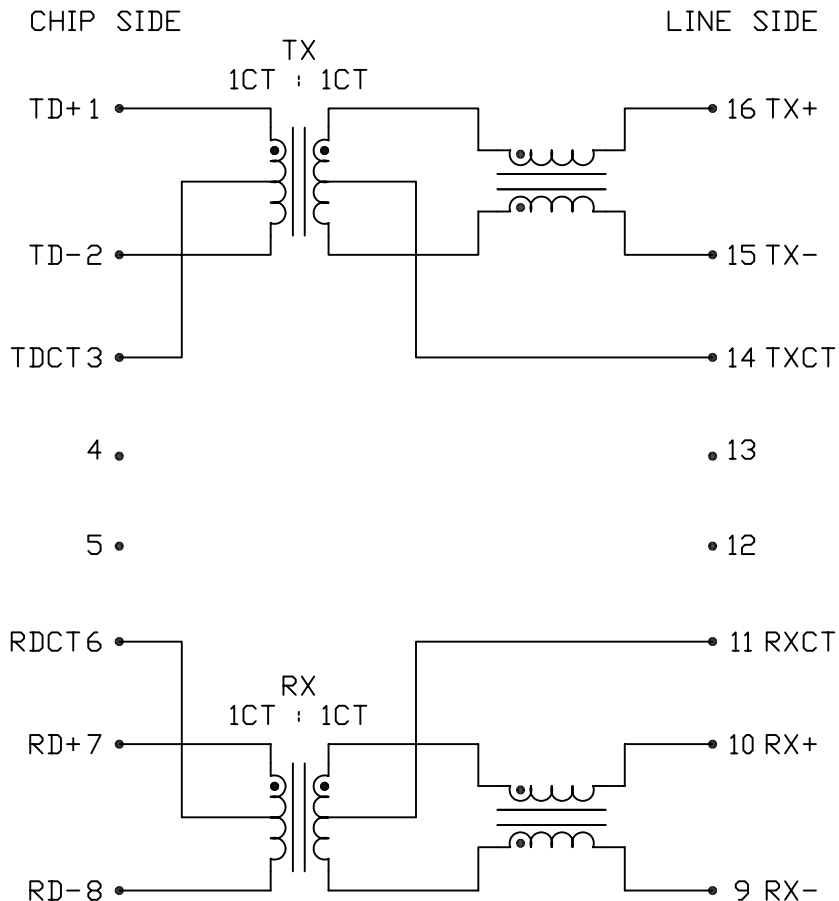
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ELECTRICAL CHARACTERISTICS @ 25°C

RoHS



SCHEMATIC



URNS RATIO

Tx (1-3-2) : (16-14-15)

Rx (7-6-8) : (10-11-9)

1CT : 1CT

1CT : 1CT

POLARITY

PER DOT CONVENTION

OCL

1-2 = 7-8

350μH MIN

@100kHz, 100mV W/8mA DC BIAS

LEAKAGE INDUCTANCE, Le

CHIP SIDE WITH LINE SIDE SHORT

0.4μH MAX

@1MHz, 20mV

INTERWINDING CAPACITANCE, Cw/w

CHIP SIDE TO LINE SIDE

25pF MAX

@1MHz, 20mV

DC RESISTANCE

(1-2) = (7-8)

1.3Ω MAX

INSERTION LOSS

@100kHz TO 80MHz

1.0dB MAX

RETURN LOSS (UNDER 100Ω ±15% ENVIRONMENT)

@0.5 TO 30 MHz

16dB MIN

@30 TO 60 MHz

16-20LOG(f/30MHz) dB MIN

@60 TO 80 MHz

10dB MIN

COMMON TO COMMON MODE ATTENUATION

@0.1 TO 80 MHz

38dB MIN

@80 TO 125 MHz

30dB MIN

@125 TO 250 MHz

10dB MIN

CROSSTALK

@0.1 TO 80 MHz

38dB MIN

@80 TO 125 MHz

30dB MIN

@125 TO 250 MHz

10dB MIN

COMMON TO DIFFERENTIAL MODE ATTENUATION

@0.1 TO 80 MHz

38dB MIN

@80 TO 125 MHz

30dB MIN

@125 TO 250 MHz

10dB MIN

HIPOT

1500Vrms

OPERATING TEMPERATURE -40°C TO +85°C

REV. : C

PAGE : 2

ORIGINATED BY		DATE	TITLE 10/100BASE-T MODULE S558-5999-W2-F	PART NO. / DRAWING NO.	STANDARD DIM.		[] METRIC DIM. AS REF.	
Alice Pang		2015-01-26		X5585999W2-F	TOL. IN INCH		UNIT : INCH [mm]	
DRAWN BY		DATE		FILE NAME X5585999W2FC.DWG	.X		SCALE : N/A	
ZC Guo		2015-01-26			.XX		SIZE : A4	
			.XXX					



POWER | PROTECT | CONNECT

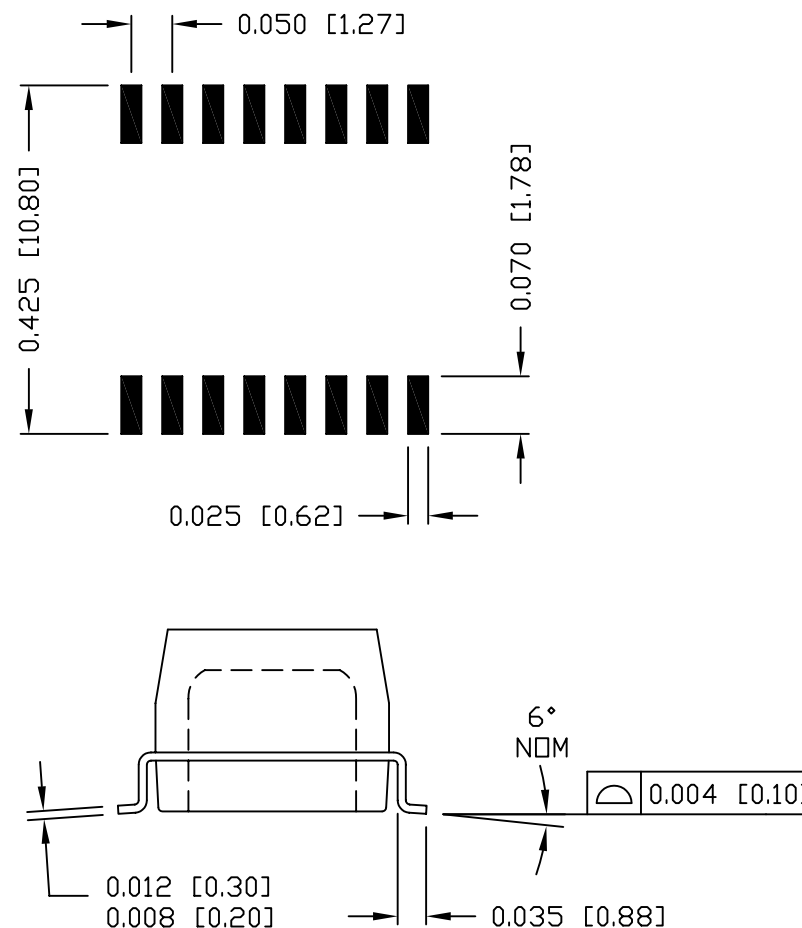
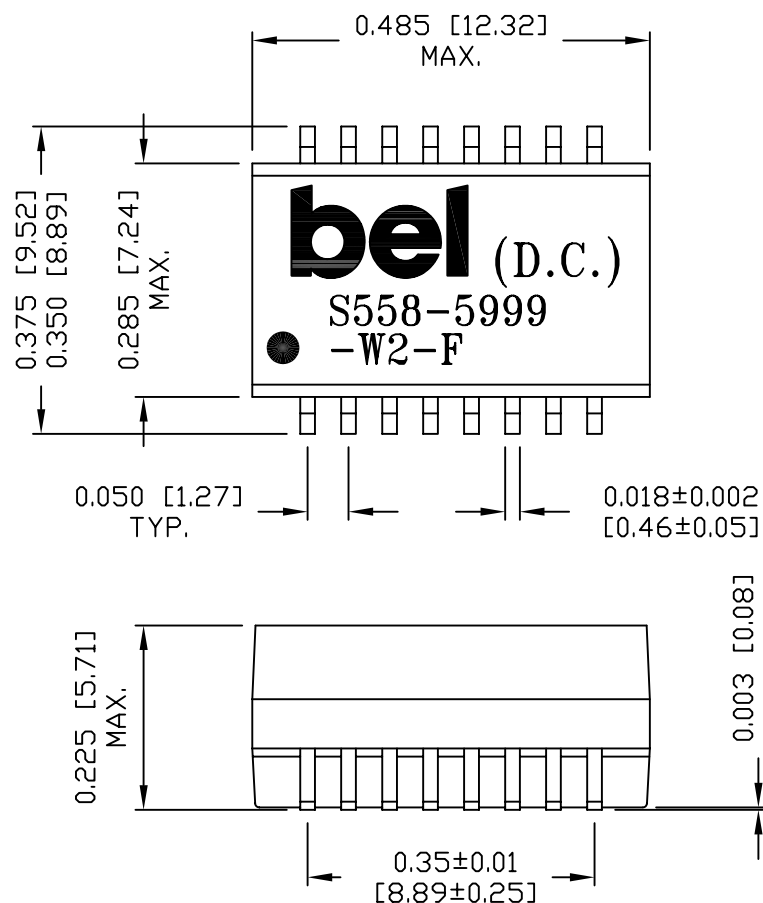


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RoHS



SUGGESTED PCB PAD LAYOUT



NOTES:

1. STANDARD MARKING REFER TO DDC. HAND-WORK-04.
2. PACKAGE CODE: "QBS001".

REV. : C PAGE : 3

ORIGINATED BY	DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM.	[] METRIC DIM. AS REF.
Lawrence Tsang	2015-01-26	MECHANICAL DRAWING S558-5999-W2-F	X5585999W2-F	TOL. IN INCH	UNIT : INCH [mm]
DRAWN BY	DATE		FILE NAME	.X	SCALE : N/A
ZC Guo	2015-01-26		X5585999W2FC.DWG	.XX ±0.01	SIZE : A4
				.XXX ±0.005	

