- **Low Input Bias Current . . . 50 pA Typ**
- **Low Input Noise Current**
  0.01 pA/$\sqrt{\text{Hz}}$ Typ
- **Low Supply Current . . . 4.5 mA Typ**
- **High Input impedance . . . 10^{12} Ω Typ**
- **Internally Trimmed Offset Voltage**
- **Wide Gain Bandwidth . . . 3 MHz Typ**
- **High Slew Rate . . . 13 V/μs Typ**

D OR P PACKAGE
(TOP VIEW)

|			
1OUT	1	8	V_{CC+}
1IN −	2	7	2OUT
1IN+	3	6	2IN −
$V_{CC−}$	4	5	2IN+
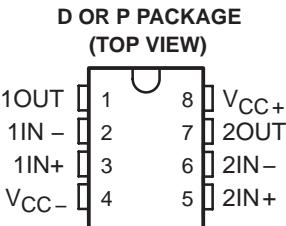
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a specified maximum input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF412C can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF412C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)

IN −

IN +

OUT
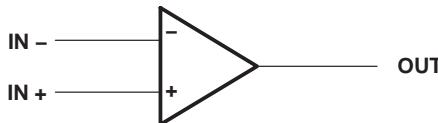
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	3 mV	LF412CD	LF412CP

The D packages are available taped and reeled. Add the suffix R to the device type (ie., LF412CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} . . . . 18 V
Supply voltage, $V_{CC−}$ . . . . −18 V
Differential input voltage, V_{ID} . . . . ±30 V
Input voltage, V_I (see Note 1) . . . . ±15 V
Duration of output short circuit . . . . unlimited
Continuous total power dissipation . . . . 500 mW
Operating temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

NOTE 1:   Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

TEXAS INSTRUMENTS

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC\pm}=\pm15$ V (unless otherwise specified)

	PARAMETER	TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC}=0$, $R_S=10$ kΩ	25°C		1	3	mV
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC}=0$, $R_S=10$ kΩ			10	20‡	µV/°C
I_{IO}	Input offset current§	$V_{IC}=0$	25°C		25	100	pA
			70°C			4	nA
I_{IB}	Input bias current§	$V_{IC}=0$	25°C		50	200	pA
			70°C			8	nA
V_{ICR}	Common-mode input voltage range			±11	−11.5 to 14.5		V
V_{OM}	Maximum peak output voltage swing	$R_L=10$ kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O=\pm10$ V, $R_L=2$ kΩ	25°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	$T_A=25$°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		70	100		dB
k_{SVR}	Supply-voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				4.5	6.8	mA

† Full range is 0°C to 70°C.
‡ At least 90% of the devices meet this limit for α_{VIO}.
§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
NOTE 2: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25$°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/µs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 20\,\Omega$		18		nV/$\sqrt{Hz}$
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/$\sqrt{Hz}$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF412 MWC	Active	Production	WAFERSALE (YS) | 0	1 | NOT REQUIRED	-	Call TI	Level-1-NA-UNLIM	-40 to 85	
LF412CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	LF412C
LF412CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF412C
LF412CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF412C
LF412CDR1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF412C
LF412CDR1G4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF412C
LF412CDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
LF412CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
LF412CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF412CP
LF412CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF412CP

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS
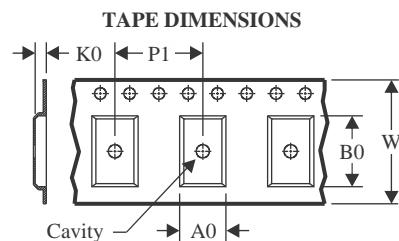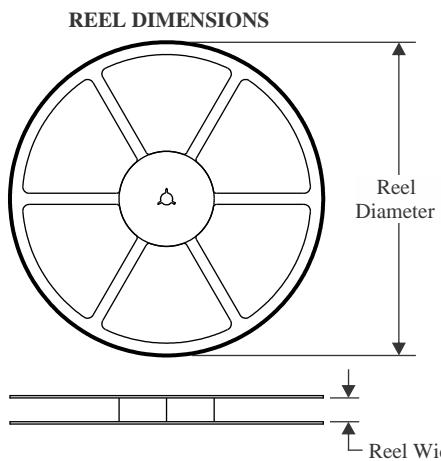
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
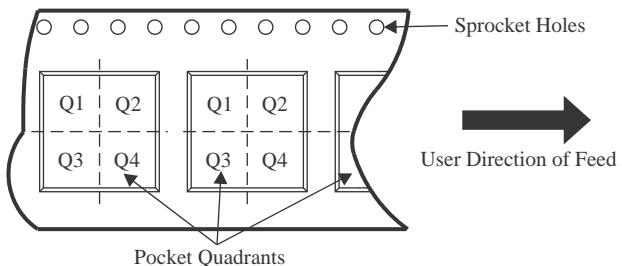
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF412CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LF412CDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
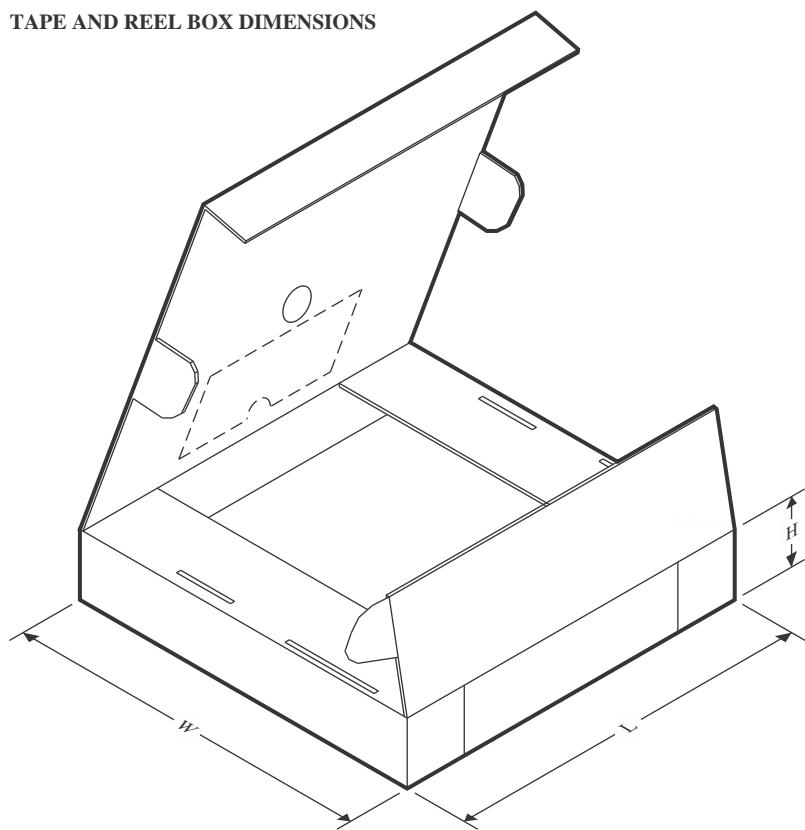
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF412CDR	SOIC	D	8	2500	353.0	353.0	32.0
LF412CDR1G4	SOIC	D	8	2500	353.0	353.0	32.0

TUBE
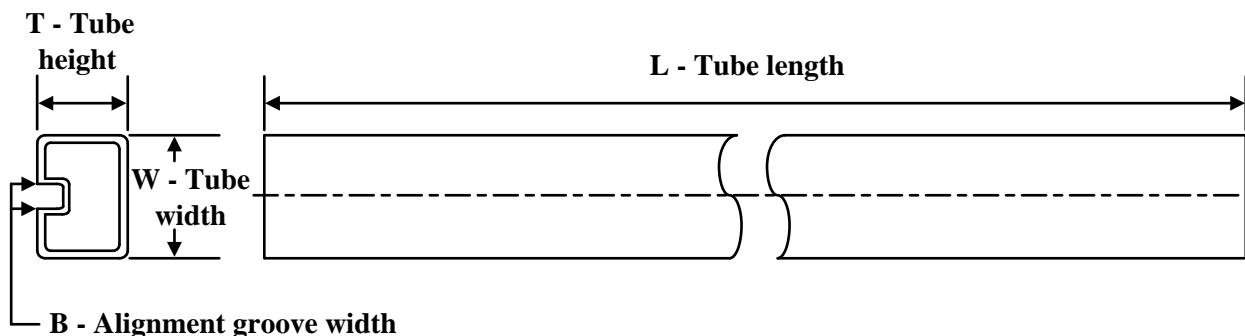
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LF412CP	P	PDIP	8	50	506	13.97	11230	4.32
LF412CP.A	P	PDIP	8	50	506	13.97	11230	4.32

.228-.244 TYP
[5.80-6.19]

PIN 1 ID AREA

6X .050
[1.27]

2X
.150
[3.81]

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25] Ⓜ C A B

.189-.197
[4.81-5.00]
NOTE 3

.150-.157
[3.81-3.98]
NOTE 4

C

SEATING PLANE

⌒ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010 TYP
[0.13-0.25]

.010
[0.25]

0° - 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL
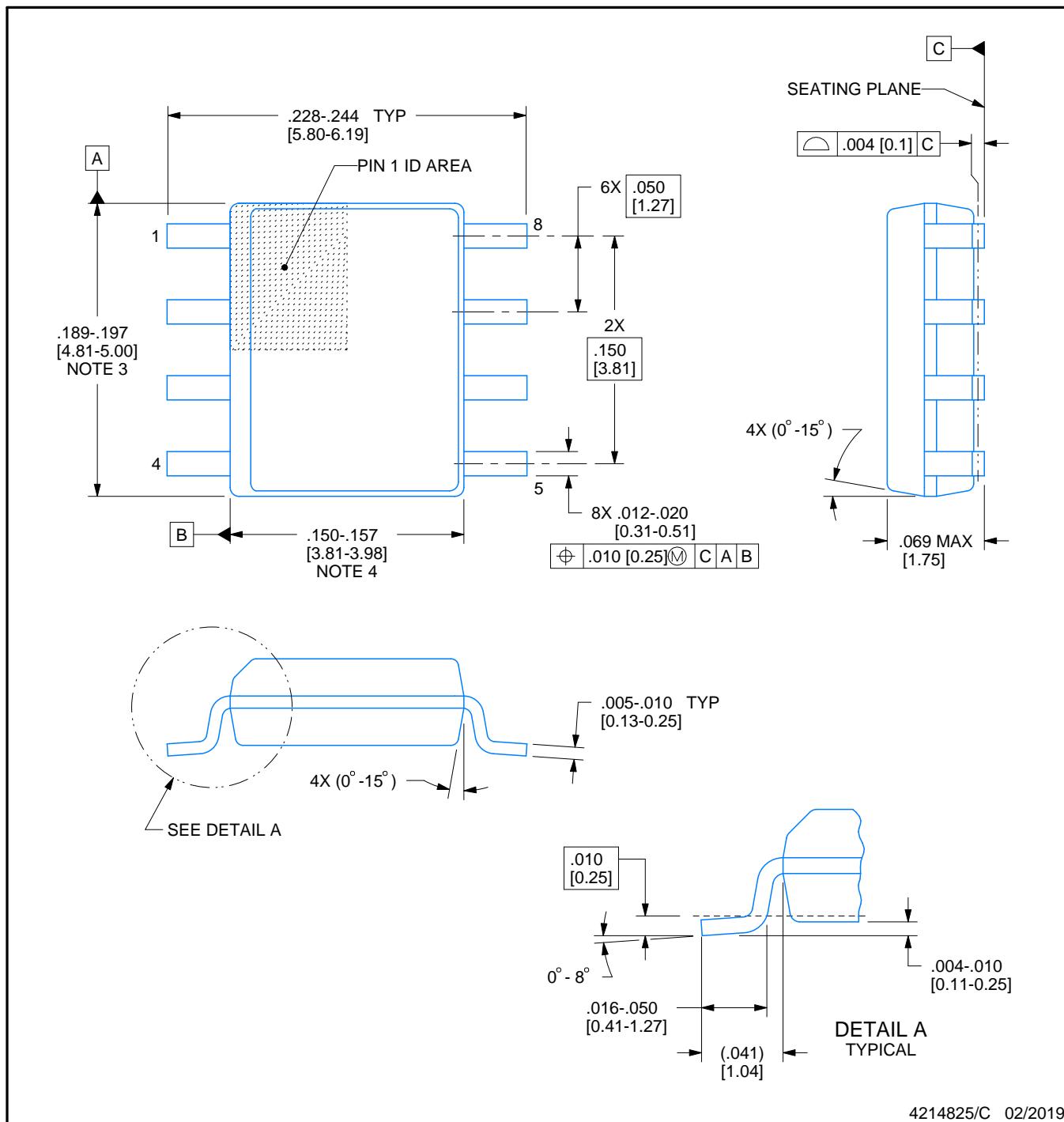
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

SYMM
₵

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM
₵

(R.002) TYP
[0.05]

4

5

6X (.050)
[1.27]

(.213)
[5.4]
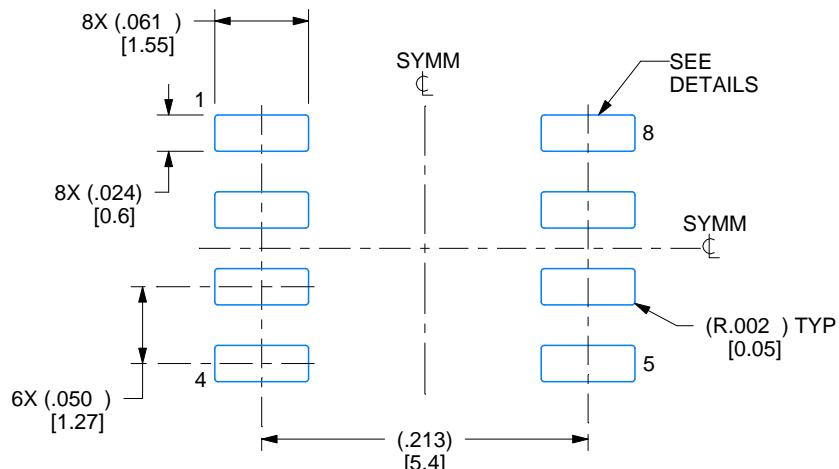
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
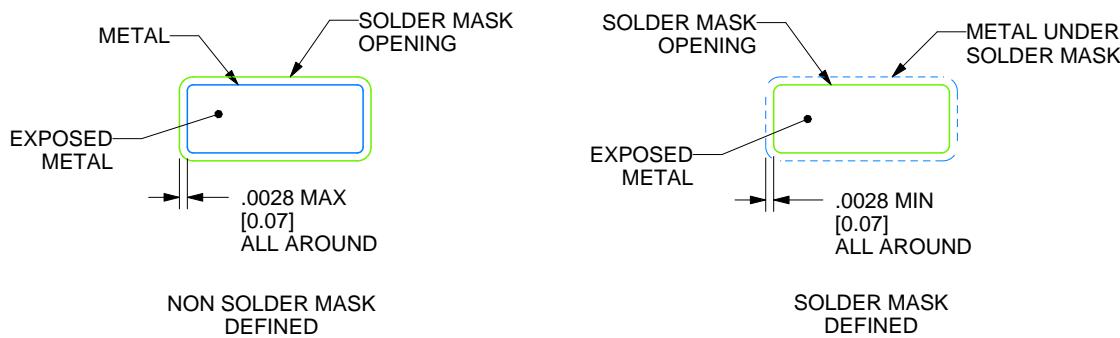
SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
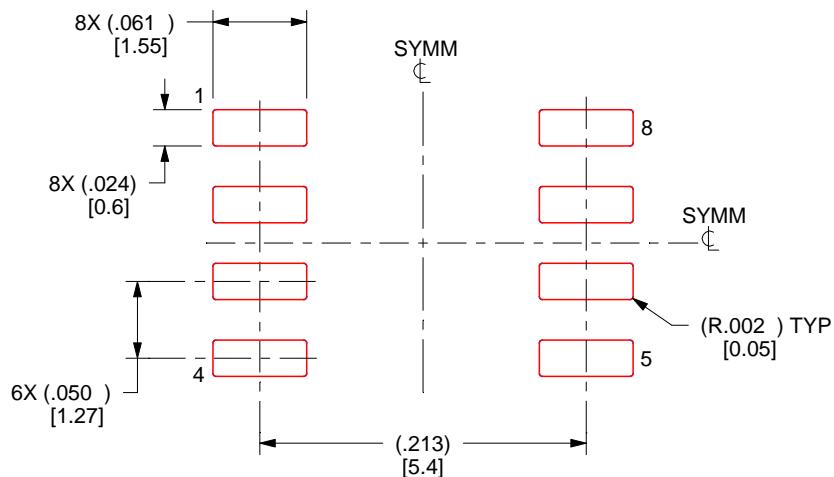
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

8X (.061)
[1.55]

8X (.024)
[0.6]

6X (.050)
[1.27]

(R.002) TYP
[0.05]

(.213)
[5.4]

SYMM

SYMM

1

4

8

5

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R−PDIP−T8)   PLASTIC DUAL−IN−LINE PACKAGE

0.400 (10,16)
0.355 (9,02)

8   5

0.260 (6,60)
0.240 (6,10)

1   4

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92)
MAX
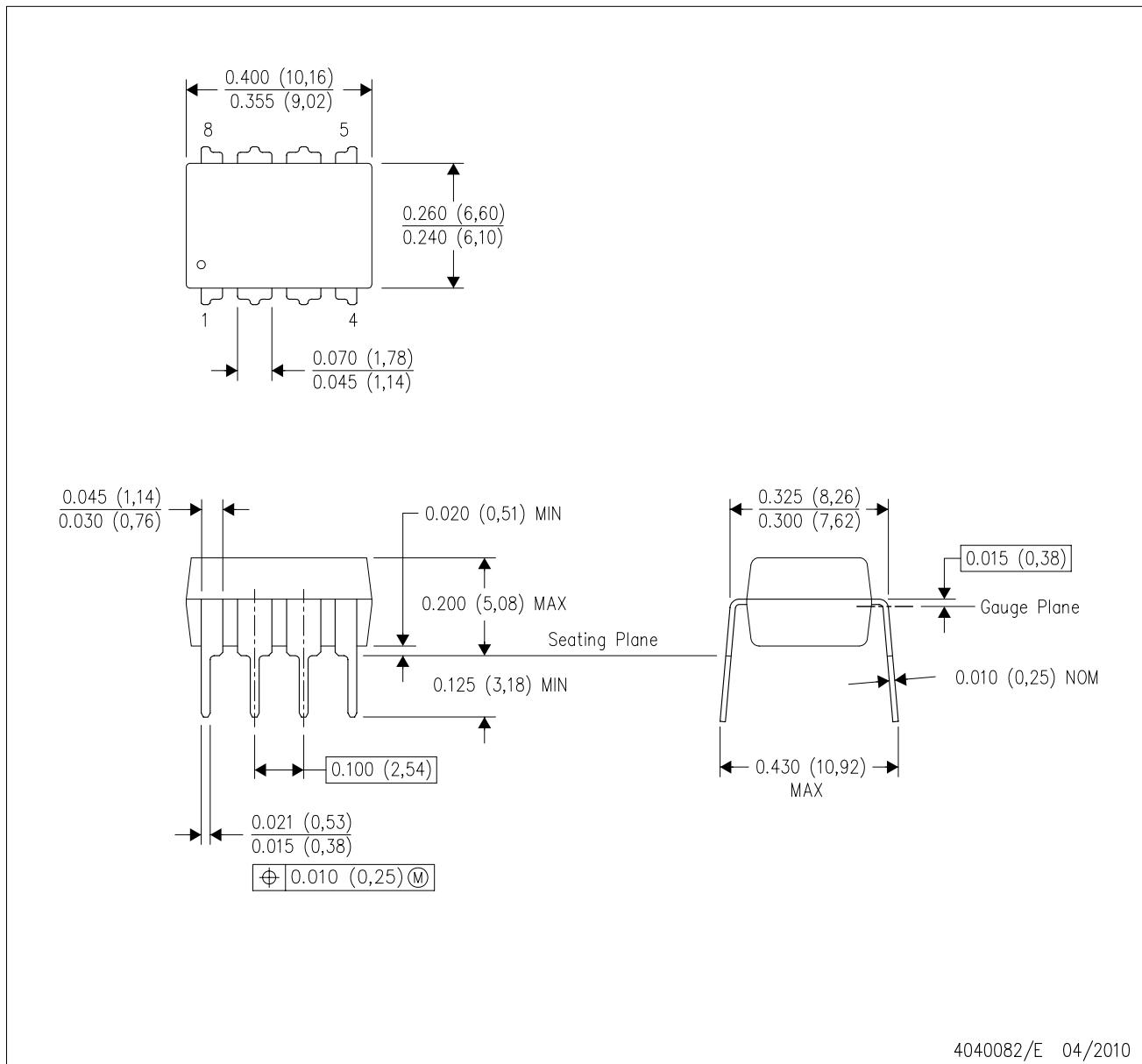
4040082/E   04/2010

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001 variation BA.

TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE AND DISCLAIMER