

# HD49334ANP/AHNP

## CDS/PGA & 10-bit A/D Converter

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Rev.2.00

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### Description

The HD49334ANP/AHNP is a CMOS IC that provides CDS-PGA analog processing (CDS/PGA) suitable for CCD camera digital signal processing systems together with a 10-bit A/D converter in a single chip.

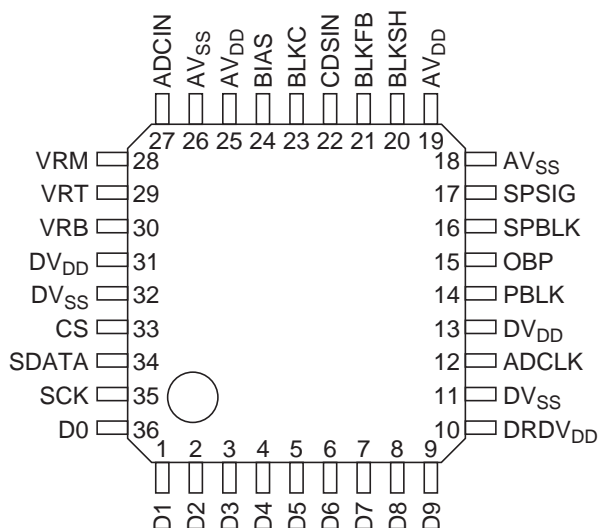
### Functions

- Correlated double sampling
- PGA
- Offset compensation
- Serial interface control
- 10-bit ADC
- Operates using only the 3 V voltage
- Corresponds to switching mode of power dissipation and operating frequency  
Power dissipation: 120 mW (Typ), maximum frequency: 36 MHz (HD49334AHNP)  
Power dissipation: 60 mW (Typ), maximum frequency: 25 MHz (HD49334ANP)
- ADC direct input mode
- QFN 36-pin package

### Features

- Suppresses low-frequency noise output from CCD by the S/H type correlated double sampling.
- The S/H response frequency characteristics for the reference level can be adjusted using values of external parts and registers.
- High sensitivity is achieved due to the high S/N ratio and a wide coverage provided by a PG amplifier.
- Feedback is used to compensate and reduce the DC offsets including the output DC offset due to PGA gain change and the CCD offset in the CDS (correlated double sampling) amplifier input.
- PGA, standby mode, etc., is achieved via a serial interface.
- High precision is provided by a 10-bit-resolution A/D converter.

## Pin Arrangement



(Top view)

## Pin Description

Pin No.	Symbol	Description	I/O	Analog(A) or Digital(D)
1 to 9	D0 to D9	Digital output	O	D
10	DRDV <sub>DD</sub>	Output buffer power supply (3 V)	—	D
11	DV <sub>SS</sub>	Digital ground (0 V)	—	D
12	ADCLK	ADC conversion clock input pin	I	D
13	DV <sub>DD</sub>	Digital power supply (3 V)	—	D
14	PBLK	Preblanking input pin	I	D
15	OBP	Optical black pulse input pin	I	D
16	SPBLK	Black level sampling clock input pin	I	D
17	SPSIG	Signal level sampling clock input pin	I	D
18	AV <sub>SS</sub>	Analog ground (0 V)	—	A
19	AV <sub>DD</sub>	Analog power supply (3 V)	—	A
20	BLKSH	Black level S/H pin	—	A
21	BLKFB	Black level FB pin	—	A
22	CDSIN	CDS input pin	I	A
23	BLKC	Black level C pin	—	A
24	BIAS	Internal bias pin Connect a 33 kΩ resistor between BIAS and AV <sub>SS</sub> .	—	A
25	AV <sub>DD</sub>	Analog power supply (3 V)	—	A
26	AV <sub>SS</sub>	Analog ground (0 V)	—	A
27	ADCIN	ADC input pin	—	A
28	VRM	Reference voltage pin 1 Connect a 0.1 μF ceramic capacitor between VRM and AV <sub>SS</sub> .	—	A
29	VRT	Reference voltage pin 3 Connect a 0.1 μF ceramic capacitor between VRT and AV <sub>SS</sub> .	—	A
30	VRB	Reference voltage pin 2 Connect a 0.1 μF ceramic capacitor between VRB and AV <sub>SS</sub> .	—	A

**Pin Description (cont.)**

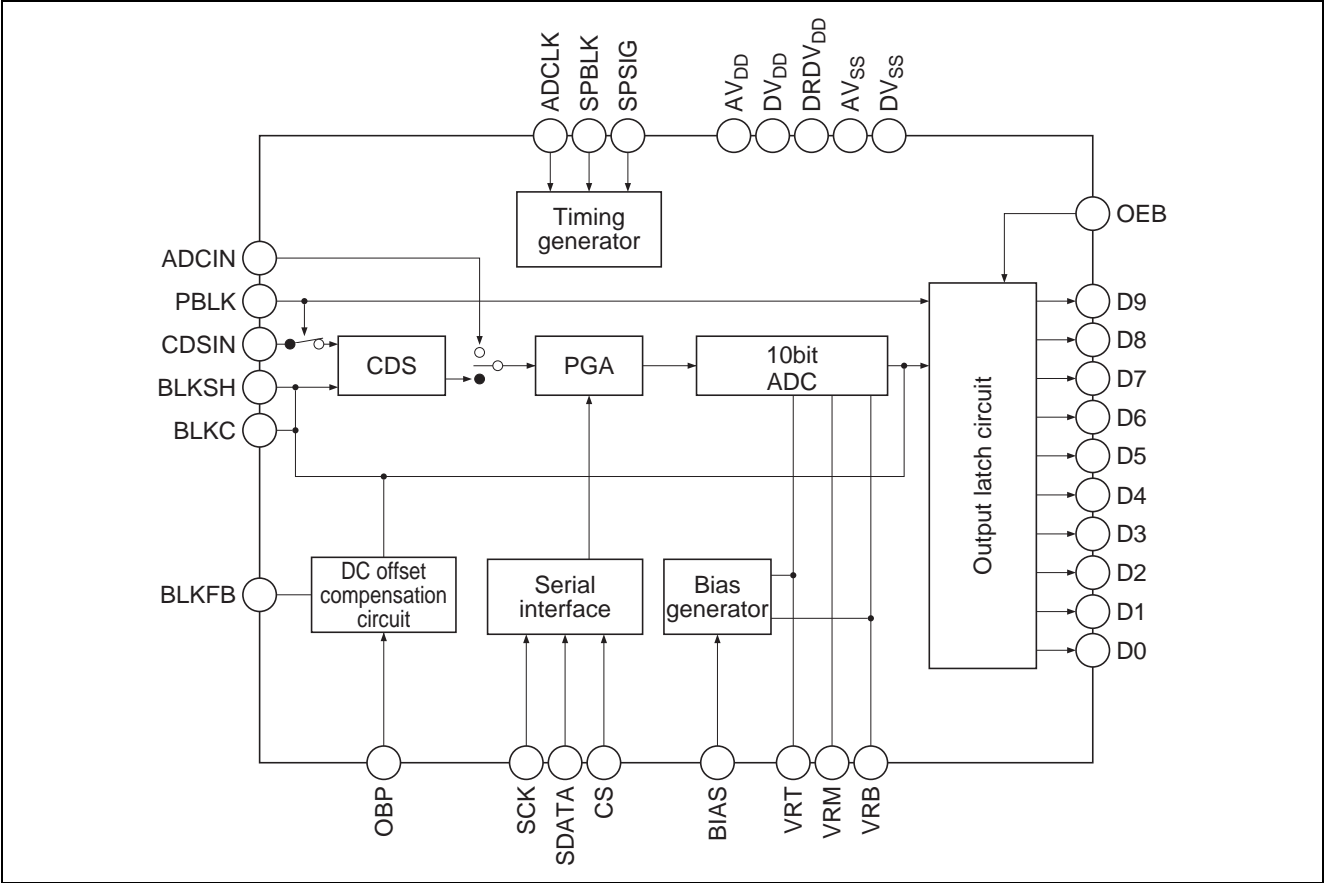
Pin No.	Symbol	Description	I/O	Analog(A) or Digital(D)
31	DV <sub>DD</sub>	Digital power supply (3 V)	—	D
32	DV <sub>SS</sub>	Digital ground (0 V)	—	D
33	CS	Serial interface control input pin	I	D
34	SDATA	Serial data input pin	I	D
35	SCK	Serial clock input pin	I	D
36	D0	Digital output	O	D

Note: 1. With pull-down resistor.

**Input/Output Equivalent Circuit**

Pin Name	Equivalent Circuit
Digital output D0 to D9	
Digital input ADCLK, OBP, SPBLK, SPSIG, CS, SCK, SDATA, PBLK	
Analog CDSIN	
ADCIN	
BLKSH, BLKFB, BLKC	
VRT, VRM, VRB	
BIAS	

Block Diagram





## 2. PGA Circuit

The PGAMP is the programmable gain amplifier for the latter stage. The PGAMP and the CDSAMP set the gain using 8 bits of register.

The equation below shows how the gain changes when register value N is from 0 to 255.

In CDSIN mode:  $\text{Gain} = (-2.36 \text{ dB} + 0.132 \text{ dB}) \times N$  (LOG linear).

In ADCIN mode:  $\text{Gain} = (0.57 \text{ times} + 0.00446 \text{ times}) \times N$  (linear).

Full-scale digital output is defined as 0 dB (one time) when 1 V is input.

## 3. Automatic Offset Calibration Function and Black-Level Clamp Data Setting

The DAC DC voltage added to the output of the PGAMP is adjusted by automatic offset calibration.

The data, which cancels the output offset of the PGAMP and the input offset of the ADC, and the clamp data (14 LSB to 76 LSB) set by register are added and input to the DAC.

The automatic offset calibration starts automatically after the RESET mode set by register 1 is cancelled and terminates after 40000 clock cycles (when fclk = 20 MHz, 2 ms).

## 4. DC Offset Compensation Feedback Function

Feedback is done to set the black signal level input during the OB period to the DC standard, and all offsets (including the CCD offset and the CDSAMP offset) are compensated for.

The offset from the ADC output is calculated during the OB period, and SHAMP feedback capacitor C3 is charged by the current DAC (see figure 1).

The open-loop differential gain ( $\Delta\text{Gain}/\Delta H$ ) per 1 H of the feedback loop is given by the following equation. 1H is the one cycle of the OBP.

$$\Delta\text{Gain}/\Delta H = 0.078 / (\text{fclk} \times C3) \quad (\text{fclk: ADCLK frequency, } C3: \text{SHAMP external feedback capacitor})$$

Example: When fclk = 20 MHz and C3 = 1.0  $\mu\text{F}$ ,  $\Delta\text{Gain}/\Delta H = 0.0039$

When the PGAMP gain setting is changed, the high-speed lead-in operation state is entered, and the feedback loop gain is increased by a multiple of N. Loop gain multiplication factor N can be selected from 4 times, 8 times, 16 times, or 32 times by changing the register settings (see table 1). Note that the open-loop differential gain ( $\Delta\text{Gain}/\Delta H$ ) must be one or lower. If it is two or more, oscillation occurs.

The time from the termination of high-speed lead-in operation to the return of normal loop gain operation can be selected from 1 H, 2 H, 4 H, or 8 H. If the offset error is over 32 LSB, the high-speed lead-in operation continues, and when the offset error is 32 LSB or less, the operation returns to the normal loop-gain operation after 1 H, 2 H, 4 H, or 8 H depending on the register settings. See table 2.

**Table 1 Loop Gain Multiplication Factor during High-Speed Lead-In Operation**

HGain-Nsel (register settings)		Multiplication Factor N
[0]	[1]	
L	L	4
H	L	8
L	H	16
H	H	32

**Table 2 High-Speed Lead-In Operation Cancellation Time**

HGstop-Hsel (register settings)		Cancellation Time
[0]	[1]	
L	L	1 H
H	L	2 H
L	H	4 H
H	H	8 H

## 5. Pre-Blanking Function

During the PBLK input period, the CDS input operation is separated and protected from the large input signal. The ADC digital output is fixed to clamp data (14 to 76 LSB).

# 6. ADC Digital Output Control Function

The ADC digital output includes the functions output enable, code conversion, and test mode. Tables 3, 4 and 5 show the output functions and the codes.

**Table 3 ADC Digital Output Functions**

STBY	TEST0	TEST1	LINV	MINV	PBLK	ADC Digital Output										Operating Mode	
							D9	D8	D7	D6	D5	D4	D3	D2	D1		D0
H	X	X	X	X	X	Hi-Z										Low-power wait state	
L	L	L	L	L	H	Same as in table 4.										Normal operation	
			L	H	H	D9 is inverted in table 4.											
			H	L	H	D8 to D0 are inverted in table 4.											
			H	H	H	D9 to D0 are inverted in table 4.											
			X	X	L	Output code is set up to Clamp Level.										Pre-blanking	
		H	L	L	H	Same as in table 5.										Normal operation	
			L	H	H	D9 is inverted in table 5.											
			H	L	H	D8 to D0 are inverted in table 5.											
			H	H	H	D9 to D0 are inverted in table 5.											
			X	X	L	Output code is set up to Clamp Level.										Pre-blanking	
	H	X	L	L	X		H	L	H	L	H	L	H	L	H	L	Test mode
			L	H	X		L	L	H	L	H	L	H	L	H	L	
			H	L	X		H	H	L	H	L	H	L	H	L	H	
			H	H	X		L	H	L	H	L	H	L	H	L	H	

Notes: 1. STBY, TEST, LINV, and MINV are set by register.  
2. Mode setting for the PBLK is done by external input pins.  
3. The polarity of the PBLK pin when the register setting is SPInv is low.

**Table 4 ADC Output Code**

Output Pin			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Output codes	Steps	3	L	L	L	L	L	L	L	L	H	H
		4	L	L	L	L	L	L	L	L	L	L
		5	L	L	L	L	L	L	L	H	L	H
		6	L	L	L	L	L	L	L	H	H	L
		...	...	...	...	...	...	...	...	...	...	...
		511	L	H	H	H	H	H	H	H	H	H
		512	H	L	L	L	L	L	L	L	L	L
		...	...	...	...	...	...	...	...	...	...	...
		1020	H	H	H	H	H	H	H	H	L	L
		1021	H	H	H	H	H	H	H	H	L	H
		1022	H	H	H	H	H	H	H	H	H	L
		1023	H	H	H	H	H	H	H	H	H	H

**Table 5 ADC Output Code (TEST1)**

Output Pin			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Output codes	Steps	3	L	L	L	L	L	L	L	L	H	L
		4	L	L	L	L	L	L	L	L	H	L
		5	L	L	L	L	L	L	L	H	H	H
		6	L	L	L	L	L	L	L	H	L	H
		...	...	...	...	...	...	...	...	...	...	...
		511	L	H	L	L	L	L	L	L	L	L
		512	H	H	L	L	L	L	L	L	L	L
		...	...	...	...	...	...	...	...	...	...	...
		1020	H	L	L	L	L	L	L	L	H	L
		1021	H	L	L	L	L	L	L	L	H	H
		1022	H	L	L	L	L	L	L	L	L	H
		1023	H	L	L	L	L	L	L	L	L	L

7. Adjustment of Black-Level S/H Response Frequency Characteristics

The CR time constant that is used for sampling/hold (S/H) at the black level can be adjusted by changing the register settings, as shown in table 6.

**Table 6 SHSW CR Time Constant Setting**

	SHSW-fsel (Register setting)																															
	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]
	L	L	L	L	H	L	L	L	L	H	L	L	H	H	L	L	L	L	H	L	H	L	H	L	H	L	L	H	H	L	H	H
CR Time Constant (Typ) (cutoff frequency conversion)	2.20 nsec (72 MHz)				2.30 nsec (69 MHz)				2.51 nsec (63 MHz)				2.64 nsec (60 MHz)				2.93 nsec (54 MHz)				3.11 nsec (51 MHz)				3.52 nsec (45 MHz)				3.77 nsec (42 MHz)			
	SHSW-fsel (Register setting)																															
	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]
	L	L	L	H	H	L	L	H	L	H	L	H	H	H	L	H	L	L	H	H	H	L	H	H	L	H	H	H	L	H	H	H
CR Time Constant (Typ) (cutoff frequency conversion)	4.40 nsec (36 MHz)				4.80 nsec (33 MHz)				5.87 nsec (27 MHz)				6.60 nsec (24 MHz)				8.80 nsec (18 MHz)				10.6 nsec (15 MHz)				17.6 nsec (9 MHz)				26.4 nsec (6 MHz)			

8. The SHAMP frequency characteristics can be adjusted by changing the register settings and the C4 value of the external 23rd pin.

The settings are shown in table 7.

Values other than those shown in the table 7 cannot be used.

BLKC

②3

⊥ C4  
⏏

**Table 7 SHAMP Frequency Characteristics Setting**

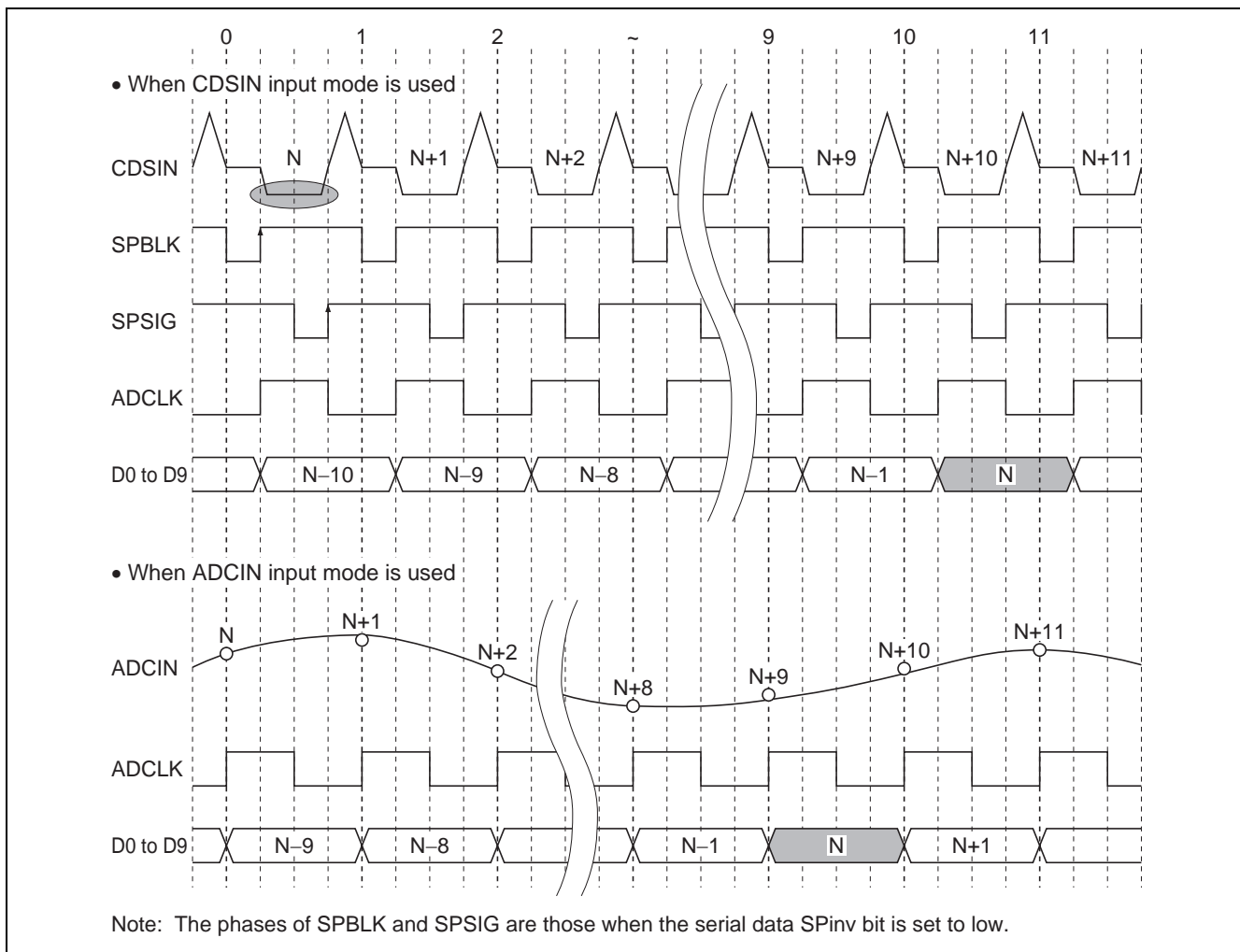
LoPwr (Register setting)	SHA-fsel (Register setting)					
	[0]	[1]	[0]	[1]	[0]	[1]
	H	L	L	H	H	H
"Lo"	116 MHz 10000 pF (270 pF)		75 MHz 13000 pF (300 pF)		56 MHz 18000 pF (360 pF)	
"Hi"	49 MHz 15000 pF (620 pF)		32 MHz 22000 pF (750 pF)		24 MHz 27000 pF (820 pF)	

Note: Upper line : SHAMP cutoff frequency (Typ)  
Middle line : Standard value of C4 (maximum value is not defined)  
Lower line : Minimum value of C4 (do not set below this value)



## Timing Chart

Figure 2 shows the timing chart when CDSIN and ADCIN input modes are used.



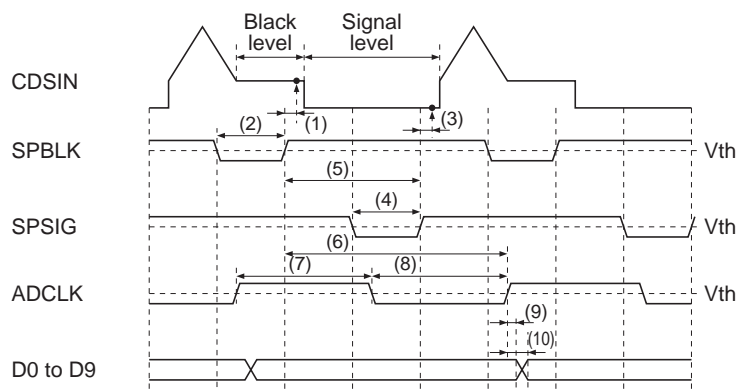
**Figure 2 Output Timing Chart when CDSIN and ADCIN Input Modes are Used**

- The ADC output (D0 to D9) is output at the rising edge of the ADCLK in both modes.
- Pipe-line delay is ten clock cycles when CDSIN is used and nine when ADCIN is used.
- In ADCIN input mode, the input signal is sampled at the rising edge of the ADCLK.

## Detailed Timing Specifications

### Detailed Timing Specifications when CDSIN Input Mode is Used

Figure 3 shows the detailed timing specifications when the CDSIN input mode is used, and table 8 shows each timing specification.



Note: 1. When serial data Spinv bit is set to low. (When the Spinv bit is set to high, the polarities of the SPBLK and the SPSIG are inverted.)

**Figure 3 Detailed Timing Chart when CDSIN Input Mode is Used**

**Table 8 Timing Specifications when the CDSIN Input Mode is Used**

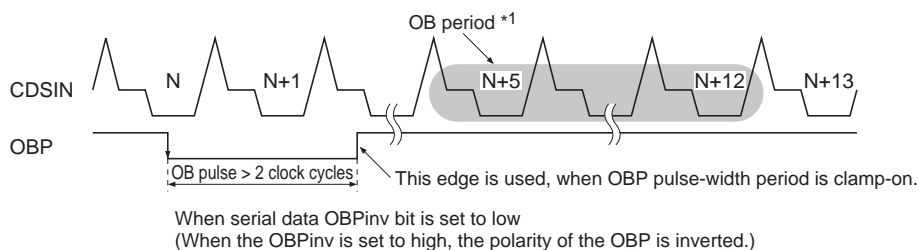
No.	Timing	Symbol	Min	Typ	Max	Unit
(1)	Black-level signal fetch time	$t_{CDS1}$	—	(1.5)	—	ns
(2)	SPBLK low period <sup>*1</sup>	$t_{CDS2}$	$Typ \times 0.8$	$1/4f_{CLK}$	$Typ \times 1.2$	ns
(3)	Signal-level fetch time	$t_{CDS3}$	—	(1.5)	—	ns
(4)	SPSIG low period <sup>*1</sup>	$t_{CDS4}$	$Typ \times 0.8$	$1/4f_{CLK}$	$Typ \times 1.2$	ns
(5)	SPBLK rising to SPSIG rising time <sup>*1</sup>	$t_{CDS5}$	$Typ \times 0.85$	$1/2f_{CLK}$	$Typ \times 1.15$	ns
(6)	SPBLK rising to ADCLK rising inhibition time <sup>*1</sup>	$t_{CDS6}$	1	5	11	ns
(7), (8)	ADCLK $t_{WH} min./t_{WL} min.$	$t_{CDS7, 8}$	11	—	—	ns
(9)	ADCLK rising to digital output hold time	$t_{CHLD9}$	3	7	—	ns
(10)	ADCLK rising to digital output delay time	$t_{COD10}$	—	16	24	ns

Note: 1. SPBLK and SPSIG polarities when serial data Spinv bit is set to low.

### OBP Detailed Timing Specifications

Figure 4 shows the OBP detailed timing specifications.

The OB period is from the fifth to the twelfth clock cycle after the OB pulse is input. The average of the black signal level is taken for eight input cycles during the OB period and becomes the clamp level (DC standard).



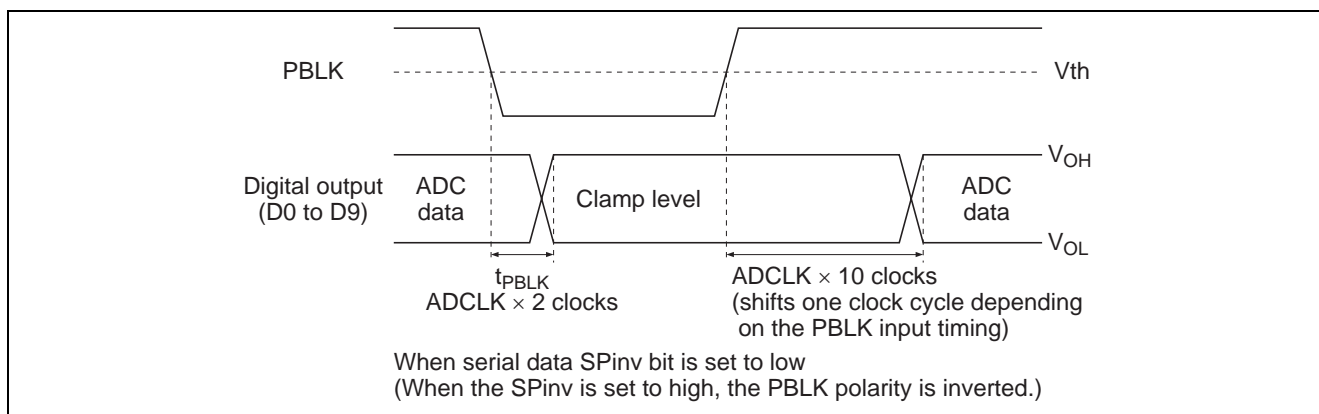
When serial data OBPinv bit is set to low  
(When the OBPinv is set to high, the polarity of the OBP is inverted.)

Note: 1. Shifts  $\pm 1$  clock cycle depending on the OBP input timing.

**Figure 4 OBP Detailed Timing Specifications**

### Detailed Timing Specifications at Pre-Blanking

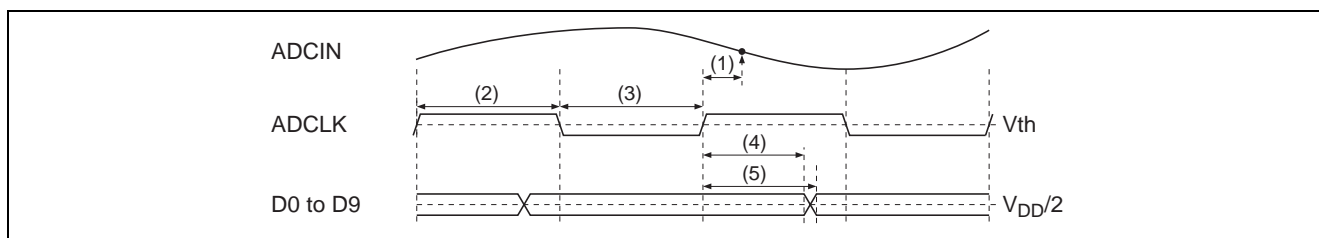
Figure 5 shows the pre-blanking detailed timing specifications.



**Figure 5 Detailed Timing Specifications at Pre-Blanking**

### Detailed Timing Specifications when ADCIN Input Mode is Used

Figure 6 shows the detailed timing chart when ADCIN input mode is used, and table 9 shows each timing specification.



**Figure 6 Detailed Timing Chart when ADCIN Input Mode is Used**

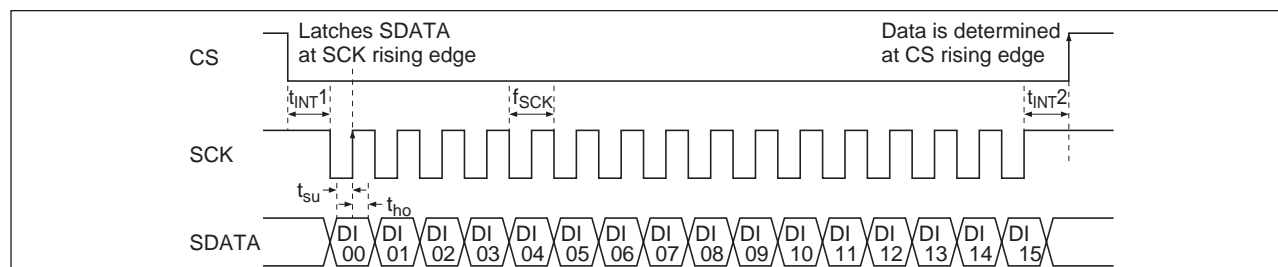
**Table 9 Timing Specifications when ADCIN Input Mode is Used**

No.	Timing	Symbol	Min	Typ	Max	Unit
(1)	Signal fetch time	$t_{ADC1}$	—	(6)	—	ns
(2), (3)	ADCLK $t_{WH}$ min./ $t_{WL}$ min.	$t_{ADC2,3}$	$Typ \times 0.85$	$1/2f_{ADCLK}$	$Typ \times 1.15$	ns
(4)	ADCLK rising to digital output hold time	$t_{AHLd4}$	10	14.5	—	ns
(5)	ADCLK rising to digital output delay time	$t_{AOD5}$	—	23.5	31.5	ns

## Serial Interface Specifications

**Table 10 Serial Data Function List**

	Resister 0	Resister 1	Resister 2	Resister 3	Resister 4 to 7 *7 Test Mode (can not be used)
DI 00 (LSB)	Low	High	Low	High	Low to High
DI 01	Low	Low	High	High	Low to High
DI 02	Low	Low	Low	Low	High
DI 03	Cannot be used. All low	SLP Low: Normal operation mode High: Sleep mode	Clamp-level [0] (LSB)	C-Bias off	Cannot be used.
DI 04		STBY Low: Normal operation mode High: Standby mode	Clamp-level [1]	Output mode setting (TEST1)	
DI 05	PGA gain setting (LSB)	Output mode setting (LINV)	Clamp-level [2]	Cannot be used. All low	
DI 06	PGA gain setting	Output mode setting (MINV)	Clamp-level [3]		
DI 07	PGA gain setting	Output mode setting (TEST0)	Clamp-level [4] (MSB)	0	
DI 08	PGA gain setting	SHA-fsel [0] (LSB)	HGstop-Hsel [0]	0	
DI 09	PGA gain setting	SHA-fsel [1] (MSB)	HGstop-Hsel [1]	0	
DI 10	PGA gain setting	SHSW-fsel [0] (LSB)	HGain-Nsel [0]	0	
DI 11	PGA gain setting	SHSW-fsel [1]	HGain-Nsel [1]	0	
DI 12	PGA gain setting (MSB)	SHSW-fsel [2]	Low_PWR	1	
DI 13	Cannot be used. All low	SHSW-fsel [3] (MSB)	SPInv, SPSIG/SPBLK/PBLK inversion	0	
DI 14		Cannot be used. All low	OBPInv, OBP inversion	0	
DI 15 (MSB)	CSEL Low: CDSIN input mode High: CIN input mode		RESET Low: Reset mode High: Normal operation mode	1	


**Figure 7 Serial Interface Timing Specifications**

- Notes:
1. 2 byte continuous communications.
  2. SDATA is latched at SCK rising edge.
  3. Insert 16 clocks of SCK while CS is low.
  4. Data is invalid if data transmission is aborted during transmission.
  5. The gain conversion table differs in the CDSIN input mode and the ADCIN input mode.
  6. STBY: Reference voltage generator circuit is in the operating state.  
SLP: All circuits are in the sleep state.
  7. This bit is used for the IC testing, and cannot be used by the user.  
The use of this address is prohibited.
  8. Circuit current and the frequency characteristic are switched.  
Data = 0: 36 MHz guarantee  
Data = 1: 25 MHz guarantee

**Timing Specifications**

	Min	Max
$f_{SCK}$	—	5 MHz
$t_{INT1, 2}$	50 ns	—
$t_{SU}$	50 ns	—
$t_{HO}$	50 ns	—

## Explanation of Serial Data of CDS Part

Serial data of CDS part has the following functions.

- PGA gain (D5 to D12 of register 0)

Details are referred to page 5 block diagram.

At CDS\_in mode:  $-2.36 \text{ dB} + 0.132 \text{ dB} \times N$  (Log linear)

At ADC\_in mode:  $0.57 \text{ times} + 0.01784 \text{ times} \times N$  (Times linear)

\*: Full-scale digital output is defined as 0 dB when 1 V is input.

Above PGA gain definition means input signal 1 Vp-p to CDS\_in, and set  $N = 18$  (correspond 2.36 dB), and then PGA outputs the 2 V full-range, and also ADC out puts the full code (1023).

This mean offset gain of PGA has  $6 \text{ dB} - 2.36 \text{ dB} = 3.64 \text{ dB}$ , therefore it should be decided that how much dB add on.

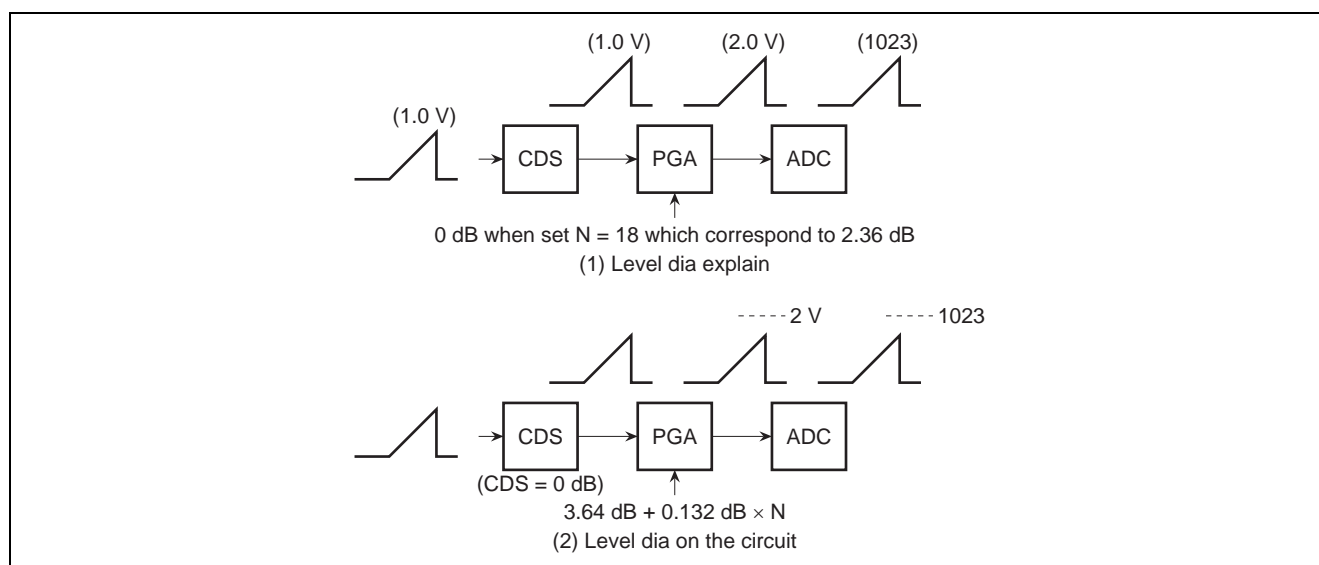


Figure 8 Level Dia of PGA

- CSEL (D15 of register 0)

Data = 0: Select CDSIN

Data = 1: Select ADCIN

Address								STD1[7:0] (L)							STD2[15:8] (H)								
1	1	1	1	0	0	0	1				D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
											test0	MINV	LINV	STBY	SLP	test_l2		SHSW_fsel			SHA_fsel		

- SLP and STBY (D3, D4 of register 1)

SLP: Stop the all circuit. Consumption current of CDS part is less than 10  $\mu\text{A}$ .

Start up from offset calibration when recover is needed.

STBY: Only the standard voltage generating circuit is operated. Consumption current of CDS part is about 3 mA.

Allow 50 H time for feedback clamp is stabilized until recover.

- Output mode (D5 to D7 of register 1 and D4 of register 3)

It is a test mode. Combination details are table 3 to 5. Normally set to all 0.

- SHA-fsel (D8 to D9 of register 1)

It is a LPF switching of SH amplifier. Frequency characteristics are referred to page 9. To get rough idea, set the double cut off frequency point with using.

- SHSW-fsel (D10 to D13 of register 1)

It is a time constant which sampling the black level of SH amplifier. Frequency characteristics are referred to page 9. To get rough idea, set the double cut off frequency point with using. S/N changes by this data, so find the appropriate point with set data to up/down.

- Clamp (D3 to D7 of register 2)  
Determine the OB part level with digital code of ADC output.  
Clamp level = setting data  $\times$  2 + 14  
Default data is 9 = 32 LSB.
- HGstop-Hsel, HGain-Nsel (D8 to D11 of register 2)  
Determine the lead-in speed of OB clamp. Details are referred to page 7. PGA gain need to be changed for switch the high speed leading mode. Transfer the gain +1/-1 to previous field, its switch to high speed leading mode.
- Low\_PWR (D12 of register 2)  
Switch circuit current and frequency characteristic.  
Data = 0: 36 MHz guarantee  
Data = 1: 25 MHz guarantee
- SPinv (D13 of register 2)  
SPSIG/SPBLK/PBLK input signal inverted switching.  
Data = 1: Normal  
Data = 0: Inverted
- Reset (D15 of register 2)  
Software reset.  
Data = 1: Normal  
Data = 0: Reset  
  
Offset calibration should be done when starting up with using this bit. Details are referred to page 18.
- C\_Bias\_off (D3 of register 3)  
Center bias is turned off in ADCIN mode.  
Data = 0: Normally on  
Data = 1: Off
- Ave\_4H (D6 of register 3)  
Clamp detection data is averaged 4H.  
Data = 0: 1H  
Data = 1: Averaged 4H

**Differential Code and Gray Code (D4 to D5 and D7 to D9 of register 3)**

- Gray code (D4 to D5 of register 3)  
DC output code can be change to following type.

Gray Code [1]	Gray Code [0]	Output Code
0	0	Binary code
0	1	Gray code
1	0	Differential encoded binary
1	1	Differential encoded gray

- Serial data setting items (D7 to D9 of register 3)

Setting Bit	Setting Contents
Gray_test[0]	Standard data output timing control signal
Gray_test[1]	(Refer to the following table)
Gray_test[2]	ADCLK polar with OBP. (Lo→Positive edge, HI→Negative edge)

- Standard data output timing

Gray_test[1]	Gray_test[0]	Standard Data Output Timing
Low	Low	Third and fourth
Low	High	Fourth and fifth
High	Low	Fifth and sixth
High	High	Sixth and seventh

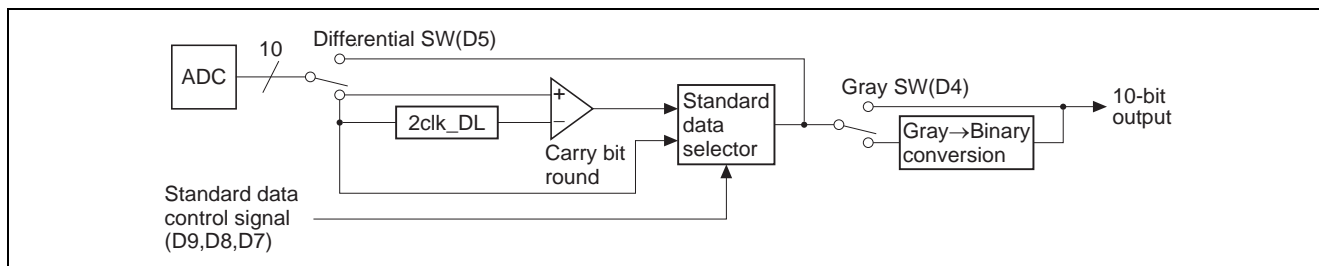
Ripple (pseudo outline made by quantized error) occurs on the point which switching the ADC output multiple bit in parallel. When switching the several of ADC output at the same time, ripple (pseudo outline caused by miss quantization) occurs to the image.

Differential code and gray code are recommended for this countermeasure.

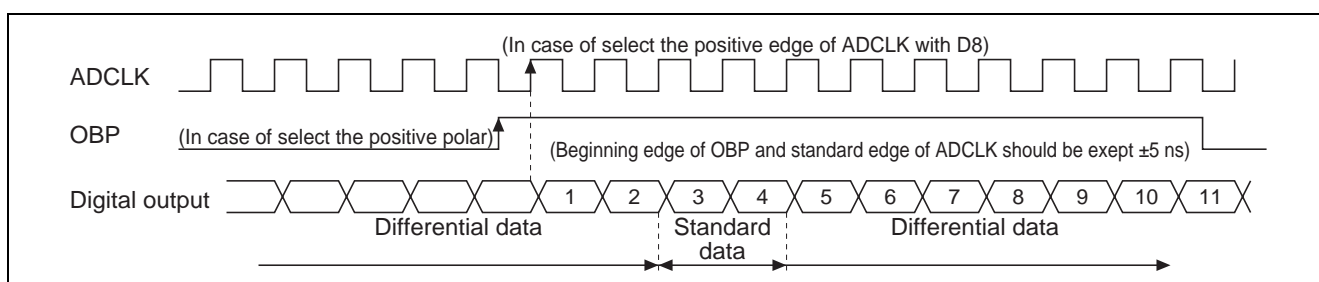
Figure 9 indicates circuit block. When luminance signal changes are smoothly, the number of bit of switching digital output bit can be reduced and easily to reduce the ripple using this function.

This function is especially effective for longer the settings of sensor more than  $\text{clk} = 30 \text{ kHz}$ , and ADC output.

Figure 10 indicates the timing specifications.

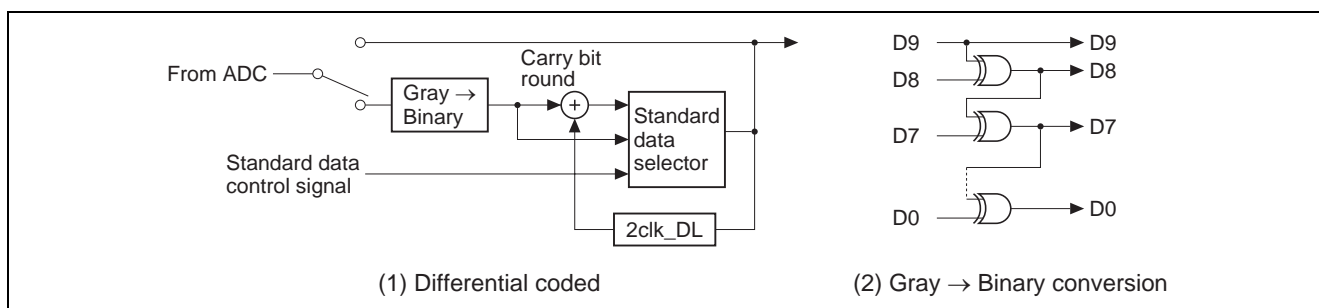


**Figure 9 Differential Code, Gray Code Circuit**



**Figure 10 Differential Code Timing Specifications**

To use differential code, complex circuit is necessary at DSP side.



**Figure 11 Complex Circuit Example**

## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Power supply voltage	V <sub>DD</sub> (max)	4.1	V
Analog input voltage	V <sub>IN</sub> (max)	−0.3 to AV <sub>DD</sub> +0.3	V
Digital input voltage	V <sub>I</sub> (max)	−0.3 to DV <sub>DD</sub> +0.3	V
Operating temperature	Topr	−10 to +75	°C
Power dissipation	Pt(max)	400	mW
Storage temperature	Tstg	−55 to +125	°C
Power supply voltage range	Vopr	2.7 to 3.3	V

Notes: 1. V<sub>DD</sub> indicates AV<sub>DD</sub> and DV<sub>DD</sub>.2. AV<sub>DD</sub> and DV<sub>DD</sub> must be commonly connected outside the IC. When they are separated by a noise filter, the potential difference must be 0.3 V or less at power on, and 0.1 V or less during operation.

## Electrical Characteristics

(Unless othewide specified, Ta = 25°C, AV<sub>DD</sub> = 3.0 V, DV<sub>DD</sub> = 3.0 V, and R<sub>BIAS</sub> = 33 kΩ)

## • Items Common to CDSIN and ADCIN Input Modes

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Power supply voltage range	V <sub>DD</sub>	2.7	3.0	3.3	V		
Conversion frequency	f <sub>CLK</sub> hi	20	—	36	MHz	LoPwr = low	HD49334AHNP
	f <sub>CLK</sub> low	5.5	—	25	MHz	LoPwr = high	HD49334ANP
Digital input voltage	V <sub>IH</sub>	$2.0 \times \frac{DV_{DD}}{3.0}$	—	DV <sub>DD</sub>	V		Digital input pins other than CS, SCK and SDATA
	V <sub>IL</sub>	0	—	$0.8 \times \frac{DV_{DD}}{3.0}$	V		
	V <sub>IH2</sub>	$2.25 \times \frac{DV_{DD}}{3.0}$	—	DV <sub>DD</sub>	V		CS, SCK, SDATA
	V <sub>IL2</sub>	0	—	$0.6 \times \frac{DV_{DD}}{3.0}$	V		
Digital output voltage	V <sub>OH</sub>	DV <sub>DD</sub> −0.5	—	—	V	I <sub>OH</sub> = −1 mA	
	V <sub>OL</sub>	—	—	0.5	V	I <sub>OL</sub> = +1 mA	
Digital input current	I <sub>IH</sub>	—	—	50	μA	V <sub>IH</sub> = 3.0 V	
	I <sub>IH2</sub>	—	—	250	μA	V <sub>IH</sub> = 3.0 V	
	I <sub>IL</sub>	−50	—	—	μA	V <sub>IL</sub> = 0 V	
Digital output current	I <sub>OZH</sub>	—	—	50	μA	V <sub>OH</sub> = V <sub>DD</sub>	
	I <sub>OZL</sub>	−50	—	—	μA	V <sub>OL</sub> = 0 V	
ADC resolution	RES	10	10	10	bit		
ADC integral linearity	INL	—	3	—	LSBp-p	f <sub>CLK</sub> = 25 MHz	
ADC differential linearity+	DNL+	—	0.3	0.9	LSB	f <sub>CLK</sub> = 25 MHz	*1
ADC differential linearity−	DNL−	−0.9	−0.3	—	LSB	f <sub>CLK</sub> = 25 MHz	*1
Sleep current	I <sub>SLP</sub>	−100	0	100	μA	Digital input pin is set to 0 V, output pin is open	
Standby current	I <sub>STBY</sub>	—	3	5	mA	Digital I/O pin is set to 0 V	

Notes: 1. Differential linearity is the calculated difference in linearity errors between adjacent codes.

2. Values within parentheses ( ) are for reference.



## Electrical Characteristics (cont.)

(Unless othewide specified, Ta = 25°C, AV<sub>DD</sub> = 3.0 V, DV<sub>DD</sub> = 3.0 V, and R<sub>BIAS</sub> = 33 kΩ)

## • Items for CDSIN Input Mode

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Consumption current (1)	I <sub>DD1</sub>	—	45.0	54.5	mA	f <sub>CLK</sub> = 36 MHz	CDSIN mode LoPwr = low
Consumption current (2)	I <sub>DD2</sub>	—	23.5	31.0	mA	f <sub>CLK</sub> = 25 MHz	CDSIN mode LoPwr = high
CCD offset tolerance range	V <sub>CCD</sub>	(-100)	—	(100)	mV		
Timing specifications (1)	t <sub>CDS1</sub>	—	(1.5)	—	ns		See table 8
Timing specifications (2)	t <sub>CDS2</sub>	Typ × 0.8	1/4f <sub>CLK</sub>	Typ × 1.2	ns		
Timing specifications (3)	t <sub>CDS3</sub>	—	(1.5)	—	ns		
Timing specifications (4)	t <sub>CDS4</sub>	Typ × 0.8	1/4f <sub>CLK</sub>	Typ × 1.2	ns		
Timing specifications (5)	t <sub>CDS5</sub>	Typ × 0.85	1/2f <sub>CLK</sub>	Typ × 1.15	ns		
Timing specifications (6)	t <sub>CDS6</sub>	1	5	9	ns		
Timing specifications (7)	t <sub>CDS7</sub>	11	—	—	ns		
Timing specifications (8)	t <sub>CDS8</sub>	11	—	—	ns		
Timing specifications (9)	t <sub>CHLD9</sub>	3	7	—	ns	C <sub>L</sub> = 10 pF	
Timing specifications (10)	t <sub>COD10</sub>	—	16	24	ns		
Clamp level	CLP(00)	—	(14)	—	LSB		
	CLP(09)	—	(32)	—	LSB		
	CLP(31)	—	(76)	—	LSB		
PGA gain at CDS input	PGA(0)	-4.4	-2.4	-0.4	dB		
	PGA(63)	4.1	6.1	8.1	dB		
	PGA(127)	12.5	14.5	16.5	dB		
	PGA(191)	21.0	23.0	25.0	dB		
	PGA(255)	29.4	31.4	33.4	dB		

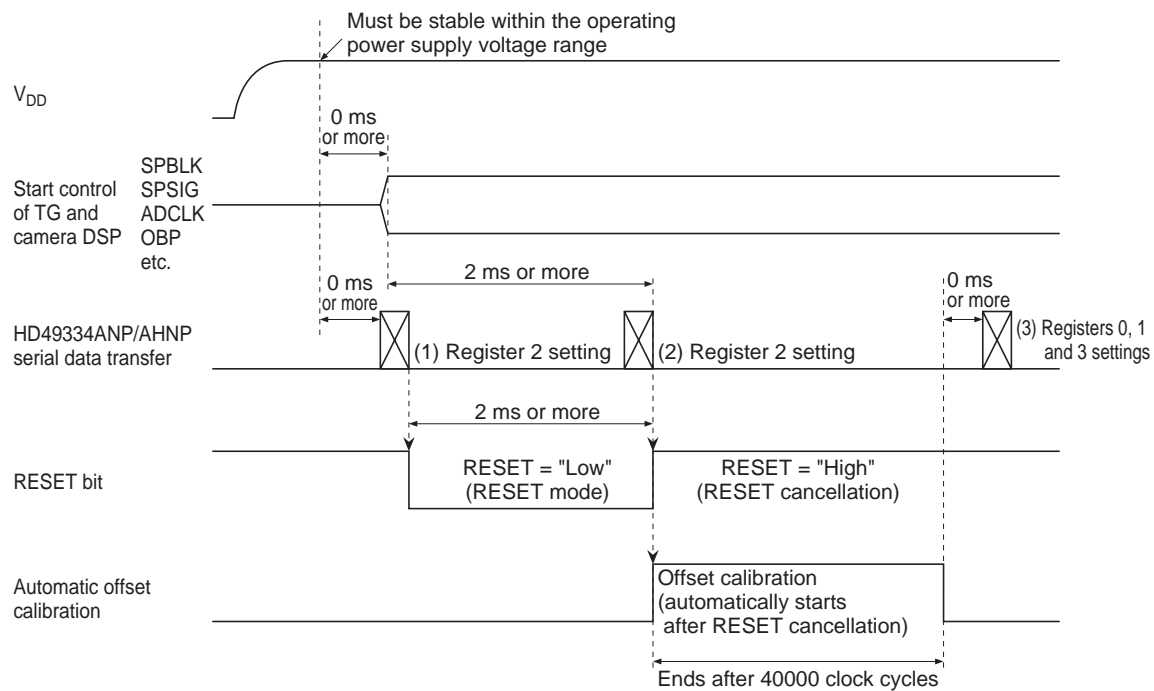
Note : Values within parentheses ( ) are for reference.

## • Items for ADCIN Input Mode

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Consumption current (3)	I <sub>DD3</sub>	—	30.0	38.0	mA	f <sub>CLK</sub> = 36 MHz	ADCIN mode LoPwr = low
Consumption current (4)	I <sub>DD4</sub>	—	17.0	21.5	mA	f <sub>CLK</sub> = 25 MHz	ADCIN mode LoPwr = high
Timing specifications (11)	t <sub>ADC1</sub>	—	(6)	—	ns		See table 9
Timing specifications (12)	t <sub>ADC2</sub>	Typ × 0.85	1/2f <sub>ADCLK</sub>	Typ × 1.15	ns		
Timing specifications (13)	t <sub>ADC3</sub>	Typ × 0.85	1/2f <sub>ADCLK</sub>	Typ × 1.15	ns		
Timing specifications (14)	t <sub>AHLD4</sub>	10	14.5	—	ns	C <sub>L</sub> = 10 pF	
Timing specifications (15)	t <sub>AOD5</sub>	—	23.5	31.5	ns		
Input current at ADC input	I <sub>IN CIN</sub>	-110	—	110	μA	V <sub>IN</sub> = 1.0 V to 2.0 V	
Clamp level at ADC input	OF2	—	(512)	—	LSB		
PGA gain at ADC input	GSL(0)	0.45	0.57	0.72	Times		
	GSL(63)	1.36	1.71	2.16	Times		
	GSL(127)	2.27	2.86	3.60	Times		
	GSL(191)	3.18	4.00	5.04	Times		
	GSL(255)	4.08	5.14	6.47	Times		

Note : Values within parentheses ( ) are for reference.

## Operation Sequence at Power On

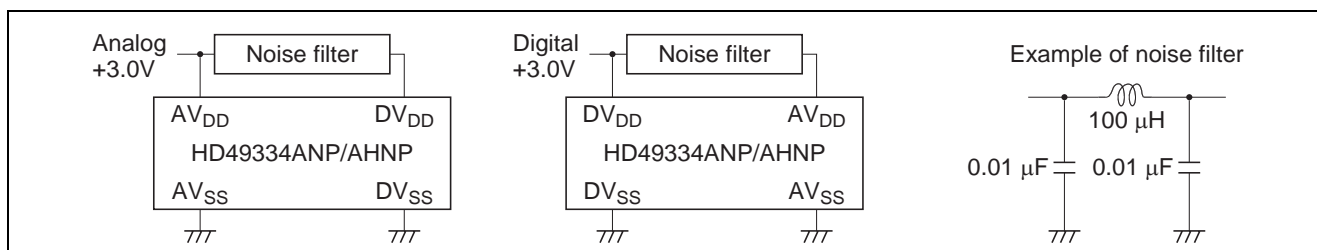


The following describes the above serial data transfer. For details on registers 0, 1, 2, and 3, refer to table 10.

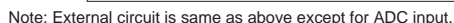
- (1) Register 2 setting : Set all bits in register 2 to the usage condition, and set the RESET bit to low.
- (2) Register 2 setting : Cancel the RESET mode by setting the register 2 RESET bit to high.  
Do not change other register 2 settings. Offset calibration starts automatically.
- (3) Register 0, 1 and 3 settings : After the offset calibration is terminated, set registers 0, 1 and 3.

## Notice for Use

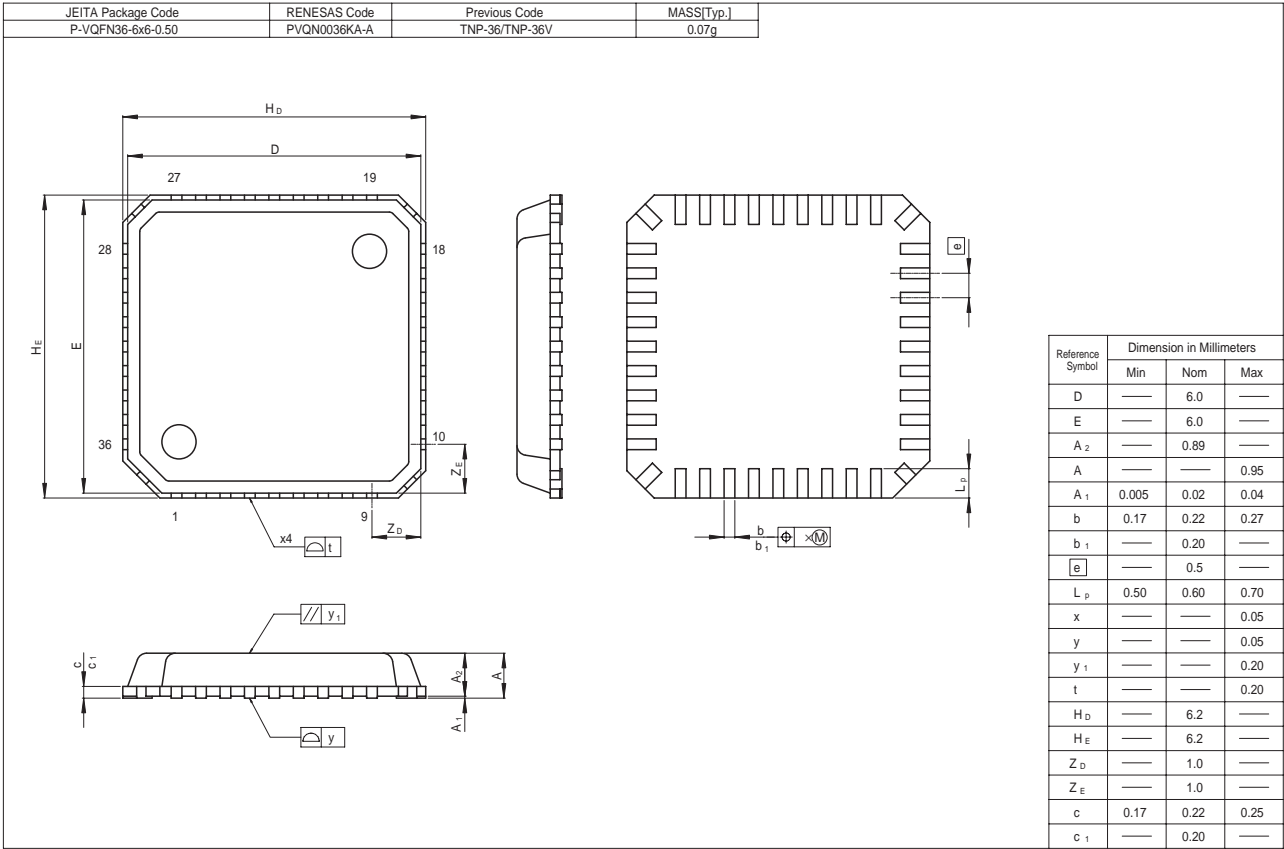
1. Careful handling is necessary to prevent damage due to static electricity.
2. This product has been developed for consumer applications, and should not be used in non-consumer applications.
3. As this IC is sensitive to power line noise, the ground impedance should be kept as small as possible. Also, to prevent latchup, a ceramic capacitor of 0.1  $\mu\text{F}$  or more and an electrolytic capacitor of 10  $\mu\text{F}$  or more should be inserted between the ground and power supply.
4. Common connection of  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$  should be made off-chip. If  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$  are isolated by a noise filter, the phase difference should be 0.3 V or less at power-on and 0.1 V or less during operation.
5. If a noise filter is necessary, make a common connection after passage through the filter, as shown in the figure below.



6. Connect  $\text{AV}_{\text{SS}}$  and  $\text{DV}_{\text{SS}}$  off-chip using a common ground. If there are separate analog system and digital system set grounds, connect to the analog system.
7. When  $V_{\text{DD}}$  is specified in the data sheet, this indicates  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$ .
8. No Connection (NC) pins are not connected inside the IC, but it is recommended that they be connected to power supply or ground pins or left open to prevent crosstalk in adjacent analog pins.
9. To ensure low thermal resistance of the package, a Cu-type lead material is used. As this material is less tolerant of bending than Fe-type lead material, careful handling is necessary.
10. The infrared reflow soldering method should be used to mount the chip. Note that general heating methods such as solder dipping cannot be used.
11. Serial communication should not be performed during the effective video period, since this will result in degraded picture quality. Also, use of dedicated ports is recommended for the SCK and SDATA signals used in the HD49330AF. If ports are to be shared with another IC, picture quality should first be thoroughly checked.
12. At power-on, automatic adjustment of the offset voltage generated from PGA, ADC, etc., must be implemented in accordance with the power-on operating sequence (see page 15).



Package Dimensions



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