Application Note:

XRD9814/16 CIS S/H No Clamp DC Coupled

INTRODUCTION

The XRD9814/16 is designed for Contact Image Sensor (CIS) based Multi Function Products (MFP), flatbed scanners, film scanners and gray scale scanners. Most CIS image sensors utilitze a no clamp DC coupled input. For AC coupled inputs see AB307. The XRD9814/16 has a wide range of offset to compensate for any DC offset inherent in the CIS output. This application brief describes a CIS No Clamp DC coupled Mode.

APPLICATION BLOCK DIAGRAM

The XRD9814/16 has a programmable mode for S/H which is ideal for interfacing with CIS image sensors. This application note describes a DC coupled function. For AC Coupled Input applications, see AB307. The gain and offset DACs in the XRD9814/16 are independent and offer a wide range for signal conditioning. Figure 1, is a block diagram of the XRD9814/16 interfacing with a CIS in a DC coupled no clamp mode.

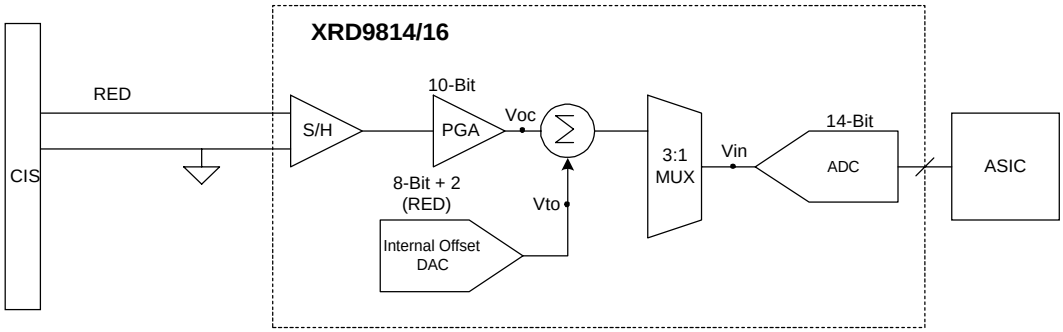

Figure 1. Block Diagram of the XRD9814/16 Interfacing With a CIS in a DC Coupled No Clamp Mode

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APPLICATION CIRCUITRY

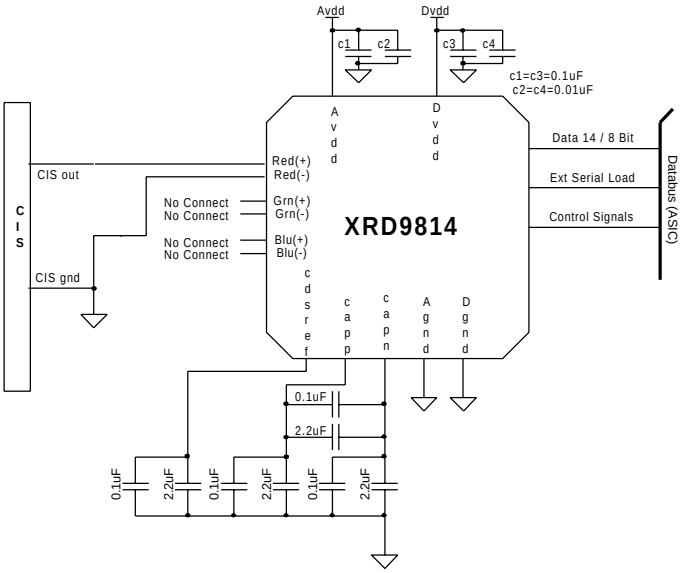

Figure 2. Schematic Diagram of Common Circuitry Used for a CIS, DC Coupled Interface

GAIN ADJUSTMENT

The PGA gain is implemented with an 10-bit DAC. For best results, it is recommended that the gain be adjusted before the offset DAC is used to compensate for any offsets in the system. The gain equation is

PGA Gain = (code/1024)*9.0 + 1.0

where code represents the binary contents of the 10-Bit gain setting register.

OFFSET ADJUSTMENT

The offset adjustment is implemented with a gross offset plus a fine offset (8-Bit DAC). After the gain DAC is used to amplify the input, the correct offset value can be determined by the following equation:

Voc = {(Sensor Offset + Internal Offsets XRD9814/16) * Gain}

Once Voc (See Figure 1) is known, the following total offset (node Vto in Figure 1) can be used to set the offset register configuration.

Vto = {Gross Offset + Fine Offset}
Set Voc = Vto

Therefore, the input to the A/D (node Vin in Figure 1) is given by the following equation:

Vin = (Vpix * Gain) + Voc - Vto

For additional information on how to implement the internal offset DAC, see AB302.

SERIAL PORT CONFIGURATION

Configuration Register #1
By default, the XRD9814/16 is configured for CCD, AC coupled pixel clamp mode. For CIS DC coupled no clamp, the serial port should be configured the following way:

A2	A1	A0	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0	0	0	0	0	1	0	0	0	1	1	0	0

Notes:
PB7 and PB6 are set to 10 for selecting S/H no clamp mode.
PB4 and PB3 are set to 01 for selecting RED single channel mode.
PB2 is set to 1 for selecting Non-inverted (CIS) mode.
PB1 is set to 1 for enabling the line buffer.

TIMING DIAGRAM

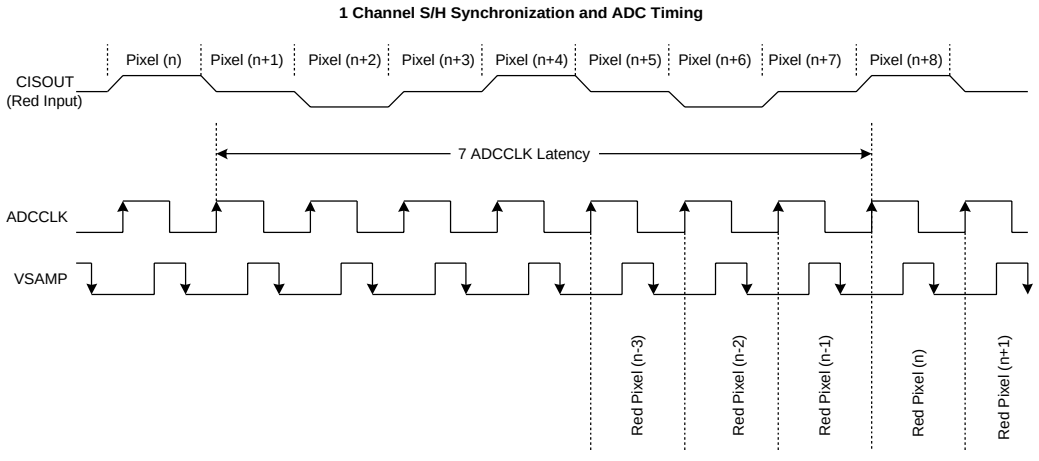

Figure 3. Timing Diagram of the XRD9814/16 Interfacing With a CIS in an DC Coupled No Clamp Mode

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