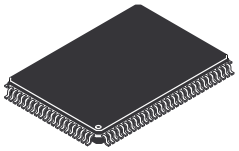
MCM63P631A

Product Preview

64K x 32 Bit Pipelined BurstRAM Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM63P631A is a 2M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, and Pentium™ microprocessors. It is organized as 64K words of 32 bits each. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$), sleep mode (ZZ), and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM63P631A (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as “a”, “b”, “c”, and “d”. $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, etc. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

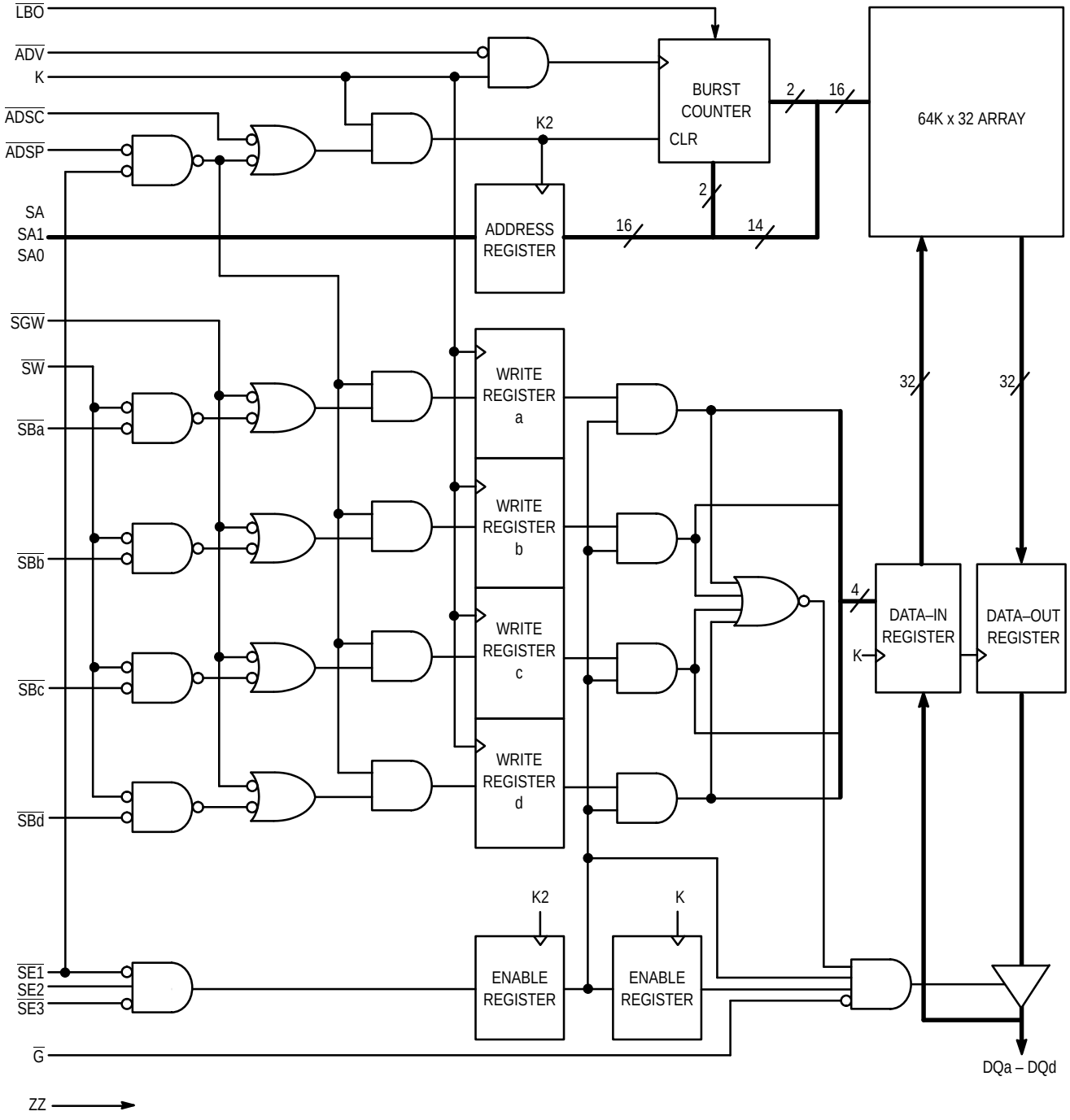
For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM63P631A operates from a 3.3 V power supply, all inputs and outputs are LVTTL compatible.

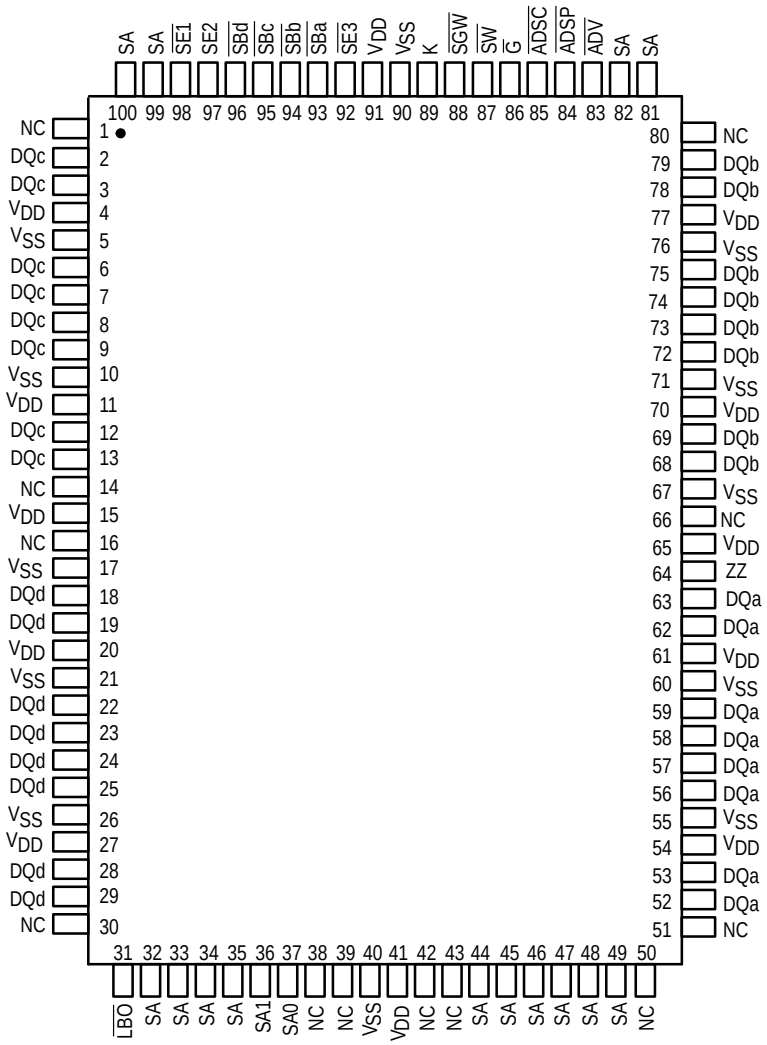
- MCM63P631A–117 = 4.5 ns access / 8.5 ns cycle (117 MHz)
  MCM63P631A–100 = 4.5 ns access / 10 ns cycle (100 MHz)
  MCM63P631A–75 = 7 ns access / 13.3 ns cycle (75 MHz)
  MCM63P631A–66 = 8 ns access / 15 ns cycle (66 MHz)
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- Sleep Mode (ZZ)
- PB1 Version 2.0 Compatible
- Single–Cycle Deselect Timing
- JEDEC Standard 100–Pin TQFP Package

9/30/97

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, is used to latch a new external address. Used to initiate a READ, WRITE or chip deselect.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ or chip deselect cycle (exception — chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79 (c) 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29	DQx	I/O	Synchronous Data I/O: “x” refers to the byte being read or written (byte a, b, c, d).
86	$\overline{G}$	Input	Asynchronous Output Enable.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$, $\overline{LBO}$, and ZZ.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: “x” refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
64	ZZ	Input	Sleep Mode: This active high asynchronous signal places the RAM into the lowest power mode. The ZZ pin disables the RAMs internal clock when placed in this mode. When ZZ is negated, the RAM remains in low power mode until it is commanded to READ or WRITE. Data integrity is maintained upon returning to normal operation.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
1, 14, 16, 30, 38, 39, 42, 43, 50, 51, 66, 80	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 5)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ[5]
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ[5]
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:

1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This READ assumes the RAM was previously deselected.

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{G}$	I/O Status
Read	L	L	Data Out (DQx)
Read	L	H	High–Z
Write	L	X	High–Z
Deselected	L	X	High–Z
Sleep	H	X	High–Z

LINEAR BURST ADDRESS TABLE ($\overline{LBO}$ = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO}$ = V_{DD})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit	Notes
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V	
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V	
Output Current (per I/O)	I_{out}	± 20	mA	
Package Power Dissipation	P_D	1.6	W	2
Ambient Temperature	T_A	0 to 70	°C	
Die Temperature	T_J	110	°C	2
Temperature Under Bias	T_{bias}	– 10 to 85	°C	
Storage Temperature	T_{stg}	– 55 to 125	°C	

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Input Low Voltage	V_{IL}	– 0.5	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.5	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg}(I)$	—	—	± 1	μA	1, 2
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg}(O)$	—	—	± 1	μA	
AC Supply Current (Device Selected, All Outputs Open, Freq = Max, V_{DD} = Max)	MCM63P631A–117 MCM63P631A–100 MCM63P631A–75 MCM63P631A–66	I_{DDA}	— — — —	— — — —	TBD	mA	3, 4, 5
CMOS Standby Supply Current (Device Deselected, Freq = 0, V_{DD} = Max, All Inputs Static at CMOS Levels)		I_{SB2}	—	—	TBD	mA	6, 7
Sleep Mode Supply Current (Sleep Mode, Freq = Max, V_{DD} = Max, All Other Inputs Static at CMOS Levels, ZZ ≥ V_{DD} – 0.2 V)		I_{ZZ}	—	—	2	mA	2, 7, 8
TTL Standby (Device Deselected, Freq = 0, V_{DD} = Max, All Inputs Static at TTL Levels)		I_{SB3}	—	—	TBD	mA	6, 9
Clock Running (Device Deselected, Freq = Max, V_{DD} = Max, All Inputs Toggling at CMOS Levels)	MCM63P631A–117 MCM63P631A–100 MCM63P631A–75 MCM63P631A–66	I_{SB4}	— — — —	— — — —	TBD	mA	6, 7
Static Clock Running (Device Deselected, Freq = Max, V_{DD} = Max, All Inputs Static at TTL Levels)	MCM63P631A–117 MCM63P631A–100 MCM63P631A–75 MCM63P631A–66	I_{SB5}	— — — —	— — — —	TBD	mA	6, 9
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	—	0.4	V	
Output High Voltage (I_{OH} = – 4 mA)		V_{OH}	2.4	—	—	V	

NOTES:
1. $\overline{LBO}$ pin has an internal pullup and will exhibit leakage currents of ± 5 μA.
2. ZZ pin has an internal pulldown and will exhibit leakage currents of ± 5 μA.
3. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V).
4. All addresses transition simultaneously low (LSB) and then high (MSB).
5. Data states are all zero.
6. Device in Deselected mode as defined by the Truth Table.
7. CMOS levels are $V_{in} \le V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V.
8. Device in Sleep Mode as defined by the Asynchronous Truth Table.
9. TTL levels are $V_{in} \le V_{IL}$ or ≥ V_{IH}.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	3	5	pF
Input/Output Capacitance	$C_{I/O}$	—	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 1 V/ns (20 to 80%)

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	63P631A–117 117 MHz		63P631A–100 100 MHz		63P631A–75 75 MHz		63P631A–66 66 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	8.5	—	10	—	13	—	15	—	ns	
Clock High Pulse Width	t_{KHKL}	3.4	—	4	—	5.2	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	3.4	—	4	—	5.2	—	6	—	ns	
Clock Access Time	t_{KHQV}	—	4.5	—	4.5	—	7	—	8	ns	
Output Enable to Output Valid	t_{GLQV}	—	4.5	—	4.5	—	5	—	5	ns	
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	0	—	ns	5
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	1.5	—	1.5	—	ns	5
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	5
Output Disable to Q High–Z	t_{GHQZ}	—	5.5	—	5.5	—	7	—	8	ns	5, 6
Clock High to Q High–Z	t_{KHQZ}	1.5	5.5	1.5	5.5	2	7	2	8	ns	5, 6
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	 t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	 t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Sleep Mode Standby	t_{ZZS}	—	2 x t_{KHKH}	—	2 x t_{KHKH}	—	2 x t_{KHKH}	—	2 x t_{KHKH}	ns	
Sleep Mode Recovery	t_{ZZREC}	2 x t_{KHKH}	—	2 x t_{KHKH}	—	2 x t_{KHKH}	—	2 x t_{KHKH}	—	ns	
Sleep Mode High to Q High–Z	t_{ZZQZ}	—	15	—	15	—	15	—	15	ns	

NOTES:
1. Write applies to all $\overline{SBx}$, $\overline{SW}$, and $\overline{SGW}$ signals when the chip is selected and $\overline{ADSP}$ high.
2. Chip Enable applies to all $\overline{SE1}$, SE2 and $\overline{SE3}$ signals whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
5. This parameter is sampled and is not 100% tested.
6. Measured at ± 200 mV from steady state.

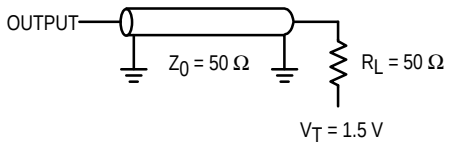
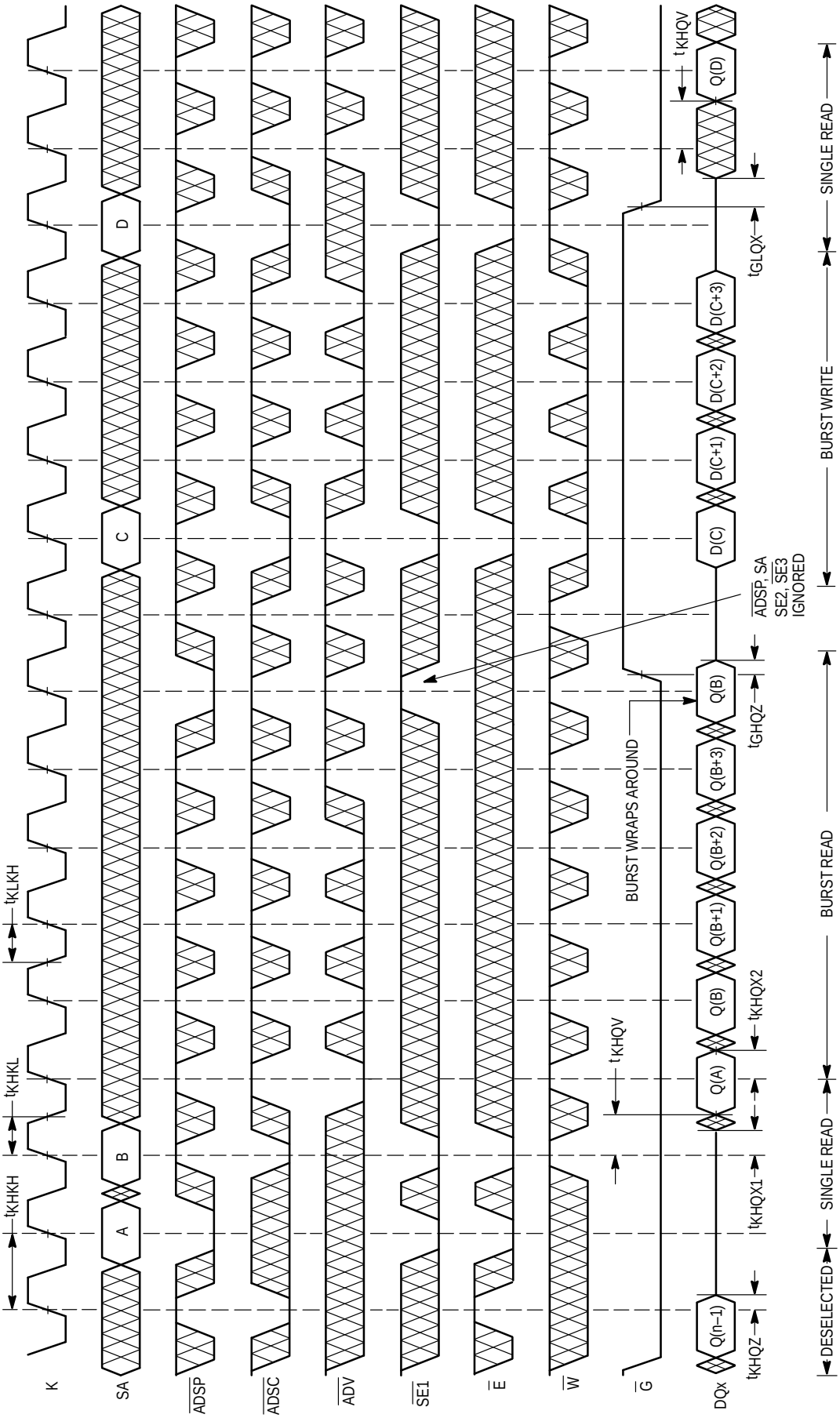


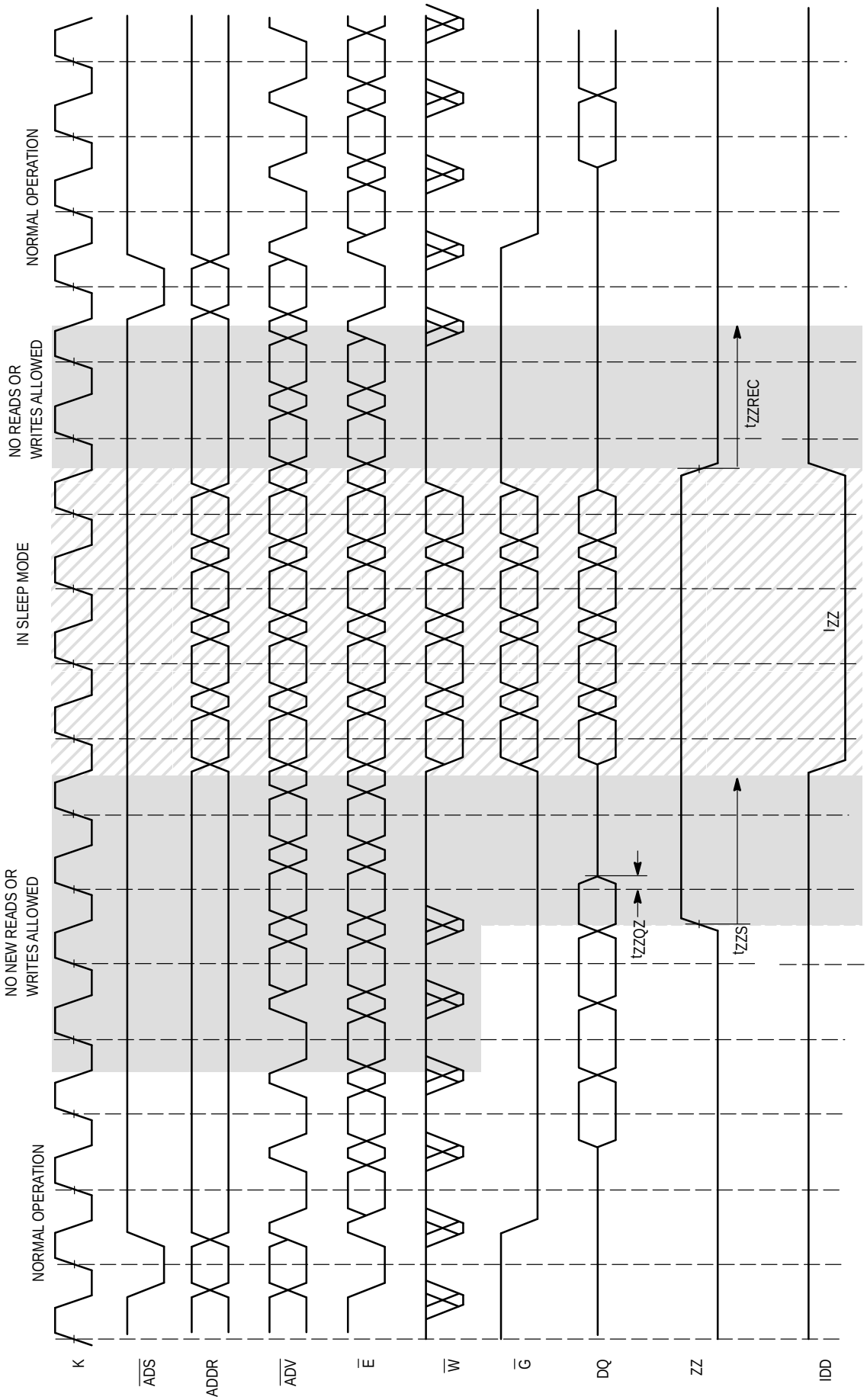
Figure 1. AC Test Load

READ/WRITE CYCLES



Note: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and / or $\overline{SW}$ and $\overline{SBx}$ low.

SLEEP MODE TIMING



NOTE: $\overline{ADS}$ low = $\overline{ADSC}$ low or $\overline{ADSP}$ low.
$\overline{ADS}$ high = both $\overline{ADSC}$, $\overline{ADSP}$ high.
$\overline{E}$ low = $\overline{SE1}$ low, SE2 high, $\overline{SE3}$ low.
I_{ZZ} (max) specifications will not be met if inputs toggle.

APPLICATION INFORMATION

The MCM63P631A BurstRAM is a high speed synchronous SRAM intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers — from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 64K x 32 BurstRAM (MCM63P631A) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency — "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. For cost–sensitive applications that require zero–wait state L2 cache bus speeds of up to 75 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

SLEEP MODE

A sleep mode feature, the ZZ pin, has been implemented on the MCM63P631A. It allows the system designer to place the RAM in the lowest possible power condition by asserting ZZ. The sleep mode timing diagram shows the different modes of operation: Normal Operation, No READ/WRITE Allowed, and Sleep Mode. Each mode has its own set of constraints and conditions that are allowed.

Normal Operation: All inputs must meet setup and hold times prior to sleep and t_{ZZREC} nanoseconds after recovering from sleep. Clock (K) must also meet cycle, high, and low times during these periods. Two cycles prior to sleep, initiation of either a read or write operation is not allowed.

No READ/WRITE: During the period of time just prior to sleep and during recovery from sleep, the assertion of either $\overline{ADSC}$, $\overline{ADSP}$, or any write signal is not allowed. If a write operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM can not be guaranteed immediately after ZZ is asserted (prior to being in sleep).

Sleep Mode: The RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current (I_{ZZ}). All inputs are allowed to toggle — the RAM will not be selected and perform any reads or writes. However, if inputs toggle, the I_{ZZ} (max) specification will not be met.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for PowerPC– and Pentium–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM63P631A. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

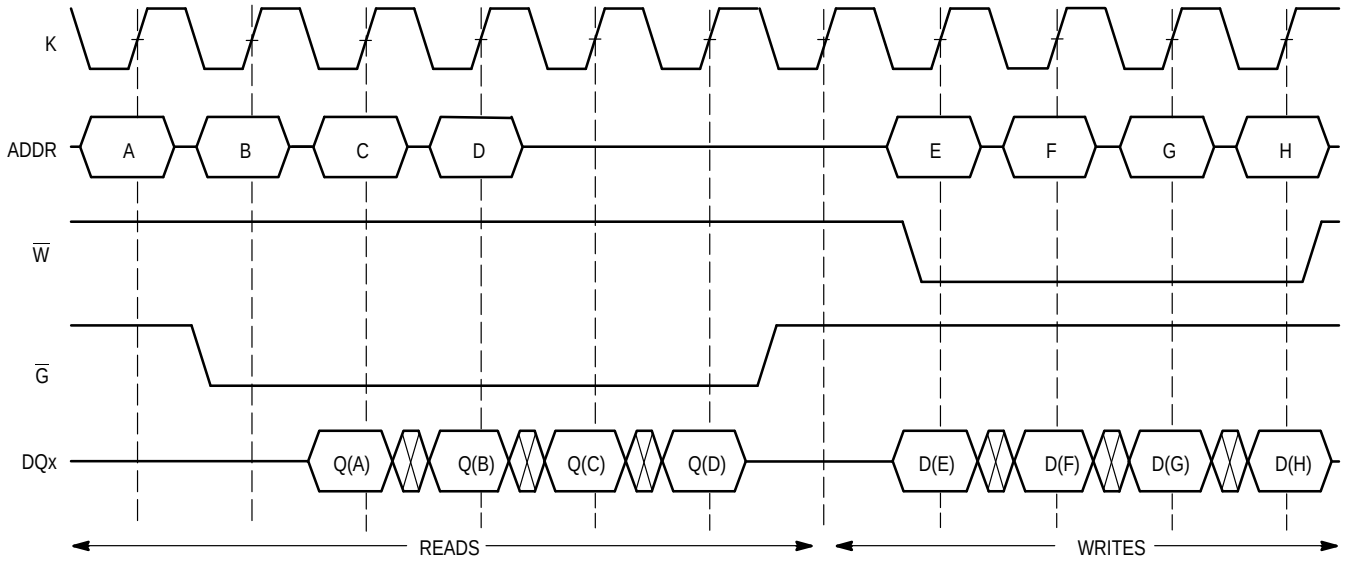
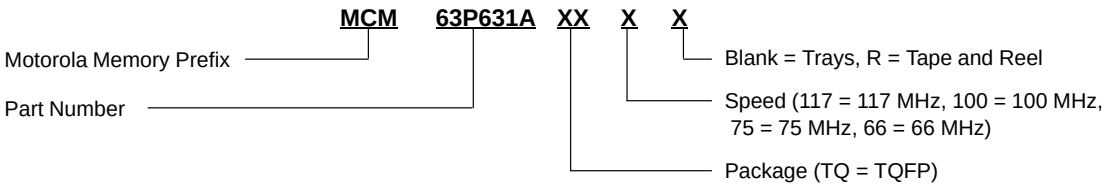


Figure 2. Configured as Non–Burst Pipelined Synchronous SRAM

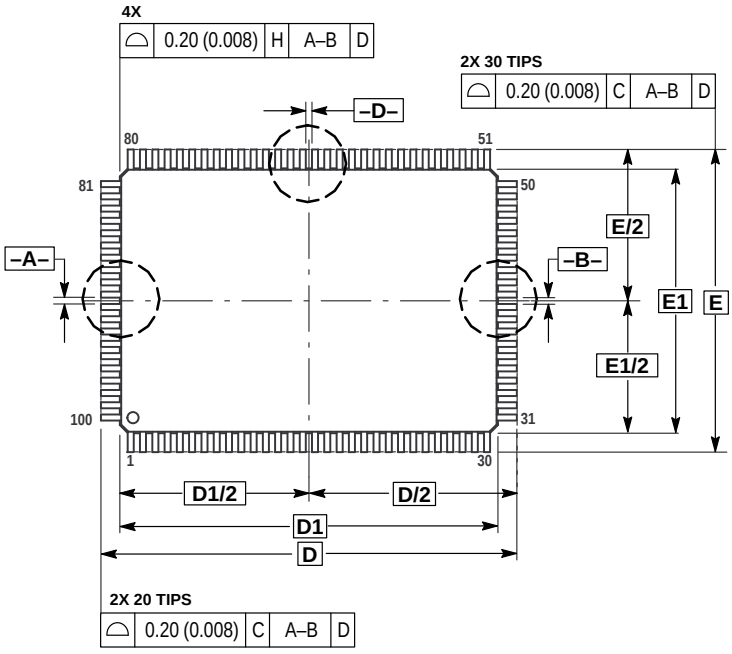
ORDERING INFORMATION
(Order by Full Part Number)

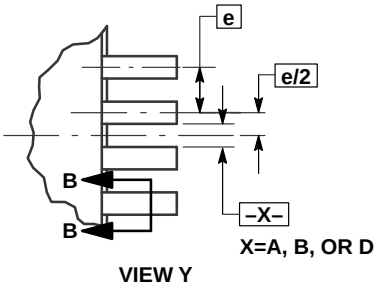


Full Part Numbers — MCM63P631ATQ117, MCM63P631ATQ117R, MCM63P631ATQ100, MCM63P631ATQ100R, MCM63P631ATQ75, MCM63P631ATQ75R, MCM63P631ATQ66, MCM63P631ATQ66R

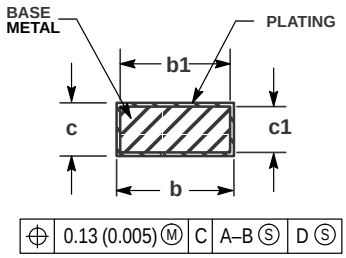
PACKAGE DIMENSIONS

TQ PACKAGE
TQFP
CASE 983A–01

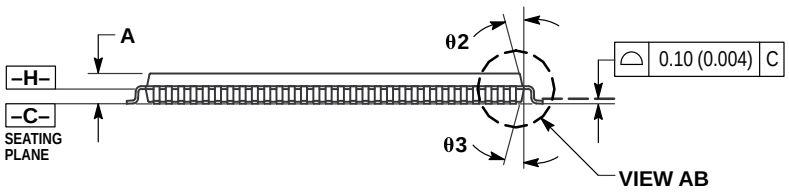




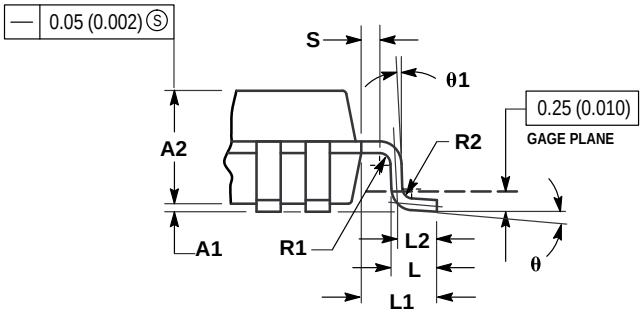
VIEW Y



SECTION B–B



VIEW AB



VIEW AB

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	—	0.008	—
R1	0.08	—	0.003	—
R2	0.08	0.20	0.003	0.008
θ	0 °	7 °	0 °	7 °
θ1	0 °	—	0 °	—
θ2	11 °	13 °	11 °	13 °
θ3	11 °	13 °	11 °	13 °

How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado, 80217. 1-303-675-2140 or 1-800-441-2447

Mfax™ : RMFAX0@email.sps.mot.com – TOUCHTONE 1-602-244-6609
Motorola Fax Back System – US & Canada ONLY 1-800-774-1848
– http://sps.motorola.com/mfax/

HOME PAGE : http://motorola.com/sps/

JAPAN: Nippon Motorola Ltd.; SPD, Strategic Planning Office; 4-32-1, Nishi-Gotanda; Shinagawa-ku, Tokyo 141, Japan. 81-3-5487-8488

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

CUSTOMER FOCUS CENTER: 1-800-521-6274