Application Note

Application of SSD181X/SSD1815A/SSD1815B to Existing LCD Modules

Solomon Systech Limited

INTRODUCTION

SSD181X/SSD1815A/SSD1815B series LCD driver IC is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix graphic display system. It is capable of driving various sizes displays, which are commonly used in mobile phone applications. This application note describes how to apply SSD181X/SSD1815A/SSD1815B into existing LCD modules.

Dot-matrix Display with separated Icon Line

- SSD1811: 132 x 48 + 1 Icon Line
- SSD1812: 132 x 54 + 1 Icon Line
- SSD1813: 132 x 32 + 1 Icon Line
- SSD1815/SSD1815A/SSD1815B: 132 x 64 + 1 Icon Line

SPECIFICATION OF DRIVER IC

Single Supply Operation, 1.8 V - 3.5V
Minimum -12.0V LCD Driving Output Voltage
Low Current Sleep Mode
On-Chip Voltage Generator or External LCD Driving Power Supply Selectable
2X / 3X / 4X On-Chip DC-DC Converter
On-Chip Oscillator
Programmable Multiplex ratio in dot-matrix display area

- SSD1811: 1Mux ~ 48Mux
- SSD1812: 1Mux ~ 54Mux
- SSD1813: 1Mux ~ 32Mux
- SSD1815/SSD1815A/SSD1815B: 1Mux ~ 64Mux

On-Chip Bias Divider
Programmable bias ratio

- SSD1811, SSD1815: 1/4, 1/5, 1/6, 1/7, 1/8, 1/9
- SSD1815A, SSD1815B: 1/4, 1/5, 1/6, 1/7, 1/8, 1/9
- SSD1812: 1/4, 1/5, 1/6, 1/7, 1/8.4, 1/9
- SSD1813: 1/4, 1/5, 1/6

8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface and Serial Peripheral Interface
On-Chip 132 X 65 Graphic Display Data RAM
Re-mapping of Row and Column Drivers
Vertical Scrolling
Display Offset Control
64 Level Internal Contrast Control
External Contrast Control
Programmable LCD Driving Voltage Temperature Coefficients
Available in Gold Bump Die and TAB (Tape Automated Bonding) Package

APPLICATION NOTE 1: ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUIT

For SSD181X/SSD1815A/SSD1815B series IC, it is recommended to design a protection circuit to prevent from unexpected external interference. This is useful especially the designed product has to go through unexpected electrostatic discharge. Figure 1 or 2 are examples of the common circuit used.

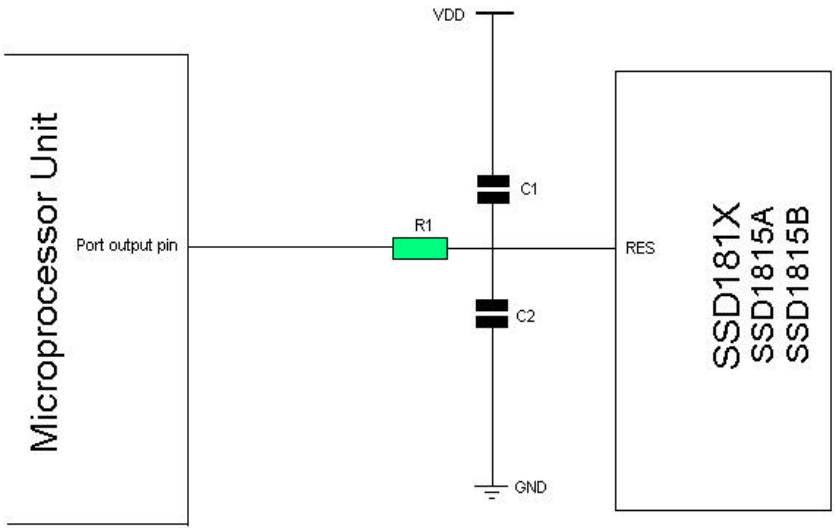


Figure 1. ESD Protection Circuit (Recommendation 1)

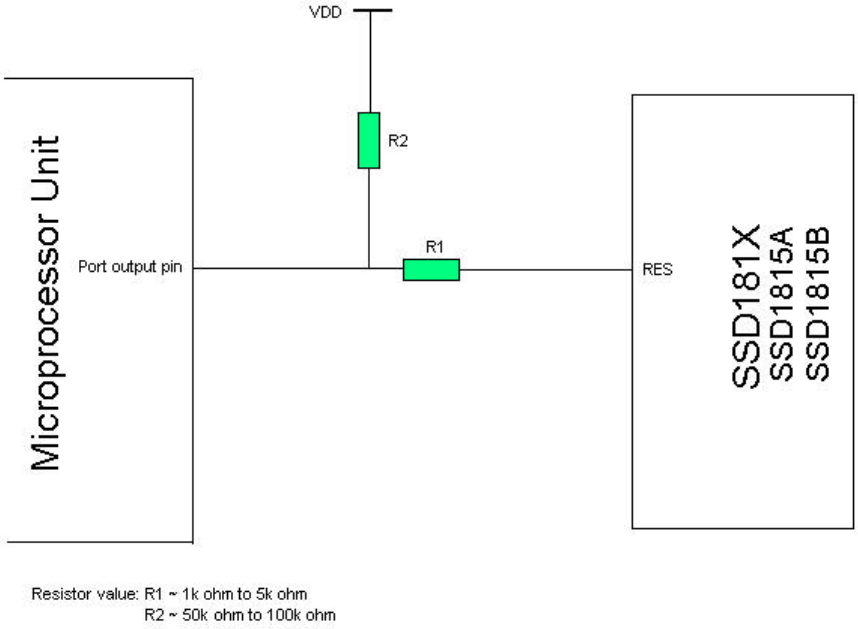


Figure 2. ESD Protection Circuit (Recommendation 2)

Figure 1 & 2 show the common connection design of the LCD driver IC and the main Microprocessor (MCU) unit, the RESET pin of the driver is connected directly to one of the port of the MCU. When external charge is brought near the device (or electrostatic discharge through the device (a spike)), it will discharge by finding its way to the shortest path to ground.

This discharge sometimes will affect the normal operation of the device, causing data loss inside RAM or internal registers, or even re-initialize / reset the device. The IC has a built-in protection circuit to protect the I/O pins from external charge or spike. It can be strengthened by adding an circuitry across the IC Reset pin and MCU port as figure 1 or figure 2.

In addition, more protection can be done by adding a resistor in series, directly in between the RESET pin of the driver IC and the port of the MCU. This will create a filter effect, that will be able to eliminate external noise entering the RESET pin of the driver IC.

Adoption of protection circuit and value of positive components used largely depends on the application printed circuit board design. It is recommended to test and evaluate to find out the best capacitor value for a particular application.

APPLICATION NOTE 2: CONTRAST CONTROL CALCULATION

In the SSD181X/SSD1815A/SSD1815B series IC revision 2.5 onwards, there has been an update on the data information, when using VL6 voltage regulator internal resistors and the electronic volume function, software control of the 64 contrast voltage levels is at each voltage regulator feedback gain can be used (without adding any external resistors). The equation given is as follows: From the above table, the formula can provide a quick estimation of the voltage generated by the software setting and the electronic booster circuit in the IC.

$$V_{L6} - V_{DD} = Gain * (1 + \frac{Contrast}{b}) * V_{ref}$$

$$V_{ref} = (\frac{V_{BE} + R * (V_{DD} - V_{SS})}{1 + R})$$

where

Int. Reg Resistor Ratio Setting (IRS)	20Hex	21Hex	22Hex	23Hex	24Hex	25Hex	26Hex	27Hex	Ext. Resistor
Gain	-3.36	-3.84	-4.38	-4.93	-5.50	-5.89	-6.54	-7.10	-(1+R2/R1)
β	90.54	89.95	89.32	88.69	88.04	87.59	86.77	86.01	96.68

and

TC	0 (-0.01%/°C)	2 (-0.10%/°C)	4 (-0.18%/°C)	7 (-0.25%/°C)
V_{BE}	0.025	0.523	0.520	0.517
R	0.72	0.423	0.272	0.121

*Note: There may be a calculation error of max. 6% when comparing with measurement values.

Case sample: When the voltage regulator internal resistance are used:

The liquid crystal power supply voltage VL6 can be set with the VL6 voltage regulator internal resistors (IRS pin is pulled "H"). When selecting Ta=25°C, with V_{DD} = 2.775V, IRS = 23hex, Contrast setting = 25hex (=37dec), Temperature Compensation (TC) = 0;

By using the formula,

$$Vref = (\frac{0.025 + 0.72 * (2.775 - 0)}{1 + 0.72})$$

V_{ref} = 1.176V
Then,

$$VL\,6 - VDD = -4.93 * (1 + \frac{37}{88.69}) * 1.176$$

Therefore, calculated V_{L6} is -8.22V.

This is a calculated value to give the electronic engineer or designer an indication where the voltage will be generated. This value will deviate in the actual IC performance. The maximum deviation (due to extreme cases) is 6%.

Please find below is a typical V_{L6} distribution:

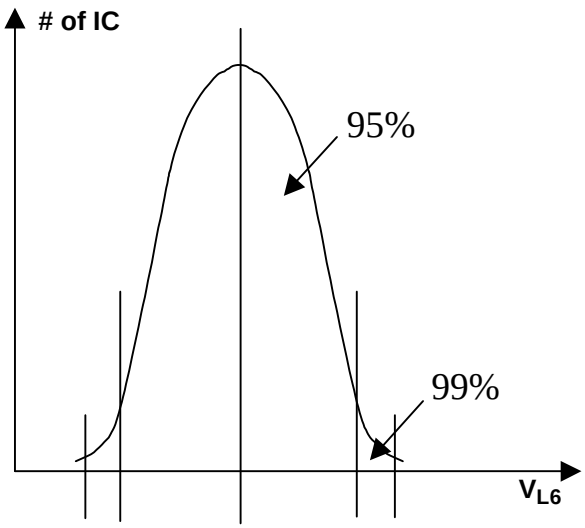


Figure: Normal distribution of the IC performance

Note: The maximum deviation takes care of the very extreme cases (usually less than 1%), it is guaranteed the driver released from mass production will stay within 6% range of the calculated V_{L6} value.

SUGGESTION:

It is strongly suggested in real-life situations, the calculated V_{L6} value should be used only as a reference information for initial design. The actual V_{L6} value of the IC performance should be measured using a number of LCD modules (normally 50 to 100 pieces) from pre-production stage or even at mass production. This value then will truly reflect the actual performance of the IC at LCD modular level.

APPLICATION NOTE 3: HIGH FREQUENCY MODE

The high frequency mode is an enhanced feature for different applications if a higher oscillation frequency is required.

For the IC used in different countries, there is the possibility with a different mains supply frequency of e.g. 50 and 60 Hz. Ambient light from 50 Hz system creates ambient light waves with frequencies of multiples of 50Hz, and same situation applies to 60 Hz mains frequency system.

This multiples of 50Hz/60Hz can interact with the normal operation of the LCD module, thus creating a superimpose interaction with the LCD module. This phenomenon, if happens, can be picked up as the “flickering” effect.

Solomon Systech Limited add an extra feature to change the oscillation frequency of its SSD181X/SSD1815A/SSD1815B series IC during initial setup stage. This feature therefore changes the operating frame frequency of the LCD module. It is hoped that in certain situations and areas, this phenomenon can be reduced.

Modify Oscillation Frequency command:

10101001
$X_7X_6X_5$.....

For default operation:	$X_7X_6X_5$ = 010 (POR for SSD1811, SSD1812) : Typ. 31 kHz
	$X_7X_6X_5$ = 011 (POR for SSD1813, SSD1815, SSD1815A, SSD1815B) : Typ. 17 kHz
For High Frequency mode:	$X_7X_6X_5$ = 110 (POR for SSD1811, SSD1812) : Typ. 38 kHz
	$X_7X_6X_5$ = 110 (POR for SSD1813, SSD1815, SSD1815A, SSD1815B) : Typ. 19 kHz

Example:
The SSD1813 series driver IC has a typical oscillation frequency of 17kHz. By calculation, the frame frequency is then 64.4 Hz. It is possible to shift the oscillation frequency up to a typical of 19 kHz. The frame frequency is thus shifted up to 73 Hz.
This shift of oscillation frequency can keep the display system away from the ambient light frequency and its harmonics, reducing interference caused by these ambient light waves.

Note: Slightly higher current consumption in high frequency mode, should be considered.

APPLICATION NOTE 4: REFERENCE CIRCUIT EXAMPLE FOR HIGH LOADING SITUATIONS

When the built-in power circuit is used to drive a liquid crystal display panel which is heavily loaded with AC or DC signals, it is recommended to connect a series of external resistors to stabilize potentials of VL_2, VL_3, VL_4 and VL_5 which are output from the built-in voltage divider (follower). The number of resistors used depends on the situations of the panel. SSL recommends customer to try in order to obtain the best result.

When installing the COG, or in special cases when designs that may cause high loading situations for the driver IC. It is necessary to consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.

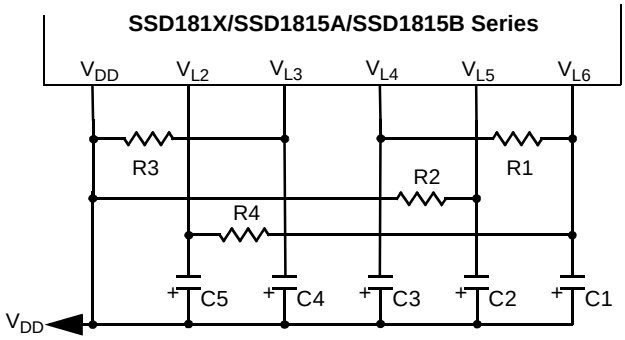
Therefore, when installing the COG design the module paying sufficient considerations to the following situations:

- suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
- suppress the resistance connecting to the power supply pin of the driver chip.
- make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

As a rule of thumb, it is more preferred to use lower resistance ITO glass panels. Normally we recommend customers to use below 15ohm square ITO glass panels.

Example:

Please find the following circuit a recommendation to LCD module designers that in case of large loading situations, it is possible to maximize the stability of the Voltage booster output.



Remarks: 1. C1 ~ C5 = 0.1 ~ 0.47uF
2. R1 ~ R4 = 100k ohm~ 1M ohm

APPLICATION NOTE 5: V_F PROTECTION FOR POTENTIAL HIGH RF INTERFERENCE SITUATIONS

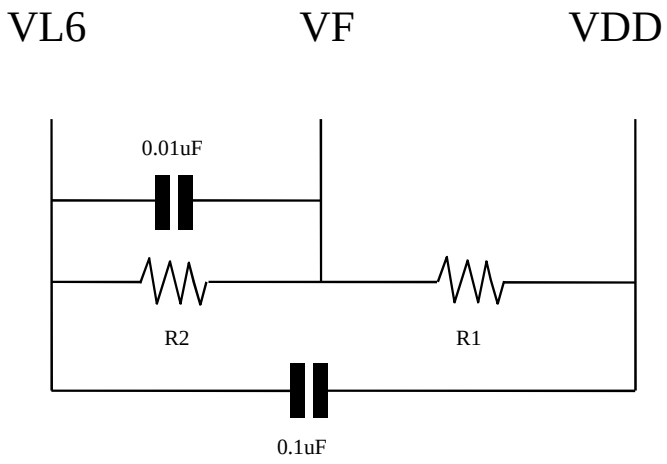
There are situations when the design of the LCD driver circuits is in close proximity with the RF components/circuits, and noise generated from the RF circuit, will potentially affect the general performance of the LCD. There are cases where interference may cause distortion to V_F circuit operation, thus it may have an unexpected effect on the LCD display.

Function of the V_F circuit: Circuit design which is using external resistor network (IRS pulled low), the V_F pin is the voltage feedback of the built-in voltage regulator for generating V_{L6}. In order to generate the LCD driving level, VL6, two external resistors, R1 and R2 should be connected between V_{DD} and V_F, and V_F and V_{L6}, respectively.

Further study needs to be done in a very careful manner, but there are a few precautions that can be done during the PCB design stage:

1) Layout consideration: PCB design should be carefully designed, so that V_F circuit can be placed as far as possible from the RF circuit. The placement of the external components in V_F circuit should be avoided to form a close loop antenna, so as to reduce the chance of RF interference. Reducing the total length of the external circuit from the V_F pin will help improve the immunity to RF signal.

2) V_F circuit: If external resistor network is used, the noise immunity of V_F can be further improved by an additional filtering capacitor as indicated in the circuit below:



This circuit will act as a feedback path which reduce the RF interference.

3) Selection of R1& R2: It is recommended in some of the designs using the values of R1+R2 - less than 1.5 Mohm.

4) Shielding: Shielding is the most effective way to resist RF noise. By covering up the V_F pin and other external components with a metal foil connected to GND, will provide the best result.

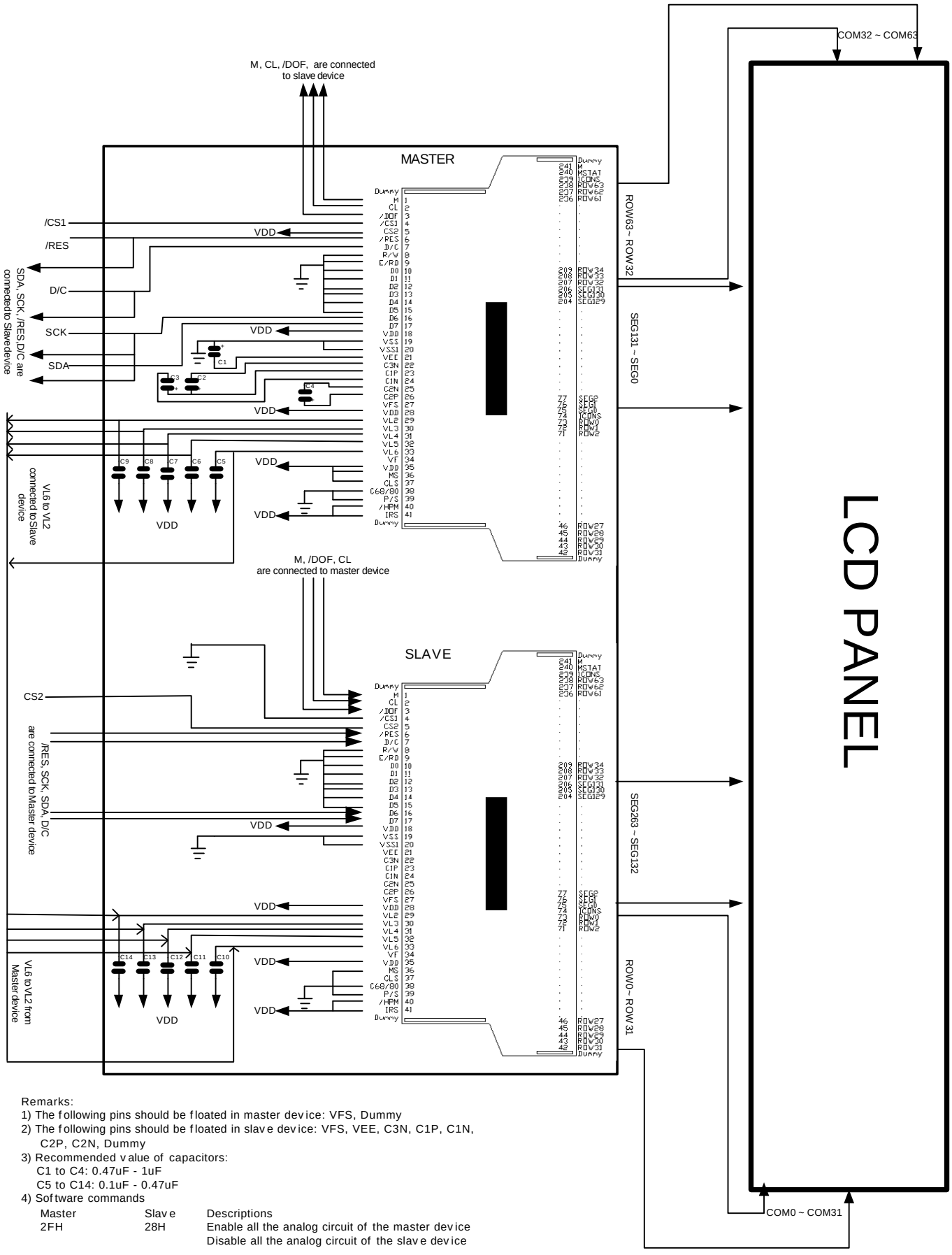
APPLICATION NOTE 6: CASCADE OPERATION FOR SSD181X/SSD1815A/SSD1815B

Two SSD181X/SSD1815A/SSD1815B ICs can be cascaded to form a “master amd slave” system which enlarge the maximum display size to 264 segment x 64 common. The master device generates all the necessary analog and digital control signals for the slave device. The following section summarizes some important note of the system.

Analog control part:
It is obvious that both master and slave devices should have the same LCD driving capability under various operating conditions. The LCD driving voltage of the whole cascade system is generated by the analog circuitry of the master device. The analog circuitry consists of DC-DC voltage booster, voltage reguator with contrast control, temperature compensation circuitry and voltage divider. The divider levels of the master device, which includes VL2 to VL6, are used to generate the divider levels of the slave device. The implementations are carried out by:
1. Connect all the divider output pins (VL2 to VL6) of master device to the slave device.
2. Disable all the analog circuitry in the slave device by software command (28H).

Digital control part:
The communication between master and slave device is carried out by three signals. These three signals are Frame signal (M), display blanking signal (DOFF) and the system clock signal (CL). The master device provides the frame, display blanking and the system clock signals to the slave device. As a result, the slave device is synchronized with the master device. The data interface of the master and slave devices should be the same, either parallel or serial interface. The clock selection pins of the master and slave devices should be the same, either external or internal clock mode.

The following digram shows an example of the cascade application. The product features are listed below.
- Maximum display size: 264 segment x 64 common
- Driving scheme: 4-lines serial interface
- Supply Vdd: 2.4 to 3.5V
- VLCD driving voltage: - 9.3V
- Regulator, clock, contrast control: All internal mode
- Boosting configuration: 4X boosting mode



Remarks:

1) The following pins should be floated in master device: VFS, Dummy
2) The following pins should be floated in slave device: VFS, VEE, C3N, C1P, C1N, C2P, C2N, Dummy
3) Recommended value of capacitors:
   C1 to C4: 0.47uF - 1uF
   C5 to C14: 0.1uF - 0.47uF
4) Software commands

Master	Slave	Descriptions
2FH	28H	Enable all the analog circuit of the master device Disable all the analog circuit of the slave device

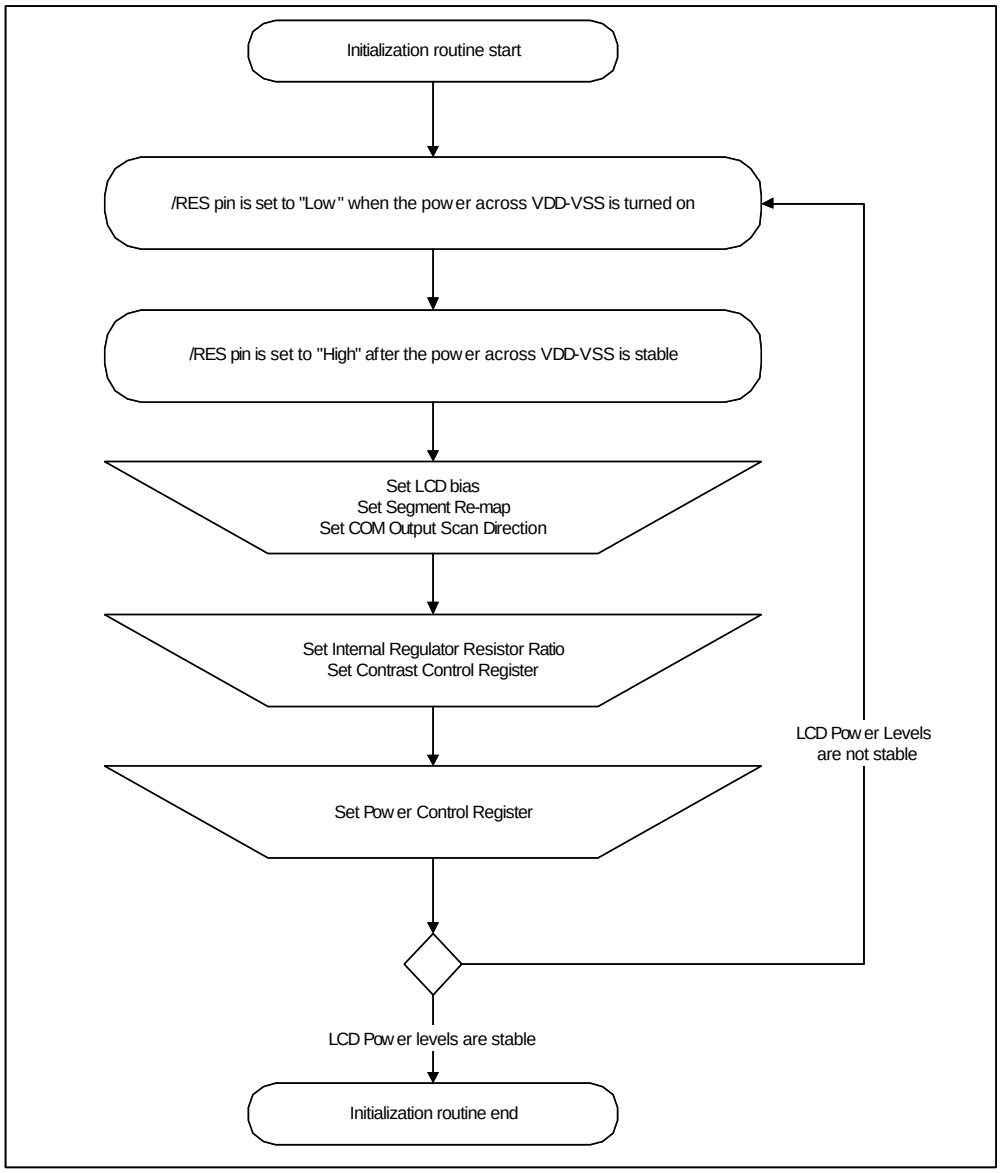
5) Optional capacitors (0.01u to 0.1uF) should be connected across the VL6 and VF

Appendix I Instruction Setup: (For reference)

This section discuss on the initialization, write display data and power off routines of the SSD181X/SSD1815A/SSD1815B. When the power is applied, the VL5 to VL2 levels are non-selected. The non-selective levels are output through the LCD driving output pins, i.e., Segment and Common. The residual electric charge of the stabilizing capacitors, which is connected across the VL6 ~ VL2 levels and Vdd, may induce back into the device. As a result, the LCD panel display totally black instantaneously during the power is turning on. We recommended the following power up sequence in order to prevent the unexpected flashing on the display.

Instruction routine: Normal procedure

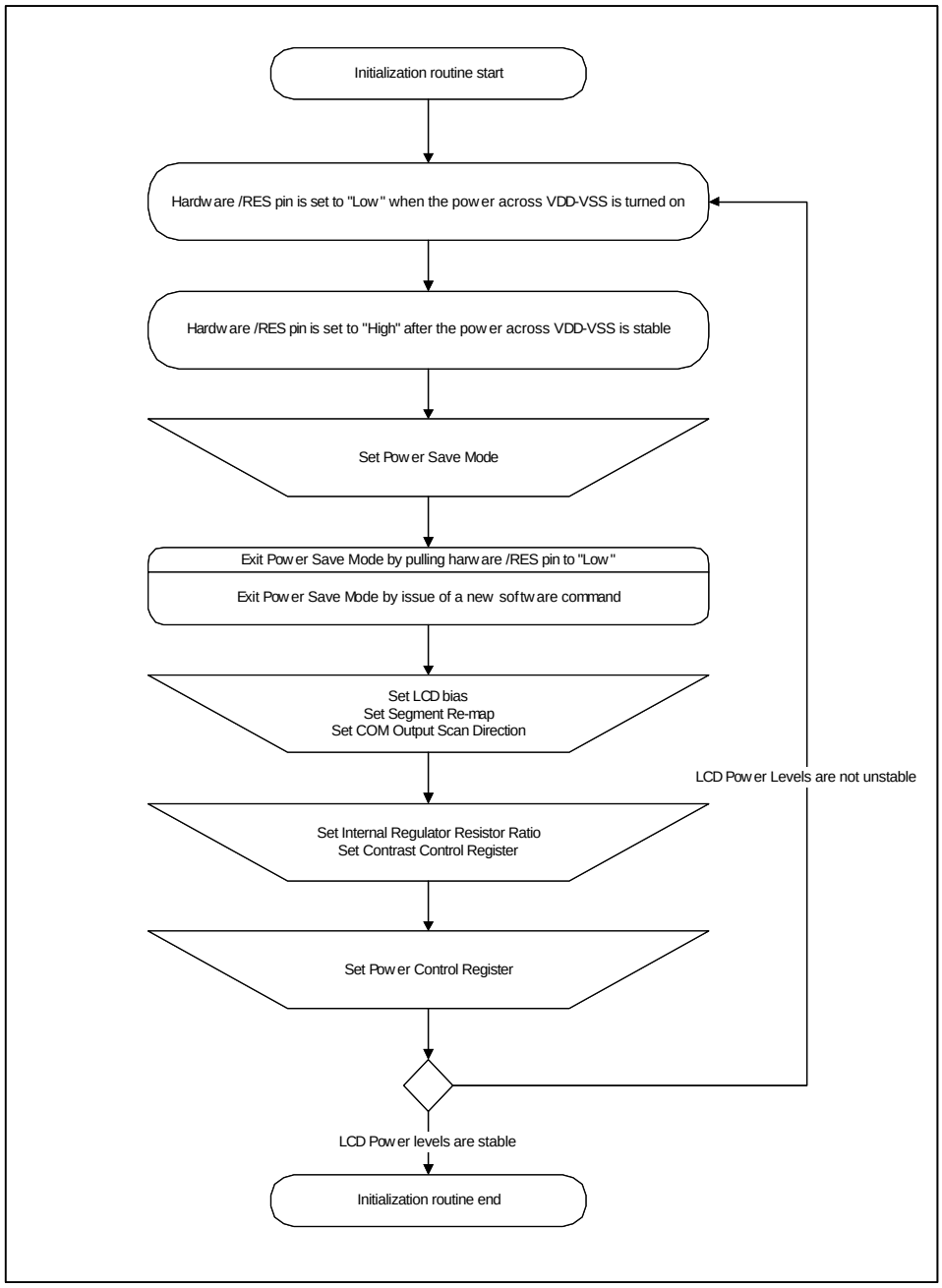
Case 1 – The built-in power is used immediately after turning on the power supply



Remarks: Initialization routine lasts for 5 ms. The estimated time 5 ms vary depending on the panel characteristics and the capacitance of stabilizing capacitors. Please ensure a proper operation check is performed by actual equipment.

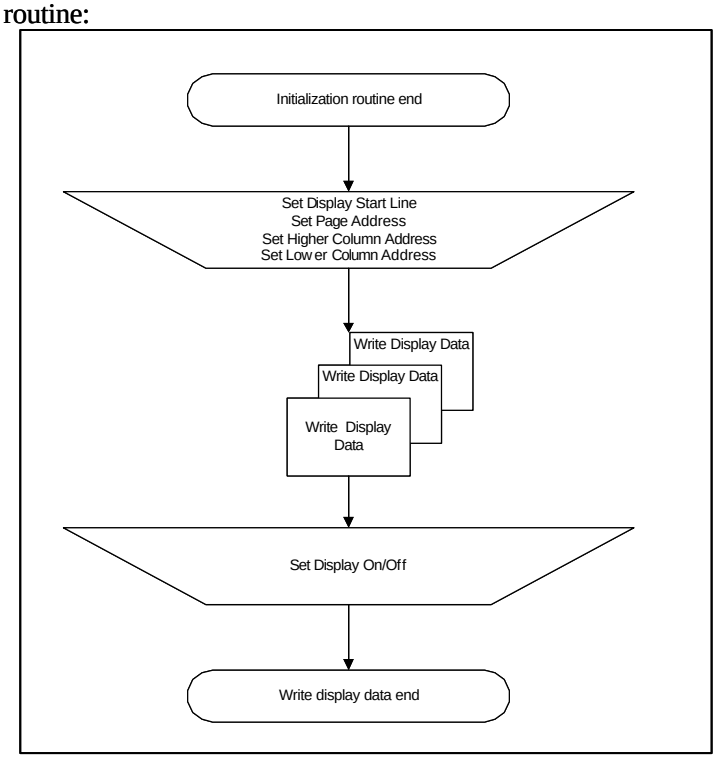
Instruction routine: Escape from power save mode procedure

Case 2 – The built-in power is not used immediately after turning on the power supply

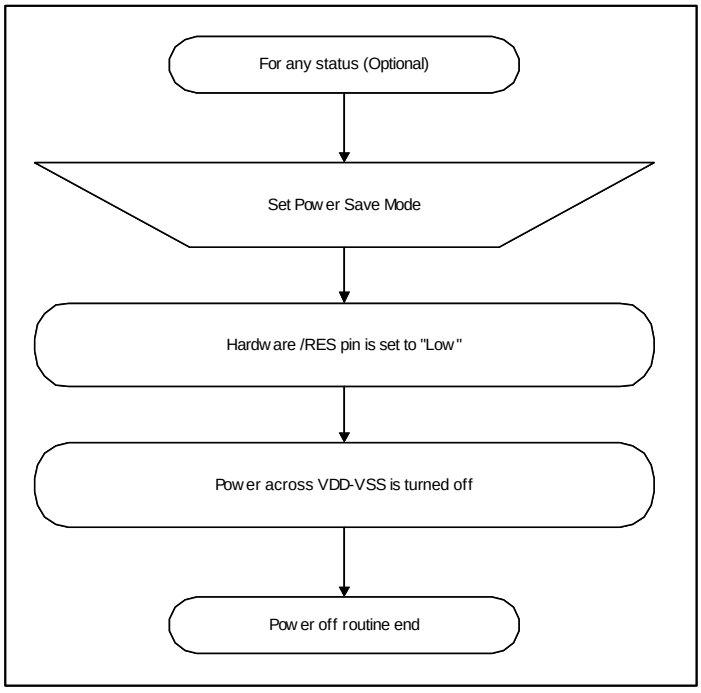


Remarks: Initialization routine lasts for 5 ms. The estimated time 5 ms vary depending on the panel characteristics and the capacitance of stabilizing capacitors. Please ensure a proper operation check is performed by actual equipment.

Display data routine:



Power Off routine:



Remarks: Set the time from "hardware reset active" to "power across VDD-VSS is turned-off" (t_{OFF})to be longer than The time when the potential of VL6 to VL2 becomes lower than the threshold voltage of the LCD panel(t_{TH}) (Approximate 1V). If t_{TH} is too long, resistor should be connected between VL2 and VDD such that t_{TH} Will be reduced.