X9314

Terminal Voltages ±5V, 32 Taps, Log Taper Single Digitally Controlled Potentiometer (XDCP™)

FN8178
Rev 3.00
July 24, 2014

The Intersil X9314 is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

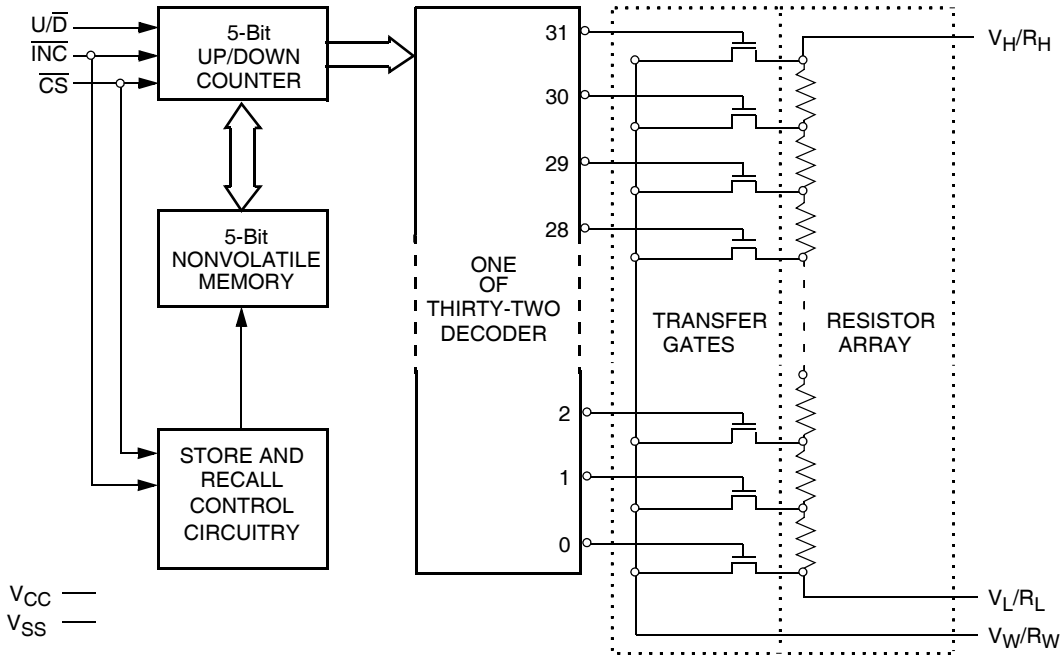
The X9314 is a resistor array composed of 31 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The XDCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- Solid State Potentiometer
- 32 Taps
- 10kΩ End to End Resistance
- Three-Wire Up/Down Serial Interface
- Wiper Resistance, 40Ω Typical
- Nonvolatile Storage and Recall on Power-up of Wiper Position Standby Current < 500µA Max (Total Package)
- V_{CC} = 3V to 5.5V Operation
- 100 Year Data Retention
- Offered in 8 Ld MSOP and SOIC Packages
- Pb-Free Plus Anneal Available (RoHS Compliant)

Block Diagram



Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	V_{CC} RANGE (V)	R_{TOTAL} (kΩ)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
X9314WSIZ	X9314W ZI	5 ±10%	10	-40 to +85	8 Ld SOIC	M8.15
X9314WSZ	X9314W Z			0 to +70	8 Ld SOIC	M8.15
X9314WMIZ-3	DEX	3 to 5.5		-40 to +85	8 Ld MSOP	M8.118
X9314WSZ-3	X9314W ZD			0 to +70	8 Ld SOIC	M8.15

NOTES:

1. Add "T1" suffix for tape and reel.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

V_H/R_H and V_L/R_L

The high (V_H/R_H) and low (V_L/R_L) terminals of the X9314 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. It should be noted that the terminology of V_L/R_L and V_H/R_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

V_W/R_W

V_W/R_W is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment ($\overline{INC}$)

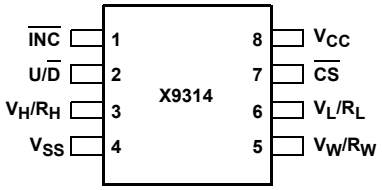
The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

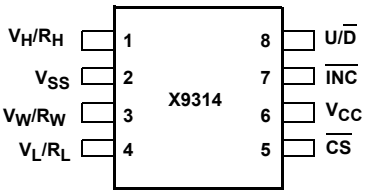
The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9314 will be placed in the low power standby mode until the device is selected once again.

Pin Configuration

X9314
8 LD SOIC
TOP VIEW



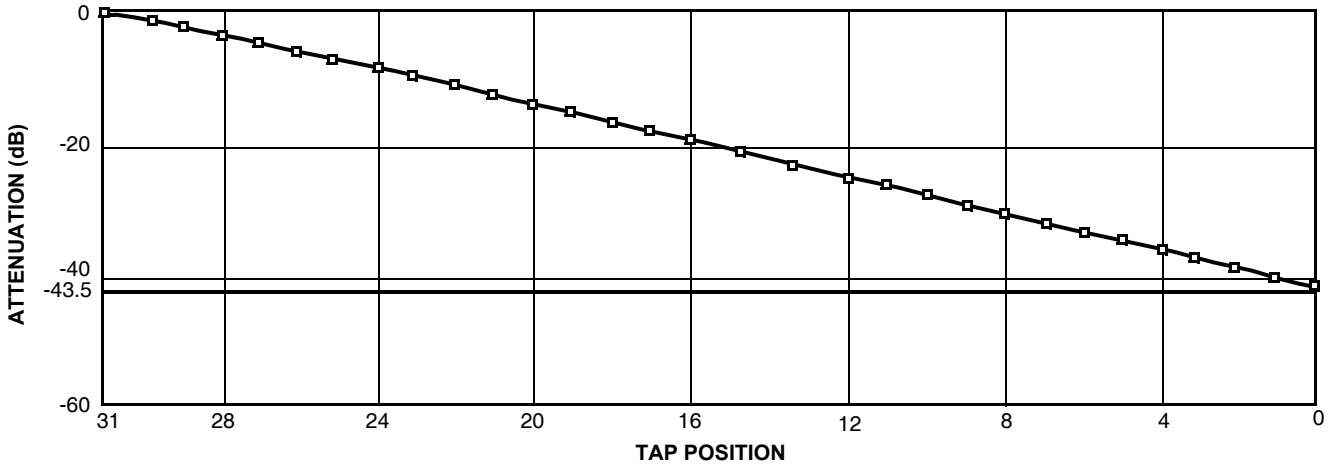
X9314
8 LD MSOP
TOP VIEW



Pin Names

SYMBOL	DESCRIPTION
V_H/R_H	High Terminal
V_W/R_W	Wiper Terminal
V_L/R_L	Low Terminal
V_{SS}	Ground
V_{CC}	Supply Voltage
U/$\overline{D}$	Up/Down Input
INC	Increment Input
CS	Chip Select Input

Typical Attenuation Characteristics (dB)



Principles of Operation

There are three sections of the X9314: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the X9314 is selected and enabled to respond to the

U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a five bit counter. The output of this counter is decoded to select one of thirty-two wiper positions along the resistive array.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transistions HIGH while the $\overline{INC}$ input is also HIGH.

When the X9314 is powered down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

Operation Notes

The system may select the X9314, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. The wiper movement is performed as described above; once the new position is reached, the system would keep the $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position would be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data.

This would allow the system to always power up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the X9314 and then move the wiper up and down until the proper trim is attained.

t_{IW}/R_{TOTAL}

The electronic switches on the X9314 operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

Power-up and Down Requirement

The are no restrictions on the sequencing of V_{CC} and the voltages applied to the potentiometer pins during power-up or power-down conditions. During power-up, the data sheet parameters for the DCP do not fully apply until 1 millisecond after V_{CC} reaches its final value. The V_{CC} ramp rate spec is always in effect.

Absolute Maximum Ratings

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, and
V_{CC} with respect to V_{SS} . . . . . -1V to +7V
Voltage on V_H/R_H and V_L/R_L referenced
to V_{SS} . . . . . -8V to +8V
$\Delta V = |V_H/R_H - V_L/R_L|$ 10V
Lead temperature (soldering 10s) . . . . . +300°C
Wiper current . . . . . ±1mA
I_W (10s) . . . . . ±8.8mA

Recommended Operating Conditions

Temperature (Commercial) . . . . . 0°C to +70°C
Temperature (Industrial) . . . . . -40°C to +85°C
Supply Voltage (V_{CC}) Limits
X9314 . . . . . 5V ± 10%
X9314-2.7 . . . . . 3V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Potentiometer Characteristics

Across recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	LIMITS			
			MIN	TYP	MAX	UNITS
R_{TOTAL}	End to End Resistance Tolerance				±20	%
	V_H/R_H Terminal Voltage		-5		+5	V
$V_{VL/RL}$	V_L/R_L Terminal Voltage		-5		+5	V
	Power Rating	at +25°C			10	mW
R_W	Wiper Resistance	I_W = ±1mA, V_{CC} = 5V		40	100	Ω
I_W	Wiper Current				±4.4	mA
	Noise	Ref: 1kHz		-120		dBV
	Relative variation. Error in step size between taps.	log ($R_{w(n)}$) - log $R_{w(n - 1)}$)	0.07-0.003		0.07 + 0.003	
	R_{TOTAL} Temperature Coefficient	for -40°C to +85°C		±600		ppm/°C
	Ratiometric Temperature Coefficient				±20	ppm/°C
$C_H/C_L/C_W$ Note 4	Potentiometer Capacitance	See "Circuit #3 SPICE Macromodel" on page 5		10/10/25	pF	

DC Electrical Specifications

Across recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP (Note 3)	MAX	
I_{CC}	V_{CC} Active Current	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V/2.4V at max. t_{CYC}		1	3	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ = V_{CC} - 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} - 0.3V			500	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current	V_{IN} = V_{SS} to V_{CC}			±10	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input HIGH Voltage		2		V_{CC} + 1	V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input LOW Voltage		-1		0.8	V
C_{IN} (Note 4)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = +25°C, f = 1MHz			10	pF

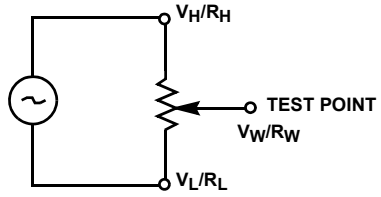
NOTES:

3. Typical values are for T_A = +25°C and nominal supply voltage.
4. This parameter is periodically sampled and not 100% tested.

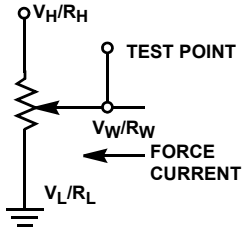
Standard Parts

PART NUMBER	MAXIMUM RESISTANCE	WIPER INCREMENTS	MINIMUM RESISTANCE
X9314W	10kΩ	Log Taper	40Ω

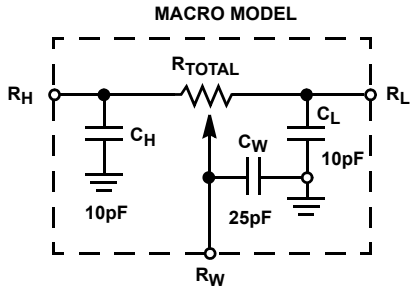
Test Circuit #1



Test Circuit #2



Circuit #3 SPICE Macromodel



A.C. Conditions of Test

INPUT PULSE LEVELS	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↓	H	Wiper up
L	↓	L	Wiper down
↑	H	X	Store wiper position
H	X	X	Standby
↑	L	X	No store, return to standby

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

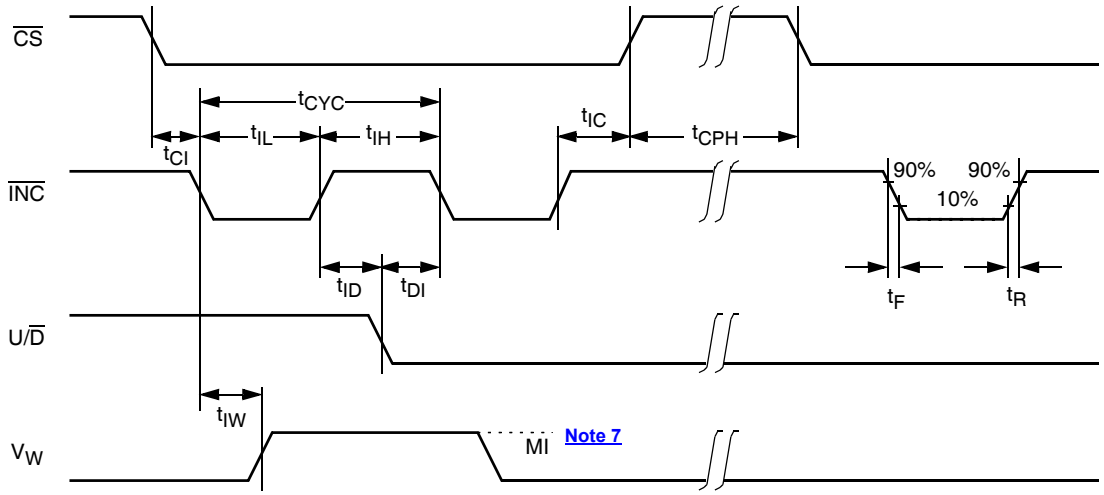
AC Electrical Specifications Across recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNITS
		MIN	TYP(Note 5)	MAX	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	2.9			µs
t_{IL}	$\overline{INC}$ LOW Period	1			µs
t_{IH}	$\overline{INC}$ HIGH Period	1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect Time	20			ms
t_{IW}	$\overline{INC}$ to V_W Change		100	500	µs
t_{CYC}	$\overline{INC}$ Cycle Time	4			µs
t_R, t_F (Note 6)	$\overline{INC}$ Input Rise and Fall Time			500	µs
t_{PU} (Note 6)	Power-up to Wiper Stable			500	µs
t_R V_{CC}	V_{CC} Power-up Rate	0.2		50	mV/µs

NOTES:

5. Typical values are for T_A = +25°C and nominal supply voltage.
6. This parameter is periodically sampled and not 100% tested.

A.C. Timing



NOTE:

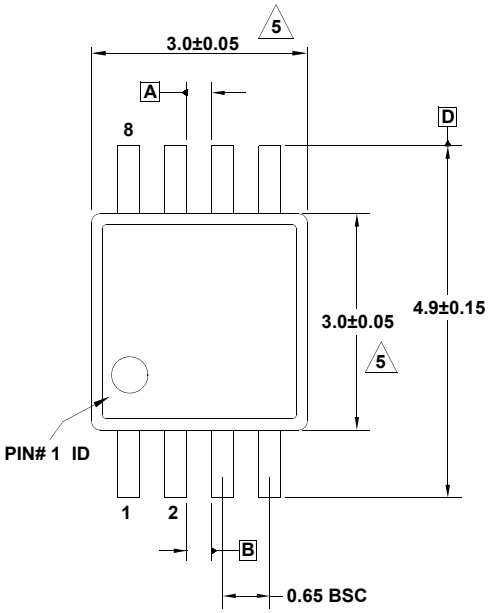
7. MI in the A.C. timing diagram refers to the minimum incremental change in the V_W output due to a change in the wiper position.

Package Outline Drawing

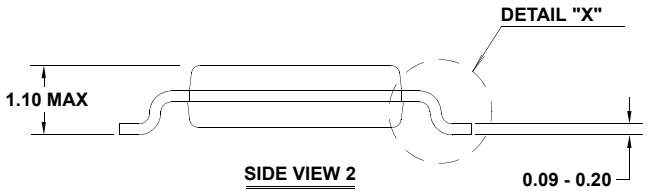
M8.118

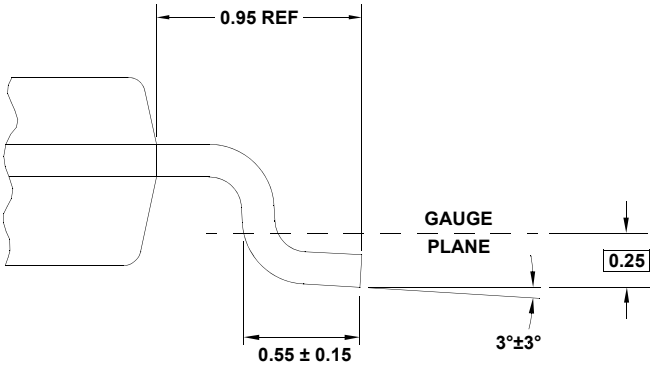
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11

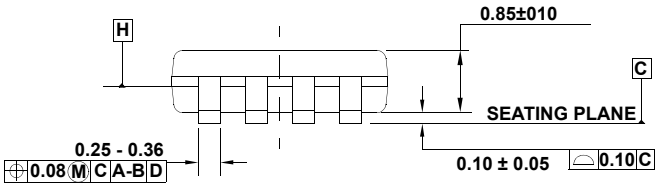


TOP VIEW

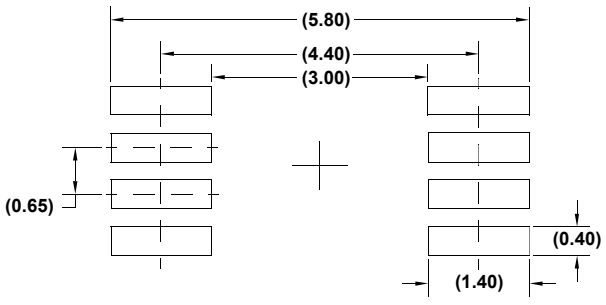




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

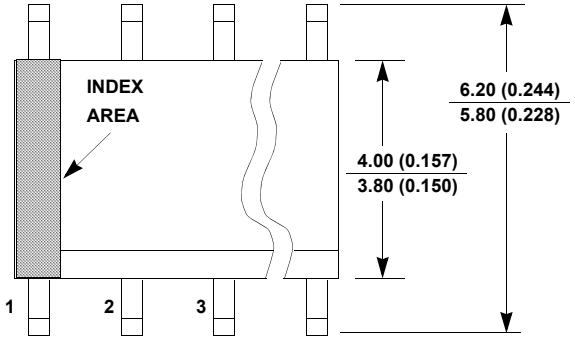
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

Package Outline Drawing

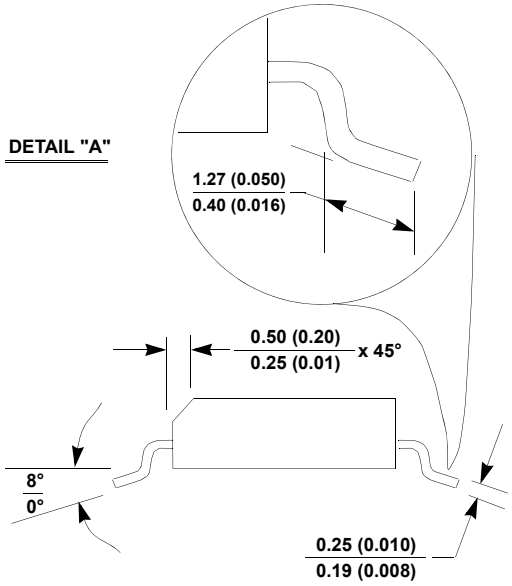
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

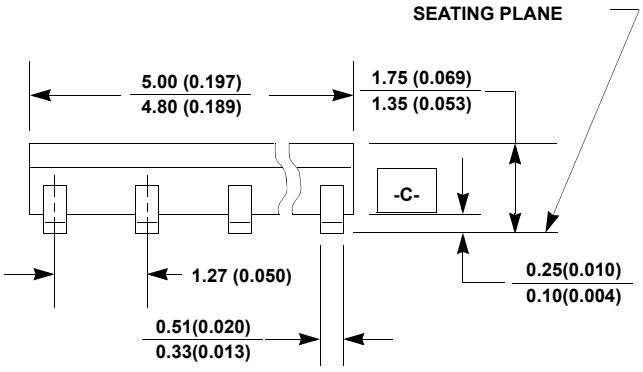
Rev 4, 1/12



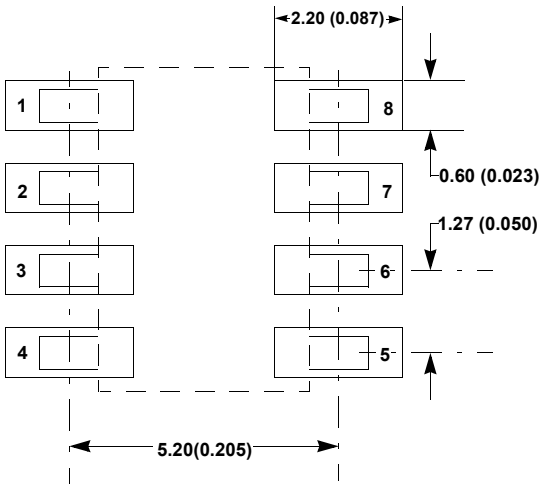
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.