

DRAM MODULE

MT2LD132U(X), MT4LD232U(X)

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
- 4MB (1 Meg x 32) and 8MB (2 Meg x 32)
- High-performance CMOS silicon-gate process
- Single +3.3V $\pm 0.3V$ power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST-PAGE-MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- Serial presence-detect (SPD)

OPTIONS

- Package
100-pin DIMM (gold)
- Timing
50ns access
60ns access
- Access Cycles
FAST PAGE MODE
EDO PAGE MODE

MARKING

G

 -5*
-6

 None
X

*EDO version only

KEY TIMING PARAMETERS

EDO Operating Mode

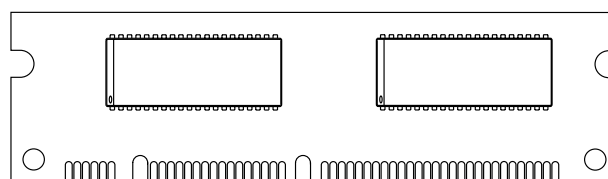
SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{CAS}
-5	84ns	50ns	20ns	25ns	15ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

FPM Operating Mode

SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{RP}
-6	110ns	60ns	35ns	30ns	15ns	40ns

PIN ASSIGNMENT (Front View)

100-Pin DIMM



PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK
1	V _{SS}	26	V _{SS}	51	V _{SS}	76	V _{SS}
2	DQ0	27	DNU	52	DQ8	77	DNU
3	DQ1	28	WE#	53	DQ9	78	OE#
4	DQ2	29	RAS0#	54	DQ10	79	RAS1#
5	DQ3	30	RAS2#	55	DQ11	80	RAS3#
6	V _{DD}	31	V _{DD}	56	V _{DD}	81	V _{DD}
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	CAS0#	36	V _{SS}	61	CAS1#	86	V _{SS}
12	V _{SS}	37	CAS2#	62	V _{SS}	87	CAS3#
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	V _{DD}	67	A9	92	V _{DD}
18	NC (A10)	43	DQ20	68	NC (A11)	93	DQ28
19	NC (A12)	44	DQ21	69	NC (A13)	94	DQ29
20	NC	45	DQ22	70	NC	95	DQ30
21	V _{DD}	46	DQ23	71	V _{DD}	96	DQ31
22	DNU	47	V _{SS}	72	DNU	97	V _{SS}
23	RFU	48	SDA	73	DNU	98	SA0
24	RFU	49	SCL	74	RFU	99	SA1
25	DNU	50	V _{DD}	75	DNU	100	SA2

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT2LD132UG-5 X	1 Meg x 32	50ns
MT2LD132UG-6 X	1 Meg x 32	60ns
MT4LD232UG-5 X	2 Meg x 32	50ns
MT4LD232UG-6 X	2 Meg x 32	60ns

FPM Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT2LD132UG-6	1 Meg x 32	60ns
MT4LD232UG-6	2 Meg x 32	60ns

GENERAL DESCRIPTION

The MT2LD132U(X) and MT4LD232U(X) are randomly accessed 4MB and 8MB memories organized in a x32 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered ten bits (A0-A9) at a time. RAS# is used to latch the first ten bits and CAS# the latter ten bits.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. If WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" option, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^tCP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH. (Refer to the 1 Meg x 16[MT4LC1M16E5] DRAM data sheet for additional information on EDO functionality.)

REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses are executed at least every ^tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time.

SERIAL PRESENCE-DETECT OPERATION

This module family incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ / WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM / EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

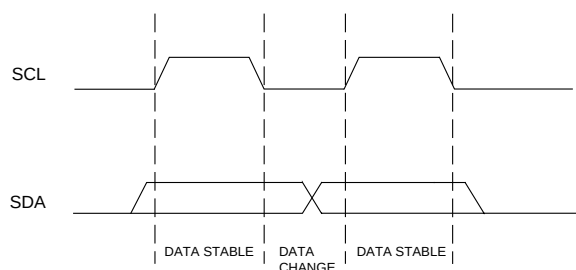


Figure 1
DATA VALIDITY

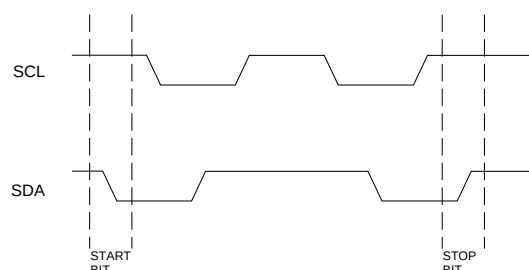


Figure 2
DEFINITION OF START AND STOP

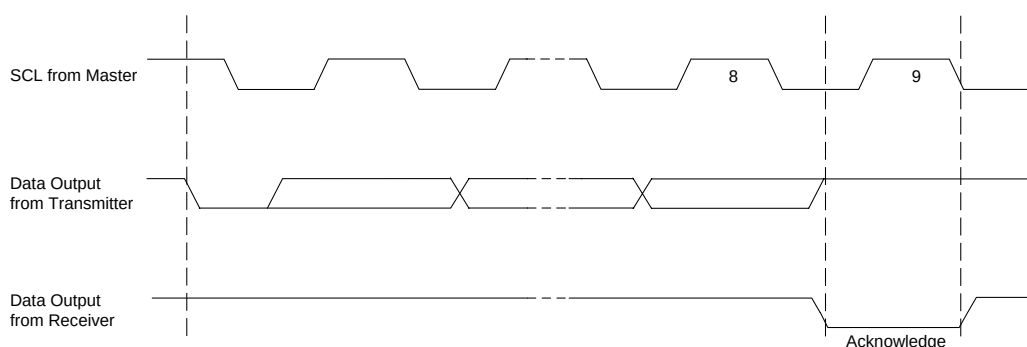
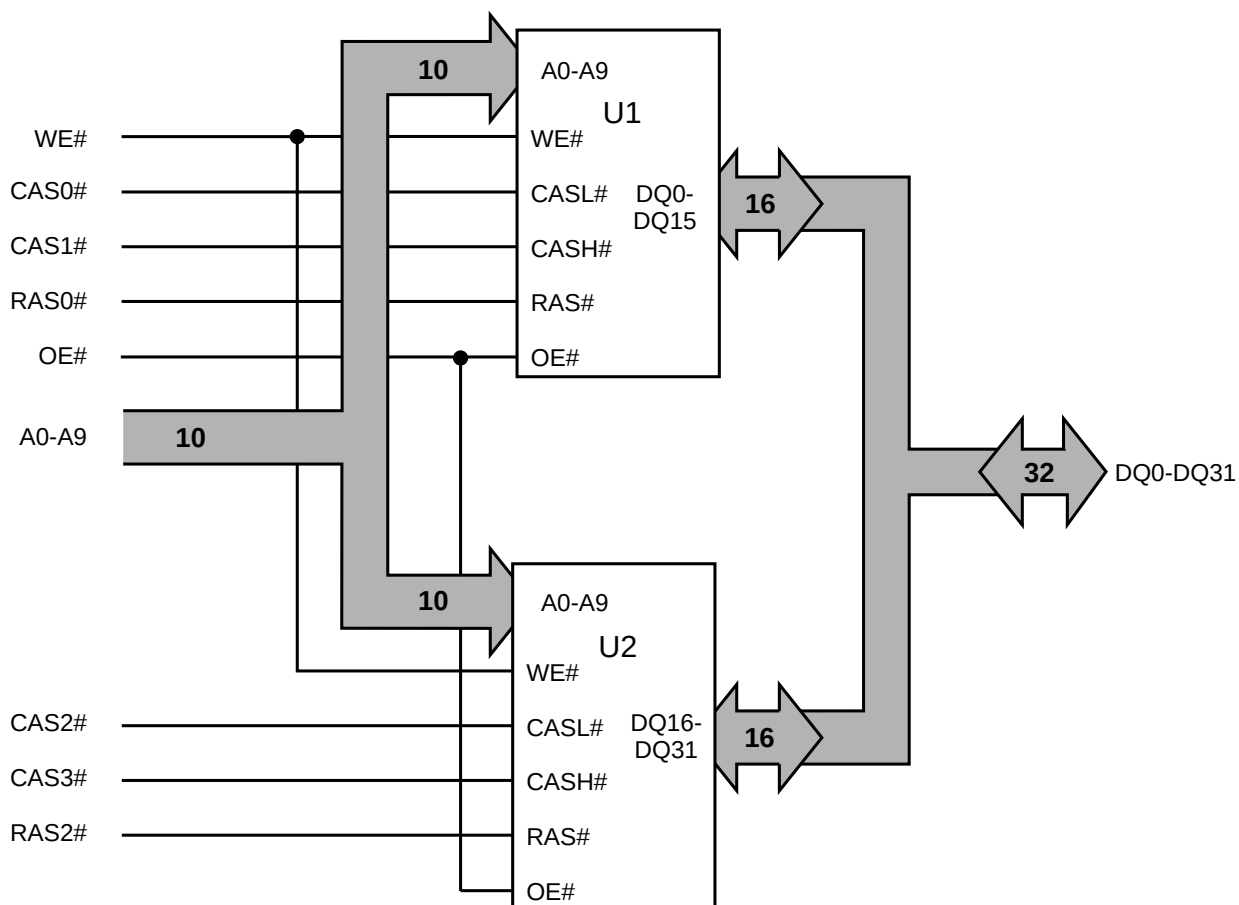


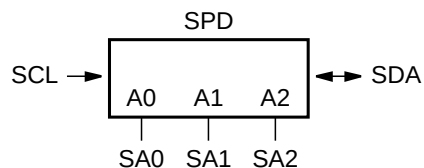
Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER

FUNCTIONAL BLOCK DIAGRAM MT2LD132U (4MB)



10 ohms
 DQn $\rightarrow$ Every DRAM DQ pin

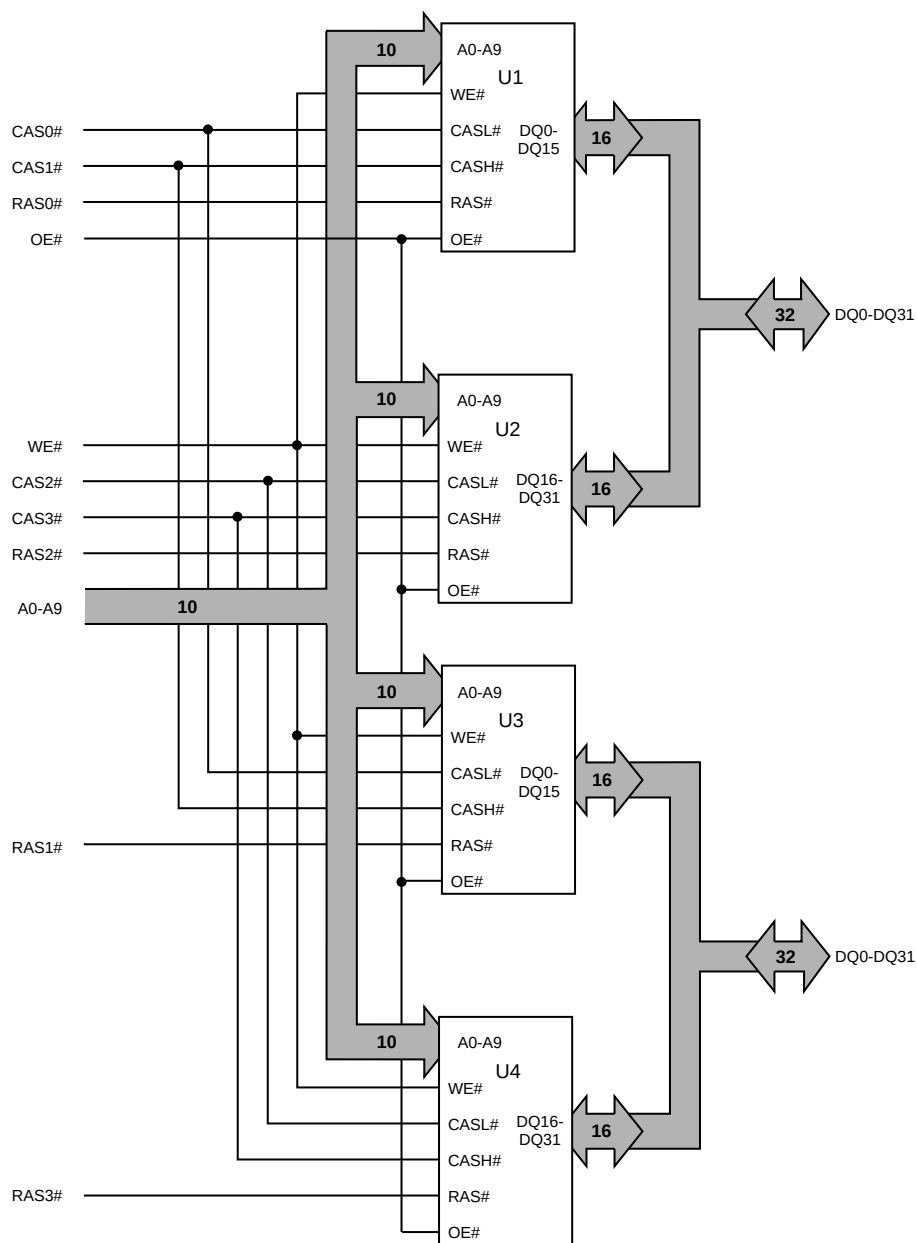
VDD $\rightarrow$ U1-U2
 VSS $\rightarrow$ U1-U2



U1-U2 = MT4LC1M16C3 FAST PAGE MODE

U1-U2 = MT4LC1M16E5 EDO PAGE MODE

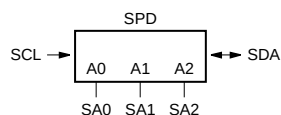
FUNCTIONAL BLOCK DIAGRAM MT4LD232U (8MB)



10 ohms
 DQn ———→ Every DRAM DQ pin

V_{DD} ———→ U1-U4

V_{SS} ———→ U1-U4



U1-U4 = MT4LC1M16C3 FAST PAGE MODE

U1-U4 = MT4LC1M16E5 EDO PAGE MODE

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	NUMBER OF BYTES USED BY MICRON	128	1	0	0	0	0	0	0	0	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	0	0	0	0	1	0	0	0	08
2	MEMORY TYPE	FAST PAGE MODE	0	0	0	0	0	0	0	1	01
		EDO PAGE MODE	0	0	0	0	0	0	1	0	02
3	NUMBER OF ROW ADDRESSES	10	0	0	0	0	1	0	1	0	0A
4	NUMBER OF COLUMN ADDRESSES	10	0	0	0	0	1	0	1	0	0A
5	NUMBER OF BANKS	1 (4MB)	0	0	0	0	0	0	0	1	01
		2 (8MB)	0	0	0	0	0	0	1	0	02
6	MODULE DATA WIDTH	x32	0	0	1	0	0	0	0	0	20
7	MODULE DATA WIDTH (continued)	0	0	0	0	0	0	0	0	0	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL	0	0	0	0	0	0	0	1	01
9	RAS# ACCESS TIME (t _{RAC})	50ns (-5)	0	0	1	1	0	0	1	0	32
		60ns (-6)	0	0	1	1	1	1	0	0	3C
10	CAS# ACCESS TIME (t _{CAC})	15ns	0	0	0	0	1	1	1	1	0F
11	MODULE CONFIGURATION TYPE	NONPARITY	0	0	0	0	0	0	0	0	00
12	REFRESH RATE/TYPE 15.6μs	NORMAL	0	0	0	0	0	0	0	0	00
13	DRAM WIDTH (PRIMARY DRAM)	x16	0	0	0	1	0	0	0	0	10
14	ERROR CHECKING DRAM DATA WIDTH	NONE	0	0	0	0	0	0	0	0	00
15-61	RESERVED		0	0	0	0	0	0	0	0	00
62	SPD REVISION	REV. 0	0	0	0	0	0	0	0	0	00
63	CHECKSUM FOR BYTES 0-62	4MB -5 (EDO)	0	0	0	1	0	0	0	1	11
		4MB -6 (EDO)	0	0	0	1	1	0	1	1	1B
		4MB -6 (FPM)	0	0	1	1	1	1	0	0	1C
		8MB -5 (EDO)	0	0	0	1	0	0	1	0	12
		8MB -6 (EDO)	0	0	0	1	1	1	0	0	1C
		8MB -6 (FPM)	0	0	0	1	1	1	0	1	1D
64	MANUFACTURER'S JEDEC ID CODE	MICRON	0	0	1	0	1	1	0	0	2C
65-71	MANUFACTURER'S JEDEC CODE (CONT.)		1	1	1	1	1	1	1	1	FF
72	MANUFACTURING LOCATION		0	0	0	0	0	0	0	1	01
			0	0	0	0	0	0	1	0	02
			0	0	0	0	0	0	1	1	03
			0	0	0	0	0	1	0	0	04
73-90	MODULE PART NUMBER (ASCII)		x	x	x	x	x	x	x	x	xx
91	PCB IDENTIFICATION CODE	1	0	0	0	0	0	0	0	1	01
		2	0	0	0	0	0	0	1	0	02
		3	0	0	0	0	0	0	1	1	03
		4	0	0	0	0	0	1	0	0	04
92	IDENTIFICATION CODE (CONT.)	0	0	0	0	0	0	0	0	0	00
93	YEAR OF MANUFACTURE IN BCD		x	x	x	x	x	x	x	x	xx
94	WEEK OF MANUFACTURE IN BCD		x	x	x	x	x	x	x	x	xx
95-98	MODULE SERIAL NUMBER		x	x	x	x	x	x	x	x	xx
99-125	MANUFACTURE SPECIFIC DATA (RSVD)		—	—	—	—	—	—	—	—	—

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} -1V to +4.6V

Voltage on Inputs or I/O Pins

Relative to V_{SS} -1V to +4.6V

Operating Temperature, T_A (ambient) 0°C to +70°C

Storage Temperature (plastic) -55°C to +125°C

Power Dissipation 4W

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V _{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V _{IH}	2	V _{DD} + 0.3	V	30
INPUT LOW VOLTAGE: Logic 0; All inputs		V _{IL}	-0.5	0.8	V	30
INPUT LEAKAGE CURRENT: Any input 0V ≤ V _{IN} ≤ V _{DD} + 0.3V (All other pins not under test = 0V)	RAS0#-RAS3#	I _{I1}	-2	2	μA	
	A0-A9, WE#, OE#	I _{I2}	-8	8	μA	23
	CAS0#-CAS3#	I _{I3}	-4	4	μA	23
OUTPUT LEAKAGE CURRENT: DQ is disabled; 0V ≤ V _{OUT} ≤ V _{DD} + 0.3V	DQ0-DQ31	I _{OZ}	-10	10	μA	23
OUTPUT LEVELS: Output High Voltage (I _{OUT} = -2mA) Output Low Voltage (I _{OUT} = 2mA)	V _{OH}		2.4	—	V	
	V _{OL}		—	0.4	V	

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

 (Notes: 1, 5, 6) ($V_{DD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX		UNITS	NOTES
			-5*	-6		
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I _{CC1}	4MB 8MB	2 4	2 4	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# = $V_{DD} - 0.2V$)	I _{CC2}	4MB 8MB	1 2	1 2	mA	26
OPERATING CURRENT: Random READ/WRITE; Average power supply current; (RAS#, CAS#, address cycling: $t_{RC} = t_{RC} [MIN]$)	I _{CC3}	4MB 8MB	360 362	340 342	mA	3, 22
OPERATING CURRENT: FAST PAGE MODE; Average power supply current; (RAS# = V_{IL} , CAS#, address cycling: $t_{PC} = t_{PC} [MIN]$; t_{CP} , $t_{ASC} = 10ns$)	I _{CC4}	4MB 8MB	– –	180 182	mA	3, 22
OPERATING CURRENT: EDO PAGE MODE; Average power supply current; (RAS# = V_{IL} , CAS#, address cycling: $t_{PC} = t_{PC} [MIN]$)	I _{CC5} (X only)	4MB 8MB	280 282	260 262	mA	3, 22
REFRESH CURRENT: RAS#-ONLY; Average power supply current; (RAS# cycling, CAS# = V_{IH} : $t_{RC} = t_{RC} [MIN]$)	I _{CC6}	4MB 8MB	360 362	340 342	mA	3, 22
REFRESH CURRENT: CBR; Average power supply current; (RAS#, CAS#, address cycling: $t_{RC} = t_{RC} [MIN]$)	I _{CC7}	4MB 8MB	360 362	340 342	mA	3, 4

* EDO version only

CAPACITANCE

PARAMETER	SYMBOL	MAX		UNITS	NOTES
		4MB	8MB		
Input Capacitance: A0-A9	C _{I1}	14	24	pF	2
Input Capacitance: WE#, OE#	C _{I2}	18	32	pF	2
Input Capacitance: CAS0#-CAS3#	C _{I3}	10	18	pF	2
Input Capacitance: RAS0#-RAS3#, SCL, SA0-SA2	C _{I4}	10	10	pF	2
Input/Output Capacitance: DQ0-DQ31, SDA	C _{IO}	10	18	pF	2

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

 (Notes: 5, 6, 7, 8, 9, 12, 19) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Access time from column address	t_{AA}		30	ns	
Column-address hold time (referenced to RAS#)	t_{AR}	45		ns	
Column-address setup time	t_{ASC}	0		ns	
Row-address setup time	t_{ASR}	0		ns	
Column address to WE# delay time	t_{AWD}	55		ns	27
Access time from CAS#	t_{CAC}		15	ns	
Column-address hold time	t_{CAH}	10		ns	
CAS# pulse width	t_{CAS}	15	10,000	ns	
CAS# hold time (CBR Refresh)	t_{CHR}	10		ns	4
CAS# to output in Low-Z	t_{CLZ}	3		ns	21
CAS# precharge time	t_{CP}	10		ns	13
Access time from CAS# precharge	t_{CPA}		35	ns	
CAS# to RAS# precharge time	t_{CRP}	5		ns	
CAS# hold time	t_{CSH}	60		ns	
CAS# setup time (CBR Refresh)	t_{CSR}	5		ns	
CAS# to WE# delay time	t_{CWD}	40		ns	27
WRITE command to CAS# lead time	t_{CWL}	15		ns	
Data-in hold time	t_{DH}	10		ns	18
Data-in setup time	t_{DS}	0		ns	18
Output disable	t_{OD}	3	15	ns	
Output enable	t_{OE}		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t_{OEh}	15		ns	28
Output buffer turn-off delay	t_{OFF}	3	15	ns	17, 24
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t_{ORD}	0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	35		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PRWC}	85		ns	
Access time from RAS#	t_{RAC}		60	ns	
RAS# to column-address delay time	t_{RAD}	15		ns	15
Row-address hold time	t_{RAH}	10		ns	
RAS# pulse width	t_{RAS}	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	t_{RASP}	60	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	110		ns	

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

 (Notes: 5, 6, 7, 8, 9, 12, 19) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
RAS# to CAS# delay time	t_{RCD}	20		ns	14
READ command hold time (referenced to CAS#)	t_{RCH}	0		ns	16
READ command setup time	t_{RCS}	0		ns	
Refresh period (1,024 cycles)	t_{REF}		16	ms	
RAS# precharge time	t_{RP}	40		ns	
RAS# to CAS# precharge time	t_{RPC}	0		ns	
READ command hold time (referenced to RAS#)	t_{RRH}	0		ns	16
RAS# hold time	t_{RSH}	15		ns	
READ-WRITE cycle time	t_{RWC}	155		ns	
RAS# to WE# delay time	t_{RWD}	85		ns	27
WRITE command to RAS# lead time	t_{RWL}	15		ns	
Transition time (rise or fall)	t_T	2	50	ns	
WRITE command hold time	t_{WCH}	10		ns	
WRITE command hold time (referenced to RAS#)	t_{WCR}	45		ns	
WE# command setup time	t_{WCS}	0		ns	27
WRITE command pulse width	t_{WP}	10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	10		ns	
WE# setup time (CBR Refresh)	t_{WRP}	10		ns	

EDO PAGE MODE

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 19) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
Access time from column address	t_{AA}		25		30	ns	
Column-address setup to CAS# precharge	t_{ACH}	12		15		ns	
Column-address hold time (referenced to RAS#)	t_{AR}	38		45		ns	
Column-address setup time	t_{ASC}	0		0		ns	
Row-address setup time	t_{ASR}	0		0		ns	
Column address to WE# delay time	t_{AWD}	42		49		ns	27
Access time from CAS#	t_{CAC}		15		15	ns	
Column-address hold time	t_{CAH}	8		10		ns	
CAS# pulse width	t_{CAS}	8	10,000	10	10,000	ns	
CAS# hold time (CBR Refresh)	t_{CHR}	8		10		ns	4
CAS# to output in Low-Z	t_{CLZ}	0		0		ns	
Data output hold after next CAS# LOW	t_{COH}	3		3		ns	
CAS# precharge time	t_{CP}	8		10		ns	13
Access time from CAS# precharge	t_{CPA}		28		35	ns	
CAS# to RAS# precharge time	t_{CRP}	5		5		ns	
CAS# hold time	t_{CSH}	38		45		ns	
CAS# setup time (CBR Refresh)	t_{CSR}	5		5		ns	
CAS# to WE# delay time	t_{CWD}	28		35		ns	27
WRITE command to CAS# lead time	t_{CWL}	8		10		ns	
Data-in hold time	t_{DH}	8		10		ns	18
Data-in setup time	t_{DS}	0		0		ns	18
Output disable	t_{OD}	0	12	0	15	ns	
Output enable	t_{OE}		12		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t_{OEHL}	8		10		ns	28
OE# HIGH hold from CAS# HIGH	t_{OEHC}	5		10		ns	28
OE# HIGH pulse width	t_{OEP}	5		5		ns	
OE# LOW to CAS# HIGH setup time	t_{OES}	4		5		ns	
Output buffer turn-off delay	t_{OFF}	0	12	0	15	ns	17, 24

EDO PAGE MODE

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 19) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t_{ORD}	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	20		25		ns	
EDO-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	47		56		ns	
Access time from RAS#	t_{RAC}		50		60	ns	
RAS# to column-address delay time	t_{RAD}	9		12		ns	15
Row-address hold time	t_{RAH}	9		10		ns	
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	t_{RASP}	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	84		104		ns	
RAS# to CAS# delay time	t_{RCD}	11		14		ns	14
READ command hold time (referenced to CAS#)	t_{RCH}	0		0		ns	16
READ command setup time	t_{RCS}	0		0		ns	
Refresh period (1,024 cycles)	t_{REF}		16		16	ms	
RAS# precharge time	t_{RP}	30		40		ns	
RAS# to CAS# precharge time	t_{RPC}	5		5		ns	
READ command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	16
RAS# hold time	t_{RSH}	13		15		ns	
READ-WRITE cycle time	t_{RWC}	116		140		ns	
RAS# to WE# delay time	t_{RWD}	67		79		ns	27
WRITE command to RAS# lead time	t_{RWL}	13		15		ns	
Transition time (rise or fall)	t_T	2	50	2	50	ns	
WRITE command hold time	t_{WCH}	8		10		ns	
WRITE command hold time (referenced to RAS#)	t_{WCR}	38		45		ns	
WE# command setup time	t_{WCS}	0		0		ns	27
Output disable delay from WE#	t_{WHZ}	0	12	0	15	ns	
WRITE command pulse width	t_{WP}	5		5		ns	
WE# pulse to disable at CAS# HIGH	t_{WPZ}	10		10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	8		10		ns	
WE# setup time (CBR Refresh)	t_{WRP}	8		10		ns	

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Notes: 1) ($V_{DD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DD} \times 0.7$	$V_{DD} + 0.5$	V	
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DD} \times 0.3$	V	
OUTPUT LOW VOLTAGE: $I_{OUT} = 3mA$	V_{OL}	—	0.4	V	
INPUT LEAKAGE CURRENT: $V_{IN} = GND$ to V_{DD}	I_{LI}	—	10	μA	
OUTPUT LEAKAGE CURRENT: $V_{OUT} = GND$ to V_{DD}	I_{LO}	—	10	μA	
STANDBY CURRENT: SCL = SDA = $V_{DD} - 0.3V$; All other inputs = GND or $3.3V + 10\%$	I_{SB}	—	30	μA	
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	—	2	mA	

SERIAL PRESENCE-DETECT EEPROM AC ELECTRICAL CHARACTERISTICS

(Notes: 1) ($V_{DD} = +3.3V \pm 0.3V$)

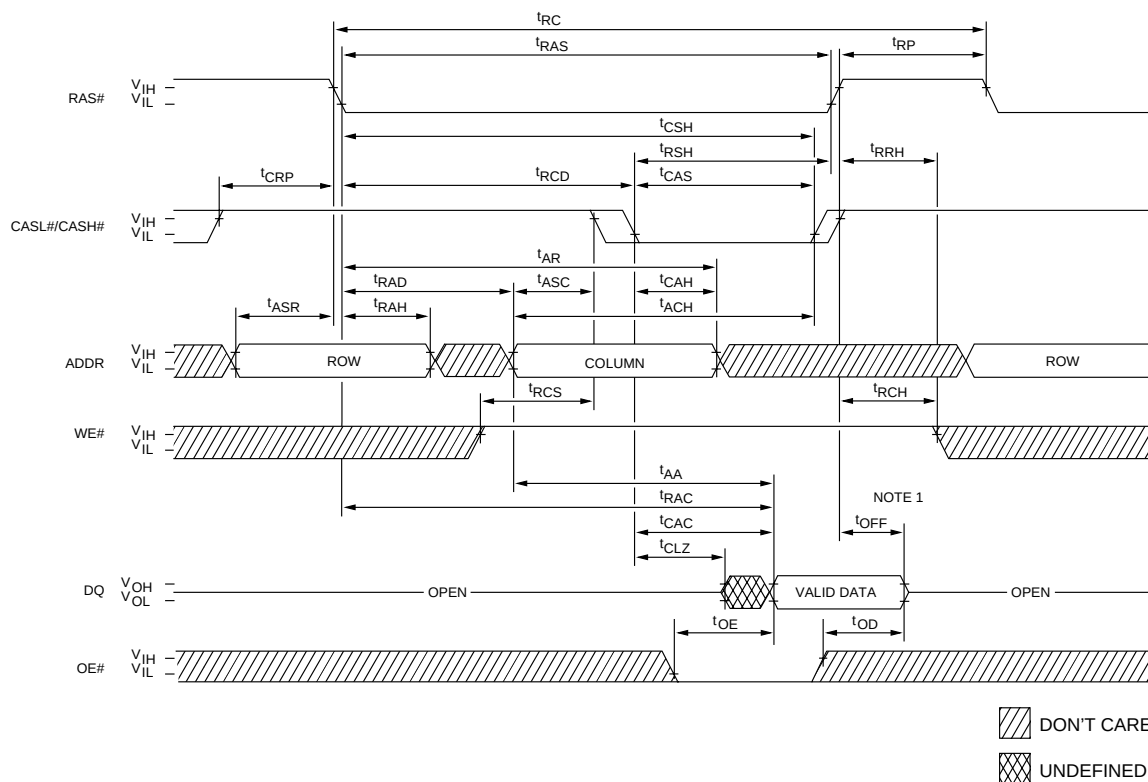
PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	t_{AA}	0.3	3.5	μs	
Time the bus must be free before a new transition can start	t_{BUF}	4.7		μs	
Data-out hold time	t_{DH}	300		ns	
SDA and SCL fall time	t_F		300	ns	
Data-in hold time	$t_{HD:DAT}$	0		μs	
Start condition hold time	$t_{HD:STA}$	4		μs	
Clock HIGH period	t_{HIGH}	4		μs	
Noise suppression time constant at SCL, SDA inputs	t_I		100	ns	
Clock LOW period	t_{LOW}	4.7		μs	
SDA and SCL rise time	t_R		1	μs	
SCL clock frequency	f_{SCL}		100	KHz	
Data-in setup time	$t_{SU:DAT}$	250		ns	
Start condition setup time	$t_{SU:STA}$	4.7		μs	
Stop condition setup time	$t_{SU:STO}$	4.7		μs	
WRITE cycle time	t_{WRC}		10	ms	29

NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{DD} = +3.3V$; $f = 1\text{ MHz}$.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of $100\mu s$ is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 5ns$ for FPM and $t_T = 2.5ns$ for EDO.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH} , data output is High-Z.
11. If CAS# = V_{IL} , data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and $100pF$ and $V_{OL} = 0.8V$ and $V_{OH} = 2V$.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for t_{CP} .
14. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} (MAX) limit, t_{AA} and t_{CAC} must always be met.
15. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA} , t_{RAC} and t_{CAC} must always be met.
16. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
17. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
18. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
19. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, with EDO, WE# must be pulsed during CAS# HIGH time in order to place I/O buffers in High-Z.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. The $3ns$ minimum is a parameter guaranteed by design.
22. Column address changed once each cycle.
23. 4MB module values will be half of those shown.
24. With the FPM option, t_{OFF} is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, t_{OFF} on an EDO option is determined by the latter of the RAS# and CAS# signals to transition HIGH.
25. Applies to both FPM and EDO operating modes.
26. All other inputs at $0.2V$ or $V_{DD} - 0.2V$.
27. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. t_{RWD} , t_{AWD} and t_{CWD} apply to READ-MODIFY-WRITE cycles. If $t_{WCS} \geq t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{WCS} < t_{WCS}$ (MIN) and $t_{RWD} \geq t_{RWD}$ (MIN), $t_{AWD} \geq t_{AWD}$ (MIN) and $t_{CWD} \geq t_{CWD}$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not applicable in a LATE WRITE cycle.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OE} met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after t_{OE} is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.

NOTES (continued)

29. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase / program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
30. V_{IH} overshoot: $V_{IH} (MAX) = V_{DD} + 2V$ for a pulse width $\leq 10ns$, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: $V_{IL} (MIN) = -2V$ for a pulse width $\leq 10ns$, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE ²⁵

**FAST PAGE MODE AND EDO PAGE MODE
 TIMING PARAMETERS**

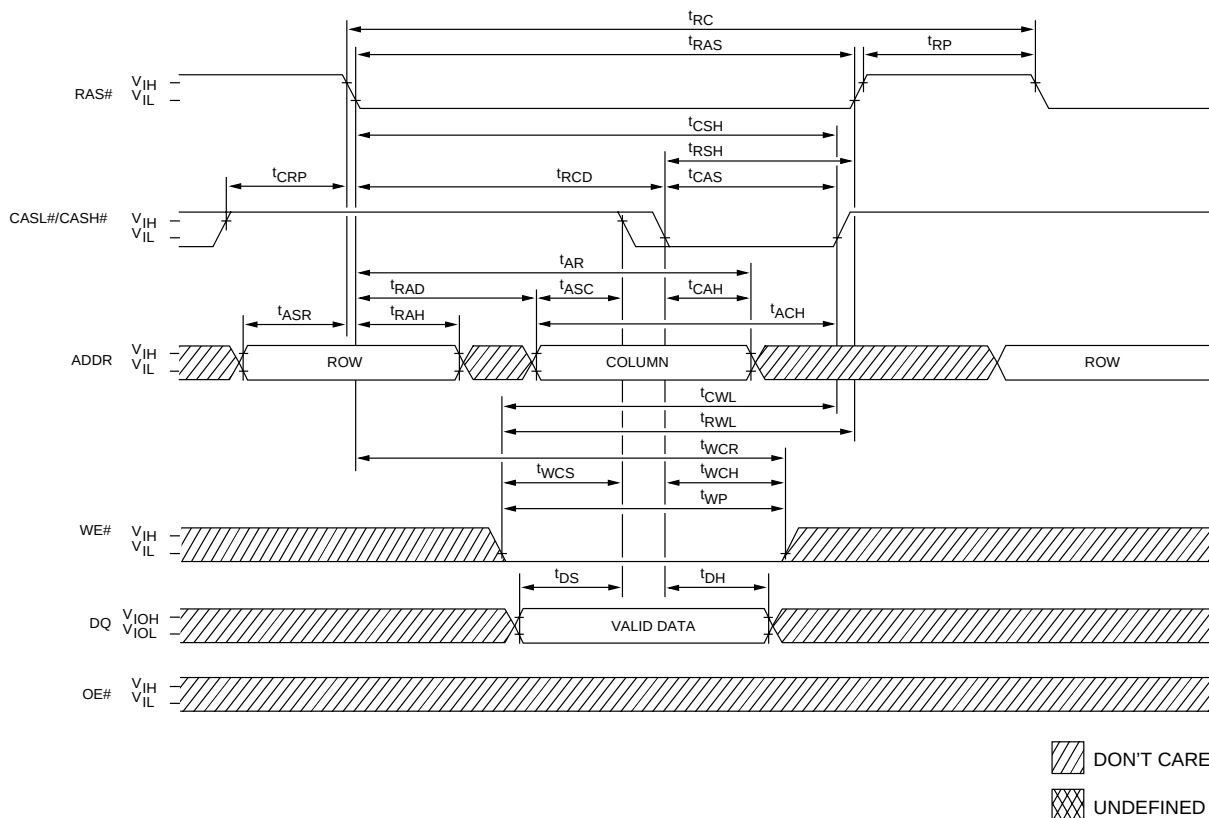
SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{ACH} (EDO)	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		15		15	ns
t_{CAH}	8		10		ns
t_{CAS} (EDO)	8	10,000	10	10,000	ns
t_{CAS} (FPM)	—	—	15	10,000	ns
t_{CLZ} (EDO)	0		0		ns
t_{CLZ} (FPM)	—		3		ns
t_{CRP}	5		5		ns
t_{CSH} (EDO)	38		45		ns
t_{CSH} (FPM)	—		60		ns
t_{OD} (EDO)	0	12	0	15	ns
t_{OD} (FPM)	—	—	3	15	ns
t_{OE}		12		15	ns

*EDO version only

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{OFF} (EDO)	0	12	0	15	ns
t_{OFF} (FPM)	—	—	3	15	ns
t_{RAC}		50		60	ns
t_{RAD} (EDO)	9		12		ns
t_{RAD} (FPM)	—		15		ns
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC} (EDO)	84		104		ns
t_{RC} (FPM)	—		110		ns
t_{RCD} (EDO)	11		14		ns
t_{RCD} (FPM)	—		20		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RRH}	0		0		ns
t_{RSH}	13		15		ns

NOTE: 1. For EDO, t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs last. For FPM, t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs first.

EARLY WRITE CYCLE ²⁵



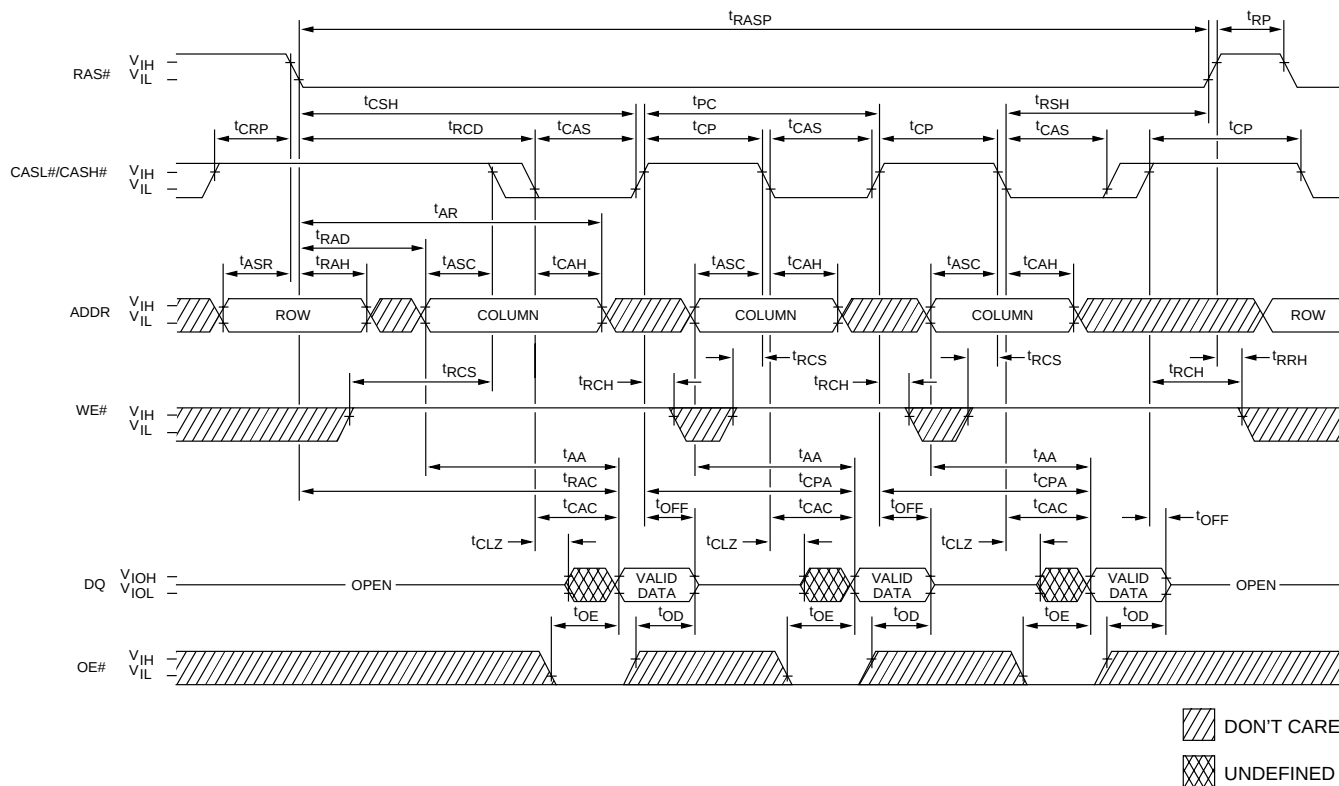
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
^t ACH (EDO)	12		15		ns
^t AR	38		45		ns
^t ASC	0		0		ns
^t ASR	0		0		ns
^t CAH	8		10		ns
^t CAS (FPM)	–	–	15	10,000	ns
^t CAS (EDO)	8	10,000	10	10,000	ns
^t CRP	5		5		ns
^t CSH (FPM)	–		60		ns
^t CSH (EDO)	38		45		ns
^t CWL (FPM)	–		15		ns
^t CWL (EDO)	8		10		ns
^t DH	8		10		ns
^t DS	0		0		ns
^t RAD (FPM)	–		15		ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
^t RAD (EDO)	9		12		ns
^t RAH	9		10		ns
^t RAS	50	10,000	60	10,000	ns
^t RC (FPM)	–		110		ns
^t RC (EDO)	84		104		ns
^t RCD (FPM)	–		20		ns
^t RCD (EDO)	11		14		ns
^t RP	30		40		ns
^t RSH	13		15		ns
^t RWL	13		15		ns
^t WCH	8		10		ns
^t WCR	38		45		ns
^t WCS	0		0		ns
^t WP (FPM)	–		10		ns
^t WP (EDO)	5		5		ns

*EDO version only

FAST-PAGE-MODE READ CYCLE

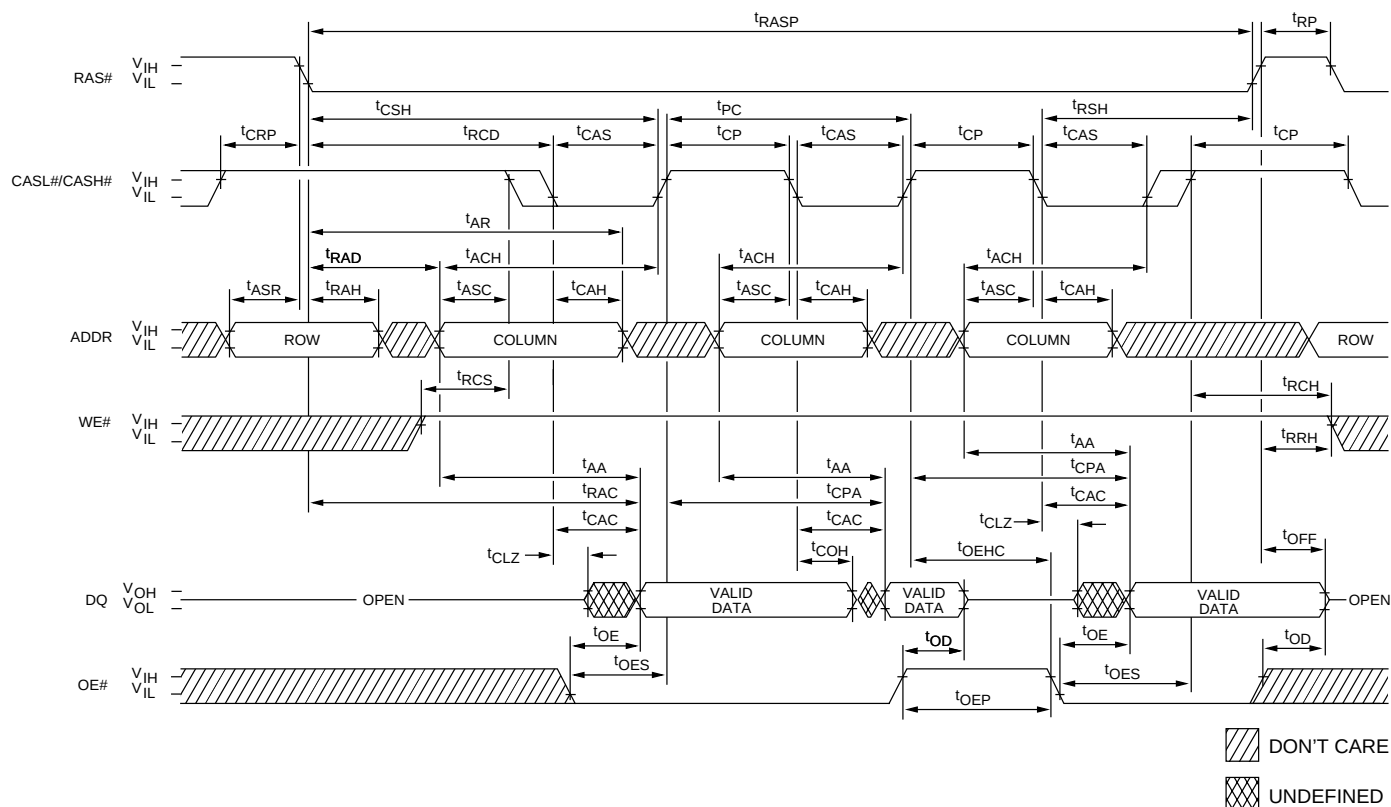


FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6		UNITS
	MIN	MAX	
^t AA		30	ns
^t AR	45		ns
^t ASC	0		ns
^t ASR	0		ns
^t CAC		15	ns
^t CAH	10		ns
^t CAS	15	10,000	ns
^t CLZ	3		ns
^t CP	10		ns
^t CPA		35	ns
^t CRP	5		ns
^t CSH	60		ns
^t OD	3	15	ns

SYMBOL	-6		UNITS
	MIN	MAX	
^t OE		15	ns
^t OFF	3	15	ns
^t PC	35		ns
^t RAC		60	ns
^t RAD	15		ns
^t RAH	10		ns
^t RASP	60	125,000	ns
^t RCD	20		ns
^t RCH	0		ns
^t RCS	0		ns
^t RP	40		ns
^t RRH	0		ns
^t RSH	15		ns

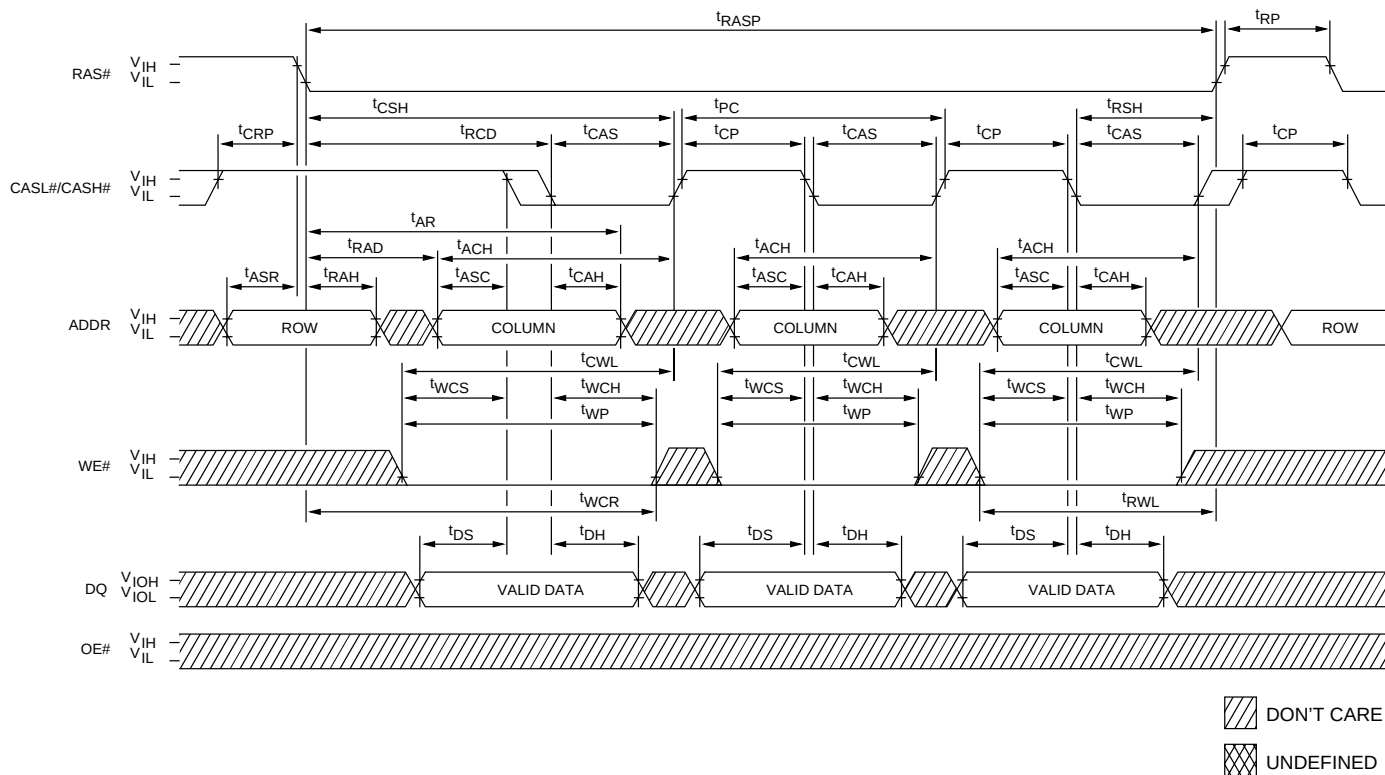
EDO-PAGE-MODE READ CYCLE



EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		15		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{COH}	3		3		ns
t_{CP}	8		10		ns
t_{CPA}		28		35	ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{OD}	0	12	0	15	ns
t_{OE}		12		15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{OEHC}	5		10		ns
t_{OEP}	5		5		ns
t_{OES}	4		5		ns
t_{OFF}	0	12	0	15	ns
t_{PC}	20		25		ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RASP}	50	125,000	60	125,000	ns
t_{RCD}	11		14		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RRH}	0		0		ns
t_{RSH}	13		15		ns

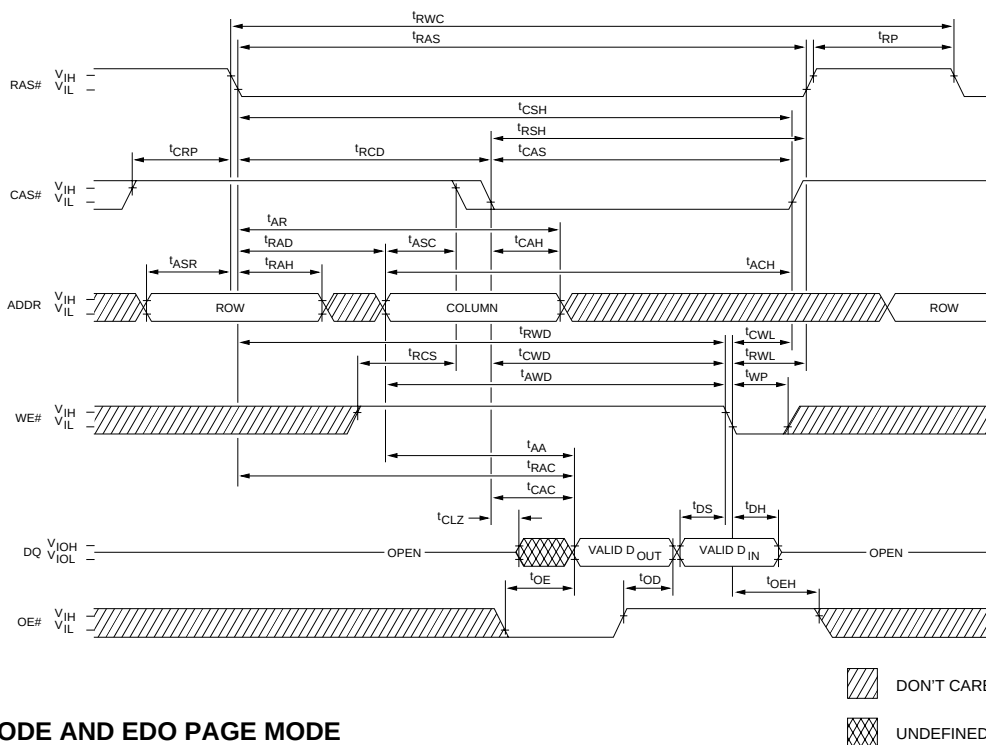
FAST/EDO-PAGE-MODE EARLY WRITE CYCLE ²⁵

**FAST PAGE MODE AND EDO PAGE MODE
 TIMING PARAMETERS**

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{ACH} (EDO)	12		15		ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAH}	8		10		ns
t _{CAS} (EDO)	8	10,000	10	10,000	ns
t _{CAS} (FPM)	—	—	15	10,000	ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSH} (EDO)	38		45		ns
t _{CSH} (FPM)	—		60		ns
t _{CWL} (EDO)	8		10		ns
t _{CWL} (FPM)	—		15		ns
t _{DH}	8		10		ns
t _{DS}	0		0		ns
t _{PC} (EDO)	20		25		ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{PC} (FPM)	—		35		ns
t _{RAD} (EDO)	9		12		ns
t _{RAD} (FPM)	—		15		ns
t _{RAH}	9		10		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD} (EDO)	11		14		ns
t _{RCD} (FPM)	—		20		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns
t _{RWL}	13		15		ns
t _{WCH}	8		10		ns
t _{WCR}	38		45		ns
t _{WCS}	0		0		ns
t _{WP} (EDO)	5		5		ns
t _{WP} (FPM)	—		10		ns

*EDO version only

READ-WRITE CYCLE ²⁵ (LATE WRITE and READ-MODIFY-WRITE cycles)



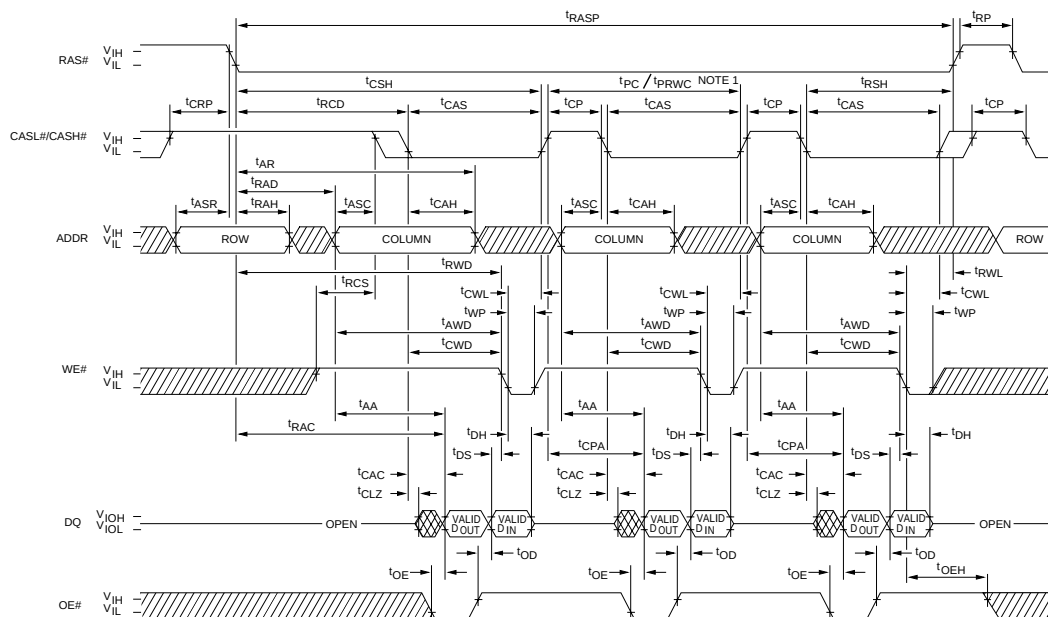
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{ACH} (EDO)	12		15		ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{AWD}	42		49		ns
t _{CAC}		15		15	ns
t _{CAH}	8		10		ns
t _{CAS} (EDO)	8	10,000	10	10,000	ns
t _{CAS} (FPM)	—	—	15	10,000	ns
t _{CLZ} (EDO)	0		0		ns
t _{CLZ} (FPM)	—		3		ns
t _{CRP}	5		5		ns
t _{CSH} (EDO)	38		45		ns
t _{CSH} (FPM)	—		60		ns
t _{CWD} (EDO)	28		35		ns
t _{CWD} (FPM)	—		40		ns
t _{CWL} (EDO)	8		10		ns
t _{CWL} (FPM)	—		15		ns
t _{DH}	8		10		ns
t _{DS}	0		0		ns
t _{OD} (EDO)	0	12	0	15	ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OD} (FPM)	—	—	3	15	ns
t _{OE}		12		15	ns
t _{OEH} (EDO)	8		10		ns
t _{OEH} (FPM)	—		15		ns
t _{RAC}		50		60	ns
t _{RAD} (EDO)	9		12		ns
t _{RAD} (FPM)	—		15		ns
t _{RAH}	9		10		ns
t _{RAS}	50	10,000	60	10,000	ns
t _{RCD} (EDO)	11		14		ns
t _{RCD} (FPM)	—		20		ns
t _{RCS}	0		0		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns
t _{RWC} (EDO)	116		140		ns
t _{RWC} (FPM)	—		155		ns
t _{RWD} (EDO)	67		79		ns
t _{RWD} (FPM)	—		85		ns
t _{RWL}	13		15		ns
t _{WP} (EDO)	5		5		ns
t _{WP} (FPM)	—		10		ns

*EDO version only

FAST/EDO-PAGE-MODE READ-WRITE CYCLE ²⁵ (LATE WRITE and READ-MODIFY-WRITE cycles)



 DON'T CARE

 UNDEFINED

FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

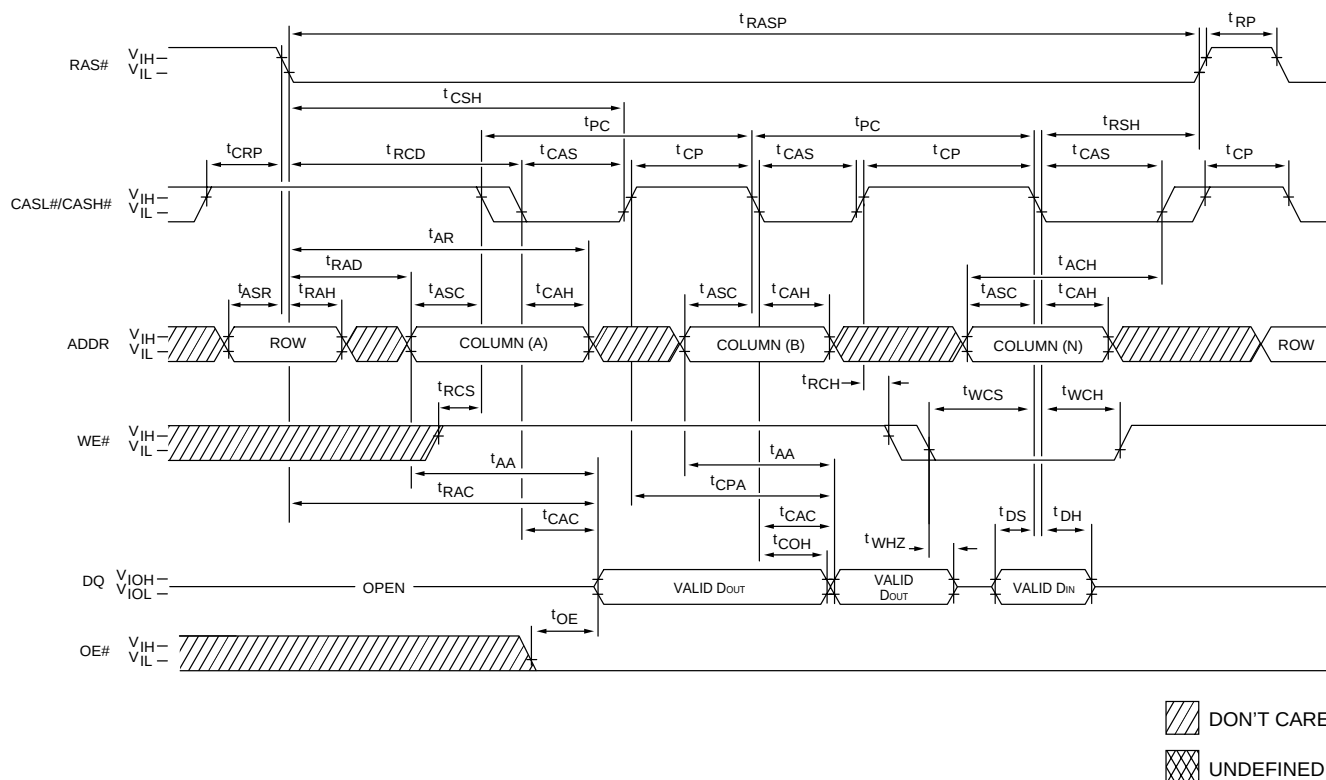
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	MIN	MAX	MIN	MAX	
^t AA		25		30	ns
^t AR	38		45		ns
^t ASC	0		0		ns
^t ASR	0		0		ns
^t AWD	42		49		ns
^t CAC		15		15	ns
^t CAH	8		10		ns
^t CAS (EDO)	8	10,000	10	10,000	ns
^t CAS (FPM)	–	–	15	10,000	ns
^t CLZ (EDO)	0		0		ns
^t CLZ (FPM)	–		3		ns
^t CP	8		10		ns
^t CPA		28		35	ns
^t CRP	5		5		ns
^t CSH (EDO)	38		45		ns
^t CSH (FPM)	–		60		ns
^t CWD (EDO)	28		35		ns
^t CWD (FPM)	–		40		ns
^t CWL (EDO)	8		10		ns
^t CWL (FPM)	–		15		ns
^t DH	8		10		ns
^t DS	0		0		ns
^t OD (EDO)	0	12	0	15	ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
^t OD (FPM)	—	—	3	15	ns
^t OE		12		15	ns
^t OEH (EDO)	8		10		ns
^t OEH (FPM)	—		15		ns
^t PC (EDO)	20		25		ns
^t PC (FPM)	—		35		ns
^t PRWC (EDO)	47		56		ns
^t PRWC (FPM)	—		85		ns
^t RAC		50		60	ns
^t RAD (EDO)	9		12		ns
^t RAD (FPM)	—		15		ns
^t RAH	9		10		ns
^t RASP	50	125,000	60	125,000	ns
^t RCD (EDO)	11		14		ns
^t RCD (FPM)	—		20		ns
^t RCS	0		0		ns
^t RP	30		40		ns
^t RSH	13		15		ns
^t RWD (EDO)	67		79		ns
^t RWD (FPM)	—		85		ns
^t RWL	13		15		ns
^t WP (EDO)	5		5		ns
^t WP (FPM)	—		10		ns

*EDO version only

NOTE: 1. ^tPC is for LATE WRITE cycles only.

EDO-PAGE-MODE READ EARLY WRITE CYCLE (Pseudo READ-MODIFY-WRITE)

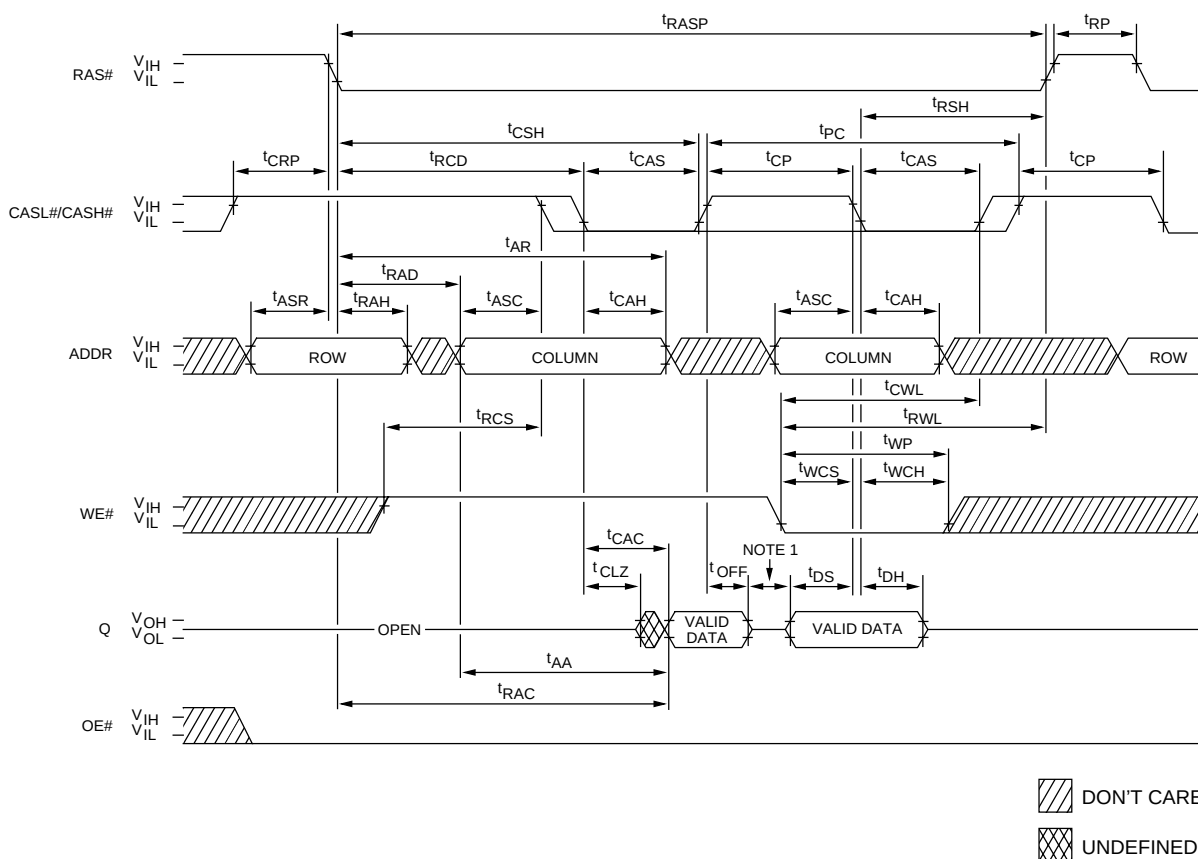


EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{ACH}	12		15		ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		15		15	ns
t _{CAH}	8		10		ns
t _{CAS}	8	10,000	10	10,000	ns
t _{COH}	3		3		ns
t _{CP}	8		10		ns
t _{CPA}		28		35	ns
t _{CRP}	5		5		ns
t _{CSH}	38		45		ns
t _{DH}	8		10		ns
t _{DS}	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OE}		12		15	ns
t _{PC}	20		25		ns
t _{RAC}		50		60	ns
t _{RAD}	9		12		ns
t _{RAH}	9		10		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD}	11		14		ns
t _{RCH}	0		0		ns
t _{RCS}	0		0		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns
t _{WCH}	8		10		ns
t _{WCS}	0		0		ns
t _{WHZ}	0	12	0	15	ns

FAST-PAGE-MODE READ EARLY WRITE CYCLE (Pseudo READ-MODIFY-WRITE)



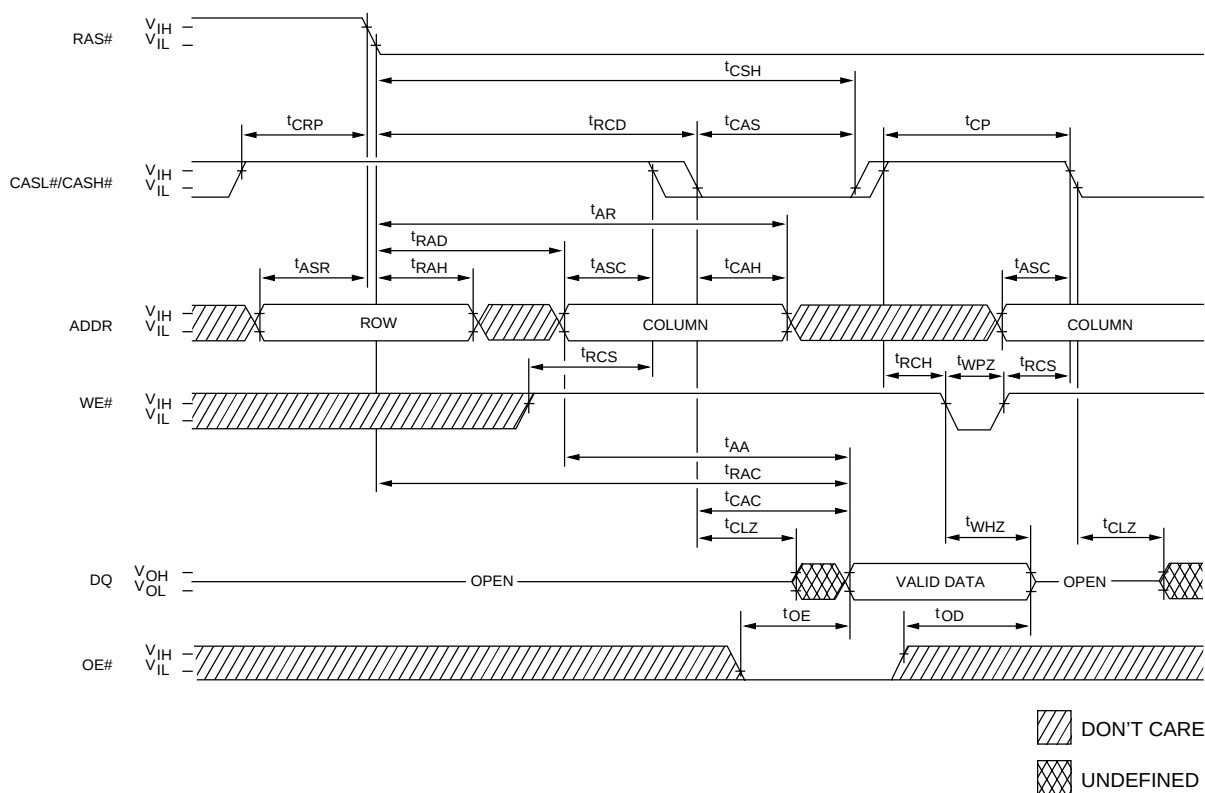
FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6		UNITS
	MIN	MAX	
t _{AA}		30	ns
t _{AR}	45		ns
t _{ASC}	0		ns
t _{ASR}	0		ns
t _{CAC}		15	ns
t _{CAH}	10		ns
t _{CAS}	15	10,000	ns
t _{CLZ}	3		ns
t _{CP}	10		ns
t _{CRP}	5		ns
t _{CSH}	60		ns
t _{CWL}	15		ns
t _{DH}	10		ns
t _{DS}	0		ns

SYMBOL	-6		UNITS
	MIN	MAX	
t _{OFF}	3	15	ns
t _{PC}	35		ns
t _{RAC}		60	ns
t _{RAD}	15		ns
t _{RAH}	10		ns
t _{RASP}	60	125,000	ns
t _{RCD}	20		ns
t _{RCS}	0		ns
t _{RP}	40		ns
t _{RSH}	15		ns
t _{RWL}	15		ns
t _{WCH}	10		ns
t _{WCS}	0		ns
t _{WP}	10		ns

NOTE: 1. Do not drive data prior to tristate.

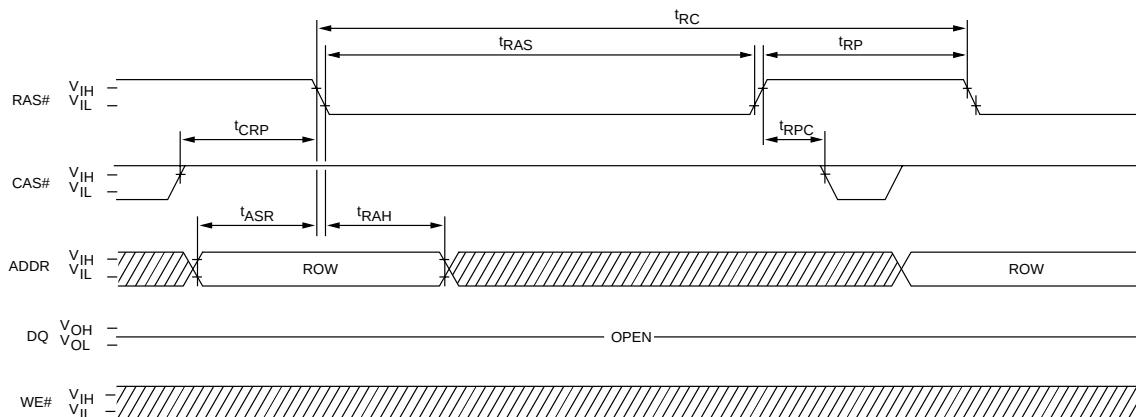
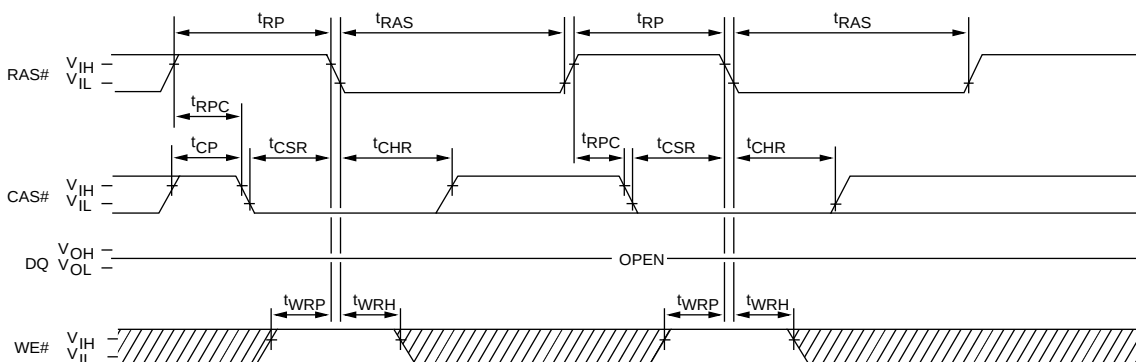
EDO READ CYCLE (with WE#-controlled disable)



EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		15		15	ns
t _{CAH}	8		10		ns
t _{CAS}	8	10,000	10	10,000	ns
t _{CLZ}	0		0		ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSH}	38		45		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OD}	0	12	0	15	ns
t _{OE}		12		15	ns
t _{RAC}		50		60	ns
t _{RAD}	9		12		ns
t _{RAH}	9		10		ns
t _{RCD}	11		14		ns
t _{RCH}	0		0		ns
t _{RCS}	0		0		ns
t _{WHZ}	0	12	0	15	ns
t _{WPZ}	10		10		ns

RAS#-ONLY REFRESH CYCLE ²⁵

CBR REFRESH CYCLE ²⁵
 (Addresses = DON'T CARE)


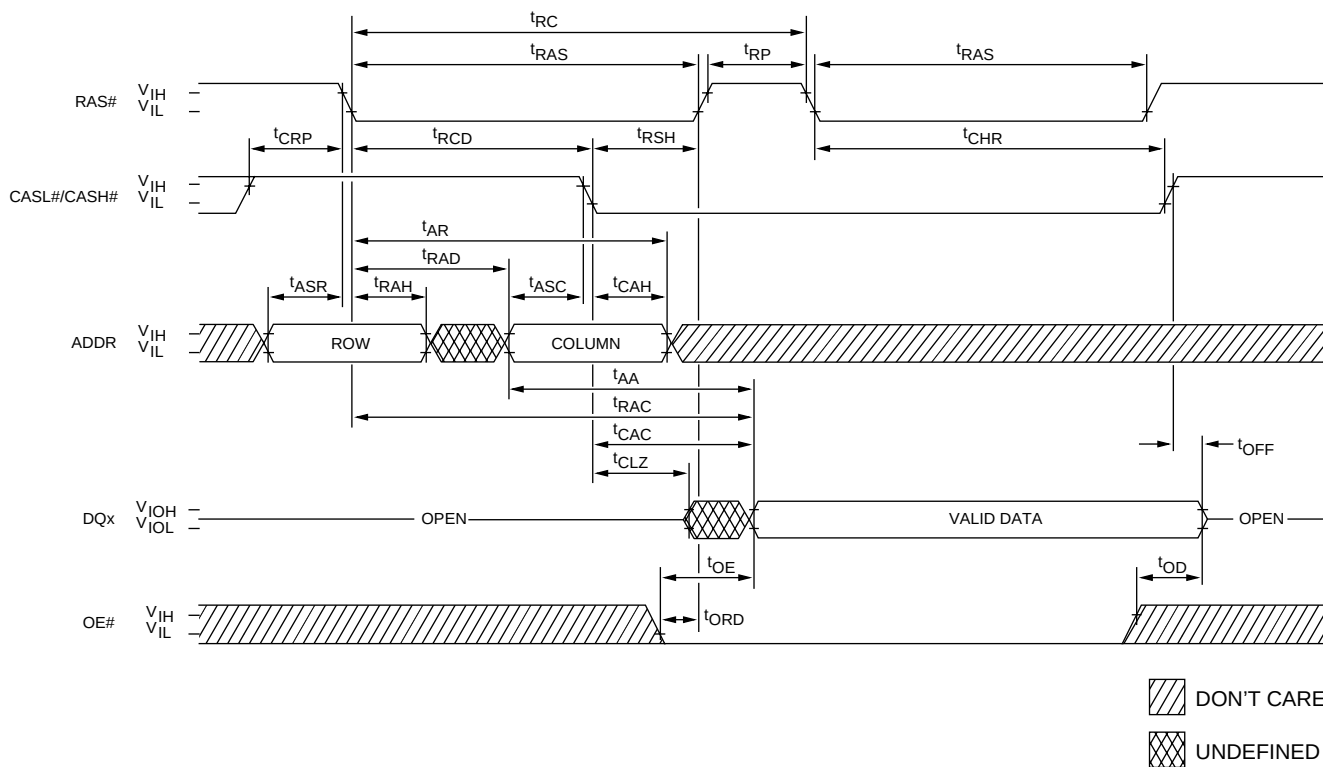
DON'T CARE
 UNDEFINED

**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{ASR}	0		0		ns
t _{CHR}	8		10		ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSR}	5		5		ns
t _{RAH}	9		10		ns
t _{RAS}	50	10,000	60	10,000	ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{RC} (FPM)	—		110		ns
t _{RC} (EDO)	84		104		ns
t _{RP}	30		40		ns
t _{RPC} (FPM)	—		0		ns
t _{RPC} (EDO)	5		5		ns
t _{WRH}	8		10		ns
t _{WRP}	8		10		ns

*EDO version only

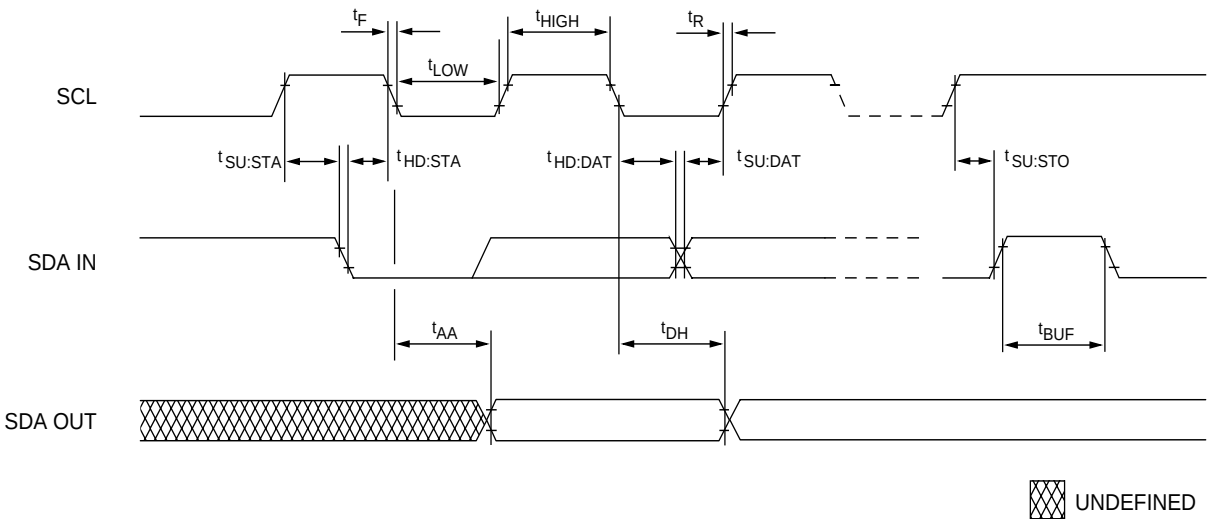
HIDDEN REFRESH CYCLE ^{20, 25}
 (WE# = HIGH)

**FAST PAGE MODE AND EDO PAGE MODE
 TIMING PARAMETERS**

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		15		15	ns
t _{CAH}	8		10		ns
t _{CHR}	8		10		ns
t _{CLZ} (FPM)	—		3		ns
t _{CLZ} (EDO)	0		0		ns
t _{CRP}	5		5		ns
t _{OD} (FPM)	—	—	3	15	ns
t _{OD} (EDO)	0	12	0	15	ns
t _{OE}		12		15	ns
t _{OFF} (FPM)	—	—	3	15	ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OFF} (EDO)	0	12	0	15	ns
t _{ORD}	0		0		ns
t _{RAC}		50		60	ns
t _{RAD} (FPM)	—		15		ns
t _{RAD} (EDO)	9		12		ns
t _{RAH}	9		10		ns
t _{RAS}	50	10,000	60	10,000	ns
t _{RC} (FPM)	—		110		ns
t _{RC} (EDO)	84		104		ns
t _{RCD} (FPM)	—		20		ns
t _{RCD} (EDO)	11		14		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns

*EDO version only

SPD EEPROM



**SERIAL PRESENCE-DETECT EEPROM
TIMING PARAMETERS**

SYMBOL	MIN	MAX	UNITS
t_{AA}	0.3	3.5	μ S
t_{BUF}	4.7		μ S
t_{DH}	300		ns
t_F		300	ns
$t_{HD:DAT}$	0		μ S
$t_{HD:STA}$	4		μ S

SYMBOL	MIN	MAX	UNITS
t_{HIGH}	4		μ S
t_{LOW}	4.7		μ S
t_R		1	μ S
$t_{SU:DAT}$	250		ns
$t_{SU:STA}$	4.7		μ S
$t_{SU:STO}$	4.7		μ S

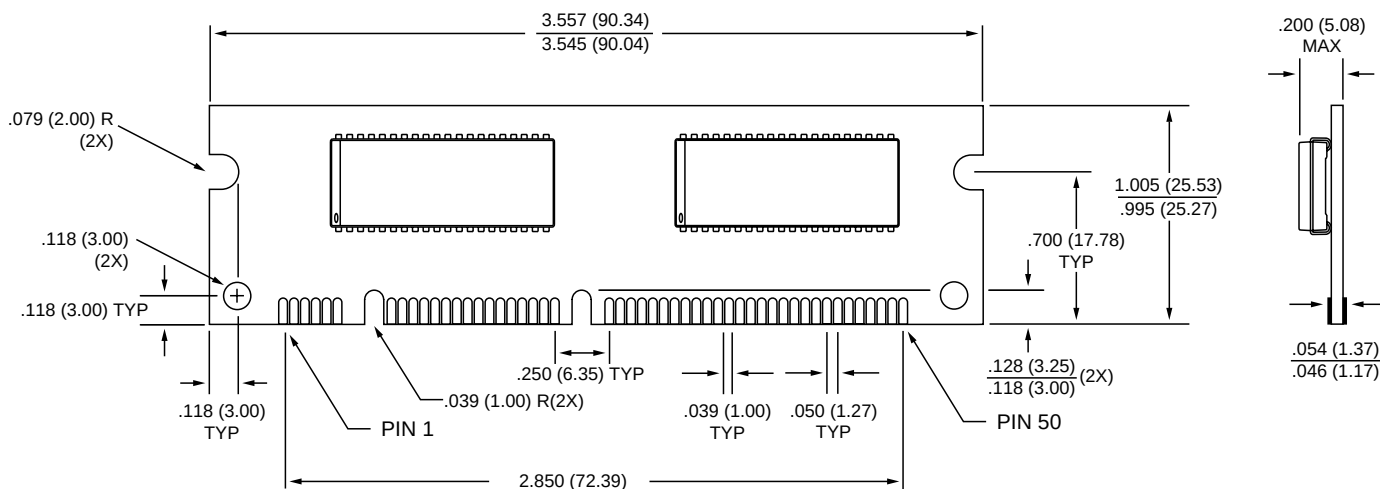
OBSOLETE

MICRON
TECHNOLOGY, INC.

**1, 2 MEG x 32
DRAM DIMMs**

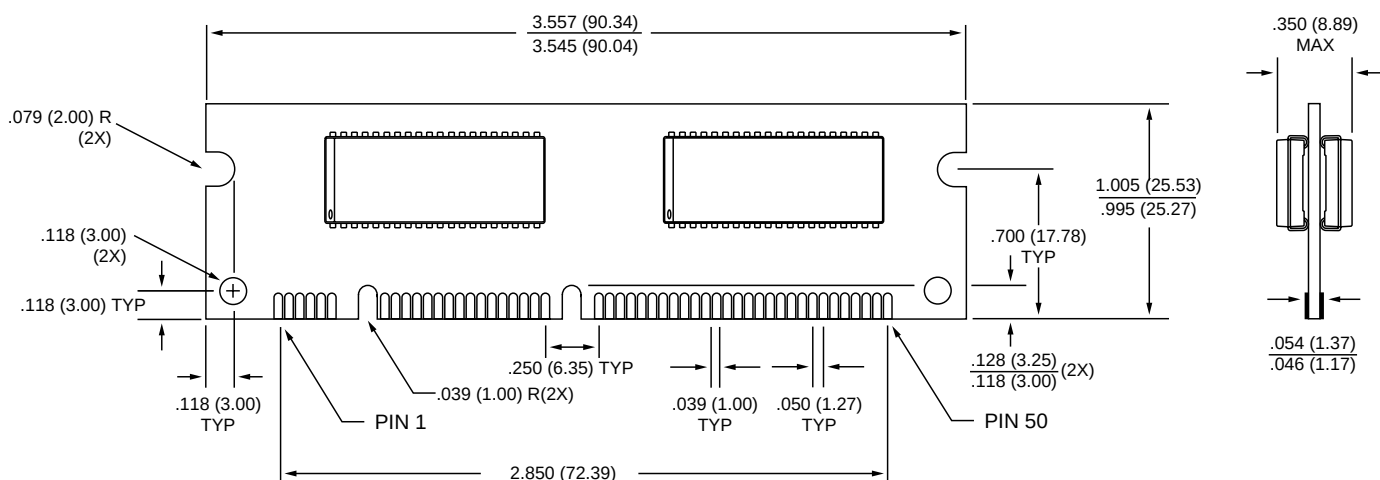
100-PIN DIMM

DF-1 (4MB)



100-PIN DIMM

DF-2 (8MB)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.