CM3202-02

DDR VDDQ and VTT Termination Voltage Regulator

ON Semiconductor®

http://onsemi.com

WDFN8
DE SUFFIX
CASE 511BH

MARKING DIAGRAM

CM320 202DE = CM3202−02DE

ORDERING INFORMATION

Device	Package	Shipping†
CM3202−02DE	WDFN8 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Product Description

The CM3202−02 is a dual−output low noise linear regulator designed to meet SSTL−2 and SSTL−3 specifications for DDR−SDRAM V_{DDQ} supply and termination voltage V_{TT} supply. With integrated power MOSFETs the CM3202−02 can source up to 2 A of VDDQ continuous current, and source or sink up to 2 A VTT continuous current. The typical dropout voltage for VDDQ is 500 mV at 2 A load current.

The CM3202−02 provides excellent full load regulation and fast response to transient load changes. It also has built−in over−current limits and thermal shutdown at 170°C.

The CM3202−02 supports Suspend−To−RAM (STR) and ACPI compliance with Shutdown Mode which tri−states VTT to minimize quiescent system current.

The CM3202−02 is available in a space saving WDFN8 surface mount packages. Low thermal resistance allows them to withstand high power dissipation at 85°C ambient. The CM3202−02 can operate over the industrial ambient temperature range of –40°C to 85°C.

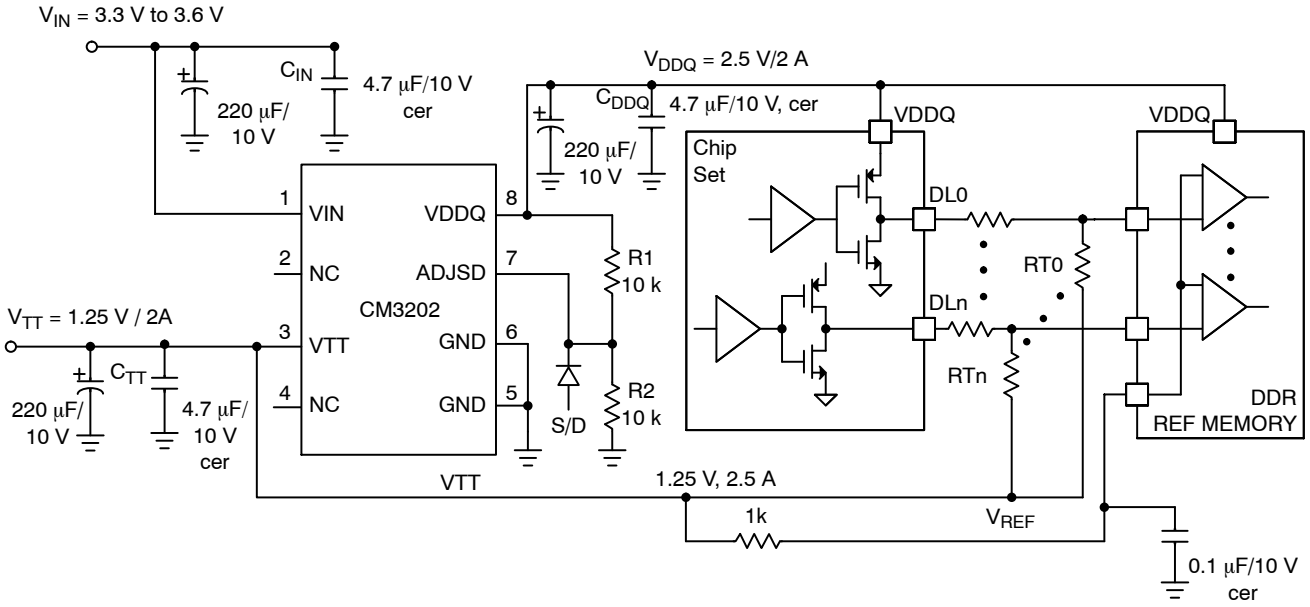
Features

- Two Linear Regulators
  - Maximum 2 A Current from VDDQ
  - Source and Sink Up to 2 A VTT Current
- 1.7 V to 2.8 V Adjustable VDDQ Output Voltage
- 0.85 V to 1.4 V VTT Output Voltage (Tracking at 50% of VDDQ)
- 500 mV Typical VDDQ Dropout Voltage at 2 A
- Excellent Load and Line Regulation, Low Noise
- Meets JEDEC DDR−I and DDR−II Memory Power Spec
- Linear Regulator Design Requires no Inductors and Has Low External Component Count
- Integrated Power MOSFETs
- Dual Purpose ADJ/Shutdown Pin
- Built−In Over−Current Limit and Thermal Shutdown for V_{DDQ} and V_{TT}
- Fast Transient Response
- Low Quiescent Current
- These Devices are Pb−Free and are RoHS Compliant

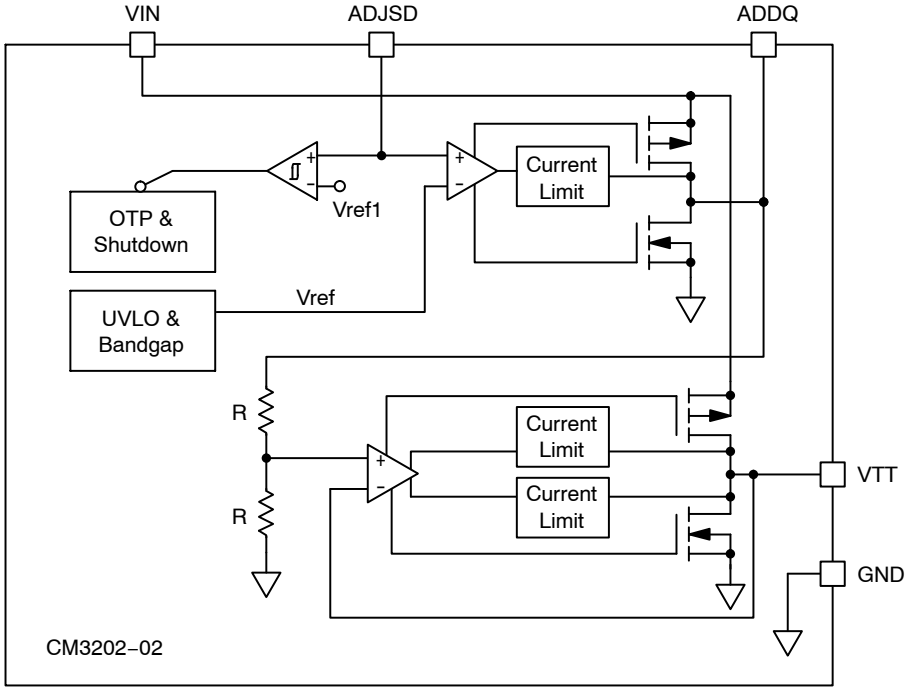
Applications

- DDR Memory and Active Termination Buses
- Desktop Computers, Servers
- Residential and Enterprise Gateways
- DSL Modems
- Routers and Switches
- DVD Recorders
- 3D AGP Cards
- LCD TV and STB

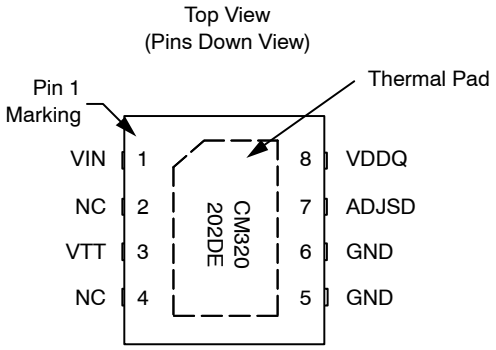
TYPICAL APPLICATION



FUNCTIONAL BLOCK DIAGRAM



PACKAGE / PINOUT DIAGRAMS



8−Lead WDFN Package
CM3202−02DE

Table 1. PIN DESCRIPTIONS

Pin(s)	Name	Description
1	VIN	Input supply voltage pin. Bypass with a 220 μF capacitor to GND.
2	NC	Not internally connected. For better heat flow, connect to GND (exposed pad).
3	VTT	V_{TT} regulator output pin, which is preset to 50% of V_{DDQ}.
4	NC	Not internally connected. For better heat flow, connect to GND (exposed pad).
5	GND	Ground pin (analog).
6	GND	Ground pin (power).
7	ADJSD	This pin is for V_{DDQ} output voltage adjustment. It is available as long as V_{DDQ} is enabled. During Manual/Thermal shutdown, it is tightened to GND. The V_{DDQ} output voltage is set using an external resistor divider connected to ADJSD: $V_{DDQ} = 1.25\ V \times ((R1 + R2) / R2)$ Where R1 is the upper resistor and R2 is the ground−side resistor. In addition, the ADJSD pin functions as a Shutdown pin. When ADJSD voltage is higher than 2.7 V (SHDN_H), the circuit is in Shutdown mode. When ADJSD voltage is below 1.5 V (SHDN_L), both VDDQ and VTT are enabled. A low−leakage Schottky diode in series with ADJSD pin is recommended to avoid interference with the voltage adjustment setting.
8	VDDQ	VDDQ regulator output voltage pin.
EPad	GND	The backside exposed pad which serves as the package heatsink. Must be connected to GND.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
VIN to GND	[GND − 0.3] to +6.0	V
Pin Voltages V_{DDQ}, V_{TT} to GND ADJSD to GND	 [GND − 0.3] to +6.0 [GND − 0.3] to +6.0	V
Output Current VDDQ / VTT, continuous (Note 1) VDDQ / VTT, peak VDDQ Source + VTT Source	 2.0 / ±2.0 2.8 / ±2.8 3	A
Temperature Operating Ambient Operating Junction Storage	 −40 to +85 −40 to +170 −40 to +150	°C
Thermal Resistance, R_{JA} (Note 2)	55	°C / W
Continuous Power Dissipation (Note 2) WDFN8, T_A = 25°C / 85°C	 2.6 / 1.5	W
ESD Protection (HBM)	2000	V
Lead Temperature (soldering, 10 sec)	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Despite the fact that the device is designed to handle large continuous/peak output currents, it is not capable of handling these under all conditions. Limited by the package thermal resistance, the maximum output current of the device cannot exceed the limit imposed by the maximum power dissipation value.
2. Measured with the package using a 4 in^2 / 2 layers PCB with thermal vias.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Ambient Operating Temperature Range	−40 to +85	°C
VDDQ Regulator Supply Voltage, VIN Load Current, Continuous Load Current, Peak (1 sec) C_{DDQ}	 3.0 to 3.6 0 to 2 2.5 220	 V A A μF
VTT Regulator Supply Voltage, VIN Load Current, Continuous Load Current, Peak (1 sec) C_{TT}	 3.0 to 3.6 0 to ±2.0 ±2.50 220	 V A A μF
VIN Supply Voltage Range	3.0 to 3.6	V
VDDQ Source + VTT Source Load Current, Continuous Load Current, Peak (1 sec)	 2.5 3.5	A
Junction Operating Temperature Range	−40 to +150	°C

SPECIFICATIONS (Cont'd)

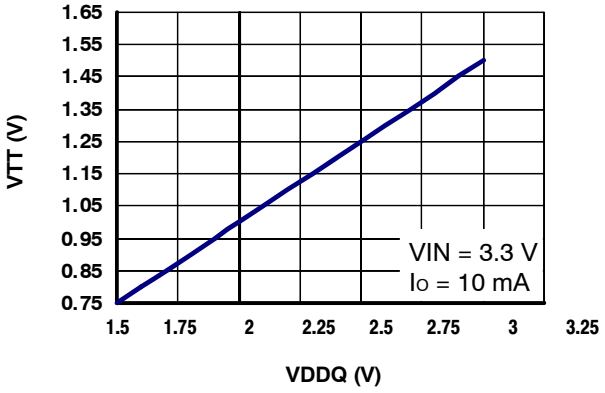
Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
VIN	Supply Voltage Range		3.0		3.6	V
I_Q	Quiescent Current	I_{DDQ} = 0, I_{TT} = 0		7	15	mA
V_{ADJSD}	ADJSD Voltage		1.225	1.250	1.275	V
I_{SHDN}	Shutdown Current	V_{ADJSD} = 3.3 V (Shutdown) (Note 3)		0.2	0.5	mA
SHDN_H	ADJSD Logic High	(Note 2)	2.7			V
SHDN_L	ADJSD Logic Low				1.5	V
UVLO	Under−Voltage Lockout	Hysteresis = 100 mV	2.40	2.70	2.90	V
T_{OVER}	Thermal SHDN Threshold		150	170		°C
T_{HYS}	Thermal SHDN Hysteresis			50		°C
TEMPCO	V_{DDQ}, V_{TT} TEMPCO	I_{OUT} = 1 A		80		ppm/°C
VDDQ Regulator						
$V_{DDQ\ DEF}$	VDDQ Output Voltage	I_{DDQ} = 100 mA	2.450	2.500	2.550	V
$V_{DDQ\ LOAD}$	VDDQ Load Regulation	10 mA ≤ I_{DDQ} ≤ 2 A (Note 3)		10	25	mV
$V_{DDQ\ LINE}$	VDDQ Line Regulation	3.0 V ≤ VIN ≤ 3.6 V, I_{DDQ} = 0.1 A		5	25	mV
V_{DROP}	VDDQ Dropout Voltage	I_{DDQ} = 2 A (Note 4)		500		mV
I_{ADJ}	ADJSD Bias Current	(Note 3)		0.8	3.0	μA
$I_{DDQ\ LIM}$	VDDQ Current Limit		2.0	2.5		A
VTT Regulator						
$V_{TT\ DEF}$	VTT Output Voltage	I_{TT} = 100 mA	1.225	1.250	1.275	V
$V_{TT\ LOAD}$	VTT Load Regulation	Source, 10 mA ≤ I_{TT} ≤ 2 A (Note 3) Sink, −2A ≤ I_{TT} ≤ 10 mA (Note 3)	 −30	10 −10	30	mV mV
$V_{TT\ LINE}$	VTT Line Regulation	3.0 V ≤ VIN ≤ 3.6 V, I_{TT} = 0.1 A		5	15	mV
$I_{TT\ LIM}$	ITT Current Limit	Source / Sink (Note 3)	±2.0	±2.5		A
$I_{VTT\ OFF}$	VTT Shutdown Leakage Current	V_{ADJSD} = 3.3 V (Shutdown)			10	μA

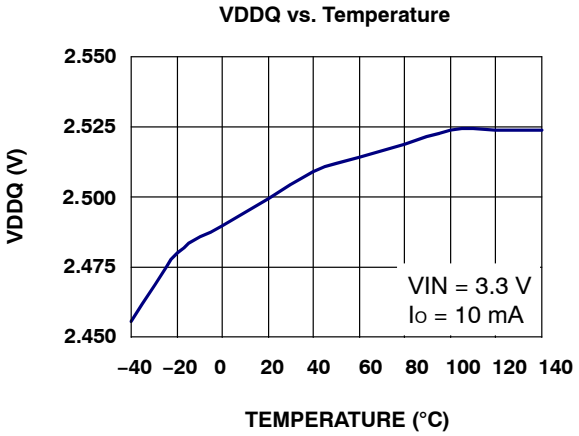
1. VIN = 3.3 V, V_{DDQ} = 2.50 V, VTT = 1.25 V (default values), C_{DDQ} = C_{TT} = 47 μF, T_A = 25°C unless otherwise specified.
2. The ADJSD Logic High value is normally satisfied for full input voltage range by using a low leakage current (below 1 μA). Schottky diode at ADJSD control pin.
3. Load and line regulation are measured at constant junction temperature by using pulse testing with a low duty cycle. For high current tests, correlation method can be used. Changes in output voltage due to heating effects must be taken into account separately. Load and line regulation values are guaranteed by design up to the maximum power dissipation.
4. Dropout voltage is the input to output voltage differential at which output voltage has dropped 100 mV from the nominal value obtained at 3.3 V input. It depends on load current and junction temperature. Guaranteed by design.

TYPICAL OPERATING CHARACTERISTICS

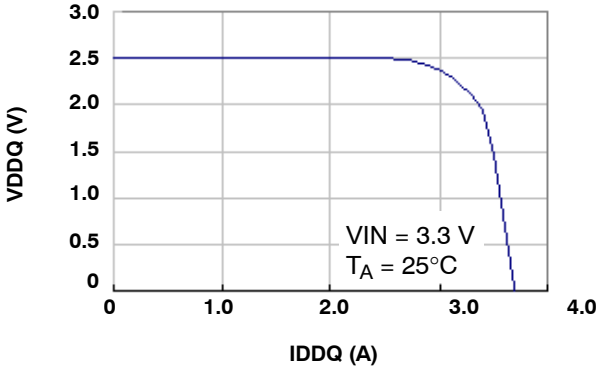
VTT vs. VDDQ



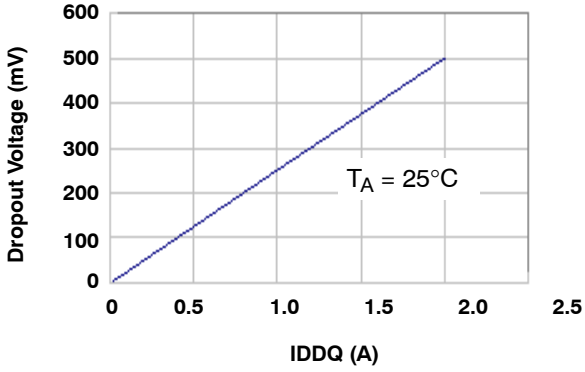
VDDQ vs. Temperature



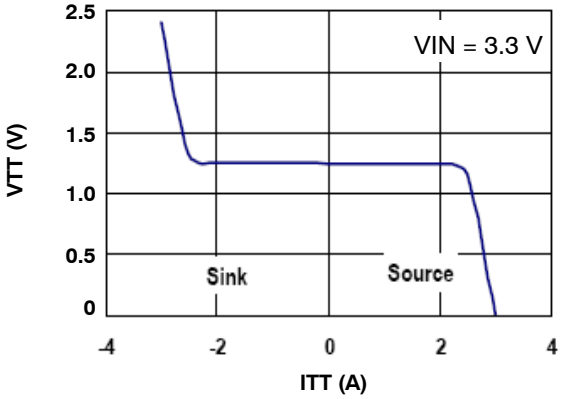
VDDQ vs. Load Current



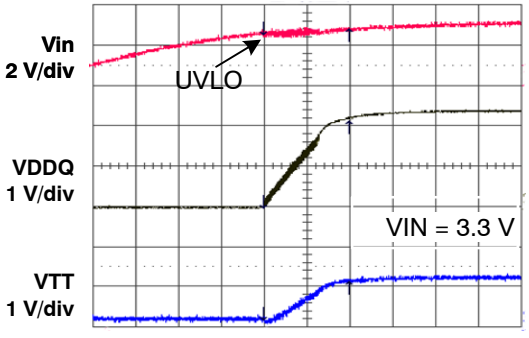
VDDQ Dropout vs. IDDQ



VTT vs. Load Current

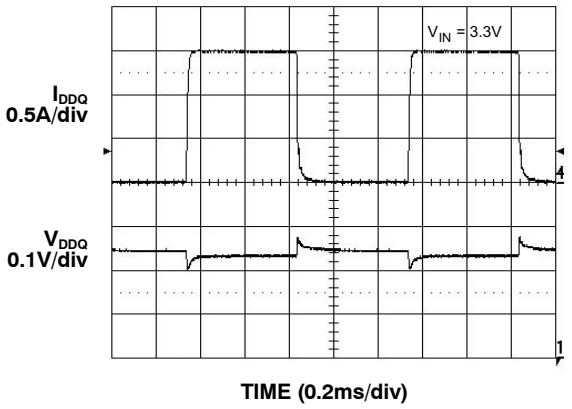


Startup into Full Load

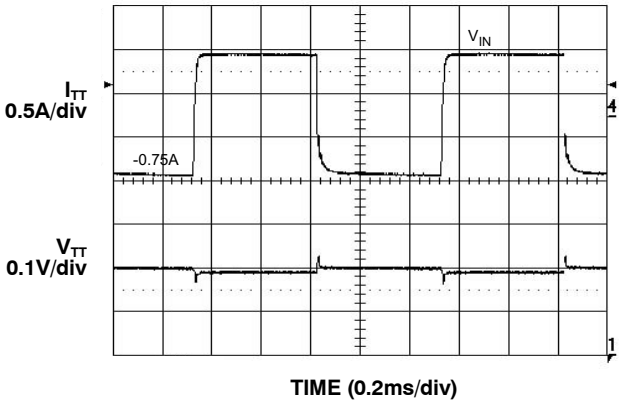


TYPICAL OPERATING CHARACTERISTICS (Cont'd)

VDDQ Transient Response



VTT Transient Response



APPLICATION INFORMATION

Powering DDR Memory

Double−Data−Rate (DDR) memory has provided a huge step in performance for personal computers, servers and graphic systems. As is apparent in its name, DDR operates at double the data rate of earlier RAM, with two memory accesses per cycle versus one. DDR SDRAMs transmit data at both the rising and falling edges of the memory bus clock.

DDR's use of Stub Series Terminated Logic (SSTL) topology improves noise immunity and power−supply rejection, while reducing power dissipation. To achieve this performance improvement, DDR requires more complex power management architecture than previous RAM technology.

Unlike the conventional DRAM technology, DDR SDRAM uses differential inputs and a reference voltage for all interface signals. This increases the data bus bandwidth, and lowers the system power consumption. Power consumption is reduced by lower operating voltage, a lower signal voltage swing associated with Stub Series Terminated Logic (SSTL_2), and by the use of a termination voltage, V_{TT}. SSTL_2 is an industry standard defined in JEDEC document JESD8−9. SSTL_2 maintains high−speed data bus signal integrity by reducing transmission reflections. JEDEC further defines the DDR SDRAM specification in JESD79C.

DDR memory requires three tightly regulated voltages: V_{DDQ}, V_{TT}, and V_{REF} (see Typical DDR terminations, Class II). In a typical SSTL_2 receiver, the higher current V_{DDQ} supply voltage is normally 2.5 V with a tolerance of ±200 mV. The active bus termination voltage, V_{TT}, is half of V_{DDQ}. V_{REF} is a reference voltage that tracks half of V_{DDQ} ±1%, and is compared with the V_{TT} terminated signal at the receiver. V_{TT} must be within ±40 mV of V_{REF}

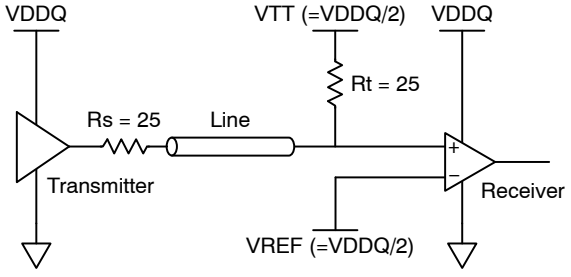


Figure 1. Typical DDR Terminations, Class II

APPLICATION INFORMATION (Cont'd)

The VTT power requirement is proportional to the number of data lines and the resistance of the termination resistor, but does not vary with memory size. In a typical DDR data bus system each data line termination may momentarily consume 16.2 mA to achieve the 405 mV minimum over V_{TT} needed at the receiver:

$$I_{terminaton} = \frac{405\,mV}{Rt(25\,\Omega)} = 16.2\,mA$$

A typical 64 Mbyte SSTL−2 memory system, with 128 terminated lines, has a worst−case maximum V_{TT} supply current up to ±2.07 A. However, a DDR memory system is dynamic, and the theoretical peak currents only occur for short durations, if they ever occur at all. These high current peaks can be handled by the V_{TT} external capacitor. In a real memory system, the continuous average V_{TT} current level in normal operation is less than ±200 mA.

The VDDQ power supply, in addition to supplying current to the memory banks, could also supply current to controllers and other circuitry. The current level typically stays within a range of 0.5 A to 1 A, with peaks up to 2 A or more, depending on memory size and the computing operations being performed.

The tight tracking requirements and the need for V_{TT} to sink, as well as source, current provide unique challenges for powering DDR SDRAM.

CM3202−02 Regulator

The CM3202−02 dual output linear regulator provides all of the power requirements of DDR memory by combining two linear regulators into a single TDFN−8 package. VDDQ regulator can supply up to 2 A current, and the two−quadrant V_{TT} termination regulator has current sink and source capability to ±2 A. The VDDQ linear regulator uses a PMOS pass element for a very low dropout voltage, typically 500 mV at a 2 A output. The output voltage of V_{DDQ} can be set by an external voltage divider. The use of regulators for both the upper and lower side of the VDDQ output allows a fast transient response to any change of the load, from high current to low current or inversely. The second output, V_{TT}, is regulated at $V_{DDQ}/2$ by an internal resistor divider. Same as VDDQ, VTT has the same fast transient response to load change in both directions. The V_{TT} regulator can source, as well as sink, up to 2 A current. The CM3202−02 is designed for optimal operation from a nominal 3.3 VDC bus, but can work with VIN up to 5 V. When operating at higher VIN voltages, attention must be given to the increased package power dissipation and proportionally increased heat generation. Limited by the package thermal resistance, the maximum output current of the device at higher VIN cannot exceed the limit imposed by the maximum power dissipation value.

V_{REF} is typically routed to inputs with high impedance, such as a comparator, with little current draw. An adequate V_{REF} can be created with a simple voltage divider of precision, matched resistors from V_{DDQ} to ground. A small ceramic bypass capacitor can also be added for improved noise performance.

Input and Output Capacitors

The CM3202−02 requires that at least a 220 μF electrolytic capacitor be located near the VIN pin for stability and to maintain the input bus voltage during load transients. An additional 4.7 μF ceramic capacitor between the VIN and GND, located as close as possible to those pins, is recommended to ensure stability.

At a minimum, a 220 μF electrolytic capacitor is recommended for the V_{DDQ} output. An additional 4.7 μF ceramic capacitor between the V_{DDQ} and GND, located very close to those pins, is recommended.

At a minimum, a 220 μF electrolytic capacitor is recommended for the V_{TT} output. This capacitor should have low ESR to achieve best output transient response. SP or OSCON capacitors provide low ESR at high frequency, and thus are a good choice. In addition, place a 4.7 μF ceramic capacitor between the V_{TT} pin and GND, located very close to those pins. The total ESR must be low enough to keep the transient within the V_{TT} window of 40 μV during the transition for source to sink. An average current step of ±0.5 A requires:

$$ESR < \frac{40\,mV}{1\,A} = 40\,m\Omega$$

Both outputs will remain stable and in regulation even during light or no load conditions.

The general recommendation for circuit stability for the CM3202−02 requires the following:

1. $C_{IN} = C_{DDQ} = C_{TT}$ = 220 μF/4.7 μF for the full temperature range of –40 to +85°C.
2. $C_{IN} = C_{DDQ} = C_{TT}$ = 100 μF/2.2 μF for the temperature range of –25 to +85°C.

APPLICATION INFORMATION (Cont'd)

Adjusting VDDQ Output Voltage

The CM3202−02 internal bandgap reference is set at 1.25 V. The V_{DDQ} voltage is adjustable by using a resistor divider, R1 and R2:

$$V_{DDQ} = V_{ADJ} \times \frac{R1 + R2}{R2}$$

where V_{ADJ} = 1.25 V. The recommended divider value is $R_1 = R_2$ = 10 kΩ for DDR−1 application, and R1 = 4.42 kΩ, R2 = 10 kΩ for DDR−2 application (V_{DDQ} = 1.8 V, V_{TT} = 0.9 V).

Shutdown

ADJSD also serves as a shutdown pin. When this is pulled high (SHDN_H), both the VDDQ and the VTT outputs tri−state and could sink/source less than 10 μA. During shutdown, the quiescent current is reduced to less than 0.5 mA, independent of output load.

It is recommended that a low leakage Schottky diode be placed between the ADJSD Pin and an external shutdown signal to prevent interference with the ADJ pin's normal operation. When the diode anode is pulled low, or left open, the CM3202−02 is again enabled.

Current Limit and Over−temperature Protection

The CM3202−02 features internal current limiting with thermal protection. During normal operation, V_{DDQ} limits the output current to approximately 2 A and V_{TT} limits the output current to approximately ±2 A. When V_{TT} is current limiting into a hard short circuit, the output current folds back to a lower level (~1 A) until the over−current condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the junction temperature of the device exceeds 170°C (typical), the thermal protection circuitry triggers and tri−states both VDDQ and VTT outputs. Once the junction temperature has cooled to below about 120°C the CM3202−02 returns to normal operation.

Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) primarily consists of two paths in the series. The first path is the junction to the case (θ_{JC}) which is defined by the package style and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any condition can be estimated by the following thermal equation:

$$\begin{aligned} T_{JUNC} &= T_{AMB} + P_D \times (\theta_{JC}) + P_D \times (\theta_{CA}) \\ &= T_{AMB} + P_D \times (\theta_{CA}) \end{aligned}$$

When a CM3202−02 using WDFN8 package is mounted on a double−sided printed circuit board with four square inches of copper allocated for "heat spreading," the θ_{JA} is approximately 55°C/W. Based on the over temperature limit of 170°C with an ambient temperature of 85°C, the available power of the package will be:

$$P_D = \frac{170°C - 85°C}{55°C/W} = 1.5W$$

APPLICATION INFORMATION (Cont'd)

PCB Layout Considerations

The CM3202−02 has a heat spreader (exposed pad) attached to the bottom of the WDFN8 package in order for the heat to be transferred more easily from the package to the PCB. The heat spreader is a copper pad with slightly smaller dimensions than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during manufacturing, the heat will be transferred between the two pads. Thermal Layout for WDFN8 package shows the CM3202−02 recommended PCB layout. Please note there are four vias to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias must be placed underneath the chip but this can result in solder blockage. The ground and power planes need to be at least 2 square inches of copper by the vias. It also helps dissipation if the chip is positioned away from the edge of the PCB, and away from other heat−dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will assure the best heat transfer from the CM3202−02 to ambient temperature.

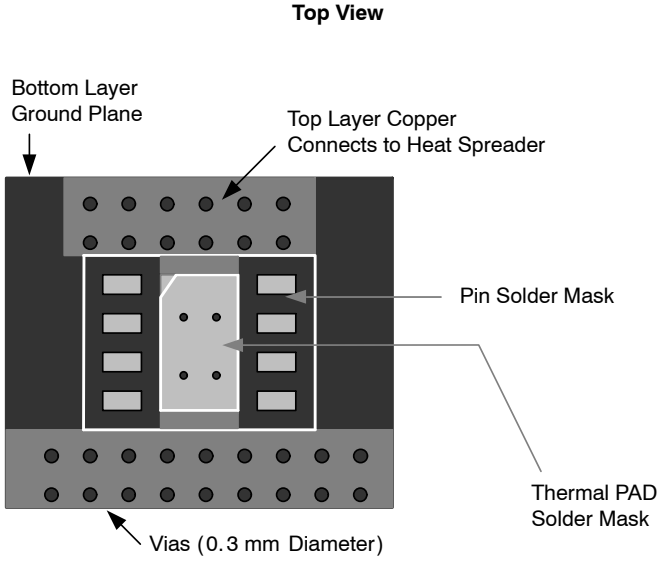
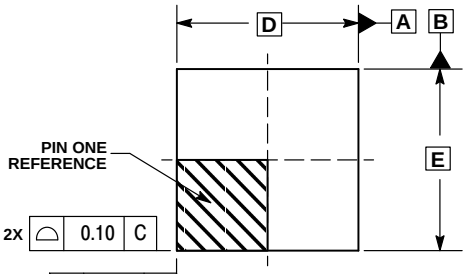


Figure 2. Thermal Layout for WDFN8 Package

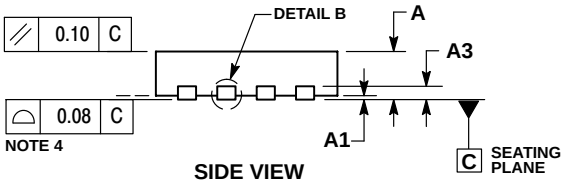
WDFN8 3x3, 0.65P
CASE 511BH
ISSUE O

DATE 21 JUL 2010

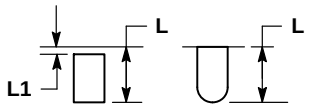
SCALE 2:1



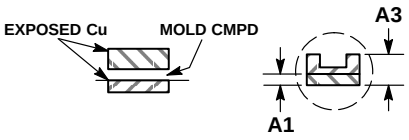
TOP VIEW



SIDE VIEW



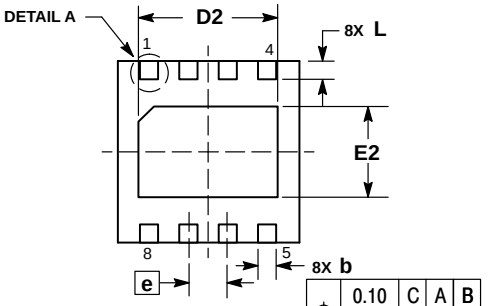
DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS

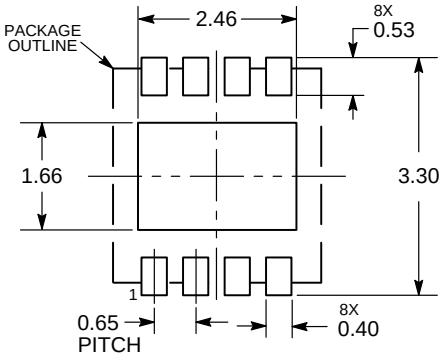
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.00 BSC	
D2	2.20	2.40
E	3.00 BSC	
E2	1.40	1.60
e	0.65 BSC	
K	0.45 REF	
L	0.20	0.40
L1	---	0.15



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON49350E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**WDFN8, 3X3, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales