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Status: **Active**

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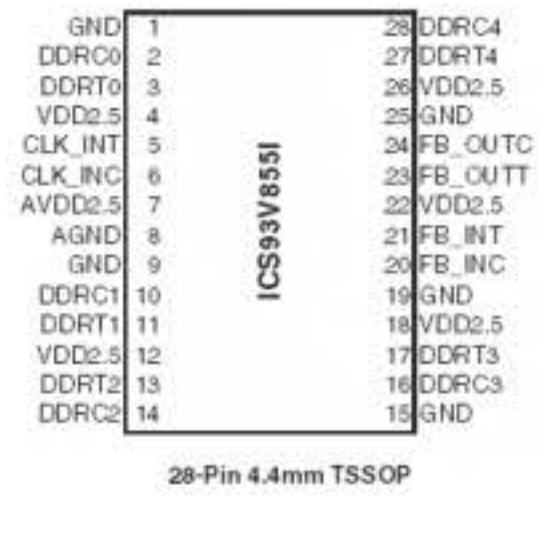
93V855A
DDR Phase Lock Loop Clock Driver

2.5V 1 to 4 differential clock distributor. Optimized for clock distribution in DDR SDRAM applications. Operating frequency: 60MHZ to 220MHz



28-Pin 4.4mm TSSOP

Features

- Low skew, low jitter PLL clock driver
- External feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs with bypass mode mux
- Operating frequency: 60 to 170 MHz
- Operating Temperature: -45°C to +85°C
- Cycle - Cycle jitter: <75ps
- Output - Output skew: <60ps
- Output Rise and Fall Time: 650ps - 950ps

Product Specification

Pkg. Code	Pkg. Type	Length (mm)	Width (mm)	Temp. Grade
PGG28, PG28	TSSOP	9.7	4.4	C, I

Product Options

Orderable Part ID	Part Status	Pkg. Code	Pkg. Type	Lead Count (#)	Temp. Grade	Pb (Lead) Free	Carrier Type	Sample & Buy
93V855AGLF	Active	PGG28	TSSOP	28	C	Yes	Tube	Check Availability
93V855AGLFT	Active	PGG28	TSSOP	28	C	Yes	Reel	Check Availability

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Technical Documentation

	Title	Type	Format	File Size	Date
Datasheets & Errata					
	93V855A Datasheet	Datasheet	PDF	72 KB	03/04/2015
PCNs & PDNs					
	PDN# : M-14-01 PRODUCT DISCONTINUANCE NOTICE	Product Discontinuation Notice	PDF	532 KB	01/26/2014
	PCN# : TB1303-02 Change of Tape & Reel Packing Method for Selective Products	Product Change Notice	PDF	361 KB	03/24/2013

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