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bq24311 Overvoltage and Overcurrent Protection IC and Li+ Charger Front-End Protection IC

1 Features

- Provides Protection for Three Variables:
  - Input Overvoltage, with Rapid Response in < 1 µs
  - User-Programmable Overcurrent with Current Limiting
  - Battery Overvoltage
- 30 V Maximum Input Voltage
- Supports up to 0.3 A Input Current
- Robust Against False Triggering Due to Current Transients
- Thermal Shutdown
- Enable Input
- Status Indication – Fault Condition

2 Applications

- Mobile Phones and Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices
- Bluetooth™ Headsets

3 Description

The bq24311 is a highly integrated circuit designed to protect Li-ion batteries from charging circuit failures. The IC continuously monitors the input voltage, input current, and battery voltage. The input overvoltage protection immediately removes power from the charging circuit by turning off an internal switch. The input protection limits the system current at the user-programmable value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the IC also monitors its own die temperature and switches off if it becomes too hot.

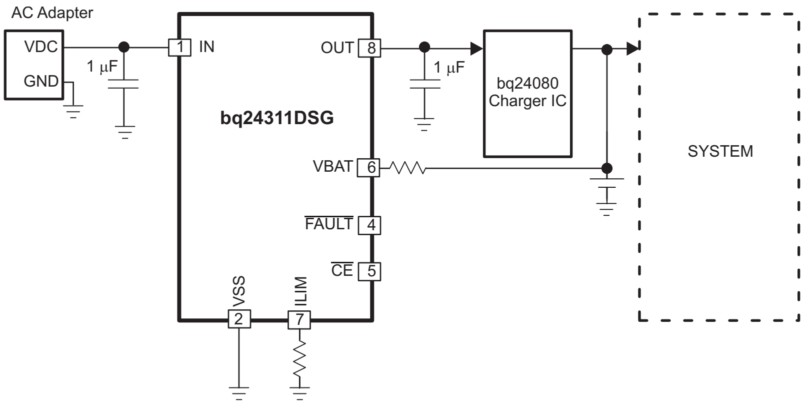
The IC can be controlled by a processor and also provides status information about fault conditions to the host.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24311	WSON (8)	2.00mm x 2.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Application Information



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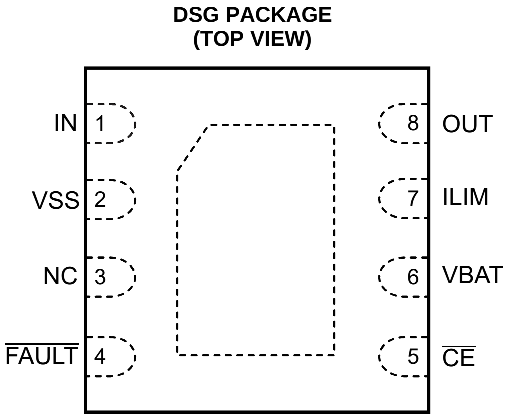
5 Revision History

Date	Revision	Notes
June	*	Initial release.

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	DSG		
IN	1	I	Input power, connect to external DC supply. Connect external 1µF ceramic capacitor (minimum) to VSS.
OUT	8	O	Output pin to the charging system. Connect external 1 µF ceramic capacitor (minimum) to VSS.
VBAT	6	I	Battery voltage sense input. Connect to pack positive pin through a resistor.
ILIM	7	I/O	Input overcurrent threshold programming. Connect a resistor to VSS to set the overcurrent threshold.
$\overline{\text{CE}}$	5	I	Chip enable input. Active low. When $\overline{\text{CE}}$ = High, the input FET is off. Internally pulled down.
$\overline{\text{FAULT}}$	4	O	Device status, open-drain output. $\overline{\text{FAULT}}$ = Low indicates that the input FET Q1 has been turned on due to input overvoltage, input overcurrent, battery overvoltage, or thermal shutdown.
VSS	2	–	Ground pin
NC	3		This pin may have internal circuits used for test purposes. Do not make any external connections at these pins for normal operation.
Thermal PAD		–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. The VSS pin must be connected to ground at all times.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
Input voltage	IN (with respect to VSS)	–0.3	30	V
	OUT (with respect to VSS)	–0.3	12	
	ILIM, $\overline{\text{FAULT}}$, $\overline{\text{CE}}$, VBAT (with respect to VSS)	–0.3	7	
Input current	IN		0.5	A
Output current	OUT		0.5	A
Output sink current	$\overline{\text{FAULT}}$		15	mA
Junction temperature, T_J		–40	150	°C

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	3	26	V
I_{IN}	Input current, IN pin	50	300	mA
I_{OUT}	Output current, OUT pin	50	300	mA
R_{ILIM}	OCP Programming resistor	83.3	500	kΩ
T_J	Junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		DSG	UNITS
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	116.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	56.1	
ψ_{JT}	Junction-to-top characterization parameter	8.1	
ψ_{JB}	Junction-to-board characterization parameter	56.4	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	25.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over junction temperature range –40°C to 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IN							
$V_{(UVLO)}$	Undervoltage lock-out, input power detected threshold	$\overline{CE}$ = Low, V_{IN} increasing from 0 V to 3 V		2.6	2.7	2.8	V
$V_{(UVLO\_HYS)}$	Hysteresis on UVLO	$\overline{CE}$ = Low, V_{IN} decreasing from 3 V to 0 V		200	260	300	mV
I_{DD}	Operating current	$\overline{CE}$ = Low, No load on OUT pin, V_{IN} = 5 V, $R_{(ILIM)}$ = 200 kΩ			400	500	µA
$I_{(STDBY)}$	Standby current	$\overline{CE}$ = High, V_{IN} = 5 V			65	95	µA
INPUT TO OUTPUT CHARACTERISTICS							
$V_{(DO)}$	Drop-out voltage IN to OUT	$\overline{CE}$ = Low, V_{IN} = 5 V, I_{OUT} = 0.125 A			21	35	mV
INPUT OVERVOLTAGE PROTECTION							
$V_{(OVP)}$	Input overvoltage protection threshold	$\overline{CE}$ = Low, V_{IN} increasing from 5V to 7.5 V		5.71	5.85	6.00	V
$V_{HYS\text{-}OVP}$	Hysteresis on OVP	$\overline{CE}$ = Low, V_{IN} decreasing from 7.5 V to 5 V		20	60	110	mV
INPUT OVERCURRENT PROTECTION							
$I_{(OCP)}$	Input overcurrent protection threshold range			50		300	mA
	Input overcurrent protection threshold	$\overline{CE}$ = Low, R_{ILIM} = 200 kΩ, 3 V ≤ V_{IN} < V_{OVP}	T_J = 0°C to 85°C	110	125	135	mA
			T_J = 0°C to 125°C	110	125	140	
BATTERY OVERVOLTAGE PROTECTION							
$V_{(BOVP)}$	Battery overvoltage protection threshold	$\overline{CE}$ = Low, V_{IN} > 4.4 V		4.30	4.35	4.4	V
$V_{(HYS\text{-}BOVP)}$	Hysteresis on $V_{(BOVP)}$	$\overline{CE}$ = Low, V_{IN} > 4.4 V		200	275	320	mV
$I_{(VBAT)}$	Input bias current on VBAT pin	V_{BAT} = 4.4 V, T_J = 25°C				10	nA
THERMAL PROTECTION							
$T_{J(OFF)}$	Thermal shutdown temperature				140	150	°C
$T_{J(OFF\text{-}HYS)}$	Thermal shutdown hysteresis				20		°C
LOGIC LEVELS ON $\overline{CE}$							
V_{IL}	Low-level input voltage			0		0.4	V
V_{IH}	High-level input voltage			1.4			V
I_{IL}	Low-level input current	V_{CE} = 0 V				1	µA
I_{IH}	High-level input current	V_{CE} = 1.8 V				15	µA
LOGIC LEVELS ON $\overline{FAULT}$							
V_{OL}	Output low voltage	$I_{(SINK)}$ = 5 mA				0.2	V
$I_{(HI\text{-}Z)}$	Leakage current, $\overline{FAULT}$ pin HI-Z	$V_{(FAULT)}$ = 5 V				10	µA

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	$\overline{CE}$ = Low. Time measured from V_{IN} 0 V → 5 V 1 µs rise-time, to output turning ON		8		ms
$t_{PD(OVP)}$	Input OV propagation delay$^{(1)}$	$\overline{CE}$ = Low			1	µs
$t_{ON(OVP)}$	Recovery time from input overvoltage condition	$\overline{CE}$ = Low, Time measured from V_{IN} 7.5 V → 5 V, 1µs fall-time		8		ms
$t_{BLANK(OCP)}$	Blanking time, input overcurrent detected			176		µs
$t_{REC(OCP)}$	Recovery time from input overcurrent condition			64		ms
$t_{DGL(BOVP)}$	Deglitch time, battery overvoltage detected	$\overline{CE}$ = Low, V_{IN} > 4.4 V. Time measured from $V_{(VBAT)}$ rising from 4.1 V to 4.4 V to $\overline{FAULT}$ going low.		176		µs

(1) Not tested in production. Specified by design.

7.7 Typical Characteristics

Test conditions (unless otherwise noted) for typical operating performance: V_{IN} = 5 V, C_{IN} = 1 μF, C_{OUT} = 1 μF, $R_{(ILIM)}$ = 200 kΩ, $R_{(BAT)}$ = 100 kΩ, T_A = 25°C, $V_{(PU)}$ = 3.3 V (see Figure 11 for the Typical Application Circuit)

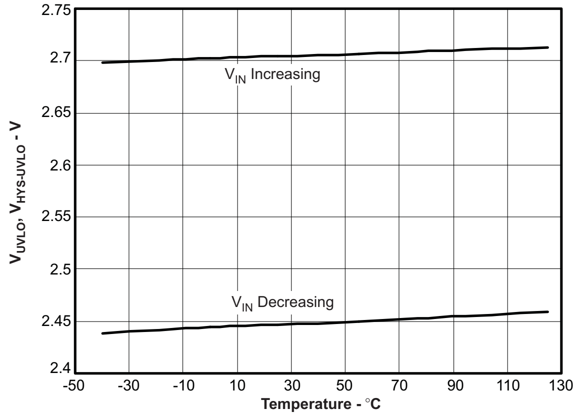


Figure 1. Undervoltage Lockout vs Free-Air Temperature

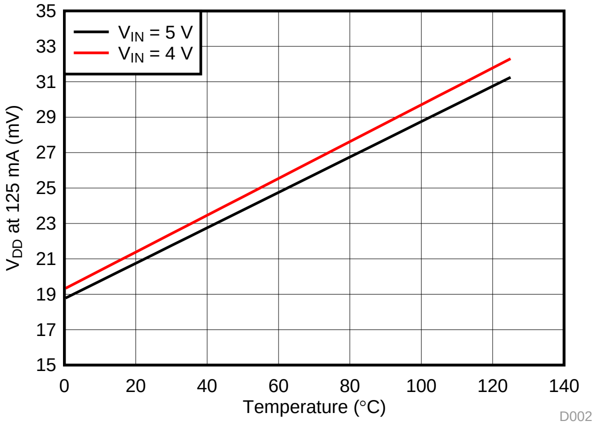


Figure 2. Dropout Voltage (In to Out) vs Free-Air Temperature

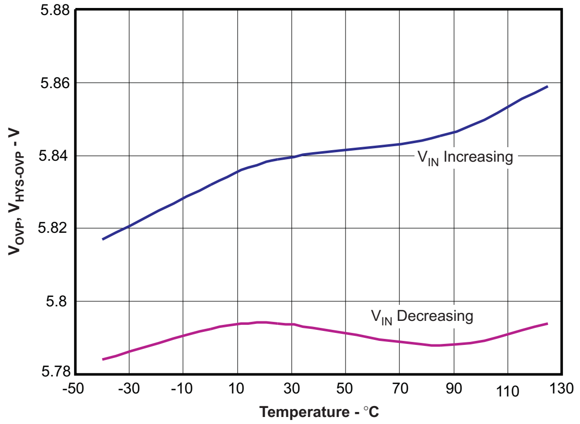


Figure 3. Overvoltage Threshold Protection vs Free-Air Temperature

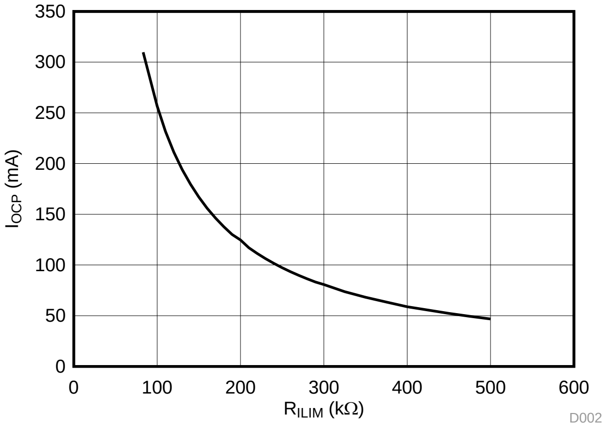


Figure 4. Input Overcurrent Protection vs ILIM Resistance

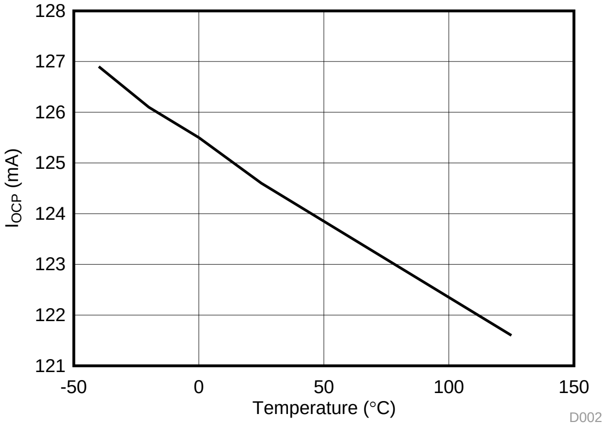


Figure 5. Input Overcurrent Protection vs Free-Air Temperature

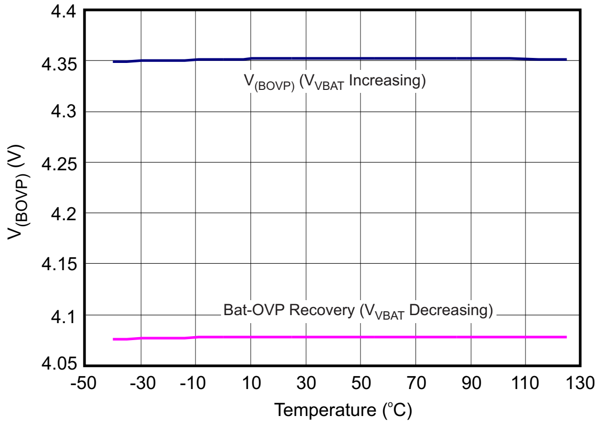


Figure 6. Battery Overvoltage Protection vs Free-Air Temperature

Typical Characteristics (continued)

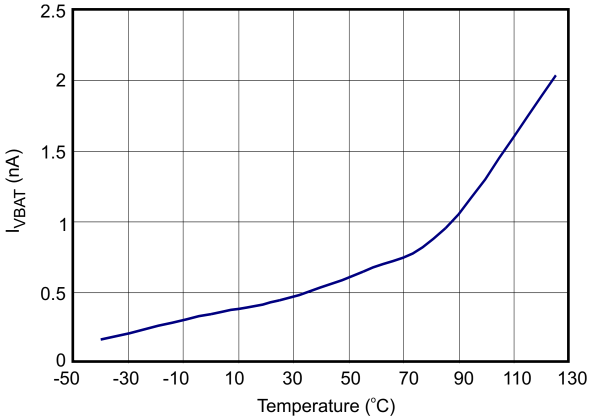


Figure 7. Leakage Current (VBAT Pin) vs Free-Air Temperature

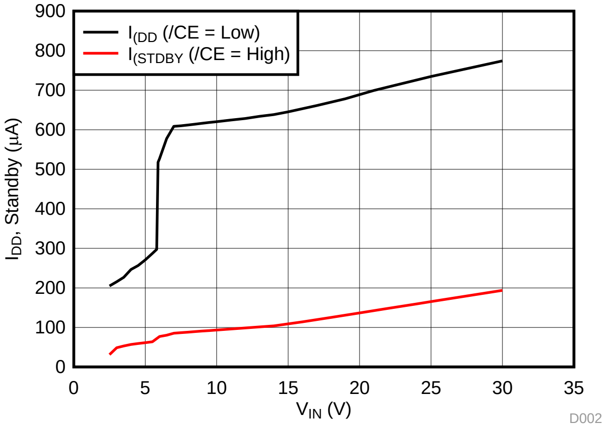


Figure 8. Supply Current vs Input Voltage

8 Detailed Description

8.1 Overview

The bq24311 is a highly integrated circuit designed to protect Li-ion batteries from charging circuit failures. The IC continuously monitors the input voltage, input current, and battery voltage. The input overvoltage protection immediately removes power from the charging circuit by turning off an internal switch. The input protection limits the system current at the user-programmable value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the IC also monitors its own die temperature and switches off if it becomes too hot.

8.2 Functional Block Diagram

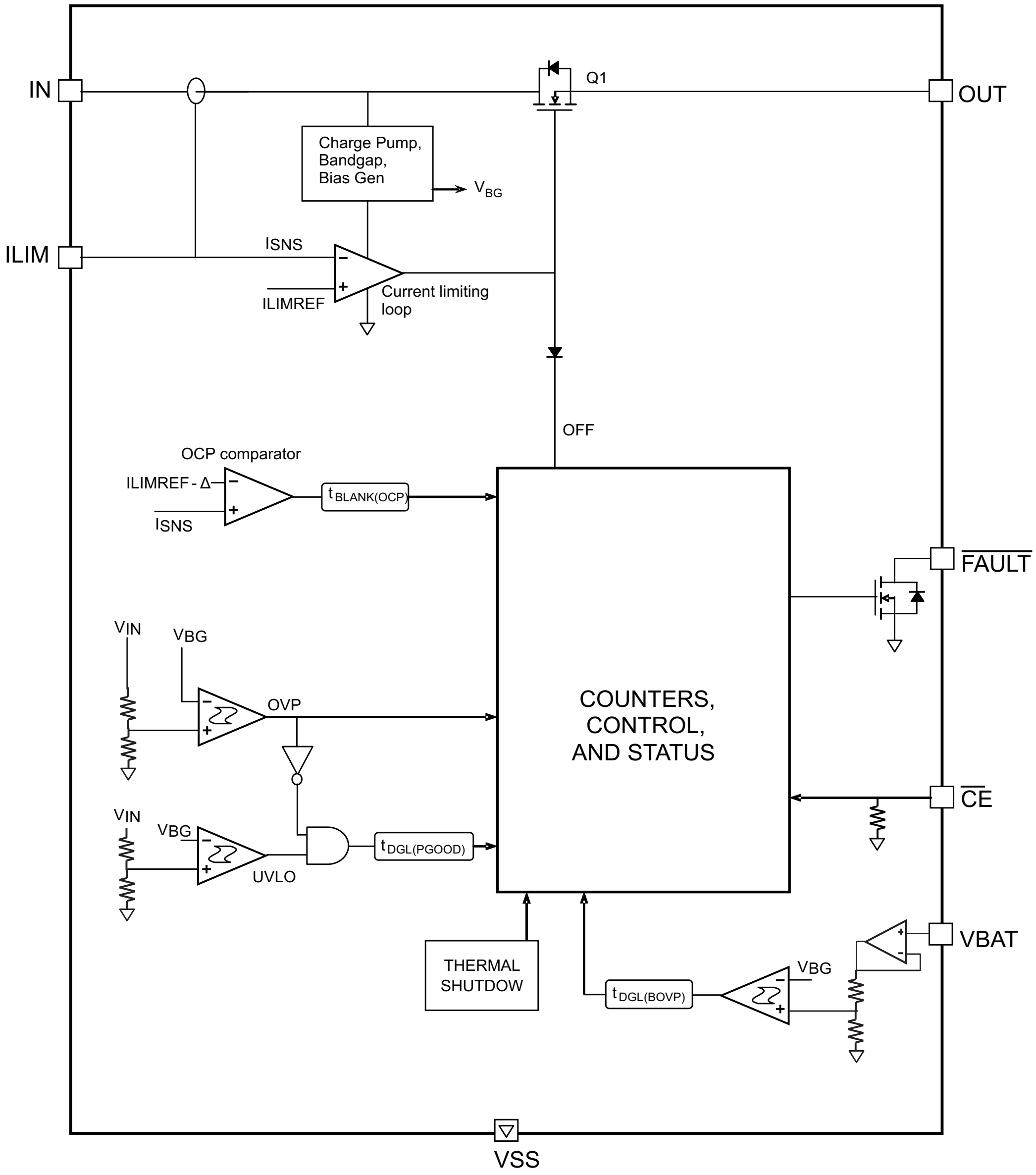


Figure 9. Simplified Block Diagram

8.3 Feature Description

8.3.1 Power Down

The device remains in power down mode when the voltage at the IN pin is below the undervoltage threshold V_{UVLO}. The FET Q1 connected between IN and OUT pins is off, and the status output, $\overline{\text{FAULT}}$, is set to Hi-Z.

8.3.2 Power-On Reset

The device resets when the voltage at the IN pin exceeds the UVLO threshold. All internal counters and other circuit blocks are reset. The IC then waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are safe, FET Q1 is turned ON. The IC has a soft-start feature to control the inrush current which minimizes the ringing at input during power up, as shown in Figure 15 (ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, instead it will go into protection mode and indicate a fault on the $\overline{\text{FAULT}}$ pin, as shown in Figure 16.

8.4 Device Functional Modes

8.4.1 Operation

The device continuously monitors the input voltage, input current, and battery voltage as described in detail in the following sections.

8.4.1.1 Input Overvoltage Protection

If the input voltage rises above V_{OVP}, the internal FET Q1 is turned off, removing power from the circuit. As shown in Figure 17, the response is rapid, with the FET turning off in less than a microsecond. The $\overline{\text{FAULT}}$ pin is driven low. When the input voltage returns below $V_{OVP} – V_{HYS\text{-}OVP}$ (but is still above V_{UVLO}), the FET Q1 is turned on again after a deglitch time of $t_{ON(OVP)}$ to ensure that the input supply has stabilized. Figure 18 shows the recovery from input OVP.

8.4.1.2 Input Overcurrent Protection

If the load current tries to exceed the I_{OCP} threshold, the device limits the current for a blanking period, $t_{BLANK(OCP)}$. If the load current returns to less than I_{OCP} before $t_{BLANK(OCP)}$ times out, the device continues to operate. However, if the overcurrent situation persists for $t_{BLANK(OCP)}$, the FET Q1 is turned off for a duration of $t_{REC(OCP)}$, and the $\overline{\text{FAULT}}$ pin is driven low. The FET is then turned on again after $t_{REC(OCP)}$ and the current is monitored all over again. Each time an OCP fault occurs, an internal counter is incremented. If 15 OCP faults occur in one charge cycle, the FET is turned off permanently, as shown in Figure 19. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the $\overline{\text{CE}}$ pin. Figure 19 and Figure 20 show what happens in an overcurrent fault.

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is turned off slowly, resulting in a “soft-stop”, as shown in Figure 22.

8.4.1.3 Battery Overvoltage Protection

The battery overvoltage threshold $V_{(BOVP)}$ is internally set to 4.35V. If the battery voltage exceeds the $V_{(BOVP)}$ threshold, the FET Q1 is turned off, and the $\overline{\text{FAULT}}$ pin is driven low. The FET is turned back on once the battery voltage drops to $V_{(BOVP)} – V_{HYS\text{-}BOVP}$ (see Figure 22 and Figure 23). Each time a battery overvoltage fault occurs, an internal counter is incremented. If 15 such faults occur in one charge cycle, the FET is turned off permanently, as shown in Figure 23. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the $\overline{\text{CE}}$ pin. In the case of a battery overvoltage fault, Q1 is switched OFF gradually, resulting in a soft-stop (see Figure 22).

Device Functional Modes (continued)

8.4.1.4 Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the FET Q1 is turned off, and the $\overline{\text{FAULT}}$ pin is driven low. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

8.4.1.5 Enable Function

The IC has an enable pin which can be used to enable or disable the device. When the $\overline{\text{CE}}$ pin is driven high, the internal FET is turned off. When the $\overline{\text{CE}}$ pin is low, the FET is turned on if other conditions are safe. The OCP counter and the Bat-OVP counter are both reset when the device is disabled and re-enabled. The $\overline{\text{CE}}$ pin has an internal pulldown resistor and can be left floating. Note that the $\overline{\text{FAULT}}$ pin functionality is also disabled when the $\overline{\text{CE}}$ pin is high.

8.4.1.6 Fault Indication

The $\overline{\text{FAULT}}$ pin is an active-low open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting $\overline{\text{CE}}$ high. With $\overline{\text{CE}}$ low, the $\overline{\text{FAULT}}$ pin goes low whenever any of these events occurs:

- Input overvoltage
- Input overcurrent
- Battery overvoltage
- IC Overtemperature

Device Functional Modes (continued)

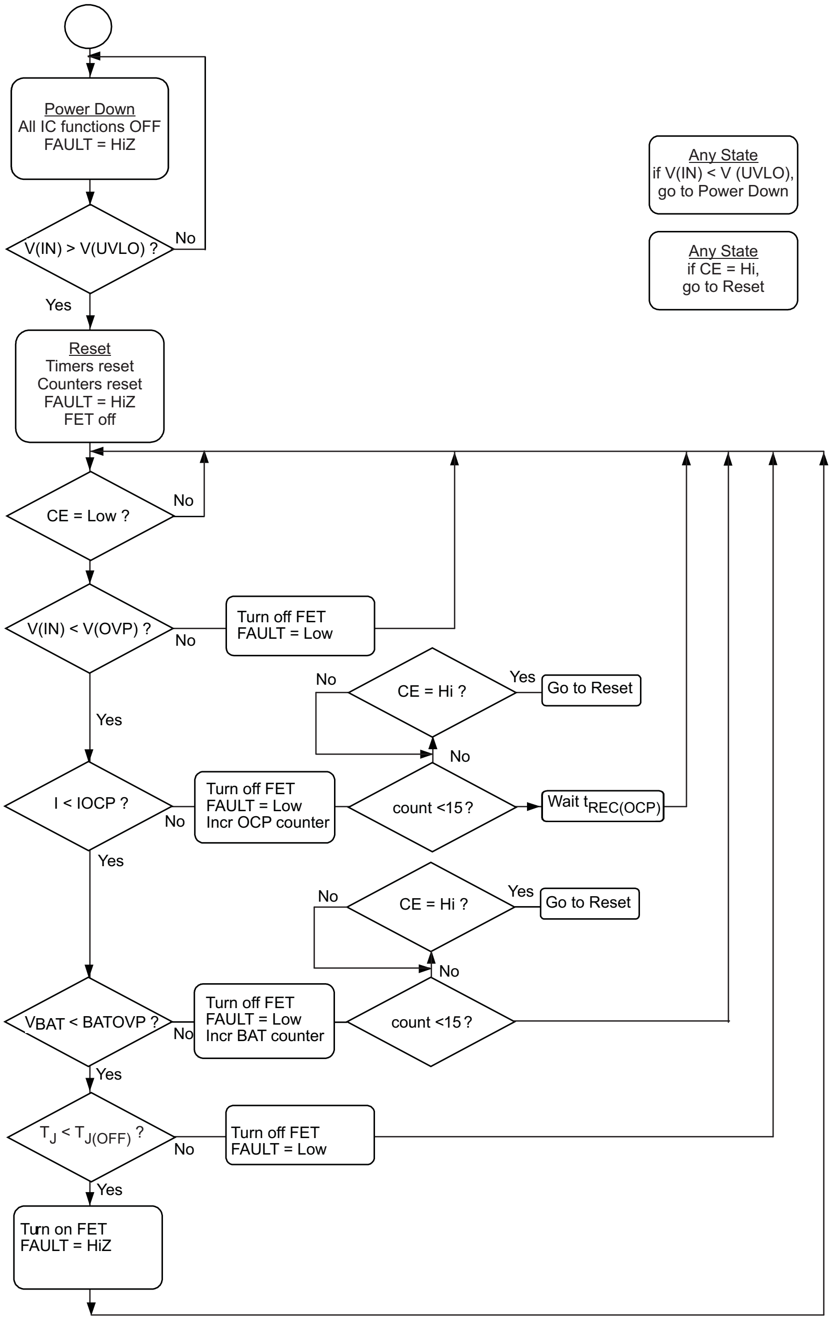


Figure 10. Flow Diagram

9 Application and Implementation

9.1 Typical Application Circuit

V_{OVP} = 5.85 V, I_{OCP} = 125 mA, $V_{(BOVP)}$ = 4.35 V.

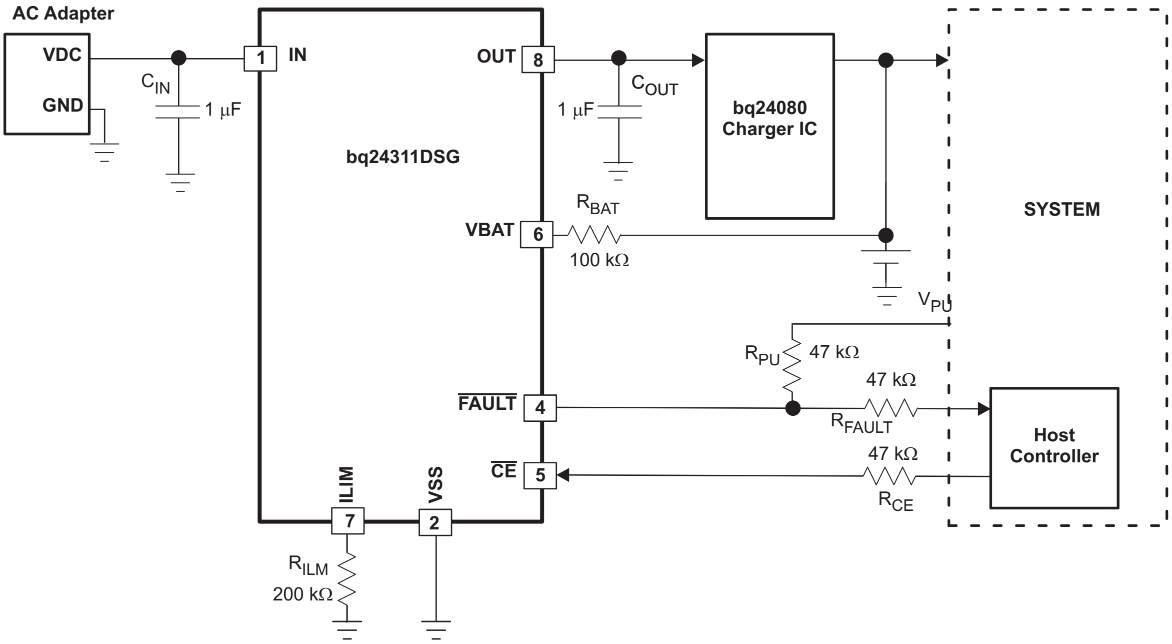


Figure 11.

9.1.1 Design Requirements

9.1.1.1 Selection of R_{ILIM}

The overcurrent threshold is programmed by a resistor, R_{ILIM}, connected from the ILIM pin to VSS. Figure 4 shows the OCP threshold as a function of R_{ILIM}, and may be approximated by the following equation:

$$I_{OCP} = 25 \div R_{ILIM} \text{ (current in A, resistance in k}\Omega) \quad (1)$$

Choose a I_{OCP} between 50 mA and 300 mA and apply the above equation to select a R_{ILIM} resistor value from 500 kΩ to 83.3 kΩ respectively. However, at lower OCP limits, approaching 50 mA, the precision of the current protection circuit decreases the achievable accuracy of the OCP threshold.

9.1.1.2 Selection of R_{BAT}

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30 V, and applying 30 V to the battery in case of the failure of the bq24311 can be hazardous. Connecting the VBAT pin through $R_{(BAT)}$ prevents a large current from flowing into the battery in case of a failure of the IC. In the interests of safety, R_{BAT} should have a high value. The problem with a large $R_{(BAT)}$ is that the voltage drop across this resistor because of the VBAT bias current $I_{(VBAT)}$ causes an error in the $V_{(BOVP)}$ threshold. This error is over and above the tolerance on the nominal 4.35V $V_{(BOVP)}$ threshold.

Choosing R_{BAT} in the range 100 kΩ to 470 kΩ is a good compromise. In the case of an IC failure, with R_{BAT} equal to 100kΩ, the maximum current flowing into the battery would be (30 V – 3 V) ÷ 100 kΩ = 246 µA, which is low enough to be absorbed by the bias currents of the system components. $R_{(BAT)}$ equal to 100 kΩ would result in a worst-case voltage drop of $R_{(BAT)} \times I_{(VBAT)}$ = 1 mV. This is negligible to compared to the internal tolerance of 50mV on $V_{(BOVP)}$ threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

Typical Application Circuit (continued)

9.1.1.3 Selection of $R_{(CE)}$, $R_{(FAULT)}$, and $R_{(PU)}$

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As in the case of the VBAT pin (see Selection of Rbat), the $\overline{CE}$ pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor should be greater than V_{IH} of the bq24311 $\overline{CE}$ pin. The drop across the resistor is given by $R_{(CE)} \times I_{IH}$.

The $\overline{FAULT}$ pin is an open-drain output that goes low during OV, OC, battery-OV, and OT events. If the application does not require monitoring of the $\overline{FAULT}$ pin, it can be left unconnected. But if the $\overline{FAULT}$ pin has to be monitored, it should be pulled high externally through $R_{(PU)}$, and connected through $R_{(FAULT)}$ to the host. $R_{(FAULT)}$ prevents damage to the host controller if the bq24311 fails (see Selection of Rbat). The resistors should be of high value, in practice values between 22 kΩ and 100 kΩ should be sufficient.

9.1.1.4 Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure 11 is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1μF be used at the input of the device. It should be located in close proximity to the IN pin.

C_{OUT} in Figure 11 is also important: If a fast (< 1 μs rise time) overvoltage transient occurs at the input, the current that charges C_{OUT} causes the device's current-limiting loop to kick in, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection. C_{OUT} should also be a ceramic capacitor of at least 1 μF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

9.1.2 Detailed Design Procedures

9.1.2.1 Powering Accessories

In some applications, the equipment that the protection IC resides in may be required to provide power to an accessory (that is, a cellphone may power a headset or an external memory card) through the same connector pins that are used by the adapter for charging. Figure 12 and Figure 13 illustrate typical charging and accessory-powering scenarios:

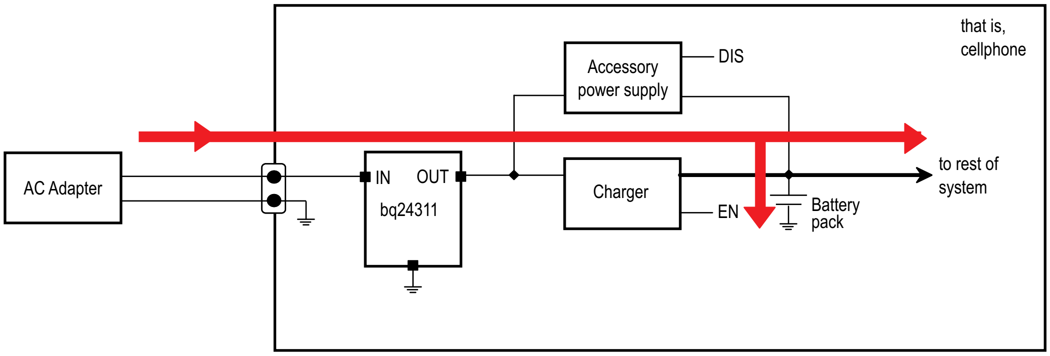


Figure 12. Charging - The Red Arrows Show the Direction of Current Flow

Typical Application Circuit (continued)

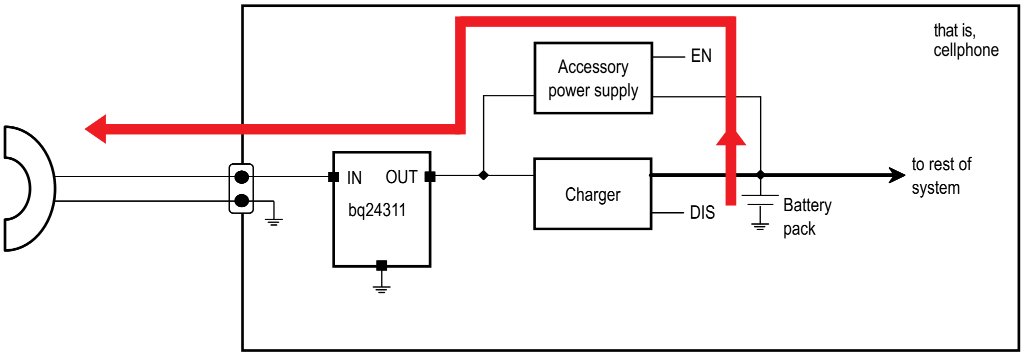


Figure 13. Powering an Accessory - The Red Arrows Show the Direction of Current Flow

In the second case, when power is being delivered to an accessory, the bq24311 device is required to support current flow from the OUT pin to the IN pin.

If $V_{OUT} > V_{(UVLO)} + 0.7$ V, FET Q1 is turned on, and the reverse current does not flow through the diode but through Q1. Q1 will then remain ON as long as $V_{OUT} > V_{(UVLO)} - V_{(HYS\text{-}UVLO)} + R_{DS(on)} \times I_{(ACCESSORY)}$. Within this voltage range, the reverse current capability is the same as the forward capability, 0.5 A. It should be noted that there is no overcurrent protection in this direction.

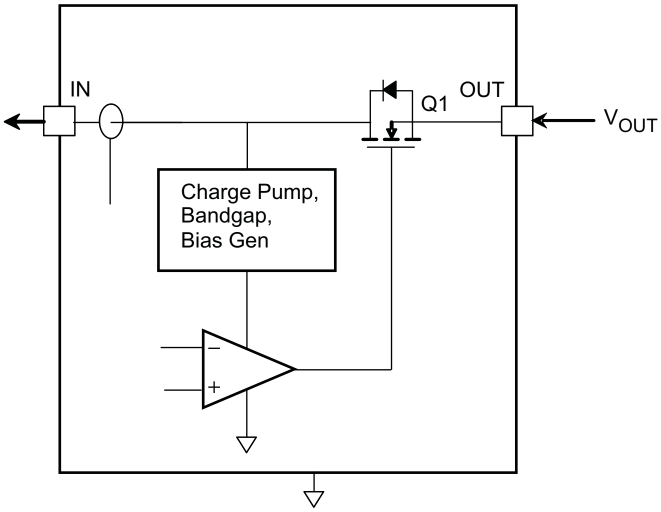
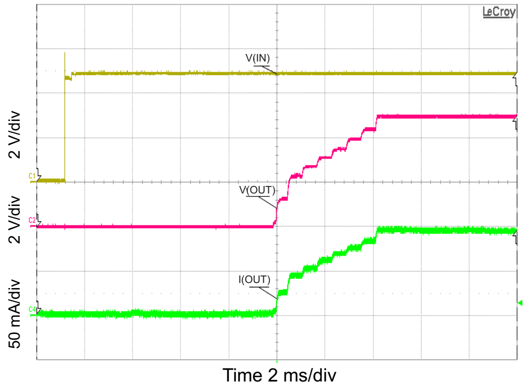


Figure 14.

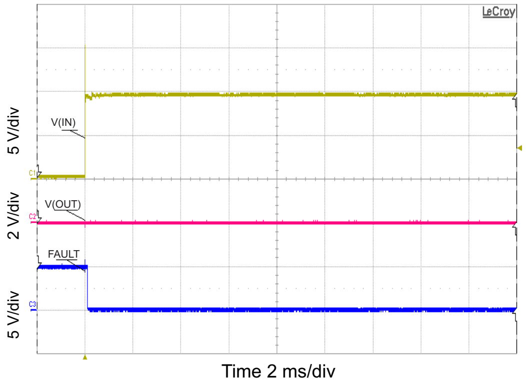
Typical Application Circuit (continued)

9.1.3 Application Curves



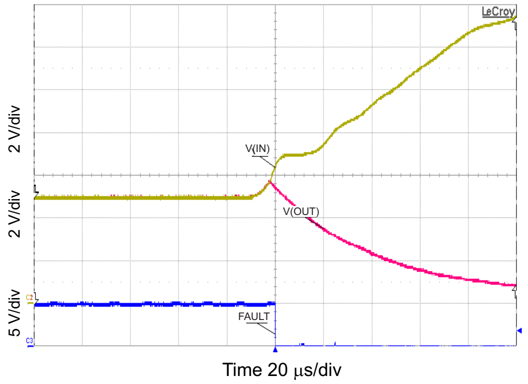
R_{OUT} = 50 Ω

Figure 15. Normal Power-On Showing Soft-Start



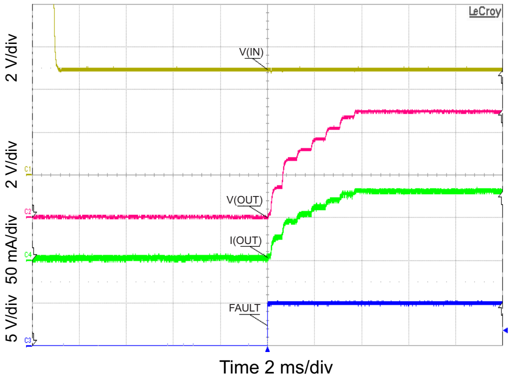
V_{IN} = 0 V to 10 V t_r = 50 µs

Figure 16. OVP at Power-On



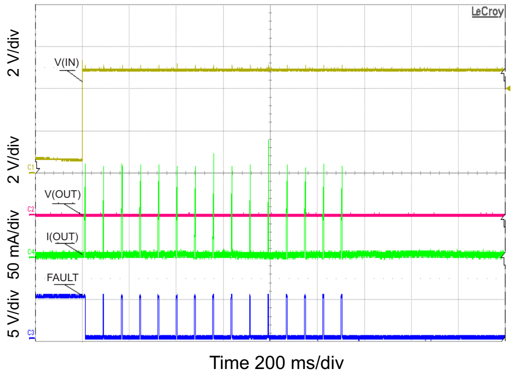
V_{IN} = 5 V to 12 V t_r = 20 µs

Figure 17. OVP Response for Input Step



V_{IN} = 15 V to 5 V t_r = 400 µs

Figure 18. Recovery from OVP



OCP Counter Counts to 15 Before Switching OFF the Device

Figure 19. OCP, Powering Up into a Short Circuit on OUT Pin

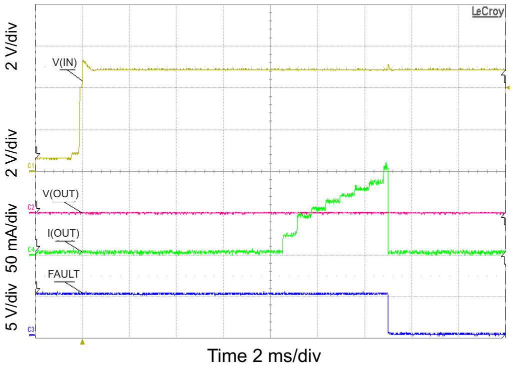


Figure 20. OCP, Zoom-in on the First Cycle of Figure 19

Typical Application Circuit (continued)

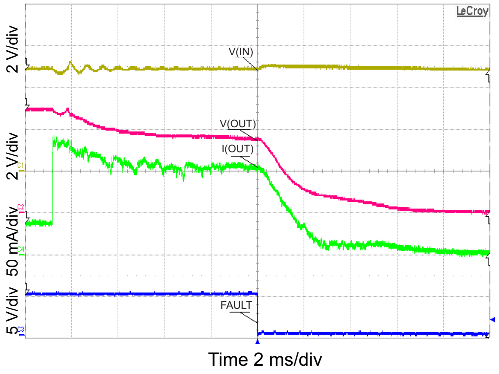


Figure 21. OCP, R_{OUT} Switches from 130 Ω to 30 Ω, Shows Current Limiting and Soft-Stop

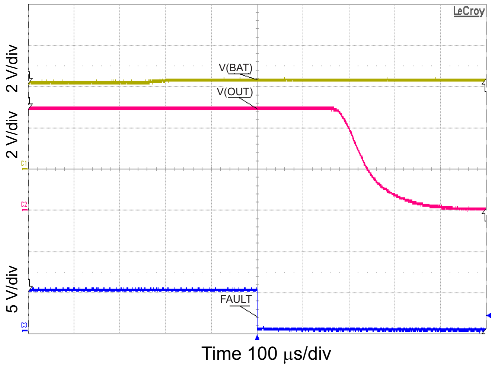


Figure 22. BAT-OVP, $V_{(VBAT)}$ Steps from 4.3 V to 4.4 V, Shows $t_{DGL(BAT-OVP)}$ and Soft-Stop

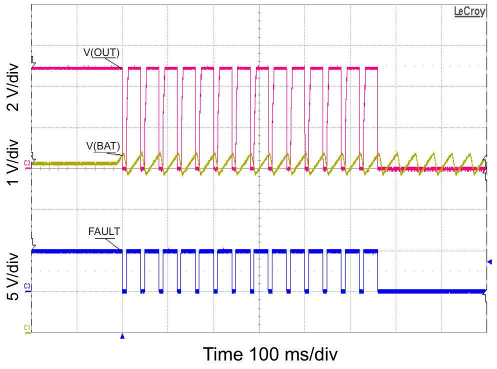


Figure 23. BAT-OVP, $V_{(VBAT)}$ Steps from 3.9V to 4.4V, Shows BAT-OVP Counter

10 Power Supply Requirements

In a typical application, the system is powered by a USB port or USB wall adapter.

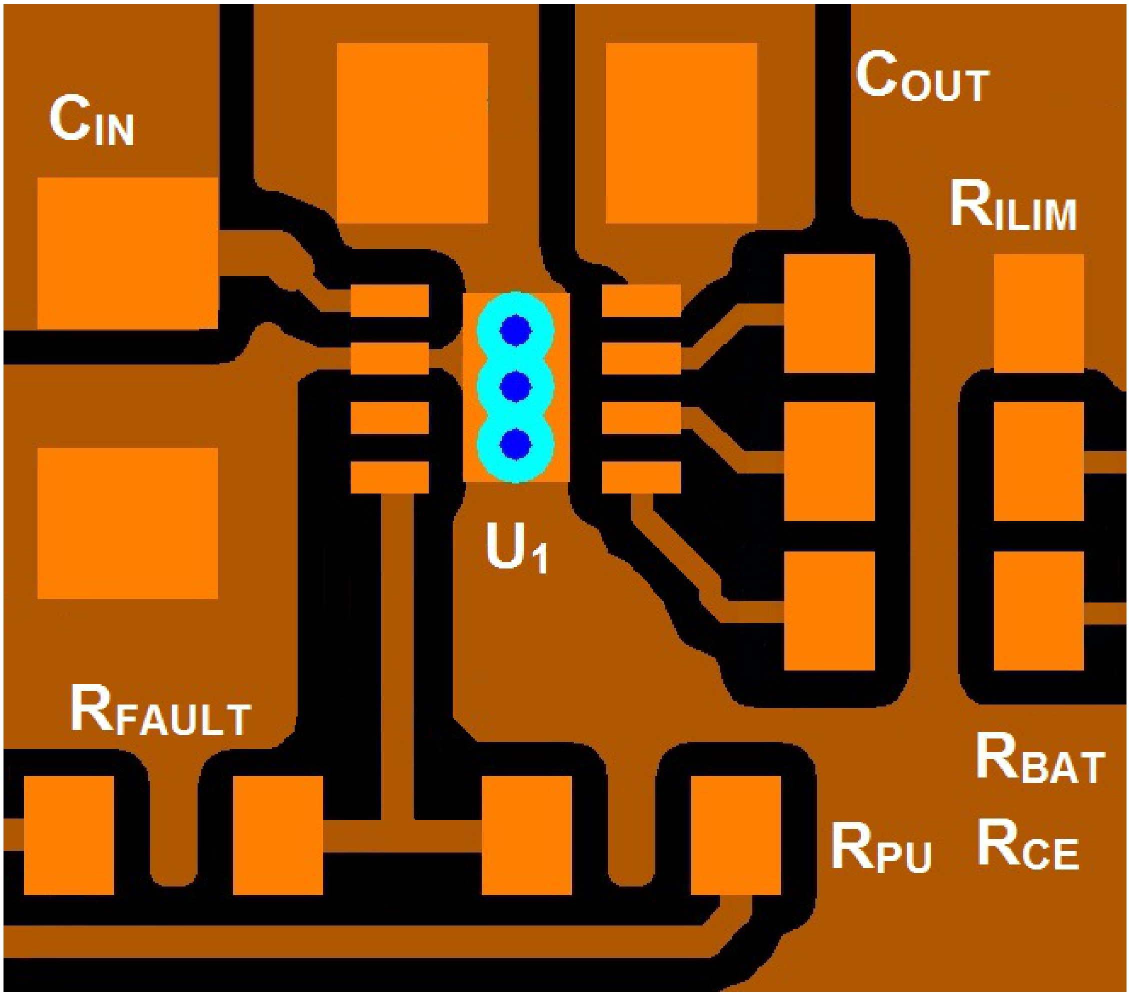
The minimum input voltage, where the protector starts to pass current assuming V_{BAT} is acceptable, could be 2.7 V. The maximum supported input voltage is up to 5.85 V; the overvoltage protection kicks in at 5.85 V and the maximum input voltage rating is 30 V input rating.

11 Layout

11.1 Layout Guidelines

- This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for high voltages.
- The device uses SON packages with a PowerPAD™. For good thermal performance, the PowerPAD should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad should be connected to the ground plane with an array of thermal vias.
- C_{IN} and C_{OUT} should be located close to the IC. Other components like R_{ILIM} and R_{BAT} should also be located close to the IC.

11.2 Layout Example



12 Device and Documentation Support

12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG, Inc.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24311DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SHN
BQ24311DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SHN
BQ24311DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SHN
BQ24311DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SHN
BQ24311DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SHN
BQ24311DSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SHN
BQ24311DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	SHN
BQ24311DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SHN
BQ24311DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SHN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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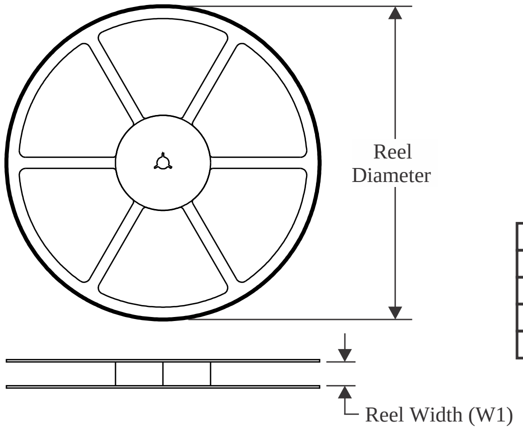
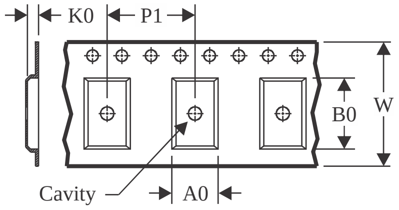
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

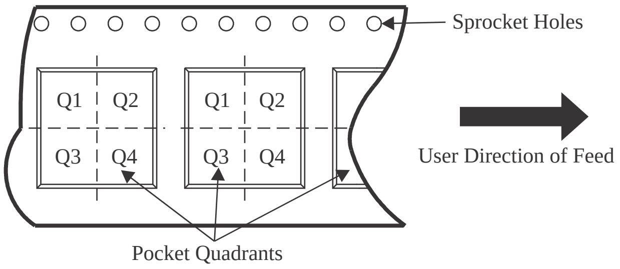


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

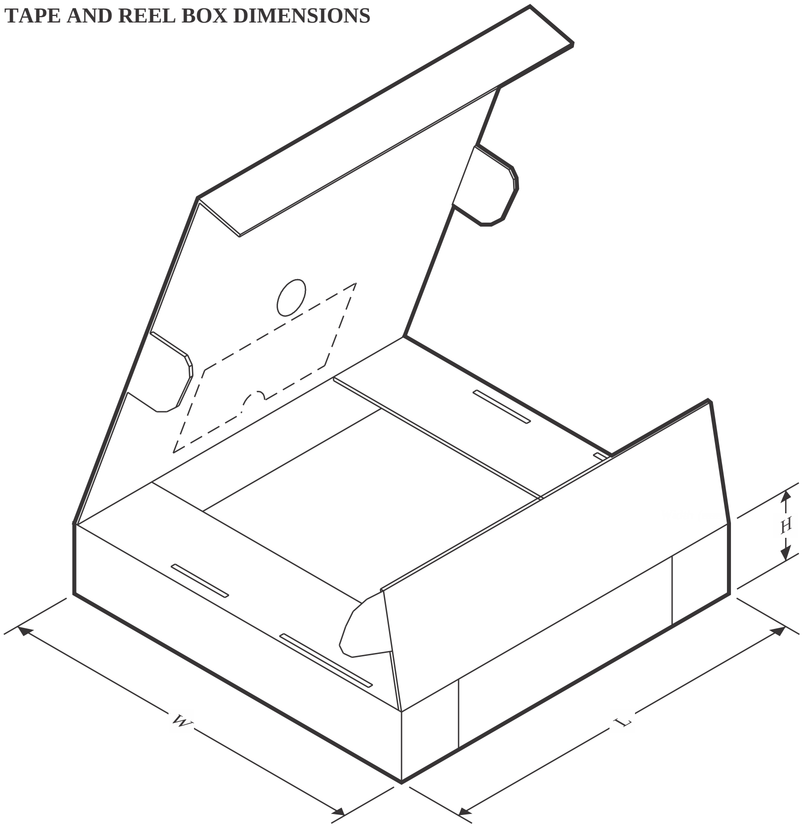
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24311DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24311DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24311DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24311DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
BQ24311DSGRG4	WSON	DSG	8	3000	182.0	182.0	20.0
BQ24311DSGT	WSON	DSG	8	250	182.0	182.0	20.0

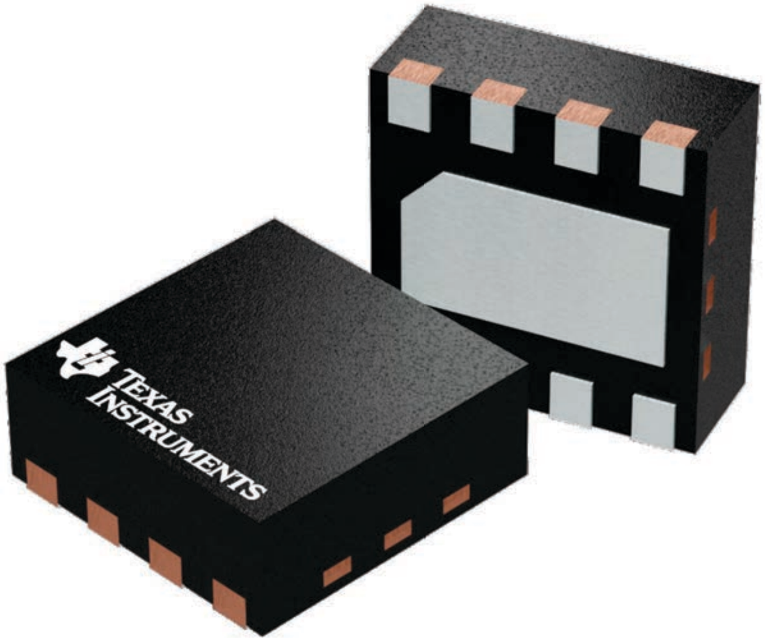
DSG 8

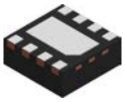
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



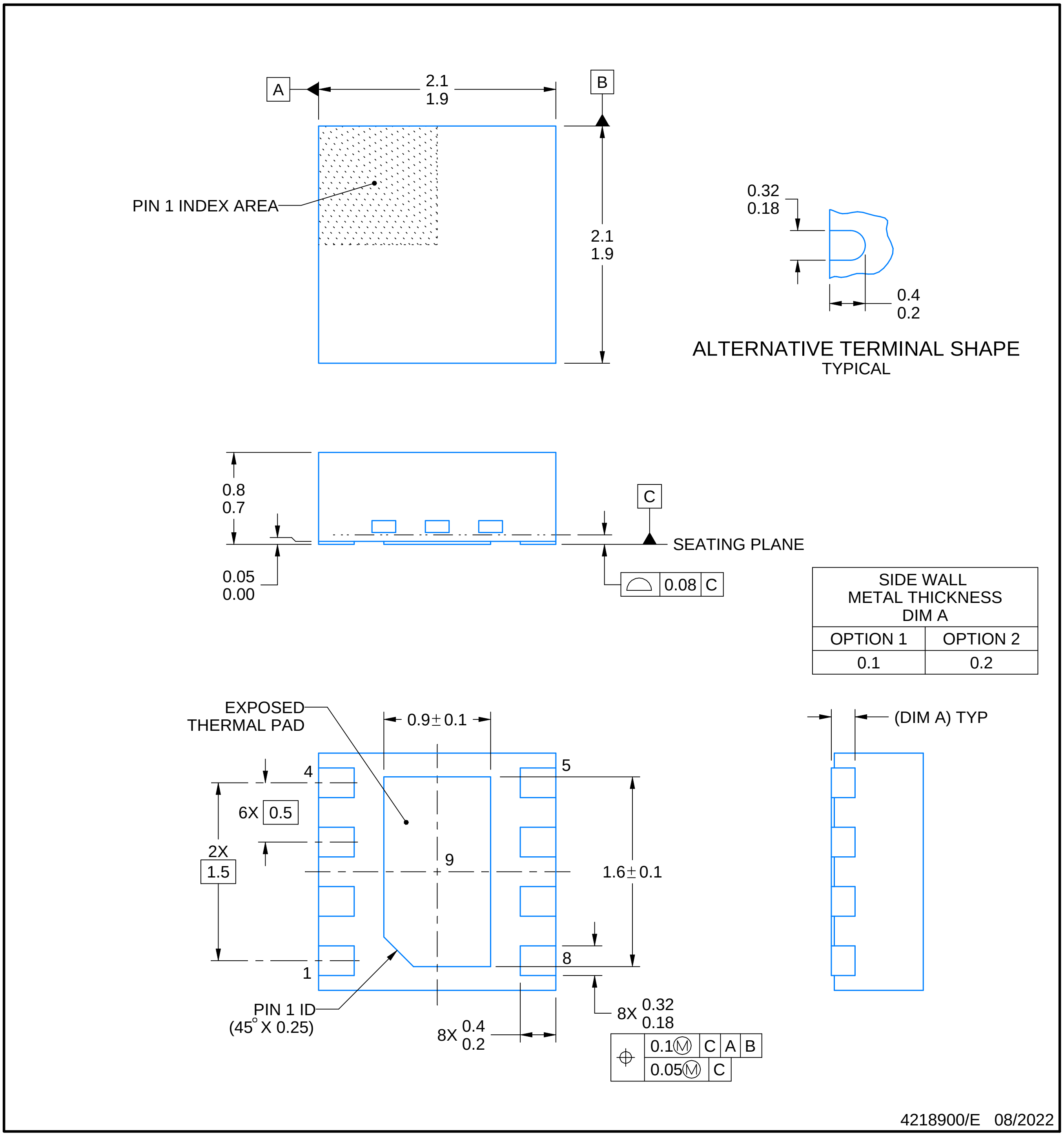


PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

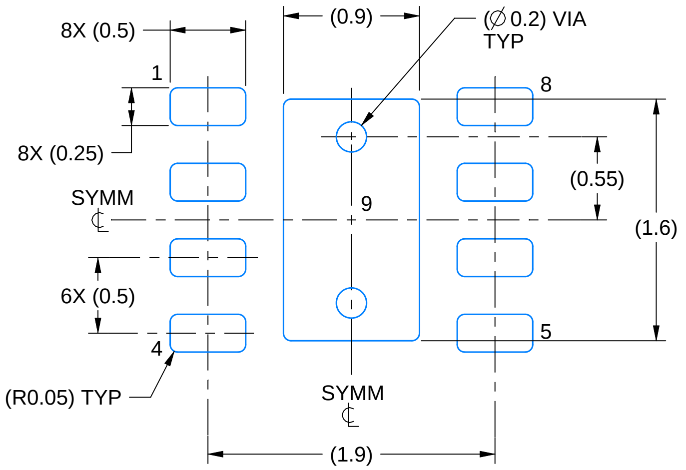


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

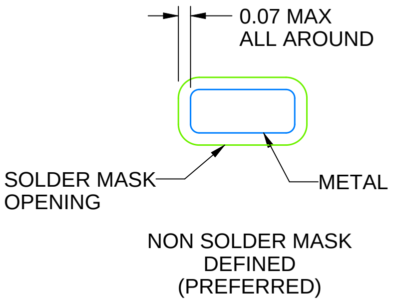
4218900/E 08/2022

NOTES:

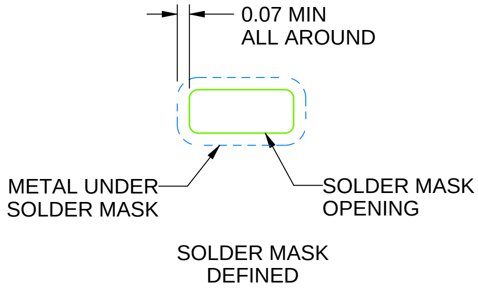
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

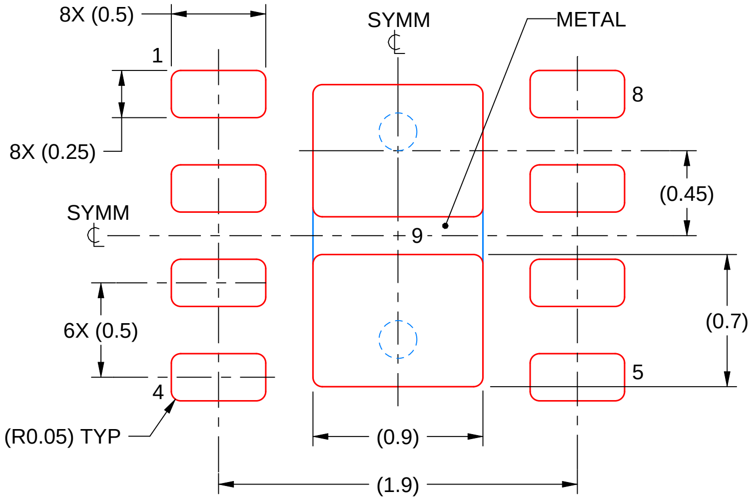


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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