NEC

MOS INTEGRATED CIRCUIT

μPD784020, 784021

16/8-BIT SINGLE-CHIP MICROCOMPUTER

The μPD784021 is a product of the μPD784026 sub-series in the 78K/IV series. It contains various peripheral hardware such as RAM, I/O ports, 8-bit resolution A/D and D/A converters, timers, serial interface, and interrupt functions, as well as a high-speed, high-performance CPU.

The μPD784021 is a ROM-less product of the μPD784025 or μPD784026.

The μPD784020 differs from the μPD784021 only in its RAM size: 512 bytes are allocated for the μPD784020, while 2048 bytes are allocated for the μPD784021.

For specific functions and other detailed information, consult the following user's manual.
This manual is required reading for design work.

μPD784026 Sub-Series User's Manual, Hardware : U10898E
78K/IV Series User's Manual, Instruction : U10905E

FEATURES

- 78K/IV series
- Pin-compatible with the μPD78234 sub-series
- Minimum instruction execution time: 160 ns (at 25 MHz)
- Number of I/O ports: 46
- Timer/counters: 16-bit timer/counter × 3 units
  16-bit timer × 1 unit
- Serial interface: 3 channels
  UART/IOE (3-wire serial I/O) :2 channels
  CSI (3-wire serial I/O, SBI) : 1 channel
- PWM outputs: 2
- Standby function
  HALT/STOP/IDLE mode
- Clock frequency division function
- Watchdog timer: 1 channel
- A/D converter : 8-bit resolution × 8 channels
- D/A converter : 8-bit resolution × 2 channels
- Supply voltage : V_{DD} = 2.7 to 5.5 V

APPLICATIONS

LBP, automatic-focusing camera, PPC, printer, electronic typewriter, air conditioner, electronic musical instruments, cellular telephone, etc.

This manual describes the μPD784021 unless otherwise specified.

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

ORDERING INFORMATION

	Part number	Package	Internal ROM (bytes)	Internal RAM (bytes)
★	μPD784020GC-3B9	80-pin plastic QFP (14 × 14 mm)	None	512
	μPD784021GC-3B9	80-pin plastic QFP (14 × 14 mm)	None	2048
★	μPD784021GK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	None	2048

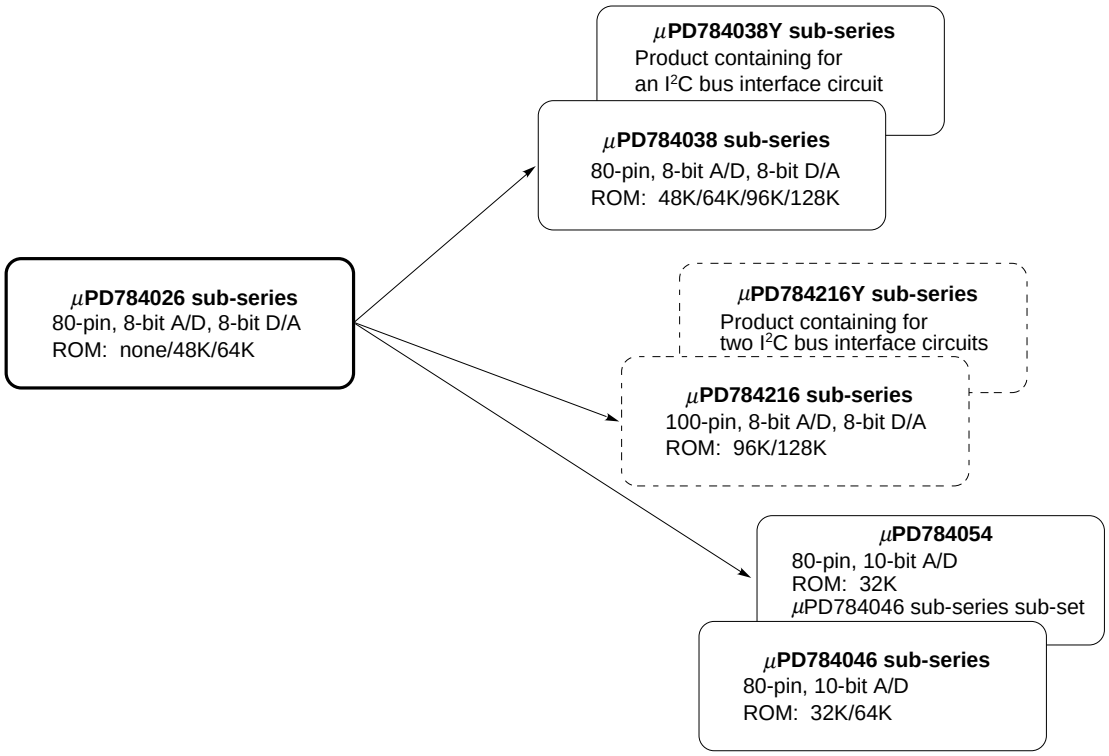
★ 78K/IV SERIES PRODUCT DEVELOPMENT DIAGRAM

: Product under mass production

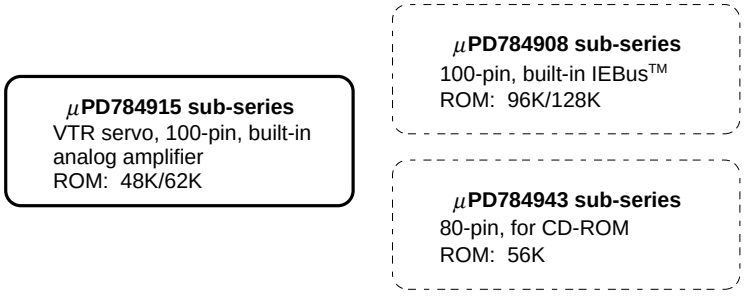
: Product under development

: Product under planning

Standard Products Development



ASSP Development



FUNCTIONS

Item \ Product			μPD784020	μPD784021
Number of basic instructions (mnemonics)			113	
General-purpose register			8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)	
Minimum instruction execution time			160 ns/320 ns/640 ns/1280 ns (at 25 MHz)	
Internal memory		ROM	None	
		RAM	512 bytes	2048 bytes
Memory space			Program and data: 1M byte	
I/O ports		Total	46	
		Input	8	
		Input/output	34	
		Output	4	
	Additional function pins**Note**	Pins with pull-up resistor	32	
		LED direct drive outputs	8	
		Transistor direct drive	8	
Real-time output ports			4 bits × 2, or 8 bits × 1	
Timer/counter			Timer/counter 0: (16 bits) — Timer register × 1, Capture register × 1, Compare register × 2 — Pulse output capability: • Toggle output • PWM/PPG output • One-shot pulse output	
			Timer/counter 1: (8/16 bits) — Timer register × 1, Capture register × 1, Capture/compare register × 1, Compare register × 1 — Pulse output capability: • Real-time output (4 bits × 2)	
			Timer/counter 2: (8/16 bits) — Timer register × 1, Capture register × 1, Capture/compare register × 1, Compare register × 1 — Pulse output capability: • Toggle output • PWM/PPG output	
			Timer 3 : (8/16 bits) — Timer register × 1, Compare register × 1	
PWM outputs			12-bit resolution × 2 channels	
Serial interface			UART/IOE (3-wire serial I/O) : 2 channels (incorporating baud rate generator) CSI (3-wire serial I/O, SBI) : 1 channel	
A/D converter			8-bit resolution × 8 channels	
D/A converter			8-bit resolution × 2 channels	
Watchdog timer			1 channel	
Standby			HALT/STOP/IDLE mode	
Interrupt		Source	23 (16 internal, 7 external (sampling clock variable input: 1)) + BRK instruction	
		Software	BRK instruction	
		Nonmaskable	1 internal, 1 external	
		Maskable	15 internal, 6 external	
			• 4-level programmable priority • 3 operation statuses: vectored interrupt, macro service, context switching	
Supply voltage			V_{DD} = 2.7 to 5.5 V	★
Package			80-pin plastic QFP (14 × 14 mm) 80-pin plastic TQFP (fine pitch) (12 × 12 mm): for the μPD784021 only	★

Note Additional function pins are included in the I/O pins.

CONTENTS

★ 1. DIFFERENCES BETWEEN μPD784026 SUB-SERIES

The only difference between the μPD784020, μPD784021, μPD784025, and μPD784026 is their capacity of internal memory, port functions, and part of their packages.

The μPD78P4026 is produced by replacing the masked ROM in the μPD784025 or μPD784026 with 64K-byte one-time PROM or EPROM. Table 1-1 shows the differences between these products.

Table 1-1 Differences between the μPD784026 Sub-Series

Item \ Product	μPD784020	μPD784021	μPD784025	μPD784026	μPD78P4026
Internal ROM	None		48K bytes (masked ROM)	64K bytes (masked ROM)	64K bytes (one-time PROM or EPROM)
Internal RAM	512 bytes	2048 bytes			
P40-P47	Functions only as an address/data bus		Can be switched to a general-purpose port or address/data bus, by using software		
P50-P57	Functions only as an address bus		Can be switched to a general-purpose port or address bus in units of 2 bits, by using software		
P60-P63	Can be switched to an output-only port or address bus in units of 2 bits, by using software				
P64, P65	Functions only as the $\overline{RD}$ or $\overline{WR}$ pin		Functions as the $\overline{RD}$ or $\overline{WR}$ pin when the local bus interface is used. Functions as a general-purpose port in other cases.		
Package	80-pin plastic QFP (14 × 14 mm)	80-pin plastic QFP (14 × 14 mm) 80-pin plastic TQFP (fine pitch) (12 × 12 mm)	80-pin plastic QFP (14 × 14 mm)		80-pin plastic QFP (14 × 14 mm) 80-pin ceramic WQFN (14 × 14 mm)

2. MAIN DIFFERENCES BETWEEN μPD784026 AND μPD78234 SUB-SERIES

Item \ Series		μPD784026 sub-series	μPD78234 sub-series
Number of basic instructions (mnemonics)		113	65
Minimum instruction execution time		160 ns (at 25 MHz)	333 ns (at 12 MHz)
Memory space (program/data)		1M byte in total	64K bytes/1M byte
Timer/counter		16-bit timer/counter × 1 8/16-bit timer/counter × 2 8/16-bit timer × 1	16-bit timer/counter × 1 8-bit timer/counter × 2 8-bit timer × 1
Clock output function		Available	Unavailable
Watchdog timer		Available	Unavailable
Serial interface		UART/IOE (3-wire serial I/O) × 2 channels CSI (3-wire serial I/O, SBI) × 1 channel	UART × 1 channel CSI (3-wire serial I/O, SBI) × 1 channel
Interrupt	Context switching	Available	Unavailable
	Priority	4 levels	2 levels
Standby function		3 modes (HALT, STOP, IDLE)	2 modes (HALT, STOP)
Operation clock switching		Selectable from $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, or $f_{XX}/16$	Fixed to $f_{XX}/2$
Pin functions	MODE pin	Unavailable	To specify ROM-less mode (always in the high level for the μPD78233 or μPD78237)
	TEST pin	Pin for testing the device Low level during ordinary use	Unavailable
Package		80-pin plastic QFP (14 × 14 mm) 80-pin plastic TQFP (fine pitch) (12 × 12 mm): for the μPD784021 only 80-pin ceramic WQFN (14 × 14 mm): for the μPD78P4026 only	80-pin plastic QFP (14 × 14 mm) 94-pin plastic QFP (20 × 20 mm) 84-pin plastic QFJ (1150 × 1150 mil) 94-pin ceramic WQFN (20 × 20 mm): for the μPD78P238 only

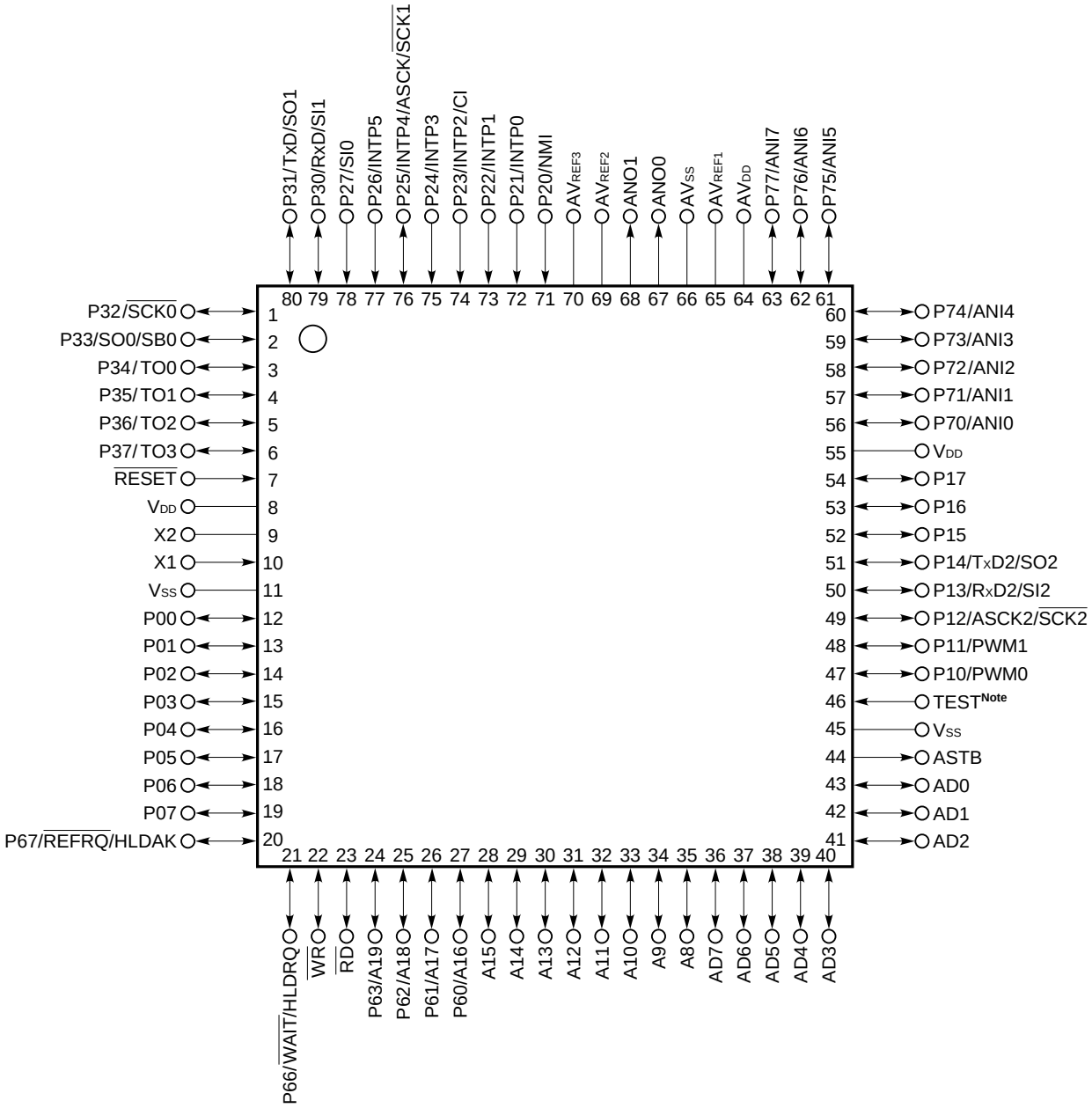
3. PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 × 14 mm)

★ μPD784020GC-3B9, μPD784021GC-3B9

- 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

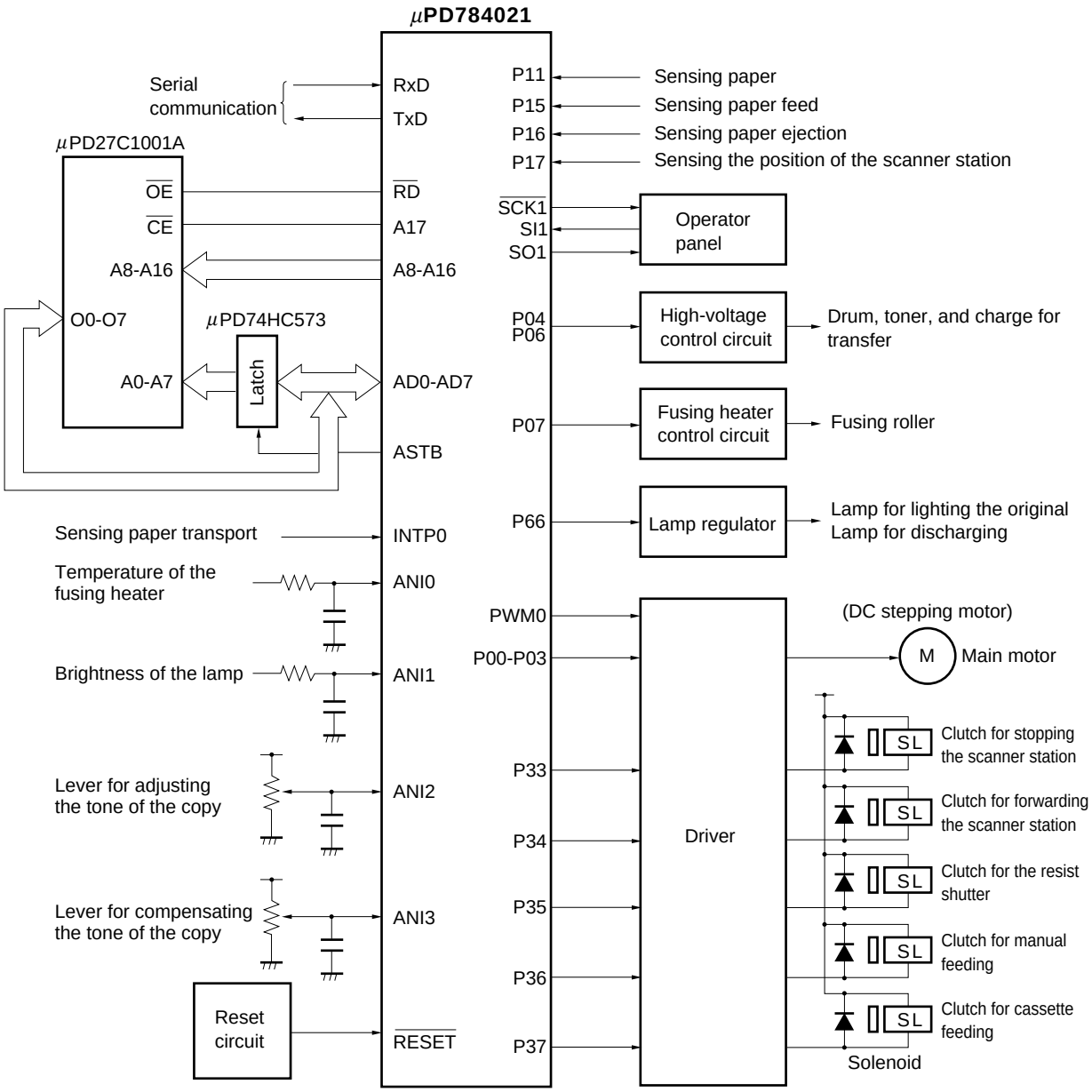
★ μPD784021GK-BE9



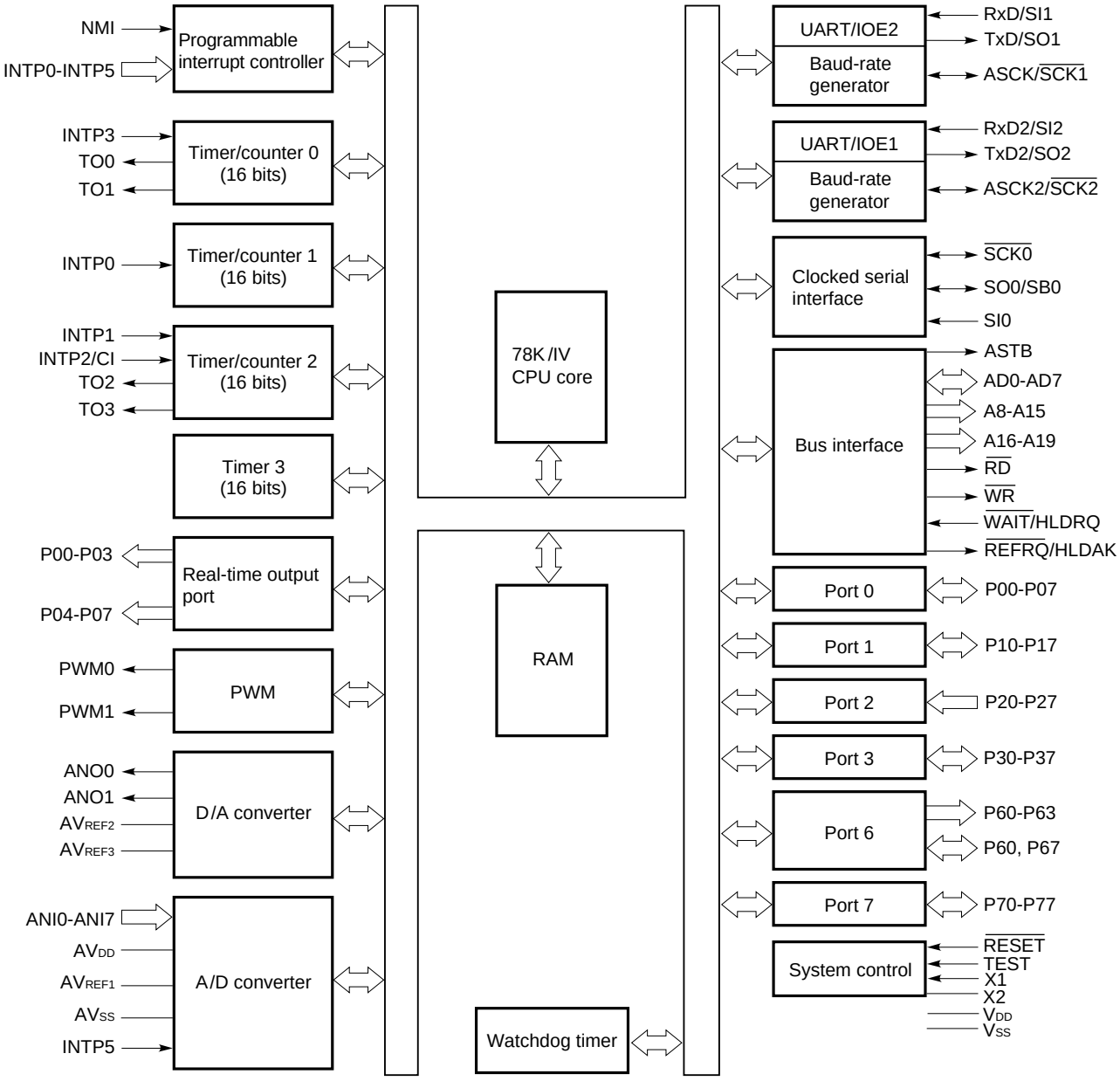
Note Connect the TEST pin to VSS directly.

P00-P07	:	Port 0
P10-P17	:	Port 1
P20-P27	:	Port 2
P30-P37	:	Port 3
P60-P63, P66, P67	:	Port 6
P70-P77	:	Port 7
TO0-TO3	:	Timer output
CI	:	Clock input
RxD, RxD2	:	Receive data
TxD, TxD2	:	Transmit data
$\overline{SCK0}$-$\overline{SCK2}$	:	Serial clock
ASCK, ASCK2	:	Asynchronous serial clock
SI0-SI2	:	Serial input
SO0-SO2	:	Serial output
SB0	:	Serial bus
PWM0, PWM1	:	Pulse width modulation output
NMI	:	Non-maskable interrupt
INTP0-INTP5	:	Interrupt from peripherals
AD0-AD7	:	Address/data bus
A8-A19	:	Address bus
$\overline{RD}$	:	Read strobe
$\overline{WR}$	:	Write strobe
$\overline{WAIT}$	:	Wait
HLDRQ	:	Hold request
HLDAK	:	Hold acknowledge
ASTB	:	Address strobe
$\overline{REFRQ}$	:	Refresh request
$\overline{RESET}$	:	Reset
X1, X2	:	Crystal
ANI0-ANI7	:	Analog input
ANO0, ANO1	:	Analog output
AV_{REF1}-AV_{REF3}	:	Reference voltage
AV_{DD}	:	Analog power supply
AV_{SS}	:	Analog ground
V_{DD}	:	Power supply
V_{SS}	:	Ground
TEST	:	Test

4. SYSTEM CONFIGURATION EXAMPLE (PPC)



5. BLOCK DIAGRAM



Remark The internal ROM or RAM capacity differs for each product.

6. LIST OF PIN FUNCTIONS

6.1 PORT PINS

Pin	I/O	Dual-function	Function
P00-P07	I/O	—	Port 0 (P0): • 8-bit I/O port • Functions as a real-time output port (4 bits × 2). • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • Can drive a transistor.
P10	I/O	PWM0	Port 1 (P1): • 8-bit I/O port • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • Can drive LED.
P11		PWM1	
P12		ASCK2/$\overline{\text{SCK2}}$	
P13		RxD2/SI2	
P14		TxD2/SO2	
P15-P17		—	
P20	Input	NMI	Port 2 (P2): • 8-bit input-only port • P20 does not function as a general-purpose port (nonmaskable interrupt). However, the input level can be checked by an interrupt service routine. • The use of the pull-up resistors can be specified by software for pins P22 to P27 (in units of 6 bits). • The P25/INTP4/ASCK/$\overline{\text{SCK1}}$ pin functions as the $\overline{\text{SCK1}}$ output pin by CSIM1.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK/$\overline{\text{SCK1}}$	
P26		INTP5	
P27		SI0	
P30	I/O	RxD/SI1	Port 3 (P3): • 8-bit I/O port • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together.
P31		TxD/SO1	
P32		$\overline{\text{SCK0}}$	
P33		SO0/SB0	
P34-P37		TO0-TO3	
P60-P63	I/O	A16-A19	Port 6 (P6): • P60 to P63 are an output-only port. • Inputs and outputs can be specified bit by bit for pins P66 and P67. • The use of the pull-up resistors can be specified by software for the pins in the input mode together.
P66		$\overline{\text{WAIT}}$/HLDRQ	
P67		$\overline{\text{REFRQ}}$/HLDAK	
P70-P77	I/O	ANI0-ANI7	Port 7 (P7): • 8-bit I/O port • Inputs and outputs can be specified bit by bit.

6.2 NON-PORT PINS (1/2)

Pin	I/O	Dual-function	Function	
TO0-TO3	Output	P34-P37	Timer output	
CI	Input	P23/INTP2	Input of a count clock for timer/counter 2	
RxD	Input	P30/SI1	Serial data input (UART0)	
RxD2		P13/SI2	Serial data input (UART2)	
TxD	Output	P31/SO1	Serial data output (UART0)	
TxD2		P14/SO2	Serial data output (UART2)	
ASCK	Input	P25/INTP4/$\overline{\text{SCK1}}$	Baud rate clock input (UART0)	
ASCK2		P12/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)	
SB0	I/O	P33/SO0	Serial data I/O (SBI)	
SI0	Input	P27	Serial data input (3-wire serial I/O0)	
SI1		P30/RxD	Serial data input (3-wire serial I/O1)	
SI2		P13/RxD2	Serial data input (3-wire serial I/O2)	
SO0	Output	P33/SB0	Serial data output (3-wire serial I/O0)	
SO1		P31/TxD	Serial data output (3-wire serial I/O1)	
SO2		P14/TxD2	Serial data output (3-wire serial I/O2)	
$\overline{\text{SCK0}}$	I/O	P32	Serial clock I/O (3-wire serial I/O0, SBI)	
$\overline{\text{SCK1}}$		P25/INTP4/ASCK	Serial clock I/O (3-wire serial I/O1)	
$\overline{\text{SCK2}}$		P12/ASCK2	Serial clock I/O (3-wire serial I/O2)	
NMI	Input	P20	External interrupt request	—
INTP0		P21		• Input of a count clock for timer/counter 1 • Capture/trigger signal for CR11 or CR12
INTP1		P22		• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR22
INTP2		P23/CI		• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR21
INTP3		P24		• Input of a count clock for timer/counter 0 • Capture/trigger signal for CR02
INTP4		P25/ASCK/$\overline{\text{SCK1}}$		—
INTP5		P26		Input of a conversion start trigger for A/D converter
AD0-AD7	I/O	—	Time multiplexing address/data bus (for connecting external memory)	
A8-A15	Output	—	High-order address bus (for connecting external memory)	
A16-A19	Output	P60-P63	High-order address bus during address expansion (for connecting external memory)	
$\overline{\text{RD}}$	Output	—	Strobe signal output for reading the contents of external memory	
$\overline{\text{WR}}$	Output	—	Strobe signal output for writing on external memory	
$\overline{\text{WAIT}}$	Input	P66/HLDRQ	Wait signal insertion	
$\overline{\text{REFRQ}}$	Output	P67/HLDAK	Refresh pulse output to external pseudo static memory	
HLDRQ	Input	P66/$\overline{\text{WAIT}}$	Input of bus hold request	
HLDAK	Output	P67/$\overline{\text{REFRQ}}$	Output of bus hold response	
ASTB	Output	—	Latch timing output of time multiplexing address (A0-A7) (for connecting external memory)	

6.2 NON-PORT PINS (2/2)

Pin	I/O	Dual-function	Function
$\overline{\text{RESET}}$	Input	—	Chip reset
X1	Input	—	Crystal input for system clock oscillation (A clock pulse can also be input to the X1 pin.)
X2	—		
ANI0-ANI7	Input	P70-P77	Analog voltage inputs for the A/D converter
ANO0, ANO1	Output	—	Analog voltage inputs for the D/A converter
AV_{REF1}	—	—	Application of A/D converter reference voltage
AV_{REF2}, AV_{REF3}			Application of D/A converter reference voltage
AV_{DD}			Positive power supply for the A/D converter
AV_{SS}			Ground for the A/D converter
V_{DD}			Positive power supply
V_{SS}			Ground
TEST			Directly connect to V_{SS}. (The TEST pin is for the IC test.)

6.3 I/O CIRCUITS FOR PINS AND HANDLING OF UNUSED PINS

Table 6-1 describes the types of I/O circuits for pins and the handling of unused pins.

Fig. 6-1 shows the configuration of these various types of I/O circuits.

Table 6-1 Types of I/O Circuits for Pins and Handling of Unused Pins (1/2)

Pin	I/O circuit type	I/O	Recommended connection method for unused pins
P00-P07	5-A	I/O	Input state : To be connected to V_{DD} Output state: To be left open
P10/PWM0 P11/PWM1			
P12/ASCK2/$\overline{SCK2}$	8-A		
P13/RxD2/SI2	5-A		
P14/TxD2/SO2			
P15-P17			
P20/NMI	2	Input	To be connected to V_{DD} or V_{SS}
P21/INTP0			
P22/INTP1	2-A		To be connected to V_{DD}
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK/$\overline{SCK1}$	8-A	I/O	Input state : To be connected to V_{DD} Output state: To be left open
P26/INTP5	2-A	Input	To be connected to V_{DD}
P27/SI0			
P30/RxD/SI1	5-A	I/O	Input state : To be connected to V_{DD} Output state: To be left open
P31/TxD/SO1			
P32/$\overline{SCK0}$	8-A		
P33/SO0/SB0	10-A		
P34/TO0-P37/TO3	5-A		
AD0-AD7			
A8-A15		Output[Note]	To be left open
P60/A16-P63/A19			
$\overline{RD}$			
$\overline{WR}$			
P66/$\overline{WAIT}$/HLDRQ		I/O	Input state : To be connected to V_{DD} Output state: To be left open
P67/$\overline{REFRQ}$/HLDAK			
P70/ANI0-P77/ANI7	20		Input state : To be connected to V_{DD} or V_{SS} Output state: To be left open
ANO0, ANO1	12	Output	To be left open
ASTB	4		

Note These pins function as output-only pins depending on the internal circuit, though their I/O type is 5-A.

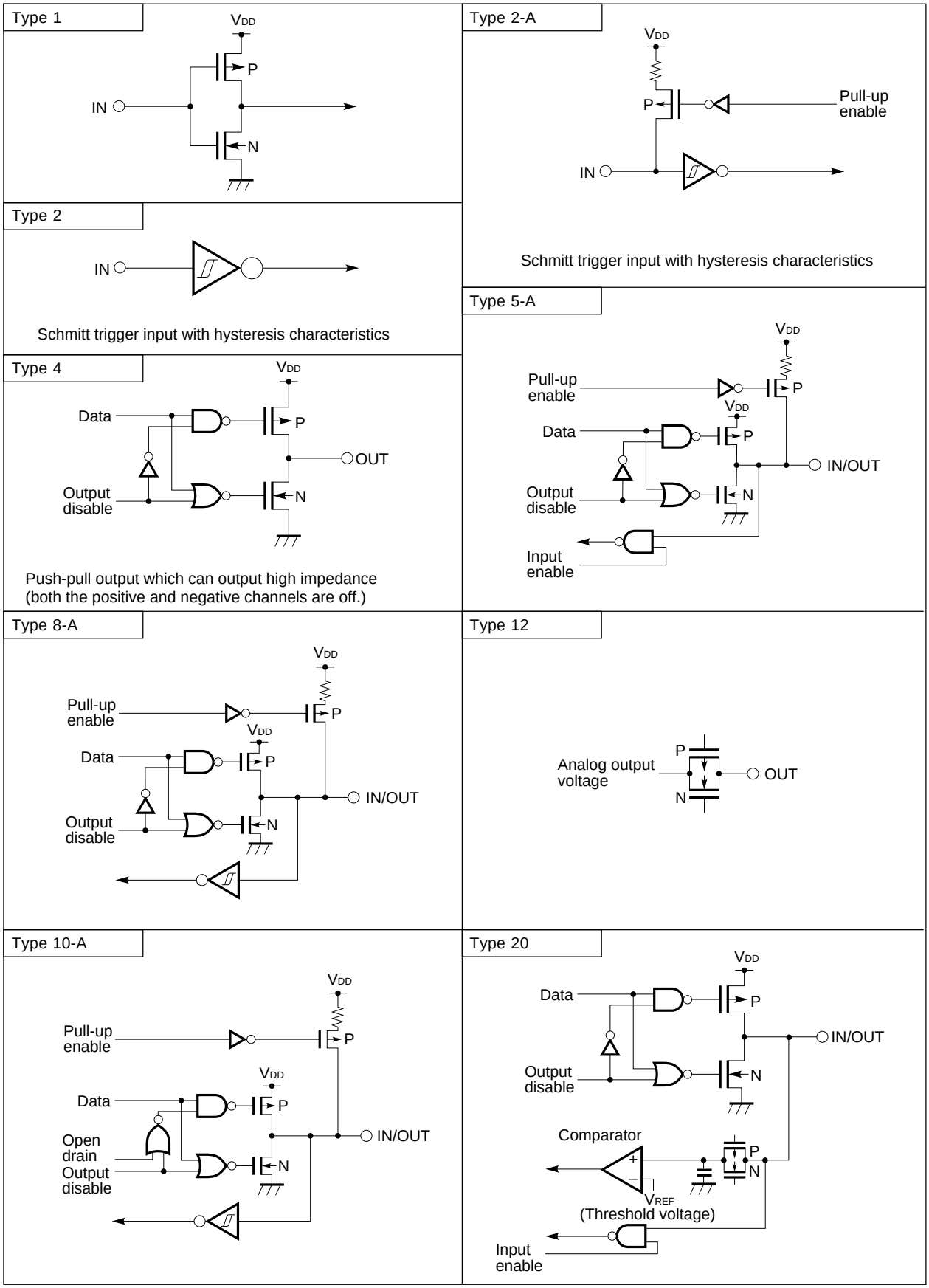
Table 6-1 Types of I/O Circuits for Pins and Handling of Unused Pins (2/2)

Pin	I/O circuit type	I/O	Recommended connection method for unused pins
$\overline{\text{RESET}}$	2	Input	—
TEST	1		To be connected to V_{SS} directly
AV_{REF1}-AV_{REF3}	—		To be connected to V_{SS}
AV_{SS}			
AV_{DD}			To be connected to V_{DD}

Caution When the I/O mode of an I/O dual-function pin is unpredictable, connect the pin to V_{DD} through a resistor of 10 to 100 kilohms (particularly when the voltage of the reset input pin becomes higher than that of the low level input at power-on or when I/O is switched by software).

Remark Since type numbers are consistent in the 78K series, those numbers are not always serial in each product. (Some circuits are not included.)

Fig. 6-1 I/O Circuits for Pins



7. CPU ARCHITECTURE

7.1 MEMORY SPACE

A 1M-byte memory space can be accessed. By using a LOCATION instruction, the mode for mapping internal data areas (special function registers and internal RAM) can be selected. A LOCATION instruction must always be executed after a reset, and can be used only once.

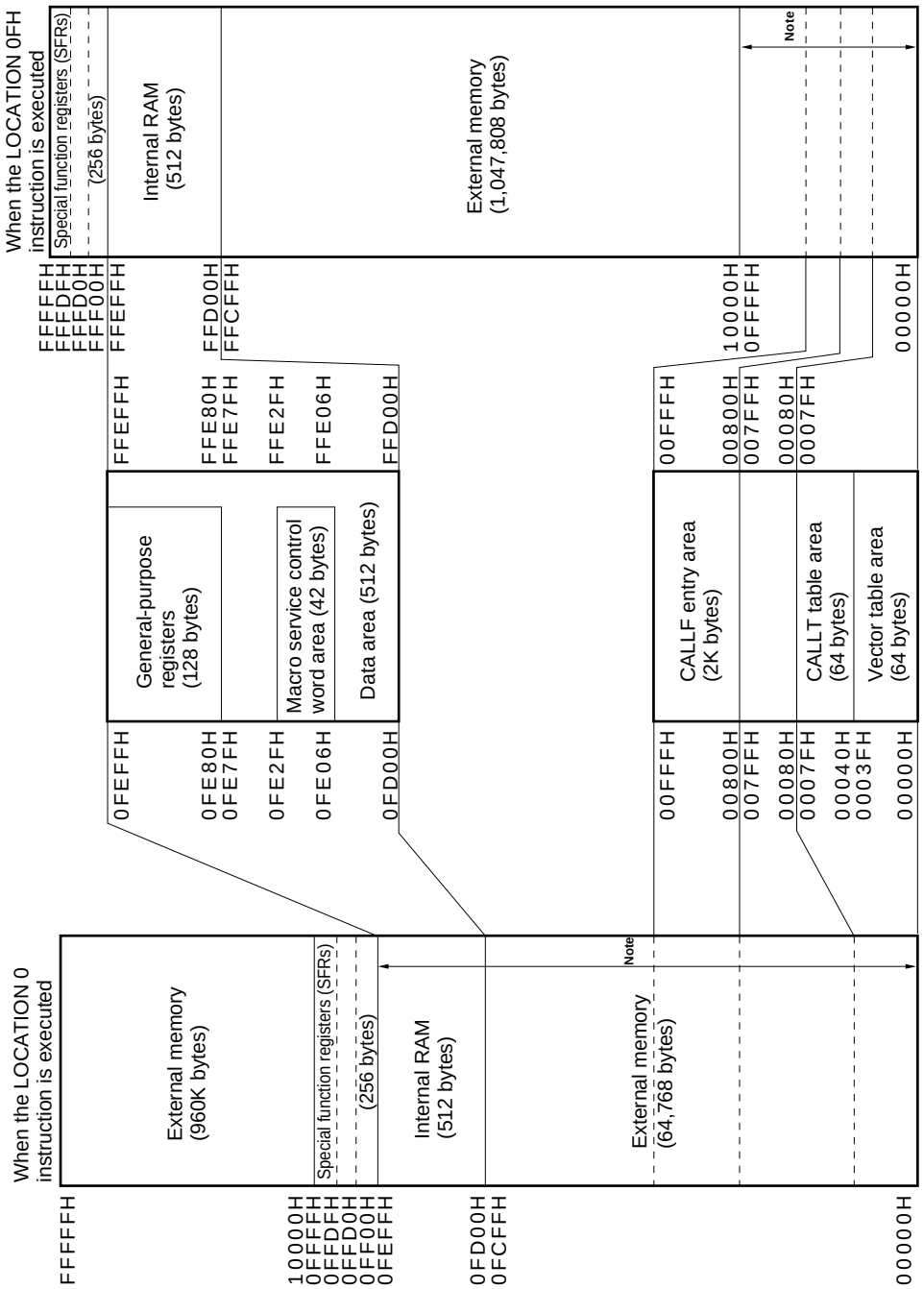
(1) When the LOCATION 0 instruction is executed

Internal data areas are mapped to 0FD00H-0FFFFH for the μPD784020 and 0F700H-0FFFFH for the μPD784021.

(2) When the LOCATION 0FH instruction is executed

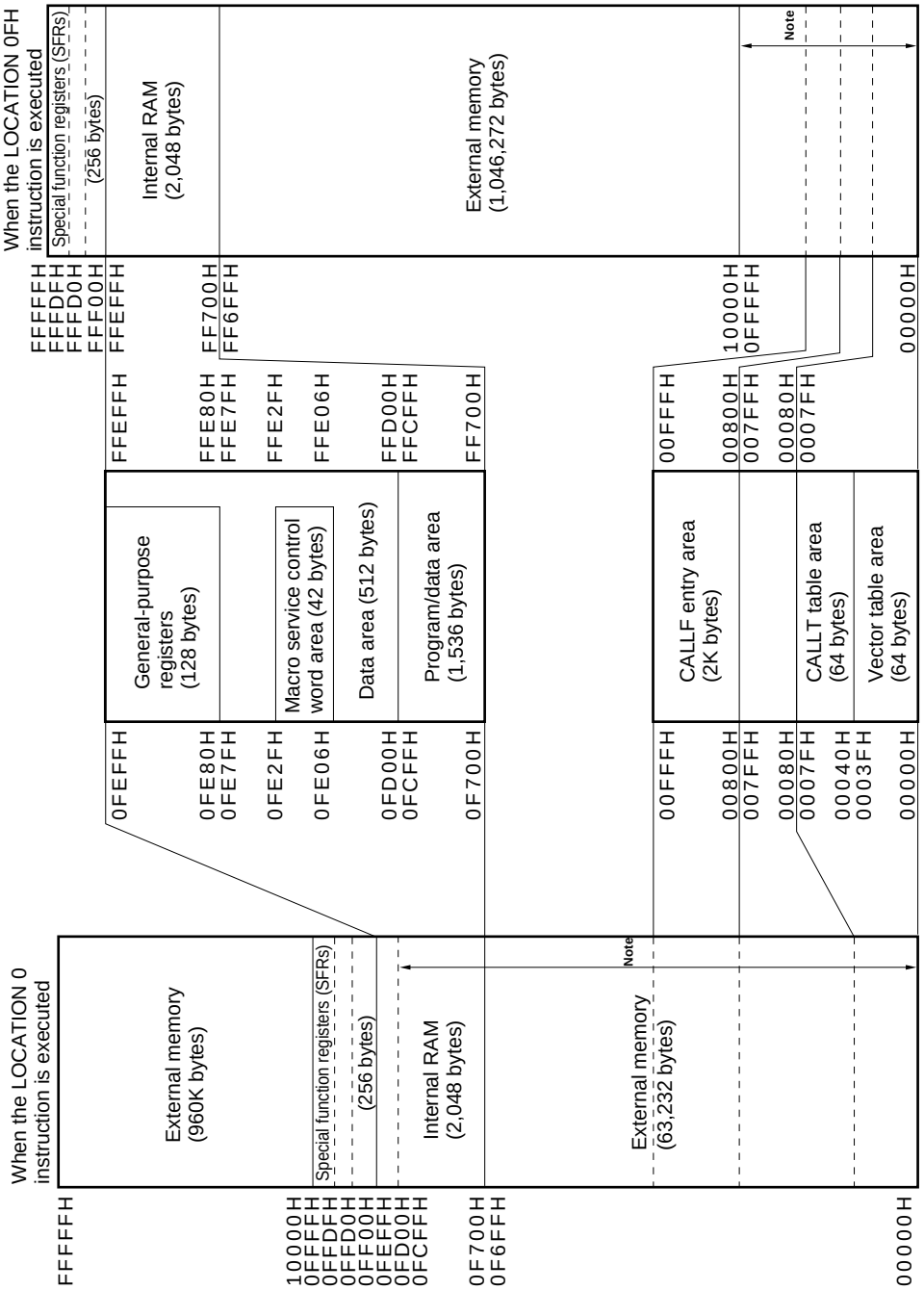
Internal data areas are mapped to FFD00H-FFFFFH for the μPD784020 and FF700H-FFFFFH for the μPD784021.

Fig. 7-1 μPD784020 Memory Map★



Note Base area, or entry area based on a reset or interrupt. Internal RAM is excluded in the case of a reset.

Fig. 7-2 μPD784021 Memory Map



Note Base area, or entry area based on a reset or interrupt. Internal RAM is excluded in the case of a reset.

7.2 CPU REGISTERS

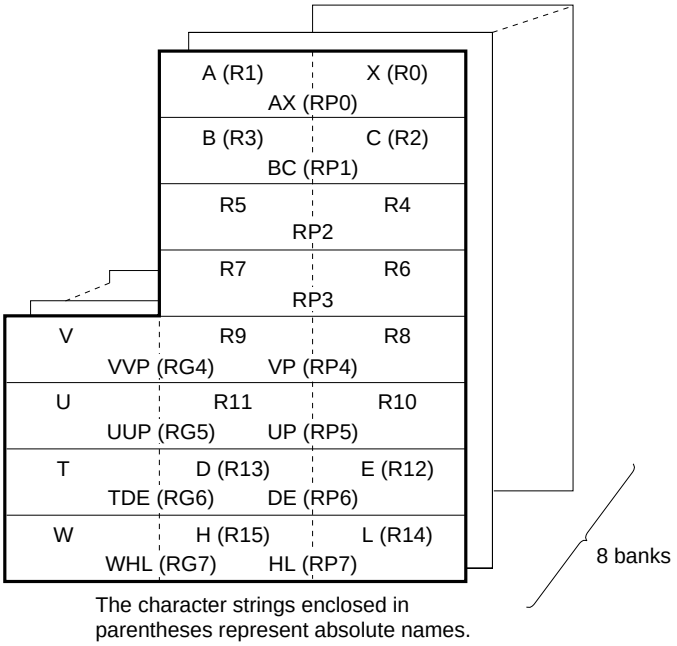
7.2.1 General-Purpose Registers

A set of general-purpose registers consists of sixteen general-purpose 8-bit registers. Two 8-bit general-purpose registers can be combined to form a 16-bit general-purpose register. Moreover, four 16-bit general-purpose registers, when combined with an 8-bit register for address extension, can be used as 24-bit address specification registers.

Eight banks of this register set are provided. The user can switch between banks by software or the context switching function.

General-purpose registers other than the V, U, T, and W registers used for address extension are mapped onto internal RAM.

Fig. 7-3 General-Purpose Register Format



The character strings enclosed in parentheses represent absolute names.

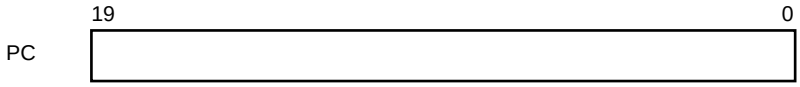
Caution By setting the RSS bit of PSW to 1, R4, R5, R6, R7, RP2, and RP3 can be used as the X, A, C, B, AX, and BC registers, respectively. However, this function must be used only when using programs for the 78K/III series.

7.2.2 Control Registers

(1) Program counter (PC)

This register is a 20-bit program counter. The program counter is automatically updated by program execution.

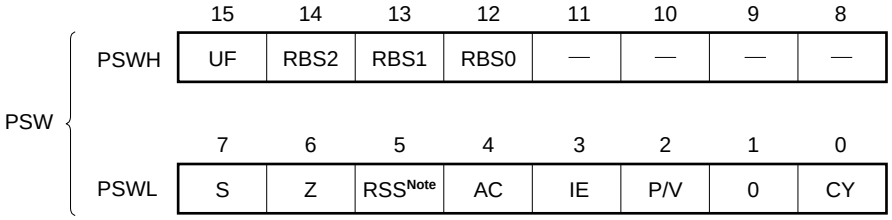
Fig. 7-4 Format of Program Counter (PC)



(2) Program Status Word (PSW)

This register holds the CPU state. The program status word is automatically updated by program execution.

Fig. 7-5 Format of Program Status Word (PSW)

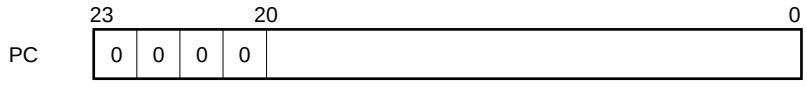


Note This flag is used to maintain compatibility with the 78K/III series. This flag must be set to 0 when programs for the 78K/III series are being used.

(3) Stack pointer (SP)

This register is a 24-bit pointer for holding the start address of the stack. The high-order 4 bits must be set to 0.

Fig. 7-6 Format of Stack Pointer (SP)



7.2.3 Special Function Registers (SFRs) ★

The special function registers are registers with special functions such as mode registers and control registers for built-in peripheral hardware. The special function registers are mapped onto the 256-byte space between 0FF00H and 0FFFFH[Note].

Note Applicable when the LOCATION 0 instruction is executed. FFF00H-FFFFFH when the LOCATION 0FH instruction is executed.

Caution Never attempt to access addresses in this area where no SFR is allocated. Otherwise, the μPD784021 may be placed in the deadlock state. The deadlock state can be cleared only by a reset.

Table 7-1 lists the special function registers (SFRs). The titles of the table columns are explained below.

- Abbreviation ..... Symbol used to represent a built-in SFR. The abbreviations listed in the table are reserved words for the NEC assembler (RA78K4). The C compiler (CC78K4) allows the abbreviations to be used as sfr variables of bit type with the #pragma sfr command.
- R/W ..... Indicates whether each SFR allows read and/or write operations.
  R/W : Allows both read and write operations.
  R : Allows read operations only.
  W : Allows write operations only.
- Manipulatable bits ..... Indicates the maximum number of bits that can be manipulated whenever an SFR is manipulated. An SFR that supports 16-bit manipulation can be described in the sfr operand. For address specification, an even-numbered address must be specified.
  An SFR that supports 1-bit manipulation can be described in a bit manipulation instruction.
- When reset ..... Indicates the state of each register when $\overline{\text{RESET}}$ is applied.

Table 7-1 Special Function Registers (SFRs) (1/4)

Address[Note]	Special function register (SFR) name	Abbreviation		R/W	Manipulatable bits			When reset
					1 bit	8 bits	16 bits	
0FF00H	Port 0	P0		R/W	●	●	–	Undefined
0FF01H	Port 1	P1			●	●	–	
0FF02H	Port 2	P2		R	●	●	–	
0FF03H	Port 3	P3		R/W	●	●	–	
0FF06H	Port 6	P6			●	●	–	00H
0FF07H	Port 7	P7			●	●	–	Undefined
0FF0EH	Port 0 buffer register L	P0L			●	●	–	
0FF0FH	Port 0 buffer register H	P0H			●	●	–	
0FF10H	Compare register (timer/counter 0)	CR00			–	–	●	
0FF12H	Capture/compare register (timer/counter 0)	CR01			–	–	●	
0FF14H	Compare register L (timer/counter 1)	CR10	CR10W		–	●	●	
0FF15H	Compare register H (timer/counter 1)	–			–	–		
0FF16H	Capture/compare register L (timer/counter 1)	CR11	CR11W		–	●	●	
0FF17H	Capture/compare register H (timer/counter 1)	–			–	–		
0FF18H	Compare register L (timer/counter 2)	CR20	CR20W		–	●	●	
0FF19H	Compare register H (timer/counter 2)	–			–	–		
0FF1AH	Capture/compare register L (timer/counter 2)	CR21	CR21W		–	●	●	
0FF1BH	Capture/compare register H (timer/counter 2)	–			–	–		
0FF1CH	Compare register L (timer 3)	CR30	CR30W		–	●	●	
0FF1DH	Compare register H (timer 3)	–			–	–		
0FF20H	Port 0 mode register	PM0			●	●	–	FFH
0FF21H	Port 1 mode register	PM1			●	●	–	
0FF23H	Port 3 mode register	PM3			●	●	–	
0FF26H	Port 6 mode register	PM6			●	●	–	
0FF27H	Port 7 mode register	PM7			●	●	–	
0FF2EH	Real-time output port control register	RTPC			●	●	–	00H
0FF30H	Capture/compare control register 0	CRC0			–	●	–	10H
0FF31H	Timer output control register	TOC			●	●	–	00H
0FF32H	Capture/compare control register 1	CRC1			–	●	–	
0FF33H	Capture/compare control register 2	CRC2			–	●	–	10H

Note Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

Table 7-1 Special Function Registers (SFRs) (2/4)

Address[Note]	Special function register (SFR) name	Abbreviation		R/W	Manipulatable bits			When reset
					1 bit	8 bits	16 bits	
0FF36H	Capture register (timer/counter 0)	CR02		R	–	–	●	0000H
0FF38H	Capture register L (timer/counter 1)	CR12	CR12W		–	●	●	
0FF39H	Capture register H (timer/counter 1)	–			–	–		
0FF3AH	Capture register L (timer/counter 2)	CR22	CR22W		–	●	●	
0FF3BH	Capture register H (timer/counter 2)	–			–	–		
0FF41H	Port 1 mode control register	PMC1		R/W	●	●	–	00H
0FF43H	Port 3 mode control register	PMC3			●	●	–	
0FF4EH	Register for optional pull-up resistor	PUO			●	●	–	
0FF50H	Timer register 0	TM0		R	–	–	●	0000H
0FF51H					–	–		
0FF52H	Timer register 1	TM1	TM1W		–	●	●	
0FF53H		–			–	–		
0FF54H	Timer register 2	TM2	TM2W		–	●	●	
0FF55H		–			–	–		
0FF56H	Timer register 3	TM3	TM3W		–	●	●	
0FF57H		–			–	–		
0FF5CH	Prescaler mode register 0	PRM0		R/W	–	●	–	11H
0FF5DH	Timer control register 0	TMC0			●	●	–	00H
0FF5EH	Prescaler mode register 1	PRM1			–	●	–	11H
0FF5FH	Timer control register 1	TMC1			●	●	–	00H
0FF60H	D/A conversion value setting register 0	DACS0			–	●	–	
0FF61H	D/A conversion value setting register 1	DACS1			–	●	–	
0FF62H	D/A converter mode register	DAM			●	●	–	03H
0FF68H	A/D converter mode register	ADM			●	●	–	00H
0FF6AH	A/D conversion result register	ADCR		R	–	●	–	Undefined
0FF70H	PWM control register	PWMC		R/W	●	●	–	05H
0FF71H	PWM prescaler register	PWPR			–	●	–	00H
0FF72H	PWM modulo register 0	PWM0			–	–	●	Undefined
0FF74H	PWM modulo register 1	PWM1			–	–	●	
0FF7DH	One-shot pulse output control register	OSPC			●	●	–	00H
0FF80H	Serial bus interface control register	SBIC			●	●	–	
0FF82H	Synchronous serial interface mode register	CSIM			●	●	–	

Note Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

Table 7-1 Special Function Registers (SFRs) (3/4)

Address[Note 1]	Special function register (SFR) name	Abbreviation	R/W	Manipulatable bits			When reset
				1 bit	8 bits	16 bits	
0FF84H	Synchronous serial interface mode register 1	CSIM1	R/W	●	●	–	00H
0FF85H	Synchronous serial interface mode register 2	CSIM2		●	●	–	
0FF86H	Serial shift register	SIO		–	●	–	
0FF88H	Asynchronous serial interface mode register	ASIM		●	●	–	
0FF89H	Asynchronous serial interface mode register 2	ASIM2		●	●	–	
0FF8AH	Asynchronous serial interface status register	ASIS	R	●	●	–	
0FF8BH	Asynchronous serial interface status register 2	ASIS2		●	●	–	
0FF8CH	Serial receive buffer: UART0	RXB		–	●	–	Undefined
	Serial transmission shift register: UART0	TXS	W	–	●	–	
	Serial shift register: IOE1	SIO1	R/W	–	●	–	
0FF8DH	Serial receive buffer: UART2	RXB2	R	–	●	–	
	Serial transmission shift register: UART2	TXS2	W	–	●	–	
	Serial shift register: IOE2	SIO2	R/W	–	●	–	
0FF90H	Baud rate generator control register	BRGC		–	●	–	00H
0FF91H	Baud rate generator control register 2	BRGC2		–	●	–	
0FFA0H	External interrupt mode register 0	INTM0		●	●	–	
0FFA1H	External interrupt mode register 1	INTM1		●	●	–	
0FFA4H	Sampling clock selection register	SCS0		–	●	–	
0FFA8H	In-service priority register	ISPR	R	●	●	–	
0FFAAH	Interrupt mode control register	IMC	R/W	●	●	–	80H
0FFACH	Interrupt mask register 0L	MK0L (MK0)		●	●	●	FFFFH
0FFADH	Interrupt mask register 0H	MK0H		●	●		
0FFAEH	Interrupt mask register 1L	MK1L		●	●	–	FFH
0FFC0H	Standby control register	STBC		–	●[Note 2]	–	30H
0FFC2H	Watchdog timer mode register	WDM		–	●[Note 2]	–	00H
0FFC4H	Memory expansion mode register	MM		●	●	–	20H
0FFC5H	Hold mode register	HLDM		●	●	–	00H
0FFC6H	Clock output mode register	CLOM		●	●	–	
0FFC7H	Programmable wait control register 1	PWC1		–	●	–	AAH
0FFC8H	Programmable wait control register 2	PWC2		–	–	●	AAAAH

Notes 1. Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

2. A write operation can be performed only with special instructions MOV STBC,#byte and MOV WDM,#byte. Other instructions cannot perform a write operation.

Table 7-1 Special Function Registers (SFRs) (4/4)

Address[Note]	Special function register (SFR) name	Abbreviation	R/W	Manipulatable bits			When reset
				1 bit	8 bits	16 bits	
0FFCCH	Refresh mode register	RFM	R/W	●	●	–	00H
0FFCDH	Refresh area specification register	RFA		●	●	–	
0FFCFH	Oscillation settling time specification register	OSTS		–	●	–	
0FFD0H-0FFDFH	External SFR area	–		●	●	–	–
0FFE0H	Interrupt control register (INTP0)	PIC0		●	●	–	43H
0FFE1H	Interrupt control register (INTP1)	PIC1		●	●	–	
0FFE2H	Interrupt control register (INTP2)	PIC2		●	●	–	
0FFE3H	Interrupt control register (INTP3)	PIC3		●	●	–	
0FFE4H	Interrupt control register (INTC00)	CIC00		●	●	–	
0FFE5H	Interrupt control register (INTC01)	CIC01		●	●	–	
0FFE6H	Interrupt control register (INTC10)	CIC10		●	●	–	
0FFE7H	Interrupt control register (INTC11)	CIC11		●	●	–	
0FFE8H	Interrupt control register (INTC20)	CIC20		●	●	–	
0FFE9H	Interrupt control register (INTC21)	CIC21		●	●	–	
0FFEAH	Interrupt control register (INTC30)	CIC30		●	●	–	
0FFEBH	Interrupt control register (INTP4)	PIC4		●	●	–	
0FFECH	Interrupt control register (INTP5)	PIC5		●	●	–	
0FFEDH	Interrupt control register (INTAD)	ADIC		●	●	–	
0FFEEH	Interrupt control register (INTSER)	SERIC		●	●	–	
0FFEFH	Interrupt control register (INTSR)	SRIC		●	●	–	
	Interrupt control register (INTCSI1)	CSIIC1		●	●	–	
0FFF0H	Interrupt control register (INTST)	STIC		●	●	–	
0FFF1H	Interrupt control register (INTCSI)	CSIIC		●	●	–	
0FFF2H	Interrupt control register (INTSER2)	SERIC2		●	●	–	
0FFF3H	Interrupt control register (INTSR2)	SRIC2		●	●	–	
	Interrupt control register (INTCSI2)	CSIIC2		●	●	–	
0FFF4H	Interrupt control register (INTST2)	STIC2		●	●	–	

Note Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

8. PERIPHERAL HARDWARE FUNCTIONS

8.1 PORTS

The ports shown in Fig. 8-1 are provided to enable the application of wide-ranging control. Table 8-1 lists the functions of the ports. For the inputs to port 0 to port 6, a built-in pull-up resistor can be specified by software.

Fig. 8-1 Port Configuration

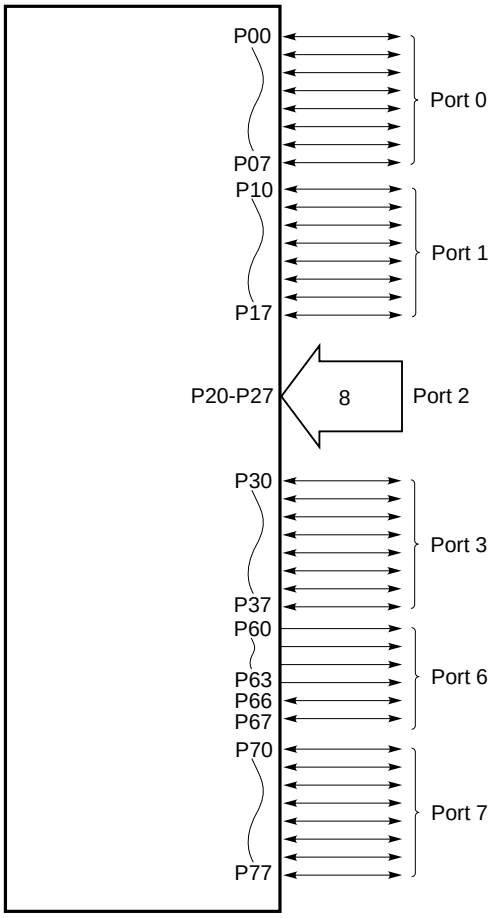


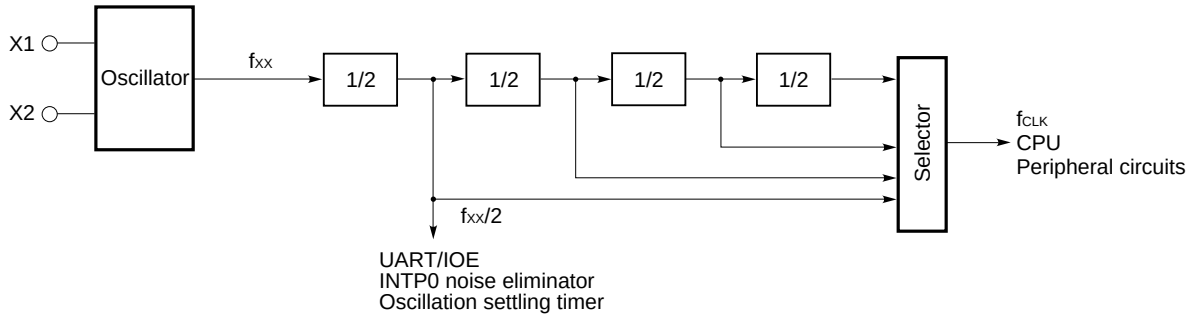
Table 8-1 Port Functions

Port name	Pin	Function	Pull-up specification by software
Port 0	P00-P07	• Bit-by-bit input/output setting supported • Operable as 4-bit real-time outputs (P00-P03, P04-P07) • Capable of driving transistors	Specified as a batch for all pins placed in input mode.
Port 1	P10-P17	• Bit-by-bit input/output setting supported • Capable of driving LEDs	Specified as a batch for all pins placed in input mode.
Port 2	P20-P27	• Input port	Specified for the 6 bits (P22-P27) as a batch.
Port 3	P30-P37	• Bit-by-bit input/output setting supported	Specified as a batch for all pins placed in input mode.
Port 6	P60-P63	• Output-only port	Specified as a batch for all pins placed in input mode.
	P66, P67	• Bit-by-bit input/output setting supported	
Port 7	P70-P77	• Bit-by-bit input/output setting supported	—

8.2 CLOCK GENERATOR

A circuit for generating the clock signal required for operation is provided. The clock generator includes a frequency divider; low current consumption can be achieved by operating at a lower internal frequency when high-speed operation is not necessary.

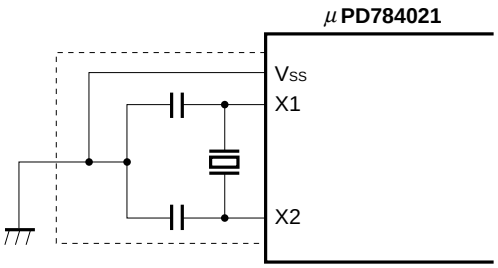
Fig. 8-2 Block Diagram of Clock Generator



Remark f_{XX} : Oscillator frequency or external clock input
f_{CLK}: Internal operating frequency

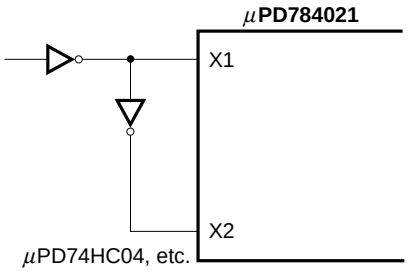
Fig. 8-3 Examples of Using Oscillator

(1) Crystal/ceramic oscillation

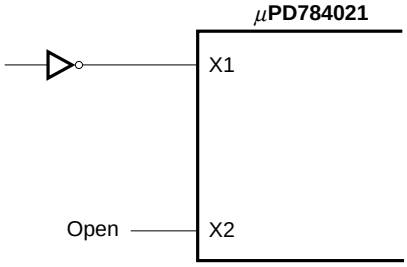


★ **(2) External clock**

- **When EXTC bit of OSTS = 1**



- **When EXTC bit of OSTS = 0**



Caution When using the clock generator, to avoid problems caused by influences such as stray capacitance, run all wiring within the area indicated by the dotted lines according to the following rules:

- **Minimize the wiring length.**
- **Wires must never cross other signal lines.**
- **Wires must never run near a line carrying a large varying current.**
- **The grounding point of the capacitor of the oscillator circuit must always be at the same potential as V_{SS}. Never connect the capacitor to a ground pattern carrying a large current.**
- **Never extract a signal from the oscillator circuit.**

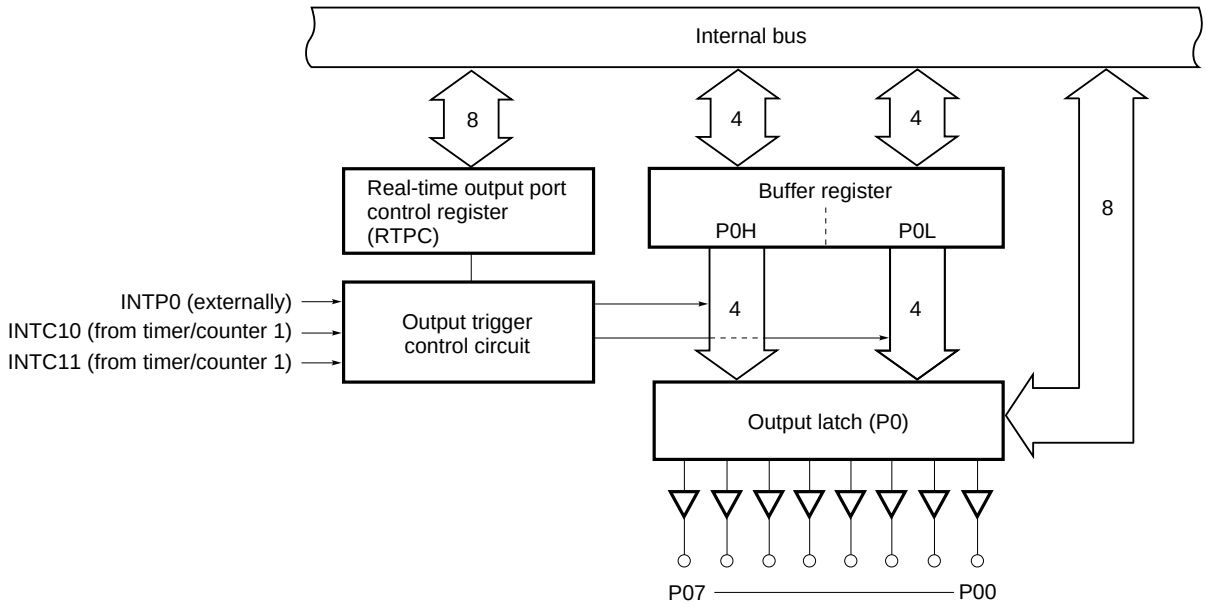
8.3 REAL-TIME OUTPUT PORT

The real-time output port outputs data stored in the buffer, synchronized with a timer/counter 1 match interrupt or external interrupt. Thus, pulse output that is free of jitter can be obtained.

Therefore, the real-time output port is best suited to applications (such as open-loop control over stepping motors) where an arbitrary pattern is output at arbitrary intervals.

As shown in Fig. 8-4, the real-time output port is built around port 0 and the port 0 buffer register (P0H, P0L).

Fig. 8-4 Block Diagram of Real-Time Output Port



8.4 TIMERS/COUNTERS

Three timer/counter units and one timer unit are incorporated.

Moreover, seven interrupt requests are supported, allowing these units to function as seven timer/counter units.

Table 8-2 Timer/Counter Operation

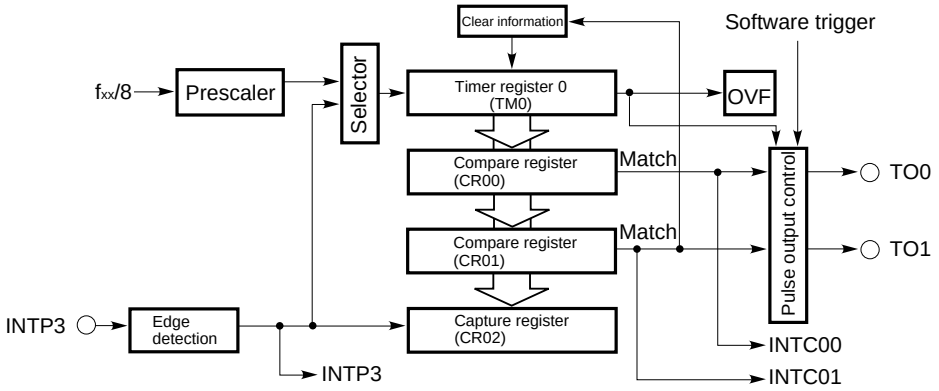
Item \ Name		Timer/counter 0	Timer/counter 1	Timer/counter 2	Timer 3
Count pulse width	8 bits	–	●	●	●
★	16 bits	●	●	●	●
Operating mode	Interval timer	2ch	2ch	2ch	1ch
	External event counter	●	●	●	–
	One-shot timer	–	–	●	–
Function	Timer output	2ch	–	2ch	–
	Toggle output	●	–	●	–
	PWM/PPG output	●	–	●	–
	One-shot pulse output[Note]	●	–	–	–
	Real-time output	–	●	–	–
	Pulse width measurement	1 input	1 input	2 inputs	–
	Number of interrupt requests	2	2	2	1

Note The one-shot pulse output function makes the level of a pulse output active by software, and makes the level of a pulse output inactive by hardware (interrupt request signal).

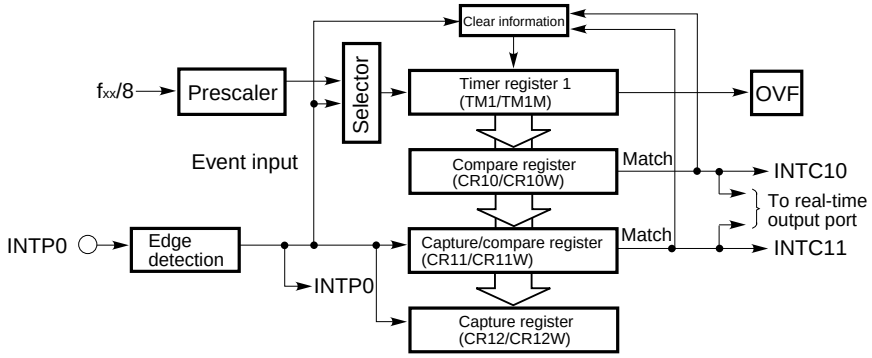
Note that this function differs from the one-shot timer function of timer/counter 2.

Fig. 8-5 Timer/Counter Block Diagram ★

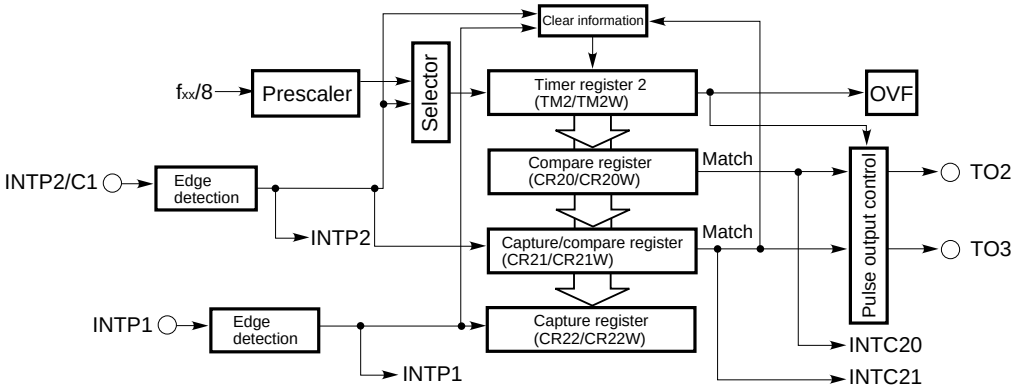
Timer/counter 0



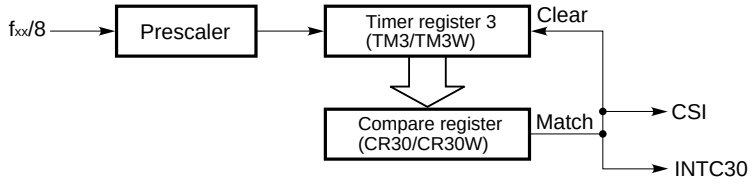
Timer/counter 1



Timer/counter 2



Timer 3

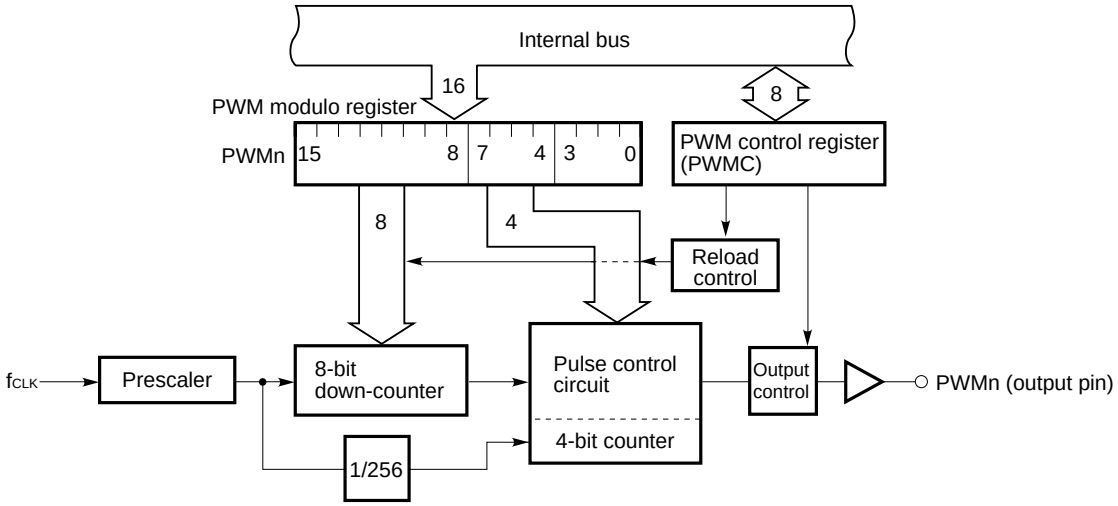


Remark OVF: Overflow flag

8.5 PWM OUTPUT (PWM0, PWM1)

Two channels of PWM (pulse width modulation) output circuitry with a resolution of 12 bits and a repetition frequency of 48.8 kHz (f_{CLK} = 12.5 MHz) are incorporated. Low or high active level can be selected for the PWM output channels, independently of each other. This output is best suited to DC motor speed control.

Fig. 8-6 Block Diagram of PWM Output Unit



Remark n = 0, 1

8.6 A/D CONVERTER

An analog/digital (A/D) converter having 8 multiplexed analog inputs (ANI0-ANI7) is incorporated.

The successive approximation system is used for conversion. The result of conversion is held in the 8-bit A/D conversion result register (ADCR). Thus, speedy high-precision conversion can be achieved. (The conversion time is about 10 μs at f_{CLK} = 12.5 MHz.)

A/D conversion can be started in any of the following modes:

- Hardware start: Conversion is started by means of trigger input (INTP5).
- Software start : Conversion is started by means of bit setting the A/D converter mode register (ADM).

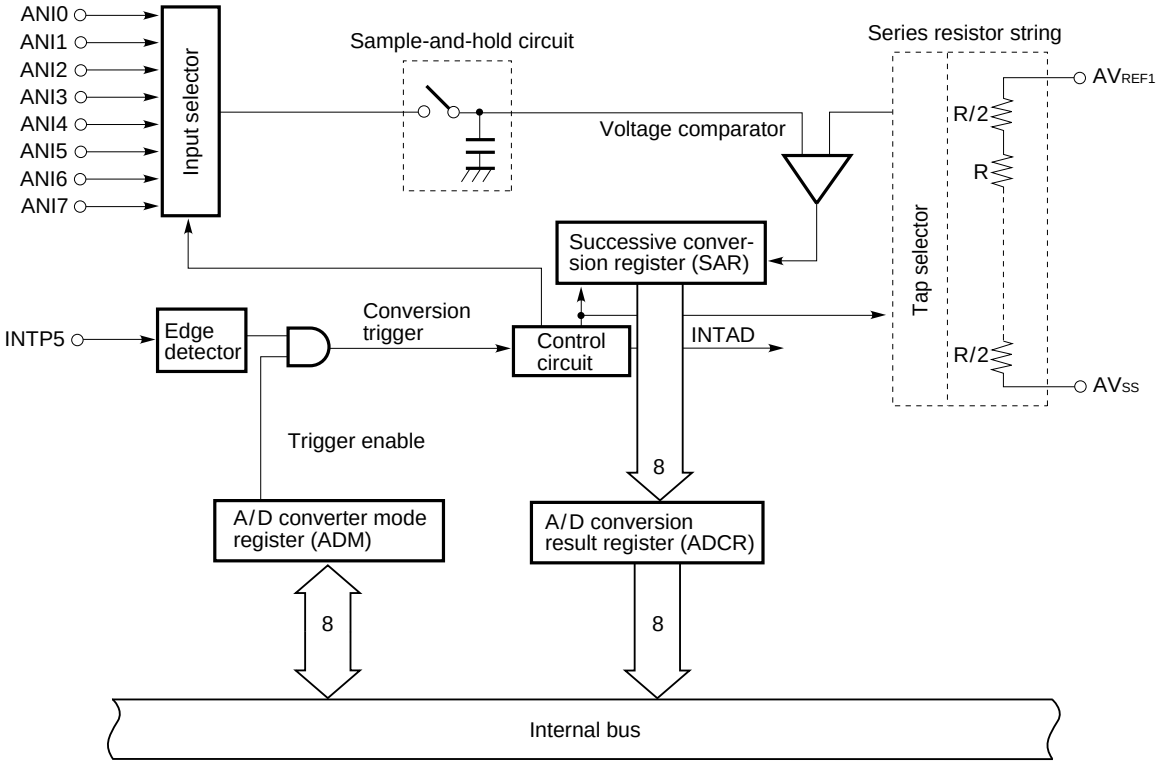
After conversion has started, one of the following modes can be selected:

- Scan mode : Multiple analog inputs are selected sequentially to obtain conversion data from all pins.
- Select mode: A single analog input is selected at all times to enable conversion data to be obtained continuously.

ADM is used to specify the above modes, as well as the termination of conversion.

When the result of conversion is transferred to ADCR, an interrupt request (INTAD) is generated. Using this feature, the results of conversion can be continuously transferred to memory by the macro service.

Fig. 8-7 Block Diagram of A/D Converter



8.7 D/A CONVERTER

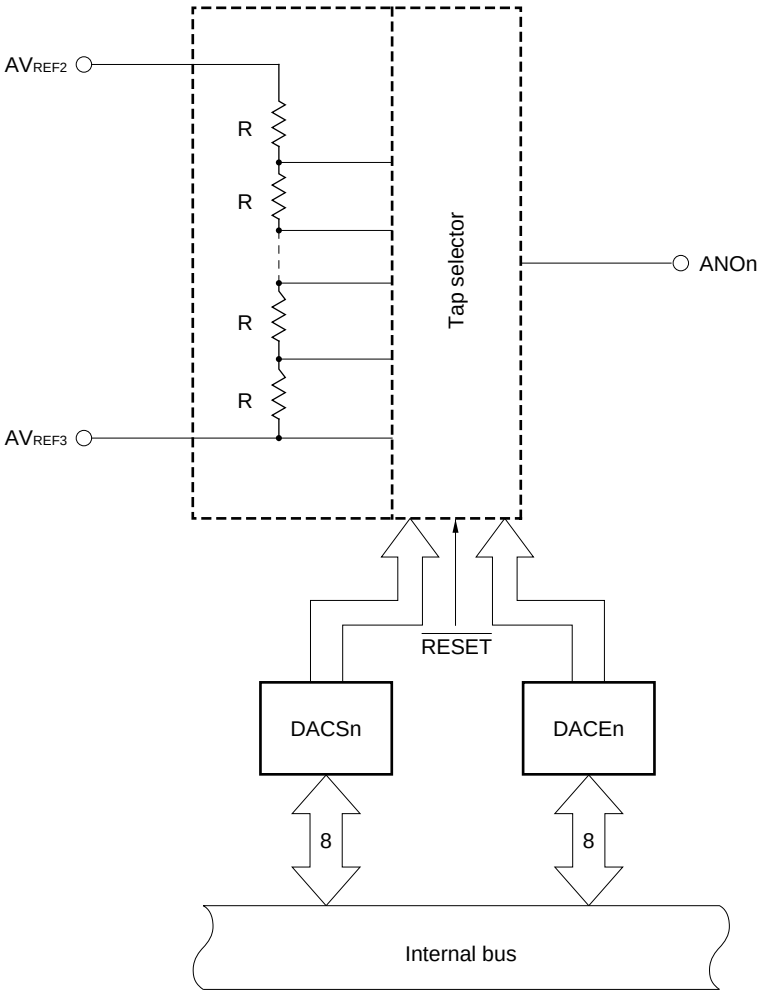
Two digital/analog (D/A) converter channels of voltage output type, having a resolution of 8 bits, are incorporated.

A resistor string system is used for conversion. By writing the value to be subject to D/A conversion in the 8-bit D/A conversion value setting register (DACSn: n = 0, 1), the resulting analog value is output on ANOn (n = 0, 1). The range of the output voltages is determined by the voltages applied to the AV_{REF2} and AV_{REF3} pins.

Because of its high output impedance, no current can be obtained from an output pin. When the load impedance is low, insert a buffer amplifier between the load and the converter.

The impedance of the ANOn pin goes high while the $\overline{\text{RESET}}$ signal is low. DACSn is set to 0 after a reset is released.

Fig. 8-8 Block Diagram of D/A Converter



Remark n = 0, 1

8.8 SERIAL INTERFACE

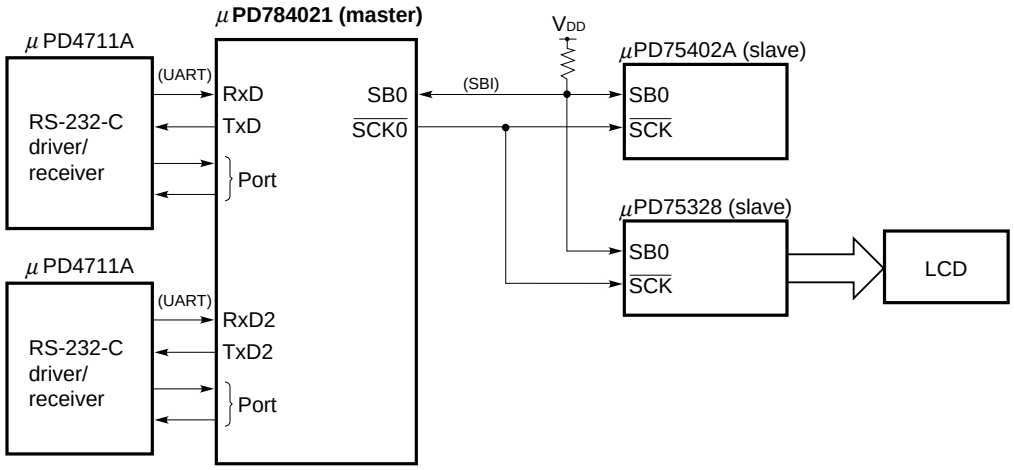
Three independent serial interface channels are incorporated.

- Asynchronous serial interface (UART)/three-wire serial I/O (IOE) × 2
- Synchronous serial interface (CSI) × 1
  - Three-wire serial I/O (IOE)
  - Serial bus interface (SBI)

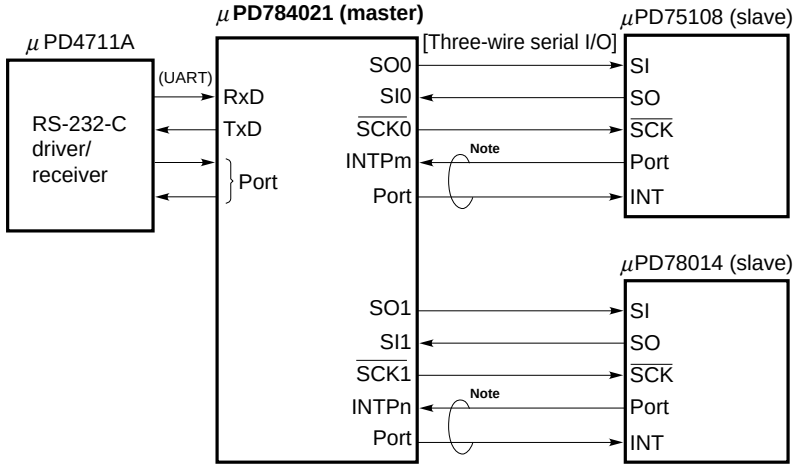
So, communication with points external to the system and local communication within the system can be performed at the same time. (See **Fig. 8-9**.)

Fig. 8-9 Example Serial Interfaces

(a) UART + SBI



(b) UART + Three-wire serial I/O



Note Handshake line

8.8.1 Asynchronous Serial Interface/Three-Wire Serial I/O (UART/IOE)

Two serial interface channels are available; for each channel, asynchronous serial interface mode or three-wire serial I/O mode can be selected.

(1) Asynchronous serial interface mode

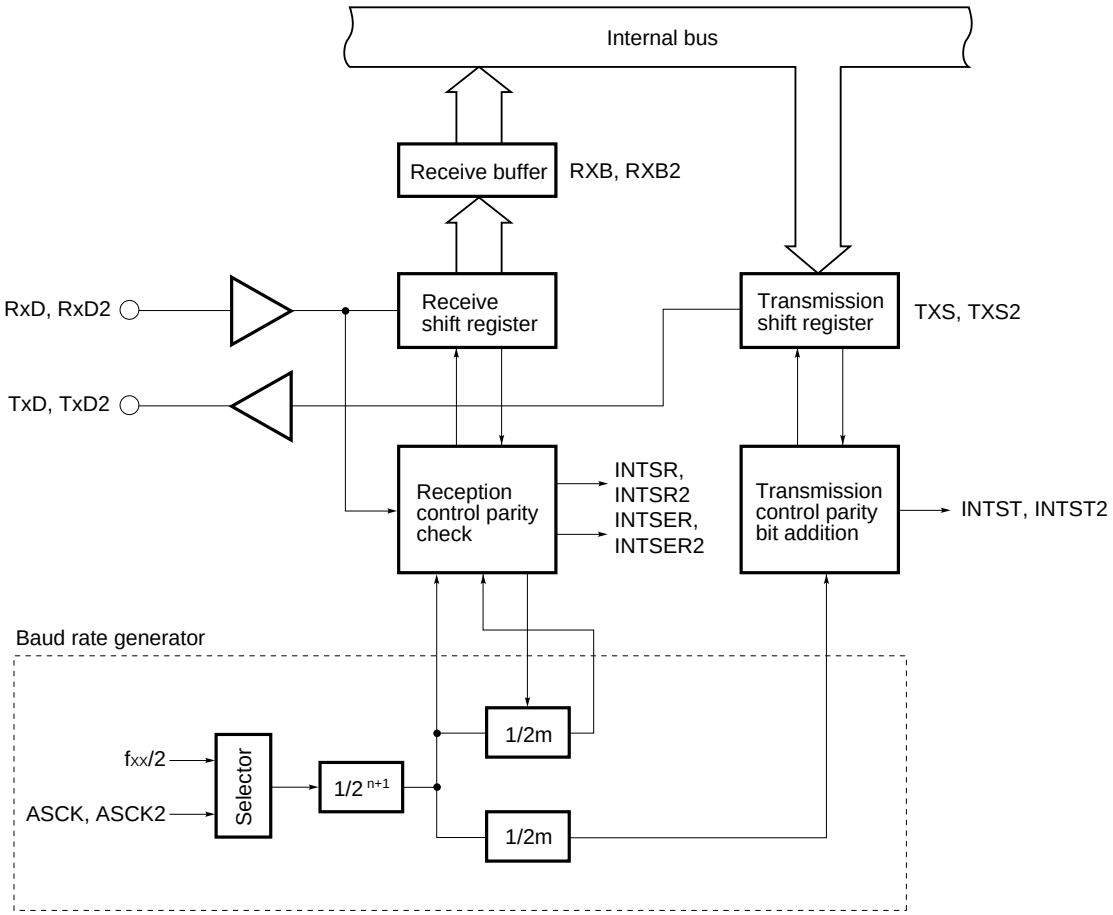
In this mode, 1-byte data is transferred after a start bit.

A baud rate generator is incorporated to enable communication at a wide range of baud rates.

Moreover, the frequency of a clock signal applied to the ASCK pin can be divided to define a baud rate.

With the baud rate generator, the baud rate conforming to the MIDI standard (31.25 kbps) can be obtained.

Fig. 8-10 Block Diagram of Asynchronous Serial Interface Mode



Remark f_{XX}: Oscillator frequency or external clock input

n = 0 to 11

m = 16 to 30

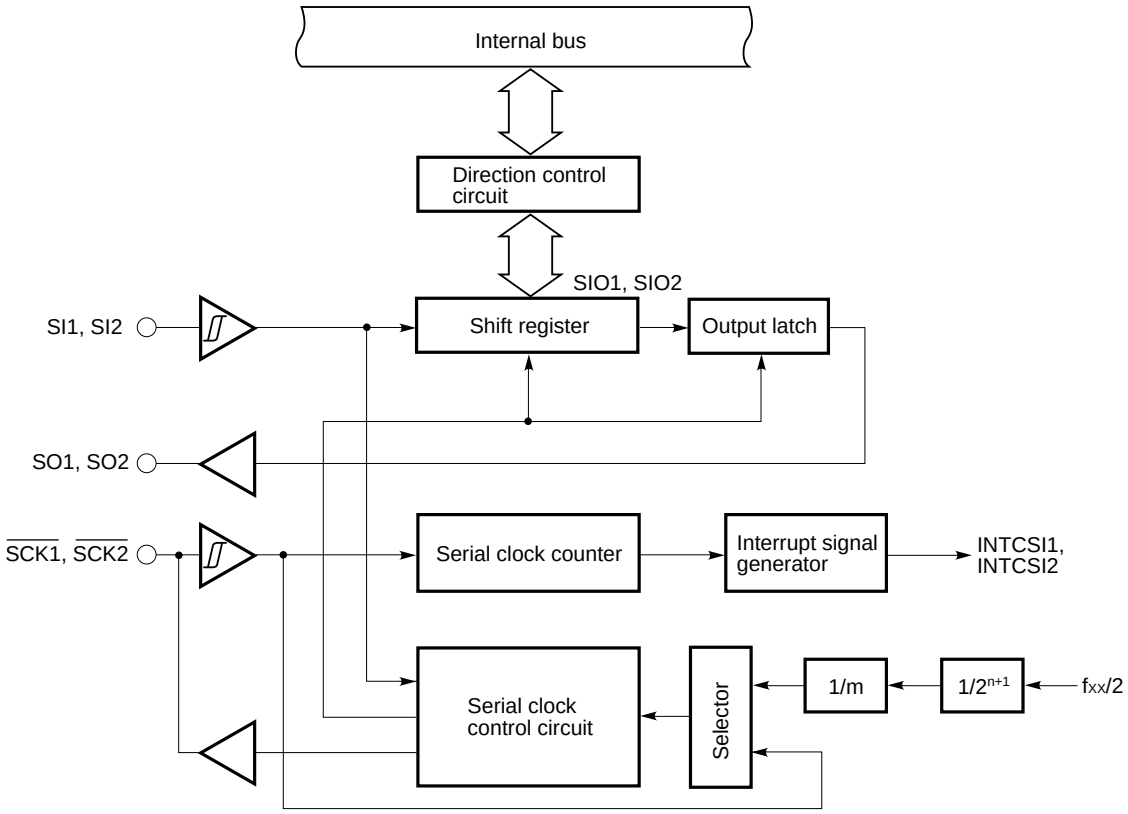
(2) Three-wire serial I/O mode

In this mode, the master device makes the serial clock active to start transmission, then transfers 1-byte data in phase with the clock.

This mode is designed for communication with a device incorporating a conventional synchronous serial interface. Basically, three lines are used for communication: the serial clock line ($\overline{SCK}$) and the two serial data lines (SI and SO).

In general, a handshake line is required to check the state of communication.

Fig. 8-11 Block Diagram of Three-Wire Serial I/O Mode



Remark f_{XX}: Oscillator frequency or external clock input

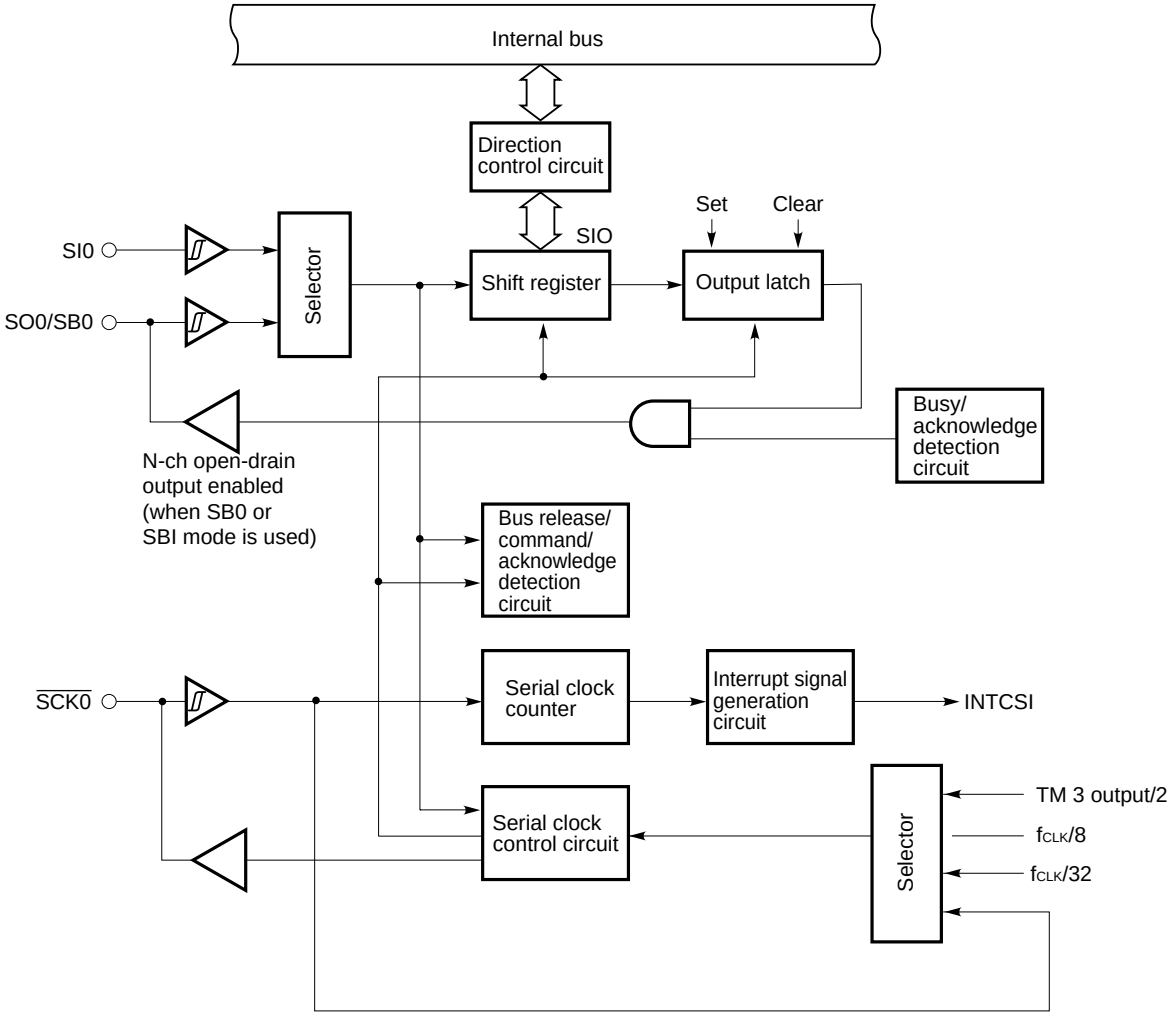
n = 0 to 11

m = 1, 16 to 30

8.8.2 Synchronous Serial Interface (CSI)

With this interface, the master device makes the serial clock active to start transmission, then transfers 1-byte data in phase with the clock.

Fig. 8-12 Block Diagram of Synchronous Serial Interface



Remark f_{CLK}: Internal system clock frequency (system clock frequency/2)

(1) Three-wire serial I/O mode

This mode is designed for communication with a device incorporating a conventional synchronous serial interface. Basically, three lines are used for communication: the serial clock line ($\overline{SCK0}$) and serial data lines (SI0 and SO0). In general, a handshake line is required to check the state of communication.

(2) SBI mode

The SBI mode allows communication with more than one device via two lines: the serial clock ($\overline{SCK0}$) and serial bus (SB0). The SBI mode is the standard NEC serial interface.

A master device outputs an address through the SB0 pin to select a slave device with which communication is to be performed. After a target device is selected, commands and data are transmitted between the master device and slave device.

8.9 EDGE DETECTION FUNCTION

The interrupt input pins (NMI, INTP0-INTP5) are used to apply not only interrupt requests but also trigger signals for the built-in circuits. As these pins are triggered by an edge (rising or falling) of an input signal, a function for edge detection is incorporated. Moreover, a noise suppression function is provided to prevent erroneous edge detection caused by noise.

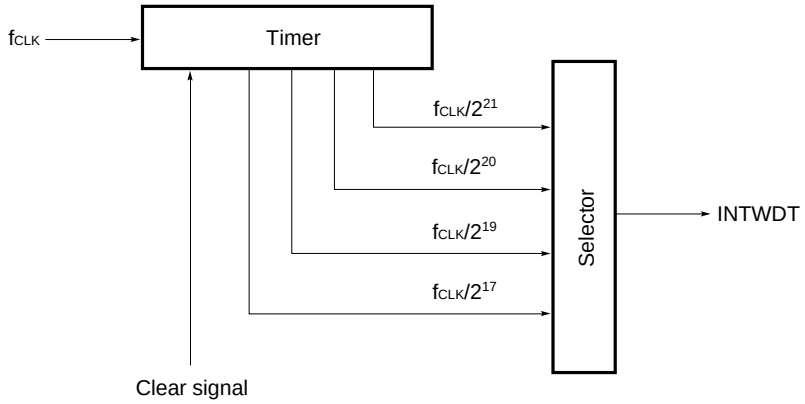
Pin	Detectable edge	Noise suppression method
NMI	Rising edge or falling edge	Analog delay
INTP0-INTP3	Rising edge or falling edge, or both edges	Clock sampling**Note**
INTP4, INTP5		Analog delay

Note INTP0 is used for sampling clock selection.

8.10 WATCHDOG TIMER

A watchdog timer is incorporated for CPU runaway detection. The watchdog timer, if not cleared by software within a specified interval, generates a nonmaskable interrupt. Furthermore, once watchdog timer operation is enabled, it cannot be disabled by software. The user can specify whether priority is placed on an interrupt based on the watchdog timer or on an interrupt based on the NMI pin.

★ **Fig. 8-13 Block Diagram of Watchdog Timer**



9. INTERRUPT FUNCTION

Table 9-1 lists the interrupt request handling modes. These modes are selected by software.

Table 9-1 Interrupt Request Handling Modes

Handling mode	Handled by	Handling	PC and PSW contents
Vectored interrupt	Software	Branches to a handling routine for execution (arbitrary handling).	The PC and PSW contents are pushed to and popped from the stack.
Context switching		Automatically selects a register bank, and branches to a handling routine for execution (arbitrary handling).	The PC and PSW contents are saved to and read from a fixed area in the register bank.
Macro service	Firmware	Performs operations such as memory-to-I/O-device data transfer (fixed handling).	Maintained

9.1 INTERRUPT SOURCE

An interrupt can be issued from any one of the interrupt sources listed in Table 9-2: execution of a BRK instruction, an operand error, or any of the 23 other interrupt sources.

Four levels of interrupt handling priority can be set. Priority levels can be set to nest control during interrupt handling or to concurrently generate interrupt requests. Nested macro services, however, are performed without suspension.

When interrupt requests having the same priority level are generated, they are handled according to the default priority (fixed). (See **Table 9-2**.)

Table 9-2 Interrupt Sources

Type	Default priority	Source		Internal/ external	Macro service
		Name	Trigger		
Software	–	BRK instruction	Instruction execution	–	–
		Operand error	When the MOV STBC,#byte or MOV WDM,#byte instruction is executed, exclusive OR of the byte operand and $\overline{\text{byte}}$ does not produce FFH.		
Nonmaskable	–	NMI	Detection of edge input on the pin	External	–
★		WDT	Watchdog timer overflow	Internal	
Maskable	0 (highest)	INTP0	Detection of edge input on the pin (TM1/TM1W capture trigger)	External	Enabled
	1	INTP1	Detection of edge input on the pin (TM2/TM2W capture trigger)		
	2	INTP2	Detection of edge input on the pin (TM2/TM2W event counter input)		
	3	INTP3	Detection of edge input on the pin (TM0 capture trigger)		
	4	INTC00	TM0-CR00 match signal issued	Internal	Enabled
	5	INTC01	TM0-CR01 match signal issued		
	6	INTC10	TM1-CR10 match signal issued (in 8-bit operation mode) TM1W-CR10W match signal issued (in 16-bit operation mode)		
	7	INTC11	TM1-CR11 match signal issued (in 8-bit operation mode) TM1W-CR11W match signal issued (in 16-bit operation mode)		
	8	INTC20	TM2-CR20 match signal issued (in 8-bit operation mode) TM2W-CR20W match signal issued (in 16-bit operation mode)		
	9	INTC21	TM2-CR21 match signal issued (in 8-bit operation mode) TM2W-CR21W match signal issued (in 16-bit operation mode)		
	10	INTC30	TM3-CR30 match signal issued (in 8-bit operation mode) TM3W-CR30W match signal issued (in 16-bit operation mode)		
	11	INTP4	Detection of edge input on the pin	External	Enabled
	12	INTP5	Detection of edge input on the pin		
	13	INTAD	A/D converter processing completed (ADCR transfer)	Internal	Enabled
	14	INTSER	ASI0 reception error		–
	15	INTSR	ASI0 reception completed or CSI1 transfer completed		Enabled
		INTCSI1			
	16	INTST	ASI0 transmission completed		
	17	INTCSI	CSI0 transfer completed		
	18	INTSER2	ASI2 reception error		–
	19	INTSR2	ASI2 reception completed or CSI2 transfer completed		Enabled
		INTCSI2			
	20 (lowest)	INTST2	ASI2 transmission completed		

Remark ASI: Asynchronous serial interface
CSI: Synchronous serial interface

9.2 VECTORED INTERRUPT

When a branch to an interrupt handling routine occurs, the vector table address corresponding to the interrupt source is used as the branch address.

Interrupt handling by the CPU consists of the following operations :

- When a branch occurs : Push the CPU status (PC and PSW contents) to the stack.
- When control is returned: Pop the CPU status (PC and PSW contents) from the stack.

To return control from the handling routine to the main routine, use the RETI instruction. The branch destination addresses must be within the range of 0 to FFFFH.

Table 9-3 Vector Table Address

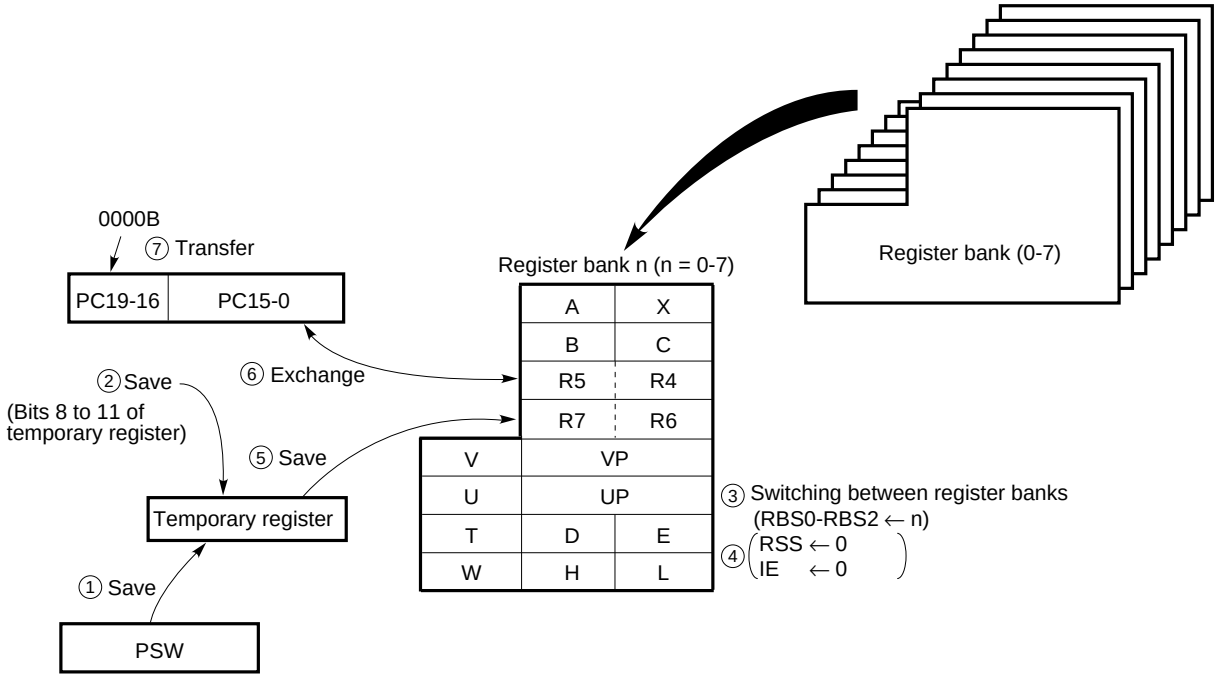
Interrupt source	Vector table address
BRK instruction	003EH
Operand error	003CH
NMI	0002H
WDT	0004H
INTP0	0006H
INTP1	0008H
INTP2	000AH
INTP3	000CH
INTC00	000EH
INTC01	0010H
INTC10	0012H
INTC11	0014H
INTC20	0016H
INTC21	0018H
INTC30	001AH
INTP4	001CH
INTP5	001EH
INTAD	0020H
INTSER	0022H
INTSR	0024H
INTCSI1	
INTST	0026H
INTCSI	0028H
INTSER2	002AH
INTSR2	002CH
INTCSI2	
INTST2	002EH

9.3 CONTEXT SWITCHING

When an interrupt request is generated, or when the BRKCS instruction is executed, an appropriate register bank is selected by the hardware. Then, a branch to a vector address stored in that register bank occurs. At the same time, the contents of the current program counter (PC) and program status word (PSW) are stacked in the register bank.

The branch address must be within the range of 0 to FFFFH.

Fig. 9-1 Context Switching Caused by an Interrupt Request

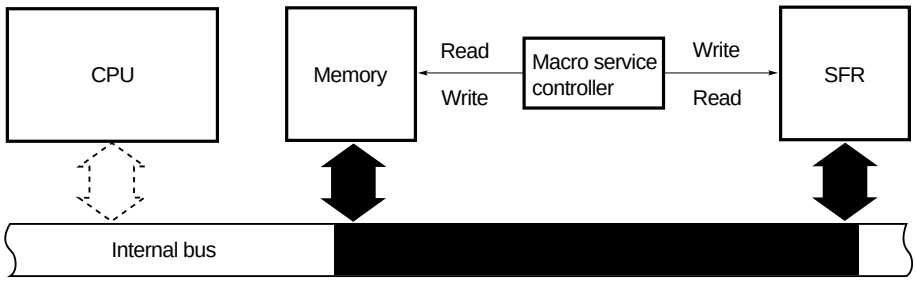


9.4 MACRO SERVICE

The macro service function enables data transfer between memory and special function registers (SFRs) without requiring the intervention of the CPU. The macro service controller accesses both memory and SFRs within the same transfer cycle to directly transfer data without having to perform data fetch.

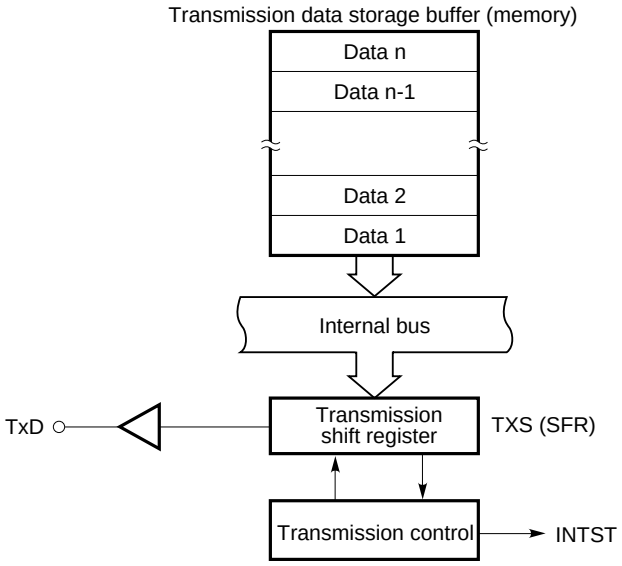
Since the CPU status is neither saved nor restored, nor is data fetch performed, high-speed data transfer is possible.

Fig. 9-2 Macro Service



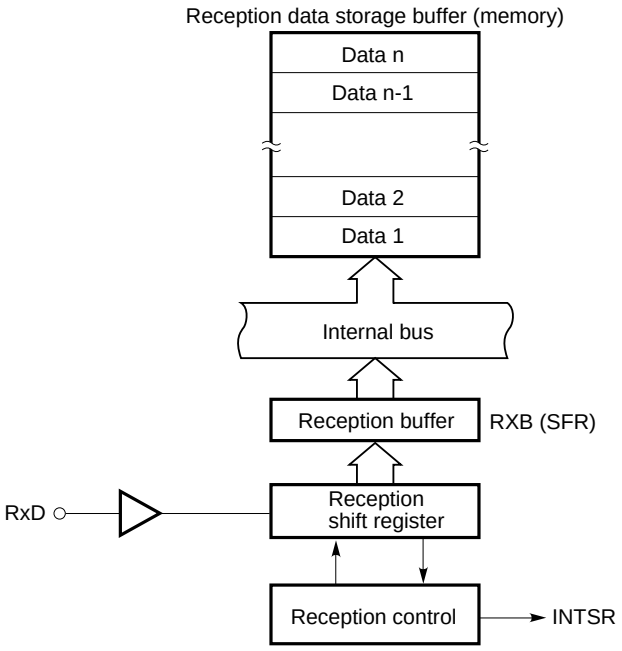
9.5 EXAMPLES OF MACRO SERVICE APPLICATIONS

(1) Serial interface transmission



Each time a macro service request (INTST) is generated, the next transmission data is transferred from memory to TXS. When data n (last byte) has been transferred to TXS (that is, once the transmission data storage buffer becomes empty), a vectored interrupt request (INTST) is generated.

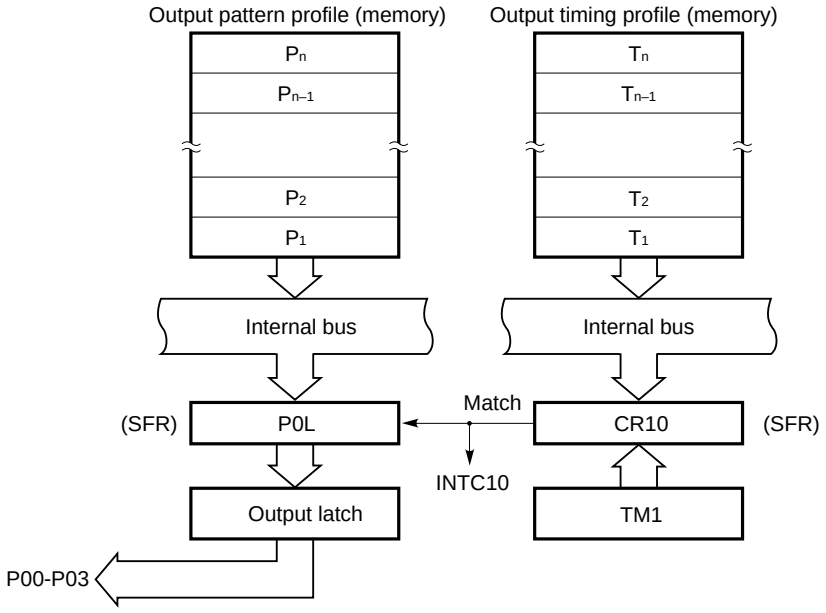
(2) Serial interface reception



Each time a macro service request (INTSR) is generated, reception data is transferred from RXB to memory. When data n (last byte) has been transferred to memory (that is, once the reception data storage buffer becomes full), a vectored interrupt request (INTSR) is generated.

(3) Real-time output port

INTC10 and INTC11 function as the output triggers for the real-time output ports. For these triggers, the macro service can simultaneously set the next output pattern and interval. Therefore, INTC10 and INTC11 can be used to independently control two stepping motors. They can also be applied to PWM and DC motor control.



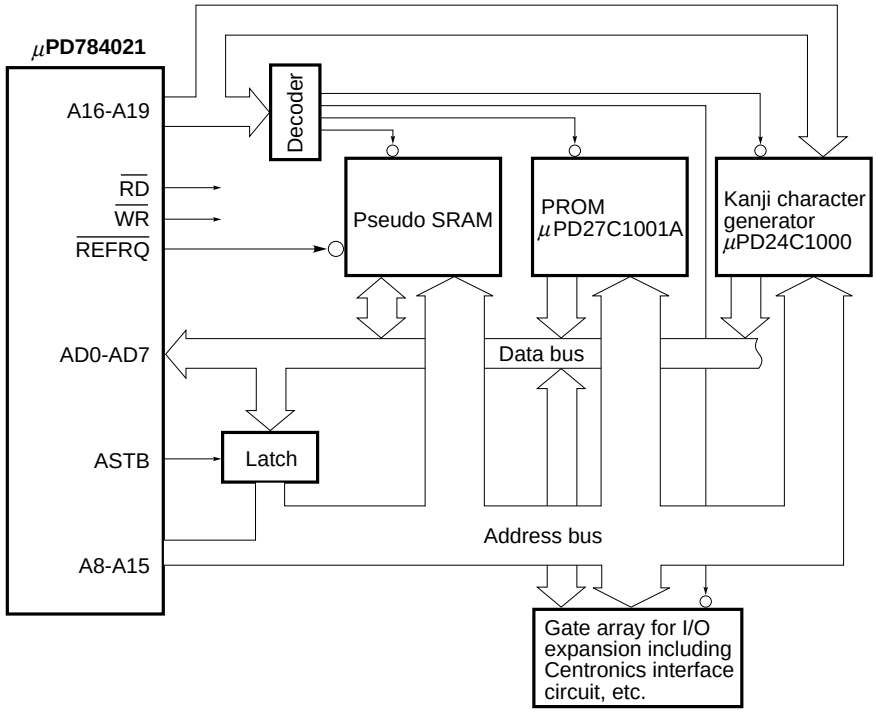
Each time a macro service request (INTC10) is generated, a pattern and timing data are transferred to the buffer register (P0L) and compare register (CR10), respectively. When the contents of timer register 1 (TM1) and CR10 match, another INTC10 is generated, and the P0L contents are transferred to the output latch. When Tn (last byte) is transferred to CR10, a vectored interrupt request (INTC10) is generated.

For INTC11, the same operation as that performed for INTC10 is performed.

10. LOCAL BUS INTERFACE

The local bus interface enables the connection of external memory and I/O devices (memory-mapped I/O). It supports a 1M-byte memory space. (See **Fig. 10-1**.)

Fig. 10-1 Example of Local Bus Interface



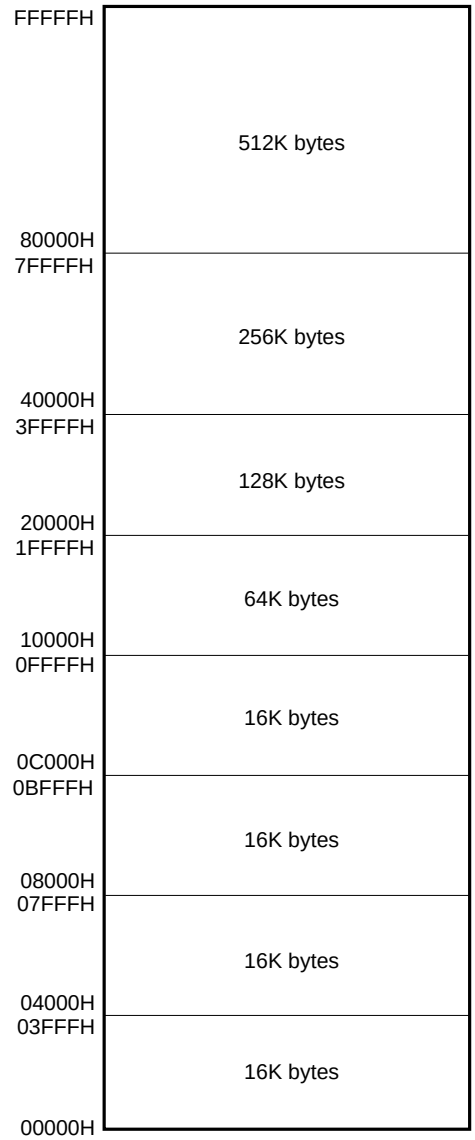
10.1 MEMORY EXPANSION

By adding external memory, program memory or data memory can be expanded, 64K bytes at a time, to approximately 1M byte (three steps).

10.2 MEMORY SPACE

The 1M-byte memory space is divided into eight spaces, each having a logical address. Each of these spaces can be controlled using the programmable wait and pseudo-static RAM refresh functions.

Fig. 10-2 Memory Space



10.3 PROGRAMMABLE WAIT

When the memory space is divided into eight spaces, a wait state can be separately inserted for each memory space while the $\overline{RD}$ or $\overline{WR}$ signal is active. This prevents the overall system efficiency from being degraded even when memory devices having different access times are connected.

In addition, an address wait function that extends the ASTB signal active period is provided to produce a longer address decode time. (This function is set for the entire space.)

10.4 PSEUDO-STATIC RAM REFRESH FUNCTION

Refresh is performed as follows:

- Pulse refresh : A bus cycle is inserted where a refresh pulse is output on the $\overline{REFRQ}$ pin at regular intervals. When the memory space is divided into eight, and a specified area is being accessed, refresh pulses can also be output on the $\overline{REFRQ}$ pin as the memory is being accessed. This can prevent the refresh cycle from suspending normal memory access.
- Power-down self-refresh : In standby mode, a low-level signal is output on the $\overline{REFRQ}$ pin to maintain the contents of pseudo-static RAM.

10.5 BUS HOLD FUNCTION

A bus hold function is provided to facilitate connection to devices such as a DMA controller. Suppose that a bus hold request signal (HLDRQ) is received from an external bus master. In this case, upon the completion of the bus cycle being performed, the address bus, address/data bus, ASTB, $\overline{RD}$, and $\overline{WR}$ pins are placed in the high-impedance state, and the bus hold acknowledge signal (HLDAK) is made active to release the bus for the external bus master.

While the bus hold function is being used, the external wait and pseudo-static RAM refresh functions are disabled.

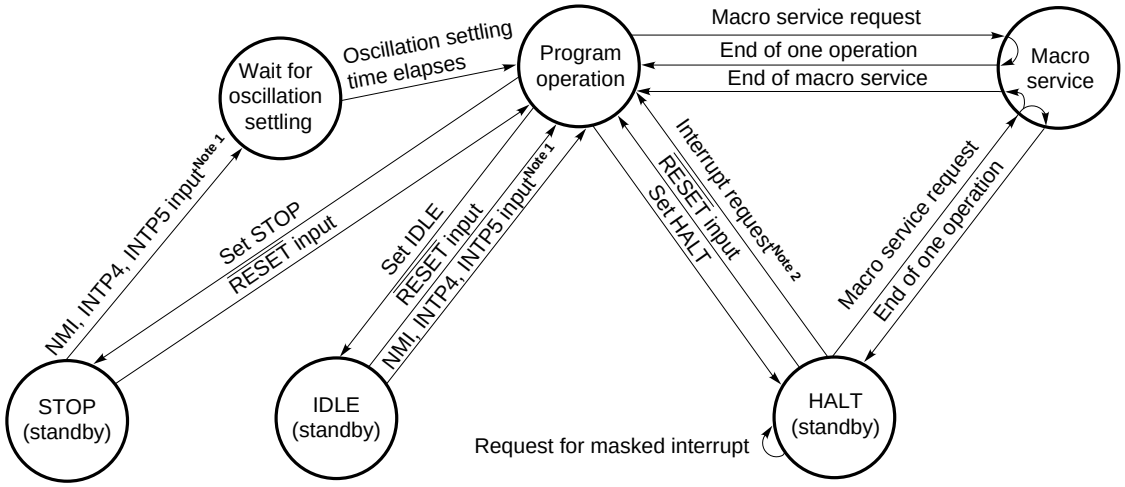
11. STANDBY FUNCTION

The standby function allows the power consumption of the chip to be reduced. The following standby modes are supported:

- HALT mode : The CPU operation clock is stopped. By occassionally inserting the HALT mode during normal operation, the overall average power consumption can be reduced.
- IDLE mode : The entire system is stopped, with the exception of the oscillator circuit. This mode consumes only very little more power than STOP mode, but normal program operation can be restored in almost as little time as that required to restore normal program operation from HALT mode.
- STOP mode : The oscillator is stopped. All operations in the chip stop, such that only leakage current flows.

These modes can be selected by software.
A macro service can be initiated in HALT mode.

Fig. 11-1 Standby Mode Status Transition



Notes 1. INTP4 and INTP5 are applied when not masked.
2. Only when the interrupt request is not masked

Remark NMI is enabled only by external input. The watchdog timer cannot be used to release one of the standby modes (STOP or IDLE mode).

12. RESET FUNCTION

Applying a low-level signal to the $\overline{\text{RESET}}$ pin initializes the internal hardware (reset status).

When the $\overline{\text{RESET}}$ input makes a low-to-high transition, the following data is loaded into the program counter (PC):

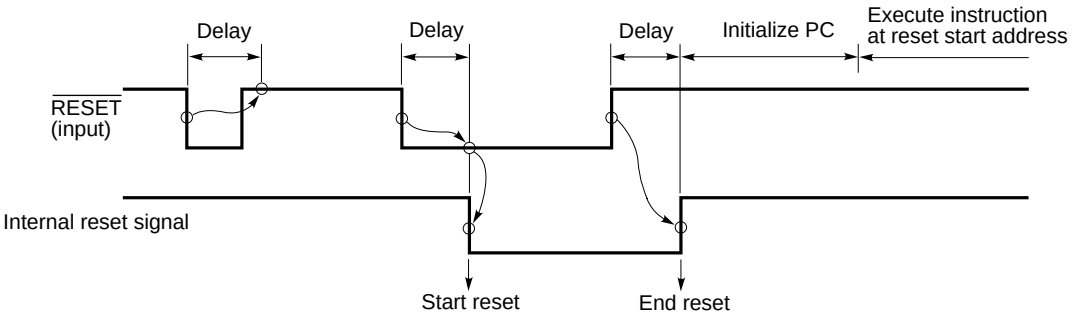
- Eight low-order bits of the PC : Contents of location at address 0000H
- Intermediate eight bits of the PC : Contents of location at address 0001H
- Four high-order bits of the PC : 0

The PC contents are used as a branch destination address. Program execution starts from that address. Therefore, a reset start can be performed from an arbitrary address.

The contents of each register can be set by software, as required.

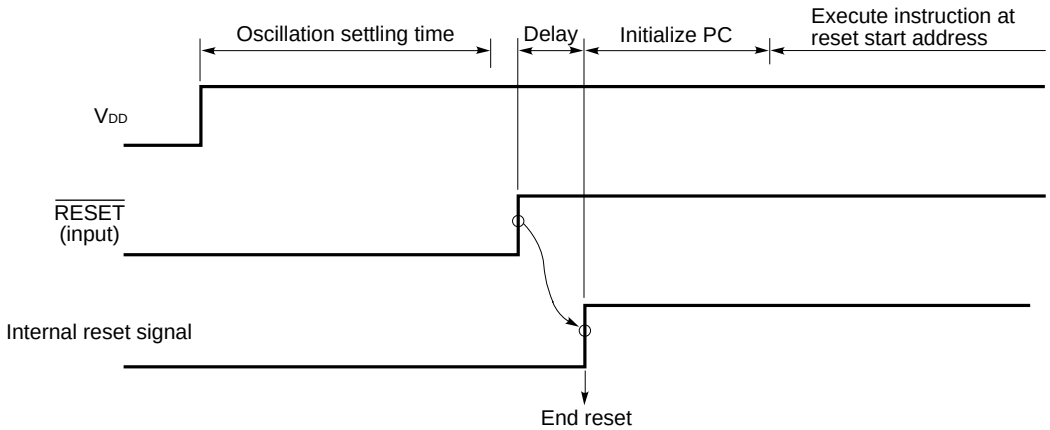
The $\overline{\text{RESET}}$ input circuit contains a noise eliminator to prevent malfunctions caused by noise. This noise eliminator is an analog delay sampling circuit.

Fig. 12-1 Accepting a Reset



For power-on reset, the $\overline{\text{RESET}}$ signal must be held active until the oscillation settling time (approximately 40 ms) has elapsed.

Fig. 12-2 Power-On Reset



13. INSTRUCTION SET

(1) 8-bit instructions (The instructions enclosed in parentheses are implemented by a combination of operands, where A is described as r.)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC, CHKL, CHKLA

Table 13-1 Instructions Implemented by 8-Bit Addressing

1st operand \ 2nd operand	#byte	A	r r'	saddr saddr'	sfr	!addr16 !!addr24	mem [saddrp] [%saddrg]	r3 PSWL PSWH	[WHL+] [WHL–]	n	None[Note 2]
A	(MOV) ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH (ADD)[Note 1]	(MOV)[Note 6] (XCH)[Note 6] (ADD)[Notes 1, 6]	MOV (XCH) (ADD)[Note 1]	(MOV) (XCH) ADD[Note 1]	MOV XCH ADD[Note 1]	MOV	(MOV) (XCH) (ADD)[Note 1]		
r	MOV ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH				ROR[Note 3]	MULU DIVUW INC DEC
saddr	MOV ADD[Note 1]	(MOV)[Note 6] (ADD)[Note 1]	MOV ADD[Note 1]	MOV XCH ADD[Note 1]							INC DEC DBNZ
sfr	MOV ADD[Note 1]	MOV (ADD)[Note 1]	MOV ADD[Note 1]								PUSH POP CHKL CHKLA
!addr16 !!addr24	MOV	(MOV) ADD[Note 1]	MOV								
mem [saddrp] [%saddrg]		MOV ADD[Note 1]									
mem3											ROR4 ROL4
r3 PSWL PSWH	MOV	MOV									
B, C											DBNZ
STBC, WDM	MOV										
[TDE+] [TDE–]		(MOV) (ADD)[Note 1] MOVM[Note 4]							MOVBK[Note 5]		

Notes 1. ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as ADD.

2. There is no second operand, or the second operand is not an operand address.

3. ROL, RORC, ROLC, SHR, and SHL are the same as ROR.

4. XCHM, CMPME, CMPMNE, CMPMNC, and CMPMC are the same as MOVM.

5. XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC are the same as MOVBK.

6. When saddr is saddr2 with this combination, an instruction with a short code exists.

(2) 16-bit instructions (The instructions enclosed in parentheses are implemented by a combination of operands, where AX is described as rp.)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

Table 13-2 Instructions Implemented by 16-Bit Addressing

1st operand \ 2nd operand	#word	AX	rp rp'	saddrp saddrp'	strp	!addr16 !!addr24	mem [saddrp] [%saddrg]	[WHL+]	byte	n	None[Note 2]
AX	(MOVW) ADDW[Note 1]	(MOVW) (XCHW) (ADD)[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	(MOVW)[Note 3] (XCHW)[Note 3] (ADDW)[Notes 1,3]	MOVW (XCHW) (ADDW)[Note 1]	(MOVW) XCHW	MOVW XCHW	(MOVW) (XCHW)			
rp	MOVW ADDW[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW				SHRW SHLW	MULW[Note 4] INCW DECW
saddrp	MOVW ADDW[Note 1]	(MOVW)[Note 3] (ADDW)[Note 1]	MOVW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]							INCW DECW
sfrp	MOVW ADDW[Note 1]	MOVW (ADDW)[Note 1]	MOVW ADDW[Note 1]								PUSH POP
!addr16 !!addr24	MOVW	(MOVW)	MOVW						MOVTBLW		
mem [saddrp] [%saddrg]		MOVW									
PSW											PUSH POP
SP	ADDWG SUBWG										
post											PUSH POP PUSHU POPU
[TDE+]		(MOVW)						SACW			
byte											MACW MACSW

Notes 1. SUBW and CMPW are the same as ADDW.

2. There is no second operand, or the second operand is not an operand address.

3. When saddrp is saddrp2 with this combination, an instruction with a short code exists.

4. MULUW and DIVUX are the same as MULW.

(3) 24-bit instructions (The instructions enclosed in parentheses are implemented by a combination of operands, where WHL is described as rg.)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 13-3 Instructions Implemented by 24-Bit Addressing

1st operand \ 2nd operand	#imm24	WHL	rg rg'	saddrg	!!addr24	mem1	[%saddrg]	SP	None[Note]
WHL	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) ADDG SUBG	(MOVG)	MOVG	MOVG	MOVG	
rg	MOVG ADDG SUBG	(MOVG) (ADDG) (SUBG)	MOVG ADDG SUBG	MOVG	MOVG				INCG DECG PUSH POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG DECG

Note There is no second operand, or the second operand is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

Table 13-4 Bit Manipulation Instructions Implemented by Addressing

2nd operand / 1st operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	/saddr.bit /sfr.bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit	None[Note]
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

Note There is no second operand, or the second operand is not an operand address.

(5) Call/return instructions and branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 13-5 Call/Return and Branch Instructions Implemented by Addressing

Instruction address operand	$addr20	$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None
Basic instruction	BC[Note] BR	CALL BR	CALL BR RETCS RETCSB	CALL BR	CALL BR	CALL BR	CALL BR	CALL BR	CALLF	CALLF	BRKCS	BRK RET RETI RETB
Composite instruction	BF BT BTCLR BFSET DBNZ											

Note BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT EI, DI, SWRS

14. ELECTRICAL CHARACTERISTICS ★

The electrical characteristics described in this chapter apply to the products which are improved versions of the μPD784020 and μPD784021 (other than K-rank products). For K-rank products yet to be improved (K-rank products), please consult with our sales offices.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

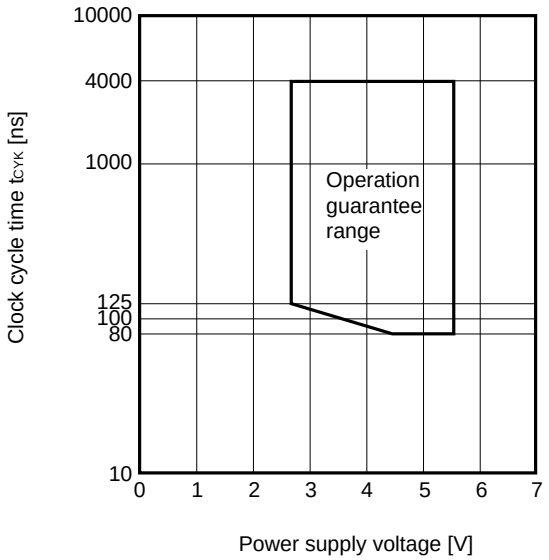
Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} + 0.5	V
	AV_{SS}		–0.5 to +0.5	V
Input voltage	V_I		–0.5 to V_{DD} + 0.5	V
Output voltage	V_O		–0.5 to V_{DD} + 0.5	V
Low-level output current	I_{OL}	Each pin	15	mA
		Total of all output pins	150	mA
High-level output current	I_{OH}	Each pin	–10	mA
		Total of all output pins	–100	mA
A/D converter reference input voltage	AV_{REF1}		–0.5 to V_{DD} + 0.3	V
D/A converter reference input voltage	AV_{REF2}		–0.5 to V_{DD} + 0.3	V
	AV_{REF3}		–0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

OPERATING CONDITIONS

- Operating ambient temperature (T_A): –40 to +85 °C
- Rising and falling time (t_r, t_f) (for pins not especially specified): 0 to 200 μs
- Power supply voltage and clock cycle time: See **Fig. 14-1**.

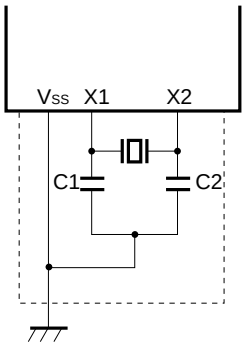
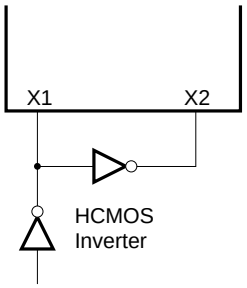
Fig. 14-1 Relationship between Power Supply Voltage and Clock Cycle Time



CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O	0 V on pins other than measured pins			10	pF
I/O capacitance	C_{IO}				10	pF

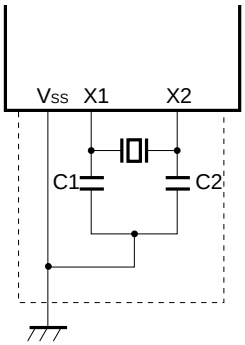
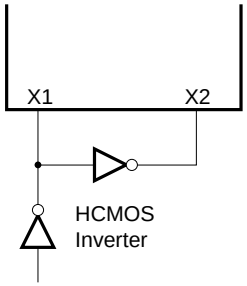
OSCILLATOR CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Ceramic resonator or crystal		Oscillator frequency (f_{XX})	4	25	MHz
External clock		X1 input frequency (f_X)	4	25	MHz
		X1 input rising and falling times (t_{XR}, t_{XF})	0	10	ns
		X1 input high-level and low-level widths (t_{WXH}, t_{WXL})	10	125	ns

Caution When using the system clock generator, run wires in the portion surrounded by dotted lines according to the following rules to avoid effects such as stray capacitance:

- **Minimize the wiring.**
- **Never cause the wires to cross other signal lines.**
- **Never cause the wires to run near a line carrying a large varying current.**
- **Cause the grounding point of the capacitor of the oscillator circuit to have the same potential as V_{SS}. Never connect the capacitor to a ground pattern carrying a large current.**
- **Never extract a signal from the oscillator.**

OSCILLATOR CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Ceramic resonator or crystal		Oscillator frequency (f_{XX})	4	16	MHz
External clock		X1 input frequency (f_X)	4	16	MHz
		X1 input rising and falling times (t_{XR}, t_{XF})	0	10	ns
		X1 input high-level and low-level widths (t_{WXH}, t_{WXL})	10	125	ns

Caution When using the system clock generator, run wires in the portion surrounded by dotted lines according to the following rules to avoid effects such as stray capacitance:

- **Minimize the wiring.**
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- **Never cause the wires to run near a line carrying a large varying current.**
- **Cause the grounding point of the capacitor of the oscillator circuit to have the same potential as V_{SS}. Never connect the capacitor to a ground pattern carrying a large current.**
- **Never extract a signal from the oscillator.**

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low-level input voltage	V_{IL1}	Pins other than those described in **Notes 1, 2, 3,** and **4**	–0.3		$0.3V_{DD}$	V
	V_{IL2}	Pins described in **Notes 1, 2, 3,** and **4**	–0.3		$0.2V_{DD}$	V
	V_{IL3}	V_{DD} = +5.0 V ±10 % Pins described in **Notes 2, 3,** and **4**	–0.3		+0.8	V
High-level input voltage	V_{IH1}	Pins other than those described in **Note 1**	$0.7V_{DD}$		V_{DD} + 0.3	V
	V_{IH2}	Pins described in **Note 1**	$0.8V_{DD}$		V_{DD} + 0.3	V
	V_{IH3}	V_{DD} = +5.0 V ±10 % Pins described in **Notes 2, 3,** and **4**	2.2		V_{DD} + 0.3	V
Low-level output voltage	V_{OL1}	I_{OL} = 2 mA			0.4	V
	V_{OL2}	V_{DD} = +5.0 V ±10 % I_{OL} = 8 mA Pins described in **Notes 2** and **5**			1.0	V
High-level output voltage	V_{OH1}	I_{OH} = –2 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{DD} = +5.0 V ±10 % I_{OH} = –5 mA Pins described in **Note 4**	2.0			V
X1 low-level input current	I_{IL}	0 V ≤ V_I ≤ V_{IL2}			–30	μA
X1 high-level input current	I_{IH}	V_{IH2} ≤ V_I ≤ V_{DD}			+30	μA

Notes 1. X1, X2, $\overline{\text{RESET}}$, P12/ASCK2/$\overline{\text{SCK2}}$, P13/RxD2/SI2, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SI0, P30/RxD/SI1, P32/$\overline{\text{SCK0}}$, P33/SO0/SB0, and TEST

2. AD0 to AD7 and A8 to A15

3. P60/A16 to P63/A19, $\overline{\text{RD}}$, $\overline{\text{WR}}$, P66/$\overline{\text{WAIT}}$/HLDRQ, and P67/$\overline{\text{REFRQ}}$/HLDAK

4. P00 to P07

5. P10 to P17

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD} Except for the X1 pin when EXTC = 0				±10	μA
		0 V ≤ V_I ≤ V_{DD} Analog input pins				±3	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operating mode	f_{XX} = 25 MHz		40	60	mA
			f_{XX} = 16 MHz V_{DD} = 2.7 to 5.5 V		12	25	mA
	I_{DD2}	HALT mode	f_{XX} = 25 MHz		22	30	mA
			f_{XX} = 16 MHz V_{DD} = 2.7 to 5.5 V		8	12	mA
	I_{DD3}	IDLE mode (EXTC = 0)	f_{XX} = 25 MHz			12	mA
			f_{XX} = 16 MHz V_{DD} = 2.7 to 5.5 V			8	mA
Pull-up resistance	R_L	V_I = 0 V V_{DD} = +5.0 V ±10 %		15		100	kΩ
		V_I = 0 V V_{DD} = 2.7 to 4.5 V		15		160	kΩ

AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (1/2)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Address setup time	t_{SAST}	V_{DD} = +5.0 V ±10 %		(0.5 + a) T – 11		ns
				(0.5 + a) T – 15		ns
ASTB high-level width	t_{WSTH}	V_{DD} = +5.0 V ±10 %		(0.5 + a) T – 17		ns
				(0.5 + a) T – 40		ns
Address hold time (referred to ASTB↓)	t_{HSTLA}	V_{DD} = +5.0 V ±10 %		0.5T – 24		ns
				0.5T – 34		ns
Address hold time (referred to $\overline{RD}$∞)	t_{HRA}			0.5T – 14		ns
Address → $\overline{RD}$↓ delay time	t_{DAR}	V_{DD} = +5.0 V ±10 %		(1 + a) T – 5		ns
				(1 + a) T – 10		ns
Address float time (referred to $\overline{RD}$↓)	t_{FRA}				0	ns
Address → data input time	t_{DAID}	V_{DD} = +5.0 V ±10 %			(2.5 + a + n) T – 37	ns
					(2.5 + a + n) T – 52	ns
ASTB↓ → data input time	t_{DSTID}	V_{DD} = +5.0 V ±10 %			(2 + n) T – 40	ns
					(2 + n) T – 60	ns
$\overline{RD}$↓ → data input time	t_{DRID}	V_{DD} = +5.0 V ±10 %			(1.5 + n) T – 50	ns
					(1.5 + n) T – 70	ns
ASTB↓ → $\overline{RD}$↓ delay time	t_{DSTR}			0.5T – 9		ns
Data hold time (referred to $\overline{RD}$∞)	t_{HRID}			0		ns
$\overline{RD}$∞ → address active time	t_{DRA}	Upon program read	V_{DD} = +5.0 V ±10 %	0.5T – 2		ns
				0.5T – 12		ns
		Upon data read	V_{DD} = +5.0 V ±10 %	1.5T – 2		ns
				1.5T – 12		ns
$\overline{RD}$∞ → ASTB∞ delay time	t_{DRST}			0.5T – 9		ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = +5.0 V ±10 %		(1.5 + n) T – 30		ns
				(1.5 + n) T – 40		ns
Address hold time (referred to $\overline{WR}$∞)	t_{HWA}			0.5T – 14		ns
Address → $\overline{WR}$↓ delay time	t_{DAW}	V_{DD} = +5.0 V ±10 %		(1 + a) T – 5		ns
				(1 + a) T – 10		ns
ASTB↓ → data output delay time	t_{DSTOD}	V_{DD} = +5.0 V ±10 %			0.5T + 15	ns
					0.5T + 20	ns
ASTB↓ → data output time	t_{DWOD}				0.5T – 11	ns
ASTB↓ → $\overline{WR}$↓ output delay time	t_{DSTW}			0.5T – 9		ns

Remark T: T_{CYK} (system clock cycle time)

a: 1 when address wait is applied, 0 in other cases

n: number of wait cycles (n ∞ 0)

(1) Read/write operation (2/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Data setup time (referred to $\overline{WR}$↓)	t_{SODW}	V_{DD} = +5.0 V ±10 %	(1.5 + n) T – 30		ns
			(1.5 + n) T – 40		ns
Data hold time (referred to $\overline{WR}$↑)**Note**	t_{HWOD}	V_{DD} = +5.0 V ±10 %	0.5T – 5		ns
			0.5T – 14		ns
$\overline{WR}$↓ → ASTB↓ delay time	t_{DWST}		0.5T – 9		ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = +5.0 V ±10 %	(1.5 + n) T – 30		ns
			(1.5 + n) T – 40		ns

Note The hold time includes the time for holding V_{OH1} and V_{OL1} on the load conditions of C_L = 50 pF and R_L = 4.7 kΩ.

Remark T: T_{CYK} (system clock cycle time)
n: number of wait cycles (n ≥ 0)

(2) Bus hold timing

Parameter	Symbol	Conditions	Min.	Max.	Unit
HLDRQ↓ → float delay time	t_{FHQC}			(6 + a + n) T + 50	ns
HLDRQ↓ → HLDAK↓ delay time	$t_{DHQHHAH}$	V_{DD} = +5.0 V ±10 %		(7 + a + n) T + 30	ns
				(7 + a + n) T + 40	ns
Float → HLDAK↓ delay time	t_{DCFHA}			1T + 30	ns
HLDRQ↓ → HLDAK↓ delay time	$t_{DHQLHAL}$	V_{DD} = +5.0 V ±10 %		2T + 40	ns
				2T + 60	ns
HLDAK↓ → active delay time	t_{DHAC}	V_{DD} = +5.0 V ±10 %	1T – 20		ns
			1T – 30		ns

Remark T: T_{CYK} (system clock cycle time)
a: 1 when address wait is applied, 0 in other cases
n: number of wait cycles (n ≥ 0)

(3) External wait timing

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address → $\overline{WAIT}$↓ input time	t_{DAWT}	V_{DD} = +5.0 V ±10 %		(2 + a) T – 40	ns
				(2 + a) T – 60	ns
ASTB↓ → $\overline{WAIT}$↓ input time	t_{DSTWT}	V_{DD} = +5.0 V ±10 %		1.5T – 40	ns
				1.5T – 60	ns
ASTB↓ → $\overline{WAIT}$ hold time	t_{HSTWTH}	V_{DD} = +5.0 V ±10 %	(0.5 + n) T + 5		ns
			(0.5 + n) T + 10		ns
ASTB↓ → $\overline{WAIT}$∞ delay time	t_{DSTWTH}	V_{DD} = +5.0 V ±10 %		(1.5 + n) T – 40	ns
				(1.5 + n) T – 60	ns
$\overline{RD}$↓ → $\overline{WAIT}$↓ input time	t_{DRWTL}	V_{DD} = +5.0 V ±10 %		T – 50	ns
				T – 70	ns
$\overline{RD}$↓ → $\overline{WAIT}$↓ hold time	t_{HRWT}	V_{DD} = +5.0 V ±10 %	nT + 5		ns
			nT + 10		ns
$\overline{RD}$↓ → $\overline{WAIT}$∞ delay time	t_{DRWTH}	V_{DD} = +5.0 V ±10 %		(1 + n) T – 40	ns
				(1 + n) T – 60	ns
$\overline{WAIT}$∞ → data input time	t_{DWTID}	V_{DD} = +5.0 V ±10 %		0.5T – 5	ns
				0.5T – 10	ns
$\overline{WAIT}$∞ → $\overline{WR}$∞ delay time	t_{DWTW}		0.5T		ns
$\overline{WAIT}$∞ → $\overline{RD}$∞ delay time	t_{DWTR}		0.5T		ns
$\overline{WR}$↓ → $\overline{WAIT}$↓ input time	t_{DWWTL}	V_{DD} = +5.0 V ±10 %		T – 50	ns
				T – 75	ns
$\overline{WR}$↓ → $\overline{WAIT}$ hold time	t_{HWWT}	V_{DD} = +5.0 V ±10 %	nT + 5		ns
			nT + 10		ns
$\overline{WR}$↓ → $\overline{WAIT}$∞ delay time	t_{DWWTH}	V_{DD} = +5.0 V ±10 %		(1 + n) T – 40	ns
				(1 + n) T – 60	ns

Remark T: T_{CYK} (system clock cycle time)
a: 1 when address wait is applied, 0 in other cases
n: number of wait cycles (n ∞ 0)

(4) Refresh timing

Parameter	Symbol	Conditions	Min.	Max.	Unit
Random read/write cycle time	t_{RC}		3T		ns
$\overline{REFRQ}$ low-level pulse width	t_{WRFQL}	V_{DD} = +5.0 V ±10 %	1.5T – 25		ns
			1.5T – 30		ns
ASTB↓ → $\overline{REFRQ}$ delay time	t_{DSTRFQ}		0.5T – 9		ns
$\overline{RD}$∞ → $\overline{REFRQ}$ delay time	t_{DRRFQ}		1.5T – 9		ns
$\overline{WR}$∞ → $\overline{REFRQ}$ delay time	t_{DWRFQ}		1.5T – 9		ns
$\overline{REFRQ}$∞ → ASTB delay time	t_{DRFQST}		0.5T – 9		ns
$\overline{REFRQ}$ high-level pulse width	t_{WRFQH}	V_{DD} = +5.0 V ±10 %	1.5T – 25		ns
			1.5T – 30		ns

Remark T: T_{CYK} (system clock cycle time)

SERIAL OPERATION (CSI)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Serial clock cycle time ($\overline{SCK0}$)	t_{CYSK0}	Input	V_{DD} = +5.0 V ±10 %	500		ns
				1000		ns
		Output		T		ns
Serial clock low-level width ($\overline{SCK0}$)	t_{WSKL0}	Input	V_{DD} = +5.0 V ±10 %	210		ns
				460		ns
		Output		0.5T – 40		ns
Serial clock high-level width ($\overline{SCK0}$)	t_{WSKH0}	Input	V_{DD} = +5.0 V ±10 %	210		ns
				460		ns
		Output		0.5T – 40		ns
SI0, SB0 setup time (referred to $\overline{SCK0}$↑)	t_{SSSK0}			80		ns
SI0, SB0 hold time (referred to $\overline{SCK0}$↑)	t_{HSSK0}			80		ns
SO0, SB0 output delay time (referred to $\overline{SCK0}$↓)	t_{DSBSK1}	CMOS push-pull output (three-wire serial I/O mode)		0	150	ns
	t_{DSBSK2}	Open-drain output (SBI mode), R_L = 1 kΩ		0	400	ns
SO0, SB0 output hold time (referred to $\overline{SCK0}$↑)	t_{HSBSK1}	During data transfer		$0.5T_{CYSK0}$ – 40		ns
SB0 high hold time (referred to $\overline{SCK0}$↑)	t_{HSBSK2}	SBI mode		4		t_{CYX}
SB0 low setup time (referred to $\overline{SCK0}$↓)	t_{SSBSK}			4		t_{CYX}
SB0 low-level width	t_{WSBL}			4		t_{CYX}
SB0 high-level width	t_{WSBH}			4		t_{CYX}

Remarks 1. The values listed in the above table are obtained when f_{XX} = 25 MHz and C_L = 100 pF.

2. $t_{CYX} = 1/f_{XX}$

3. T: Serial clock frequency specified using software. The minimum value is $16/f_{XX}$.

SERIAL OPERATION (IOE1, IOE2)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Serial clock cycle time ($\overline{SCK1}$, $\overline{SCK2}$)	t_{CYSK1}	Input	V_{DD} = +5.0 V ±10 %	250		ns
				500		ns
		Output	Internal clock divided by 16	T		ns
Serial clock low-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKL1}	Input	V_{DD} = +5.0 V ±10 %	85		ns
				210		ns
		Output	Internal clock divided by 16	0.5T – 40		ns
Serial clock high-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKH1}	Input	V_{DD} = +5.0 V ±10 %	85		ns
				210		ns
		Output	Internal clock divided by 16	0.5T – 40		ns
SI1, SI2 setup time (referred to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{SSSK1}			40		ns
SI1, SI2 hold time (referred to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSSK1}			40		ns
SO1, SO2 output delay time (referred to $\overline{SCK1}$, $\overline{SCK2}$↓)	t_{DSOSK}			0	50	ns
SO1, SO2 output hold time (referred to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSOSK}	During data transfer		$0.5T_{CYSK1}$ – 40		ns

Remarks 1. The values listed in the above table are obtained when C_L = 100 pF.

2. T: Serial clock frequency specified using software. The minimum value is $16/f_{XX}$.

SERIAL OPERATION (UART, UART2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
ASCK clock input cycle time	t_{CYASK}	V_{DD} = +5.0 V ±10 %	125		ns
			250		ns
ASCK clock low-level width	t_{WASKL}	V_{DD} = +5.0 V ±10 %	52.5		ns
			85		ns
ASCK clock high-level width	t_{WASKH}	V_{DD} = +5.0 V ±10 %	52.5		ns
			85		ns

OTHER OPERATIONS

Parameter	Symbol	Conditions	Min.	Max.	Unit
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0 low-level width	t_{WIT0L}		$3t_{CYSMP}$ + 10		ns
INTP0 high-level width	t_{WIT0H}		$3t_{CYSMP}$ + 10		ns
INTP1-INTP3 and CI low-level width	t_{WIT1L}		$3t_{CYCPU}$ + 10		ns
INTP1-INTP3 and CI high-level width	t_{WIT1H}		$3t_{CYCPU}$ + 10		ns
INTP4 and INTP5 low-level width	t_{WIT2L}		10		μs
INTP4 and INTP5 high-level width	t_{WIT2H}		10		μs
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		10		μs

Remark t_{CYSMP}: sampling clock specified using software
t_{CYCPU}: CPU operating clock specified using CPU software

A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = 3.4 to 5.5 V, +3.4 V ≤ AV_{REF1} ≤ AV_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution			8			bit
Total error[Note]					1.2	%
		V_{DD} = AV_{DD} = +5.0 V ±10 % +3.4 V ≤ AV_{REF1} ≤ AV_{DD}			1.0	%
		+2.7 V ≤ V_{DD} = AV_{DD} ≤ +3.3 V +2.5 V ≤ AV_{REF1} ≤ AV_{DD}			1.0	%
Linearity calibration[Note]					0.6	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	t_{CYK} ≤ 500 ns, FR = 1	120			t_{CYK}
		t_{CYK} ≤ 500 ns, FR = 0	180			t_{CYK}
Sampling time	t_{SAMP}	t_{CYK} ≤ 500 ns, FR = 1	24			t_{CYK}
		t_{CYK} ≤ 500 ns, FR = 0	36			t_{CYK}
Analog input voltage	V_{IAN}		–0.3		AV_{REF1} + 0.3	V
Analog input impedance	R_{AN}			1000		MΩ
AV_{REF1} current	AI_{REF1}			0.5	1.5	mA
AV_{DD} supply current	AI_{DD1}	f_{XX} = 25 MHz		2.0	5.0	mA
	AI_{DD2}	STOP mode, CS = 0			20	μA

Note Quantization error is excluded. The error is represented in percent with respect to a full-scale value.

Remark t_{CYK}: system clock cycle time

D/A CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, AV_{REF2} = V_{DD} = AV_{DD} = 2.7 to 5.5 V, AV_{REF3} = V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution				8			bit
Total error[Note]		Load condition: 4 MΩ, 30 pF	V_{DD} = 4.5 to 5.5 V			0.4	%
						0.6	%
			V_{DD} = 4.5 to 5.5 V AV_{REF2} = 0.75V_{DD} AV_{REF3} = 0.25V_{DD}			0.6	%
			AV_{REF2} = 0.75V_{DD} AV_{REF3} = 0.25V_{DD}			0.8	%
		Load condition: 2 MΩ, 30 pF	V_{DD} = 4.5 to 5.5 V			0.6	%
						0.8	%
			V_{DD} = 4.5 to 5.5 V AV_{REF2} = 0.75V_{DD} AV_{REF3} = 0.25V_{DD}			0.8	%
			AV_{REF2} = 0.75V_{DD} AV_{REF3} = 0.25V_{DD}			1.0	%
Settling time		Load condition: 2 MΩ, 30 pF				10	μs
Output resistance	R_O	Note			20		kΩ
Analog reference voltage	AV_{REF2}			0.75V_{DD}		V_{DD}	V
	AV_{REF3}			0		0.25V_{DD}	V
Reference supply input current	AI_{REF2}			0		5	mA
	AI_{REF3}			–5		0	mA

Note DACS0, DACS1 = 7FH

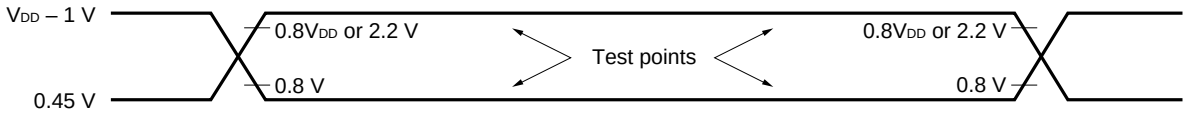
DATA RETENTION CHARACTERISTICS (T_A = –40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.5 to 5.5 V **Note 1**		10	50	μA
		V_{DDDR} = 2.5 V **Note 1**		2	10	μA
V_{DD} rising time	t_{RVD}		200			μs
V_{DD} falling time	t_{FVD}		200			μs
V_{DD} retention time (referred to STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation settling time	t_{WAIT}	Crystal	30			ms
		Ceramic resonator	5			ms
Low-level input voltage	V_{IL}	Specified pins **Note 2**	0		$0.1V_{DDDR}$	V
High-level input voltage	V_{IH}		$0.9V_{DDDR}$		V_{DDDR}	V

Notes 1. When the input voltage for the pins described in **Note 2** satisfies the V_{IL} and V_{IH} conditions in the above table

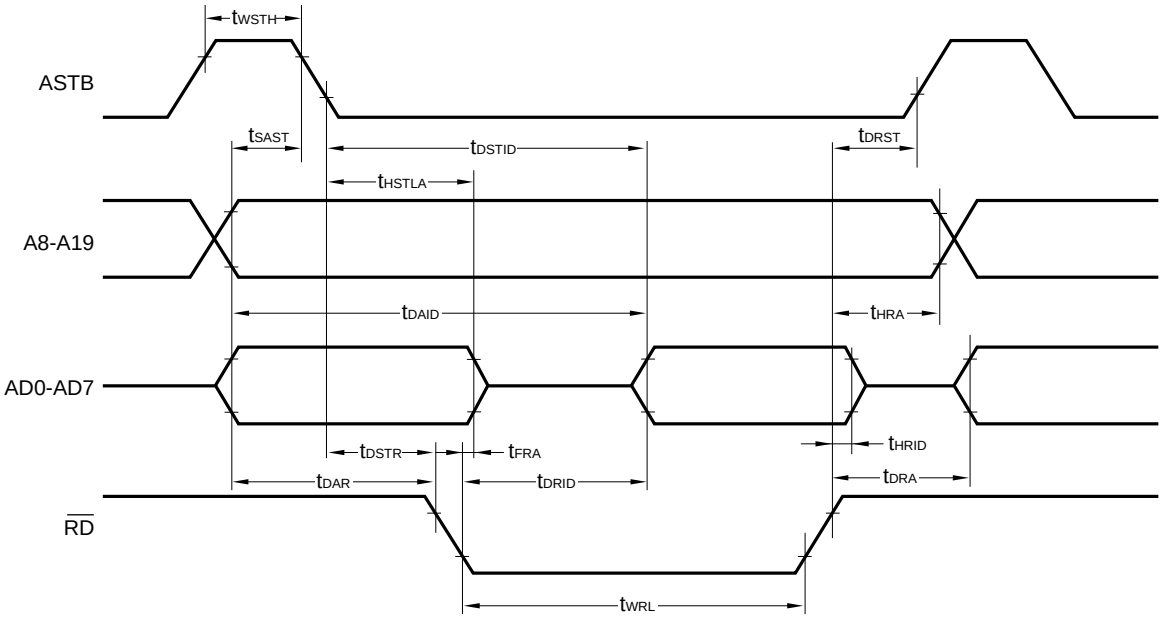
2. Pins $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SI0, P32/$\overline{\text{SCK0}}$, and P33/SO0/SB0

AC Timing Test Points

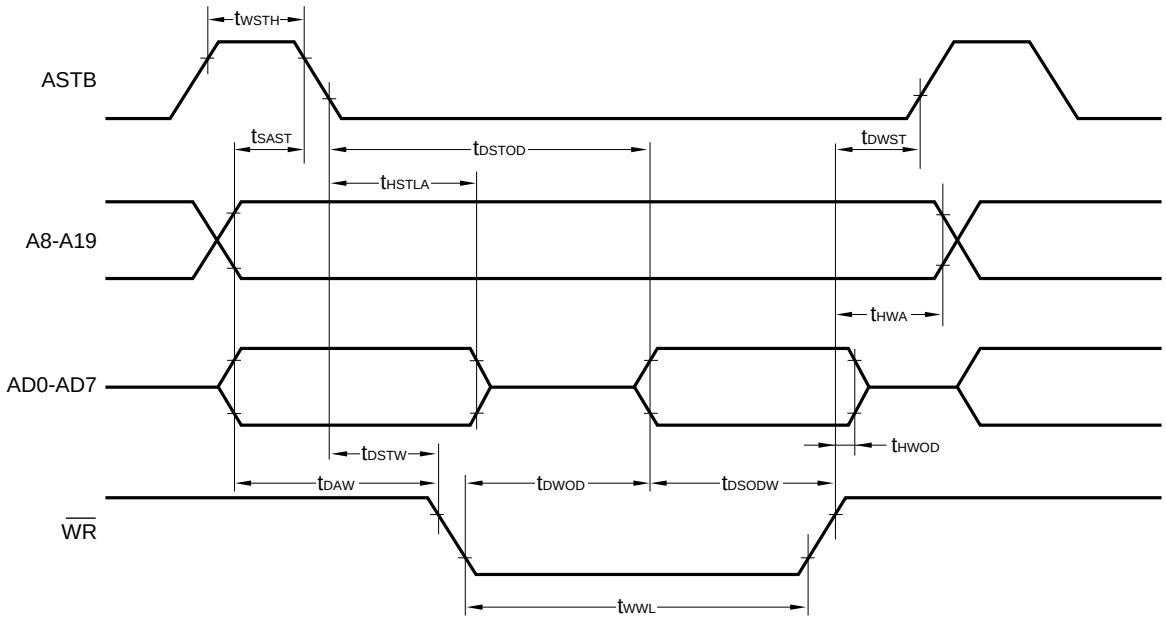


Timing Waveform

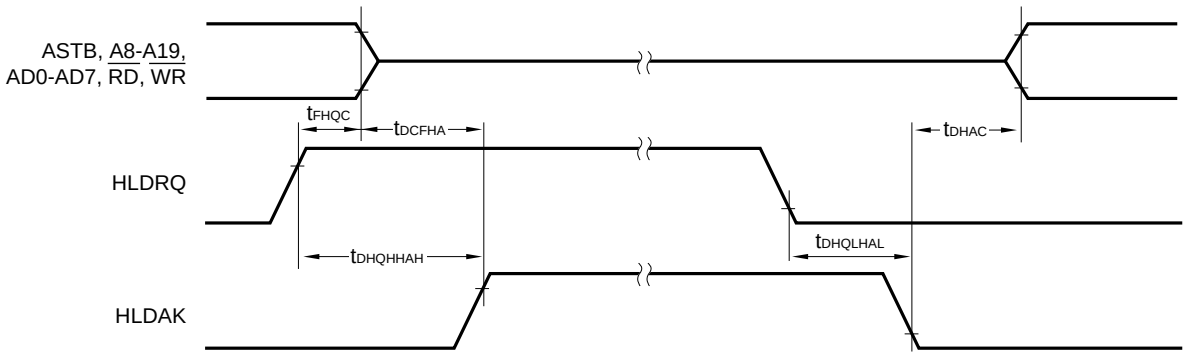
(1) Read operation



(2) Write operation

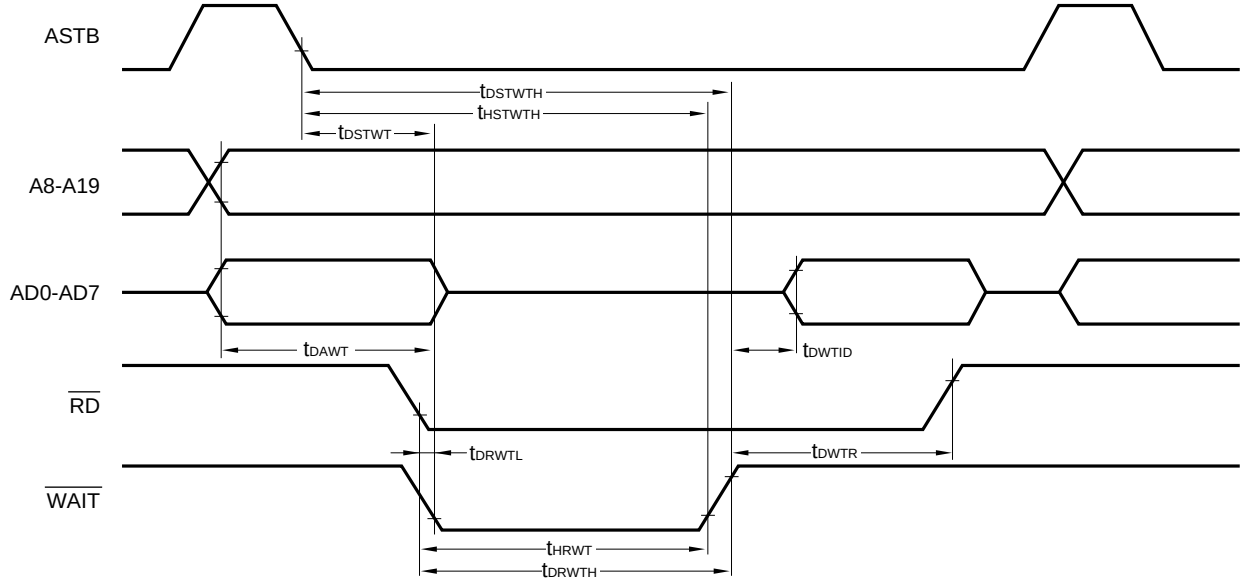


Hold Timing

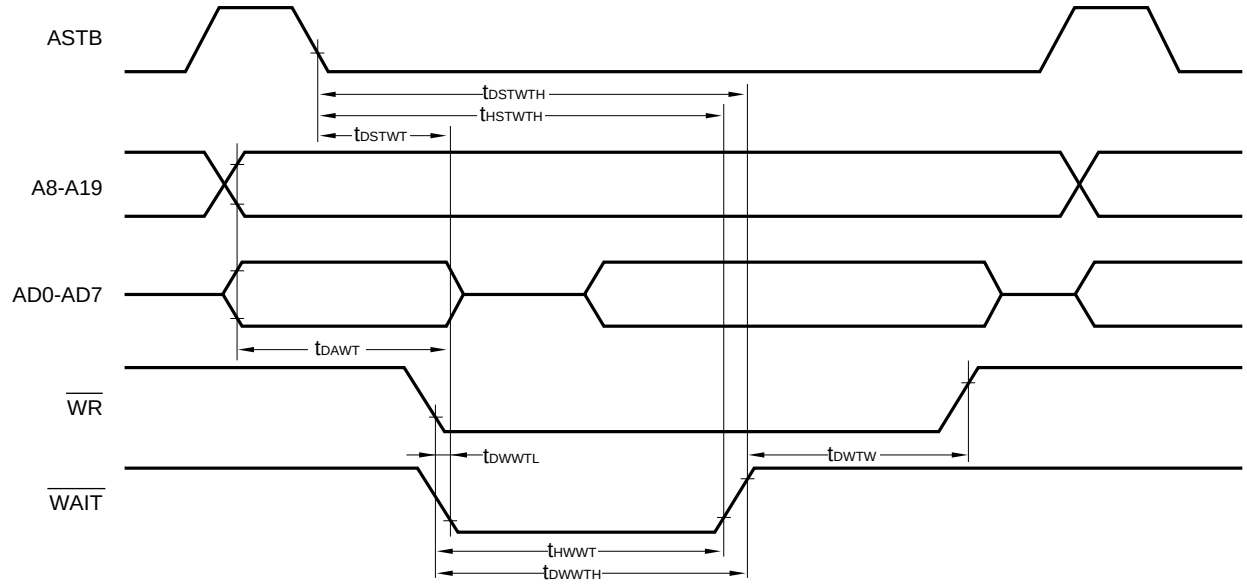


External WAIT Signal Input Timing

(1) Read operation

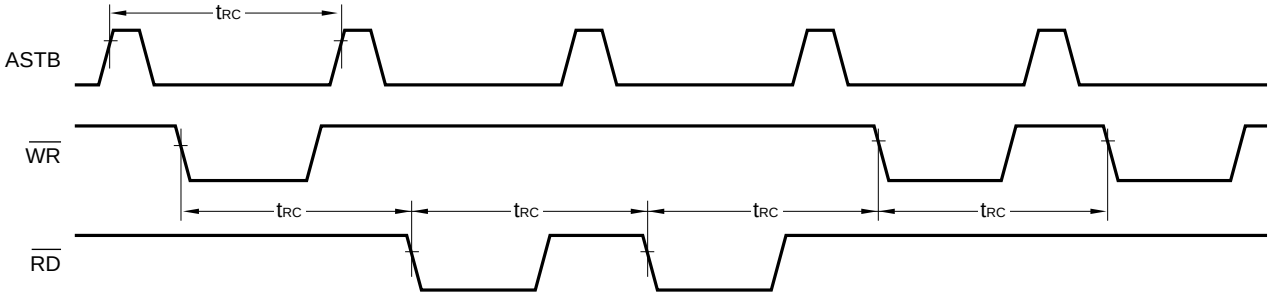


(2) Write operation

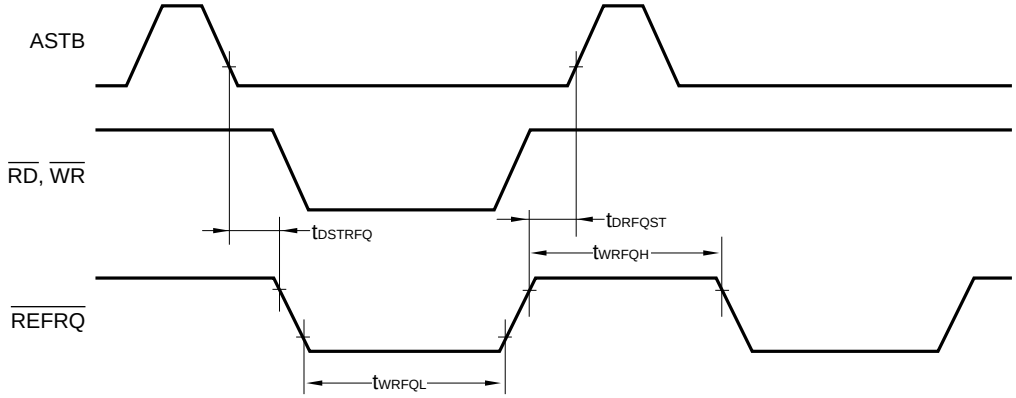


Timing Waveform for Refresh

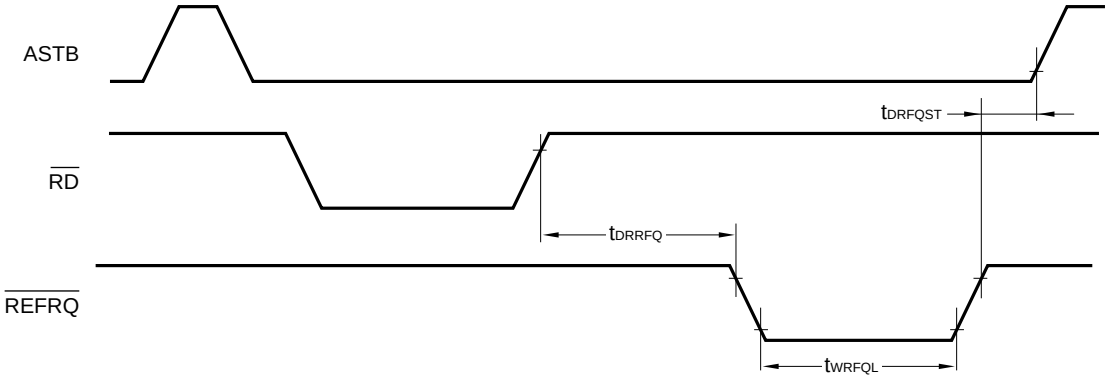
(1) Random read/write cycle



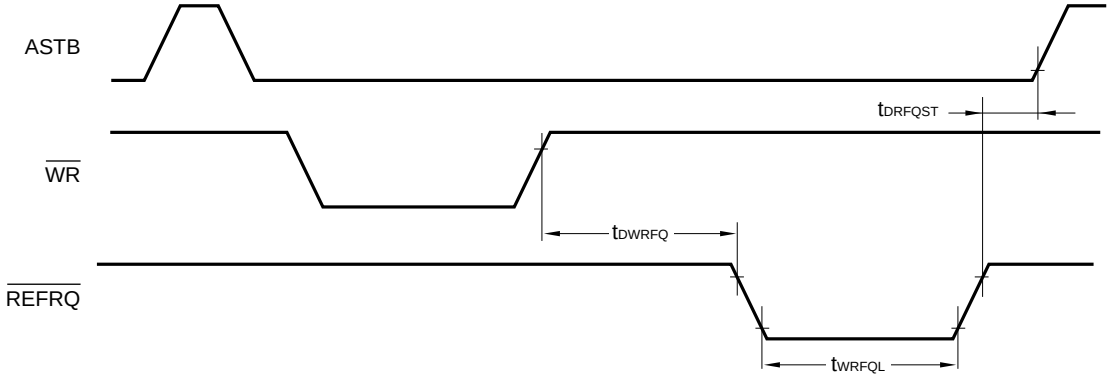
(2) When a refresh is performed simultaneously with a memory access



(3) Refresh after reading

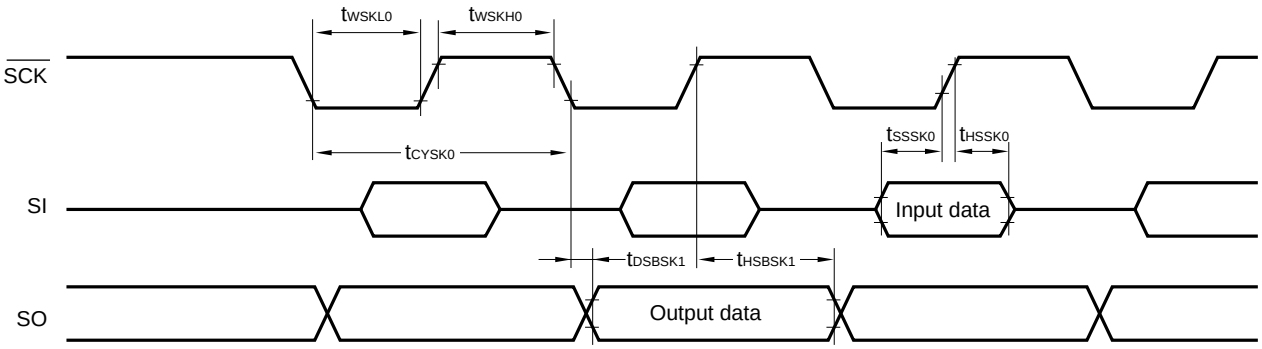


(4) Refresh after writing



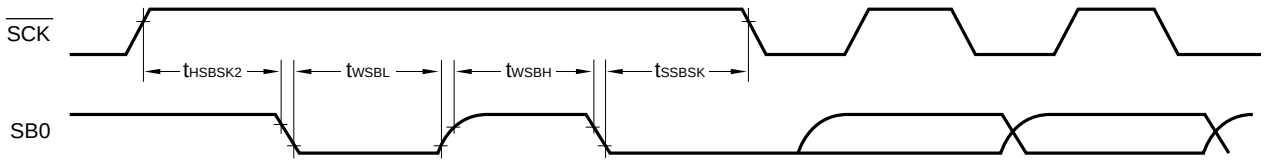
Serial Operation (CSI)

(1) Three-wire serial I/O mode

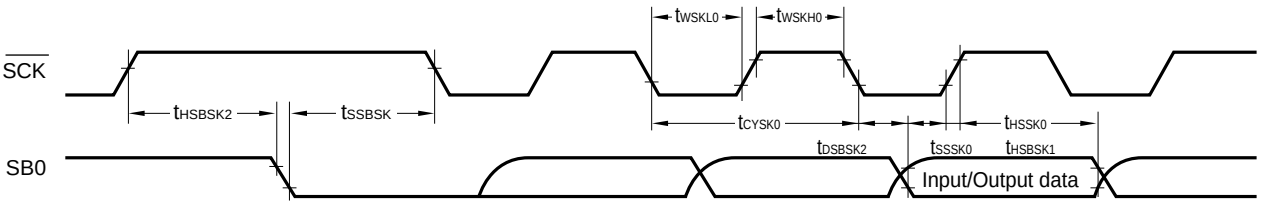


(2) SBI mode

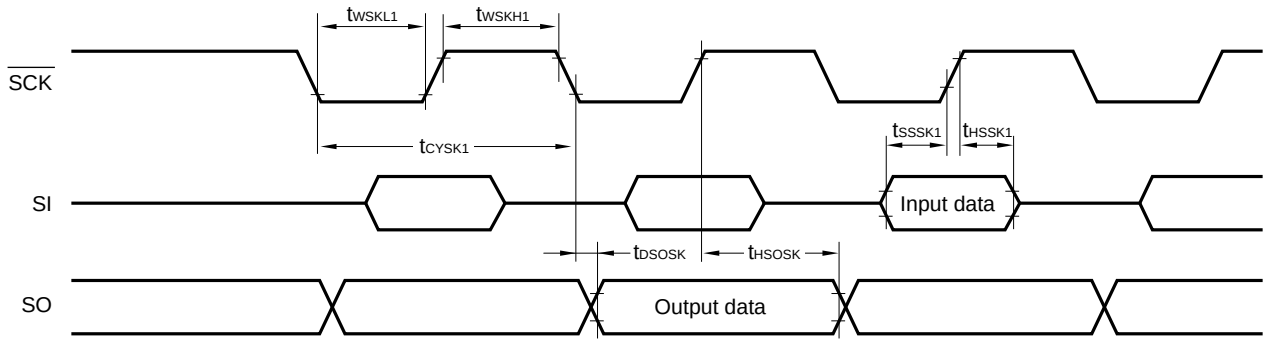
- Bus release signal transfer



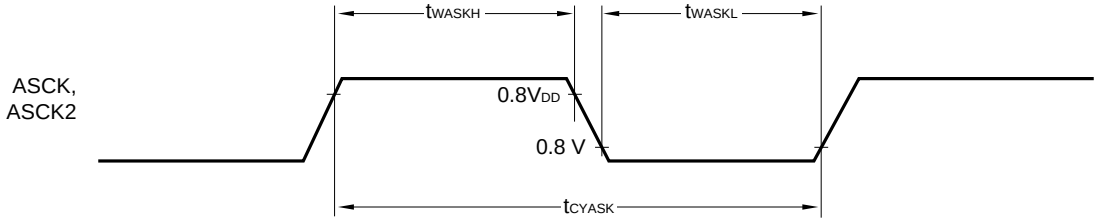
- Command signal transfer



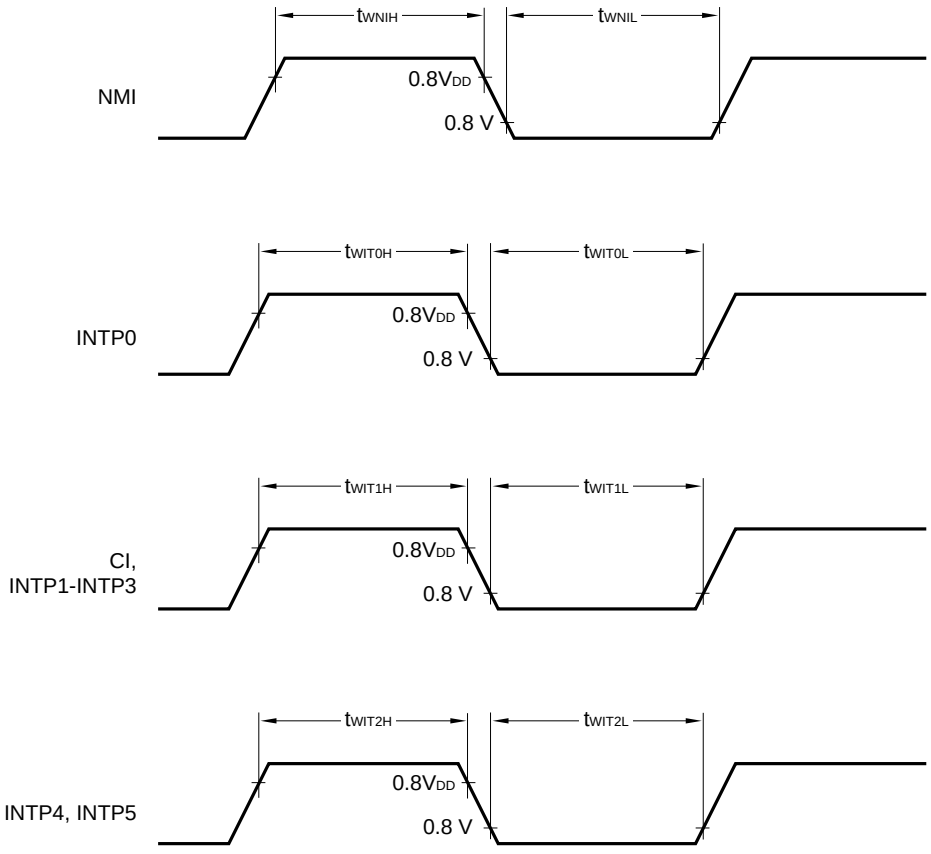
Serial Operation (IOE1, IOE2)



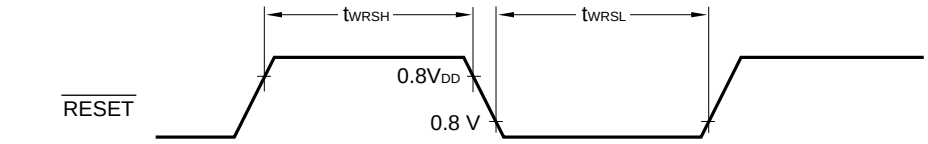
Serial Operation (UART, UART2)



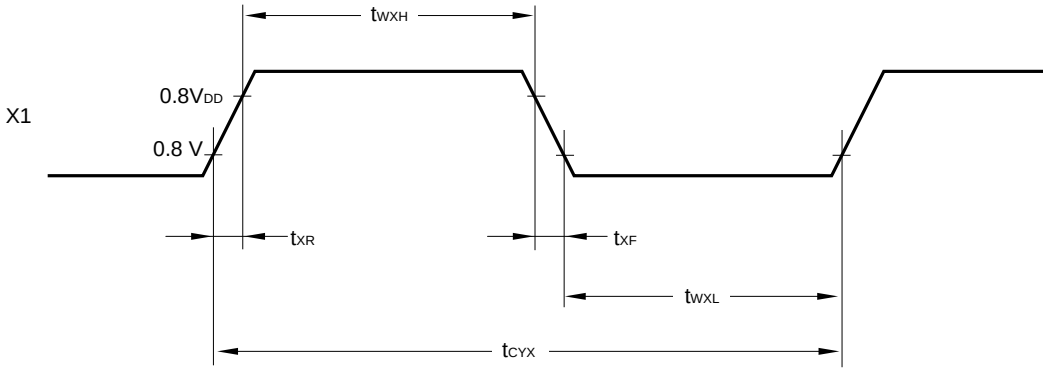
Interrupt Input Timing



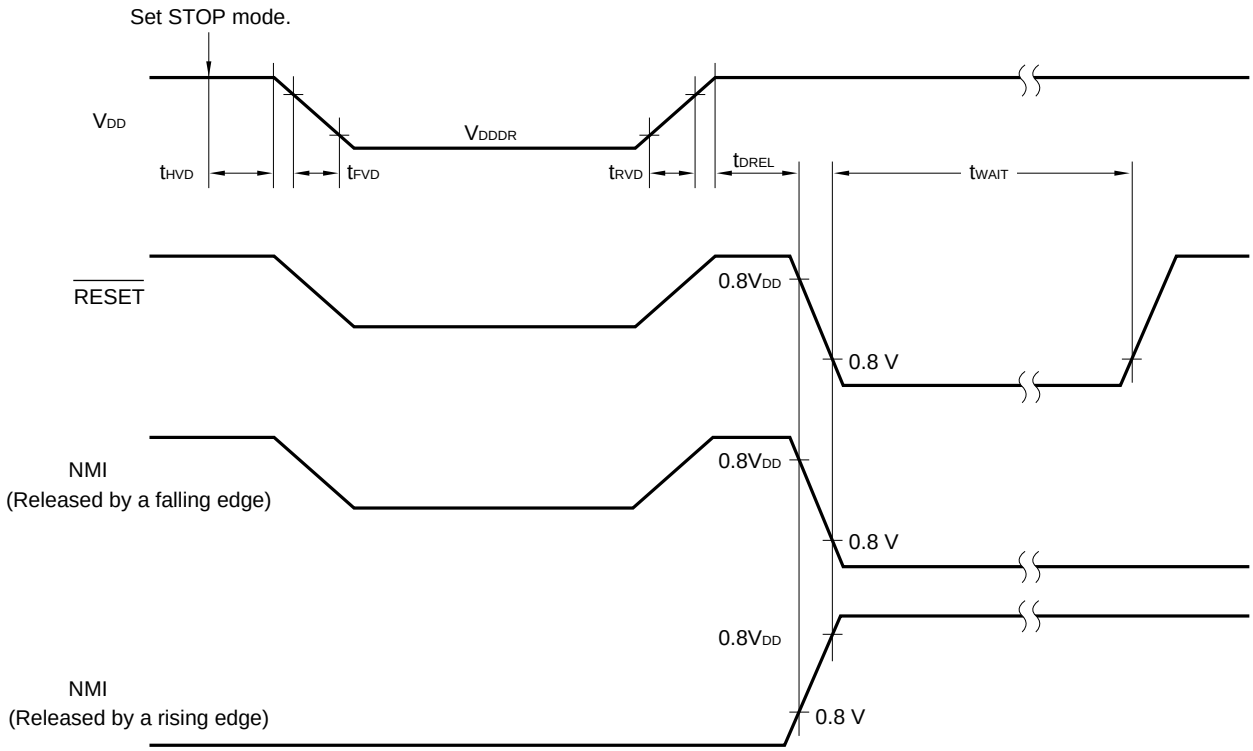
Reset Input Timing



External Clock Timing

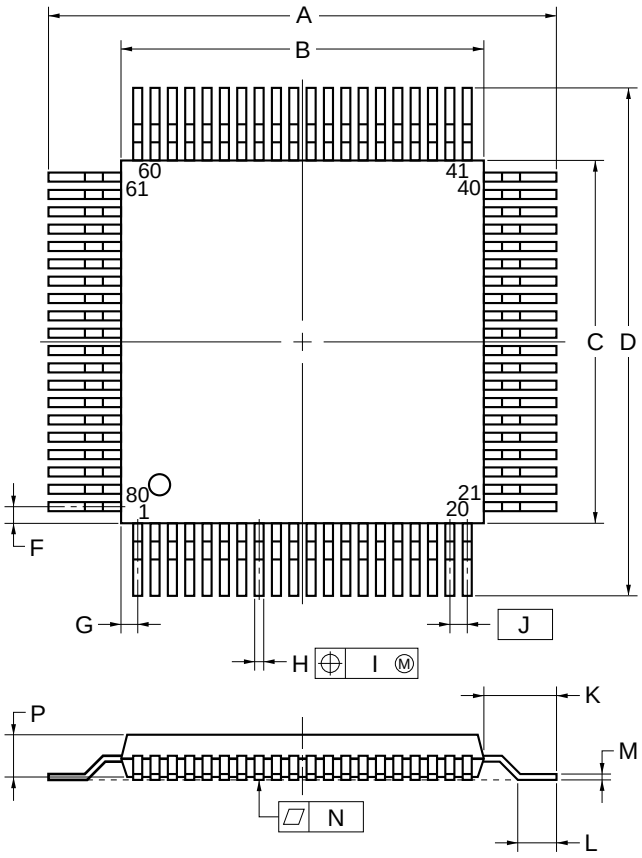


Data Retention Timing

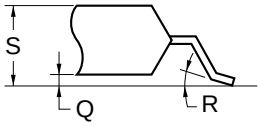


15. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

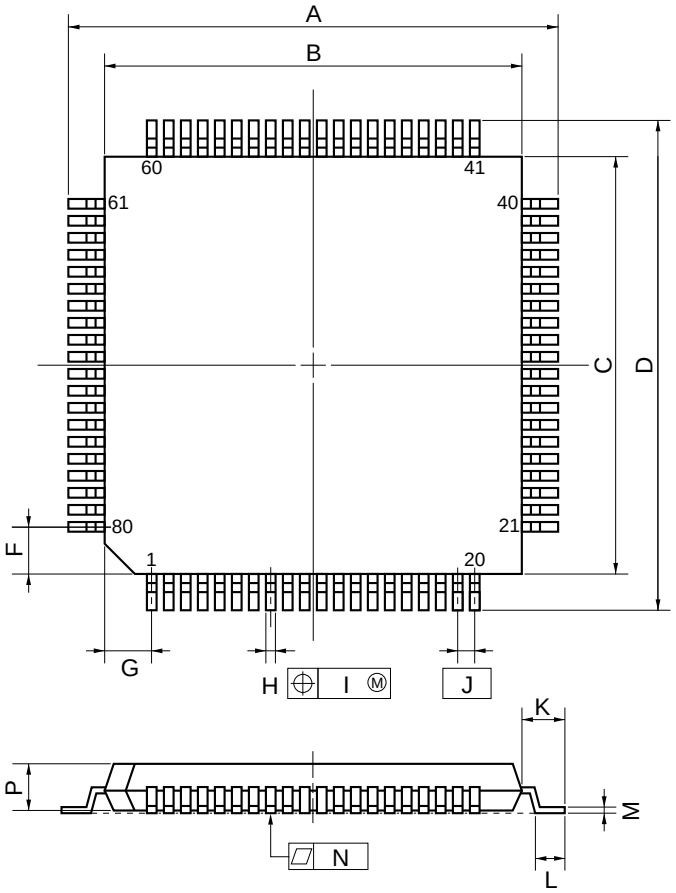
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

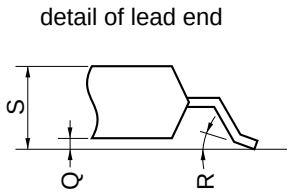
ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced products.

80 PIN PLASTIC TQFP (FINE PITCH) (□12) ★





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced products.

★ 16. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD784021.

For details of the recommended soldering conditions, refer to our document *SMD Surface Mount Technology Manual* (C10535E).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 16-1 Soldering Conditions for Surface-Mount Devices

(1) μPD784020GC-3B9 : 80-pin plastic QFP (14 × 14 mm)
μPD784021GC-3B9 : 80-pin plastic QFP (14 × 14 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 ½C Reflow time: 30 seconds or less (at 210 ½C or more) Maximum allowable number of reflow processes: 3	IR35-00-3
VPS	Peak package's surface temperature: 215 ½C Reflow time: 40 seconds or less (at 210 ½C or more) Maximum allowable number of reflow processes: 3	VP15-00-3
Wave soldering	Solder temperature: 260 ½C or less Flow time: 10 seconds or less Number of flow process: 1 Preheating temperature: 120 ½C max. (measured on the package surface)	WS60-00-1
Partial heating method	Terminal temperature: 300 ½C or less Flow time: 3 seconds or less (for each side of device)	–

(2) μPD784021GK-BE9: 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 ½C Reflow time: 30 seconds or less (at 210 ½C or more) Maximum allowable number of reflow processes: 2 Exposure limit[Note]: 7 days (10 hours of pre-baking is required at 125 ½C afterward.) <Cautions> Non-heat resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR35-107-2
VPS	Peak package's surface temperature: 215 ½C Reflow time: 40 seconds or less (at 200 ½C or more) Maximum allowable number of reflow processes: 2 Exposure limit[Note]: 7 days (10 hours of pre-baking is required at 125 ½C afterward.) <Cautions> Non-heat resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	VP15-107-2
Partial heating method	Terminal temperature: 300 ½C or less Flow time: 3 seconds or less (for each side of device)	–

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 ½C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD784021.

Language Processing Software

RA78K4[Note 1]	Assembler package for all 78K/IV series models
CC78K4[Note 1]	C compiler package for all 78K/IV series models
CC78K4-L[Note 1]	C compiler library source file for all 78K/IV series models

PROM Write Tools

PG-1500	PROM programmer
PA-78P4026GC PA-78P4038GK PA-78P4026KK	Programmer adaptor, connects to PG-1500
PG-1500 controller[Note 2]	Control program for PG-1500

Debugging Tools

IE-784000-R	In-circuit emulator for all μPD784026 sub-series models
IE-784000-R-BK	Break board for all 78K/IV series models
IE-784026-R-EM1 IE-784000-R-EM	Emulation board for evaluating μPD784026 sub-series models
IE-70000-98-IF-B	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine
IE-70000-98N-IF	Interface adapter and cable when a PC-9800 series notebook is used as the host machine
IE-70000-PC-IF-B	Interface adapter when the IBM PC/AT™ is used as the host machine
IE-78000-R-SV3	Interface adapter and cable when the EWS is used as the host machine
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (14 × 14 mm) for all μPD784026 sub-series
EP-78054GK-R	Emulation probe for 80-pin plastic TQFP (fine pitch) (12 × 12 mm) for all μPD784021
EV-9200GC-80	Socket for mounting on target system board made for 80-pin plastic QFP (14 × 14 mm)
EV-9500GK-80	Adapter for mounting on target system board made for 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
EV-9900	Tool used to remove the μPD78P4026KK-T from the EV-9200GC-80
SM78K4[Note 3]	System simulator for all 78K/IV series models
ID78K4[Note 3]	Integrated debugger for IE-784000-R
DF784026[Note 4]	Device file for all μPD784026 sub-series models

Real-time OS

RX78K/IV[Note 4]	Real-time OS for 78K/IV series models
MX78K4[Note 2]	OS for all 78K/IV series models

Remark The RA78K4, CC78K4, SM78K4, and ID78K4 are used with the DF784026.

Notes 1. • Based on PC-9800 series (MS-DOS™)
- Based on IBM PC/AT and compatibles (PC DOS™, Windows™, MS-DOS, and IBM DOS™)
- Based on HP9000 series 700™ (HP-UX™)
- Based on SPARCstation™ (SunOS™)
- Based on NEWS™ (NEWS-OS™)

2. • Based on PC-9800 series (MS-DOS)
- Based on IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, and IBM DOS)

3. • Based on PC-9800 series (MS-DOS + Windows)
- Based on IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, and IBM DOS)
- Based on HP9000 series 700 (HP-UX)
- Based on SPARCstation (SunOS)

4. • Based on PC-9800 series (MS-DOS)
- Based on IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, and IBM DOS)
- Based on HP9000 series 700 (HP-UX)
- Based on SPARCstation (SunOS)

APPENDIX B RELATED DOCUMENTS

Documents Related to Devices

Document name	Document No.	
	Japanese	English
μPD784020, 784021 Data Sheet	U11514J	This manual
μPD784025, 784026 Data Sheet	To be released soon	IP-3230
μPD78P4026 Data Sheet	To be released soon	IP3231
μPD784026 Sub-Series User's Manual, Hardware	U10898J	U10898E
μPD784026 Sub-Series Special Function Registers	U10593J	—
μPD784026 Sub-Series Application Note, Hardware Basic	U10573J	—
78K/IV Series User's Manual, Instruction	U10905J	IEU-1386
78K/IV Series Instruction Summary Sheet	U10594J	—
78K/IV Series Instruction Set	U10595J	—
78K/IV Series Application Note, Software Basic	U10095J	—

Documents Related to Development Tools (User's Manual)

Document name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Base		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Base		EEU-5008	U10540E
IE-784000-R		EEU-5004	EEU-1534
IE-784026-R-EM1		EEU-5017	EEU-1528
EP-78230		EEU-985	EEU-1515
EP-78054GK-R		EEU-932	EEU-1468
SM78K4 System Simulator Windows Base	Reference	U10093J	U10093E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K4 Integrated Debugger	Reference	U10440J	U10440E

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

Documents Related to Software to Be Incorporated into the Product (User's Manual)

Document name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Basic	U10603J	—
	Installation	U10604J	—
	Debugger	U10364J	—
OS for 78K/IV Series MX78K4		To be created	—

Other Documents

Document name	Document No.	
	Japanese	English
IC PACKAGE MANUAL	C10943X	
SMD Surface Mount Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Device	MEI-603	MEI-1202
Guide for Products Related to Micro-Computer: Other Companies	MEI-604	—

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

[MEMO]

Cautions on CMOS Devices

☒ Countermeasures against static electricity for all MOSs

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins.

Also handle boards on which MOS devices are mounted in the same way.

☒ CMOS-specific handling of unused input pins

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

☒ Statuses of all MOS devices at initialization

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Some related documents may be preliminary versions. Note that, however, what documents are preliminary is not indicated in this document.

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