- Synchronous Counting and Loading
- Two Count-Enable Inputs for n-Bit Cascading
- Asynchronous Reset (CD54HC160)
- Synchronous Reset (CD54HC162)
- Look-Ahead Carry for High-Speed Counting
- Operating Range 2-V to 6-V V_{CC}
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Process**
- Packaged in Ceramic (F) DIPs

CD54HC160, CD54HC162 . . . F PACKAGE (TOP VIEW) 16 V_{CC} CLR CLK [] 15 RCO A 🛮 3 14 Q_A В П 4 13 Q_B C [] 5 12 Q_C DΓ 11 Q_D 6 ENP [] 10 ENT GND ∏8 9 LOAD

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The CD54HC160 and CD54HC162 are BCD decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the CD54HC160 is asynchronous. A low level at the clear (CLR) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load (LOAD), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or LOAD) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The CD54HC160 and CD54HC162 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix), and are characterized for operation over the full military temperature range of -55°C to 125°C.



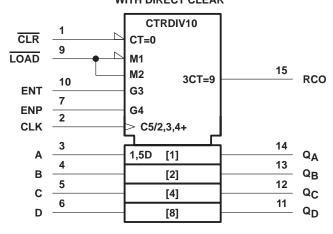
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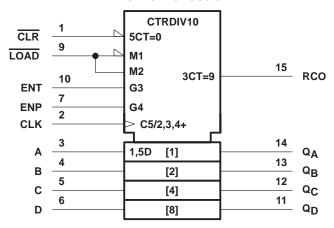


logic symbol[†]

CD54HC160 BINARY COUNTER WITH DIRECT CLEAR

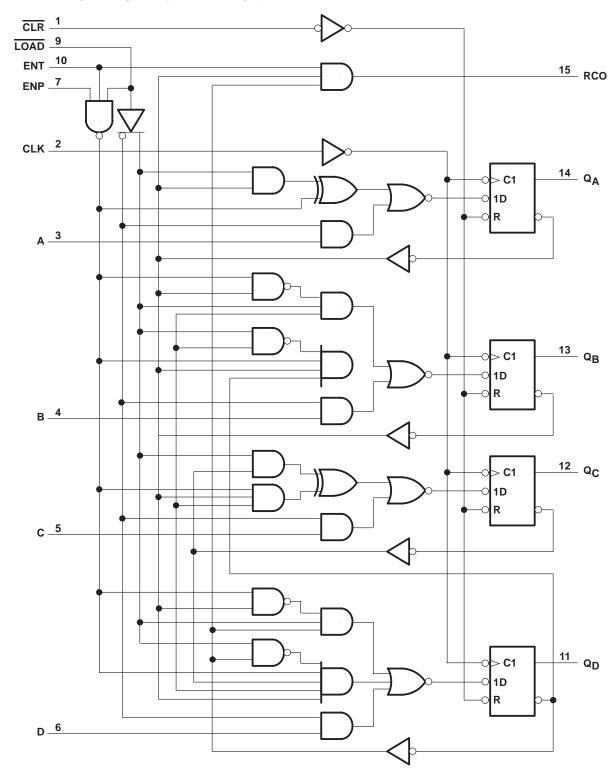


CD54HC162 BINARY COUNTER WITH SYNCHRONOUS CLEAR



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

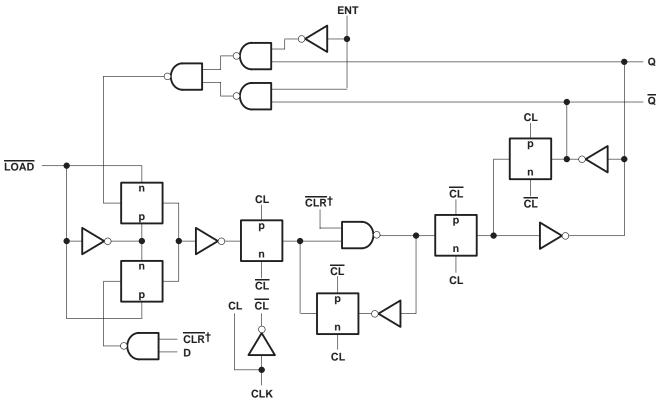
CD54HC160 logic diagram (positive logic)†



 $[\]ensuremath{^\dagger}$ CD54HC162 decade counter is similar; however, the clear is synchronous.



logic diagram, each D/T flip-flop (positive logic)



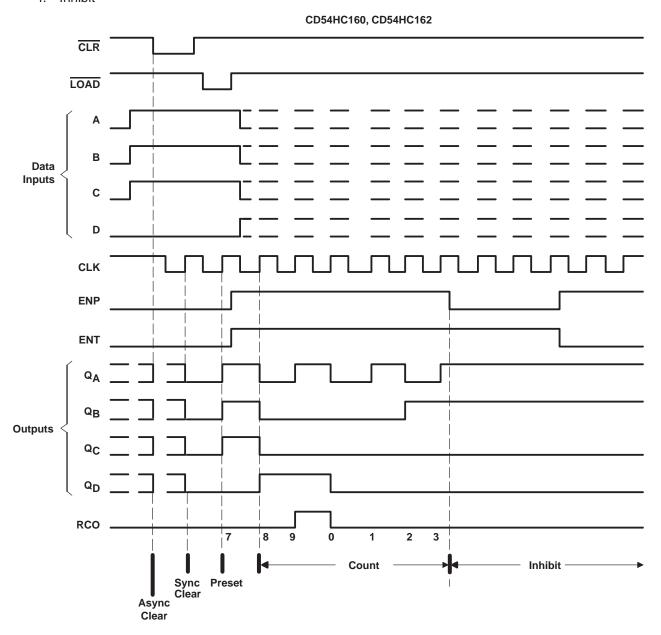
 \dagger Connect to VDD for CD54HC162.



typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

- 1. Clear outputs to zero (CD54HC160 is asynchronous; CD54HC162 is synchronous)
- 2. Preset BCD to seven
- 3. Count to eight, nine, zero, one, two, and three
- 4. Inhibit





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5	V to 7 V
Input voltage range, V _I (see Note 1)	V to 7 V
Output voltage range, VO (see Note 1)	+ 0.5 V
Input clamp current, I_{IK} ($V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$)	$\pm 20~\text{mA}$
Output clamp current, I_{OK} ($V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$)	±20 mA
Continuous output current, I_O ($V_O = -0.5 \text{ V}$ to $V_{CC} + 0.5 \text{ V}$)	±25 mA
Continuous current through V _{CC} or GND	
Power dissipation, PD (see Note 2)	500 mW
Storage temperature range, T _{stq} –65°C t	o 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	
Lead temperature, unit inserted into a PC board (minimum thickness 1,6 mm, 1/16 inch)	
with solder contacting lead tips only	. 300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Above 100°C, derate linearly at a factor of 8 mW/°C.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2	6	V
		V _{CC} = 2 V	1.5		
VIH		V _{CC} = 4.5 V	3.15		V
		V _{CC} = 6 V	4.2		
		V _{CC} = 2 V		0.5	
V_{IL}	Low-level input voltage	V _{CC} = 4.5 V		1.35	5 V
	V _{CC} = 6 V			1.8	
VI	Input voltage		0	VCC	V
VO	Output voltage		0	VCC	V
		V _{CC} = 2 V	0	1000	
t _r , t _f	Input transition rise or fall times	V _{CC} = 4.5 V	0	500	ns
	V _{CC} = 6 V			400	
T _A	Operating free-air temperature		-55	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vcc	T,	գ = 25°C	;	CD54HC160 CD54HC162		UNIT
			MIN	TYP	MAX	MIN	MAX	
		2 V	1.9			1.9		
	I _{OH} = -20 μA	4.5 V	4.4			4.4		
VOH		6 V	5.9			5.9		V
	I _{OH} = -4 mA	4.5 V	3.98			3.7		
	I _{OH} = -5.2 mA	6 V	5.48			5.2		
		2 V			0.1		0.1	
	I _{OL} = 20 μA	4.5 V			0.1		0.1	
V _{OL}		6 V			0.1		0.1	V
	I _{OL} = 4 mA	4.5 V			0.26		0.4	
	I _{OL} = 5.2 mA	6 V			0.26		0.4	
lı	$V_I = V_{CC}$ or GND	6 V			±0.1		±1	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	6 V			8		160	μΑ
C _{IN}					10		10	pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		CD54H CD54H	UNIT	
			MIN	MAX	MIN	MAX	
f _{max}	Maximum frequency	CLK	6		4		MHz
	Pulse duration	CLK low	80		120		
t _W	-uise duration	CLR low ('160 only)	100		150		ns
		Data (A, B, C, and D)	60		90		
		ENP, ENT	50		75		
t_{SU}	Setup time before CLK↑	LOAD low	60		90		ns
		CLR ('162 only)	65		100		
		CLR high ('160 only)	75		110		
		Data (A, B, C, and D)	3		3		
th	Hold time after CLK↑	ENP, ENT	0		0		ns
		LOAD low	3		3		

CD54HC160, CD54HC162 BCD SYNCHRONOUS DECADE COUNTERS

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timing requirements over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 1)

			T _A = 2	25°C	5°C CD54HC160 CD54HC162			
			MIN	MAX	MIN	MAX		
f _{max}	Maximum frequency	CLK	30		20		MHz	
t _w Pulse duration		CLK low	16		24		no	
t _W	Pulse duration	CLR low ('160 only)	20		30		ns	
		Data (A, B, C, and D)			18			
		ENP, ENT	10		15			
t _{su}	Setup time before CLK↑	LOAD low	12		18		ns	
		CLR ('162 only)	13		20			
		CLR high ('160 only)	15		22			
		Data (A, B, C, and D)	3		3			
t _h	Hold time after CLK↑	ENP, ENT	0		0		ns	
		LOAD low	3		3			

timing requirements over recommended operating free-air temperature range, V_{CC} = 6 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C CD54HC160 CD54HC162				UNIT
			MIN	MAX	MIN	MAX	
f _{max}	Maximum frequency	CLK	35		24		MHz
	Pulse duration	CLK low	14		20		
t _W	Pulse duration	CLR low ('160 only)	17		26		ns
		Data (A, B, C, and D)	10		15		
		ENP, ENT	9		13		
t _{su}	Setup time before CLK↑	LOAD low	10		15		ns
		CLR ('162 only)	11		17		
		CLR high ('160 only)	13		19		
		Data (A, B, C, and D)	3		3		
t _h	Hold time after CLK↑	ENP, ENT	0		0		ns
		LOAD low	3		3		1

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C	CD54HC160 CD54HC162	UNIT
	(1141 01)	(0011 01)	CALACITANCE	MIN MAX	MIN MAX	
^t PLH	CLIX	RCO	C _L = 50 pF	185	280	ns
^t PHL	CLK	RCO	CL = 30 pr	185	280	115
^t PLH	CLK	0	C _L = 50 pF	185	280	ns
^t PHL		Q	оц = 30 рі	185	280	113
^t PLH	ENT	DOO	C _L = 50 pF	120	180	ns
^t PHL		RCO	CL = 30 μr	120	180	115
+		Q ('160 only)	C _I = 50 pF	210	315	ns
^t PHL	CLR	RCO ('160 only)		210	315	115
tTLH			C ₁ = 50 pF	75	110	ns
tTHL			CL = 50 pr	75	110	115

switching characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C	CD54HC160 CD54HC162	UNIT								
	(INI O1)	(0011 01)	CAI ACITANCE	MIN MAX	MIN MAX									
t _{PLH}	CLK	RCO	C ₁ = 50 pF	37	56	ns								
^t PHL	CLK	RCO	С <u> = 30 рі</u>	37	56	113								
^t PLH	CLK	0	C _L = 50 pF	37	56	ns								
^t PHL		Q	CL = 30 pr	37	56	115								
^t PLH	ENT	DOO	C _L = 50 pF	24	36	ns								
^t PHL	ENT	RCO	CL = 30 pr	24	36	115								
+		Q ('160 only)	C 50 pE	42	63									
^t PHL	CLR RCO ('160 only)		CLR	RCO ('160 only)		RCO ('160 only)		RCO ('160 only)		CLR	RCO ('160 only)		63	ns
t _{TLH}			C 50 pF	15	22									
tTHL			$C_L = 50 \text{ pF}$	15	22	ns								

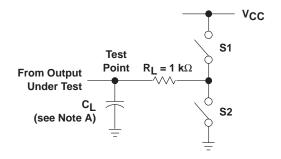
CD54HC160, CD54HC162 BCD SYNCHRONOUS DECADE COUNTERS

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 6 V (unless otherwise noted) (see Figure 1)

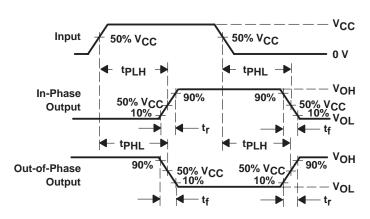
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C	CD54HC160 CD54HC162	UNIT
	(INI O1)	(0011 01)	CALACITANCE	MIN MAX	MIN MAX	
^t PLH	0114	B00	C _L = 50 pF	3	1 48	ns
^t PHL	CLK	RCO	CL = 50 pr	3	1 48	115
t _{PLH}	CLK		C _L = 50 pF	3	1 48	ns
^t PHL		Q	CL = 30 μ	3	1 48	115
^t PLH	ENIT		C 50 pE	20	31	ns
^t PHL	ENT	RCO	C _L = 50 pF	20	31	115
4		Q ('160 only)	C. 50 pF	30	54	
^t PHL	CLR	RCO ('160 only)	$C_L = 50 \text{ pF}$	30	5 54	ns
tTLH			C 50 pF	1;	3 19	no
^t THL			$C_L = 50 \text{ pF}$	1;	3 19	ns

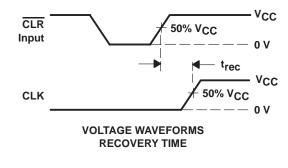
PARAMETER MEASUREMENT INFORMATION



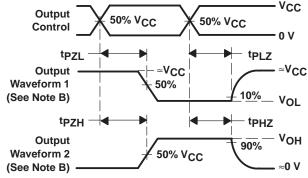
LOAD CIRCUIT

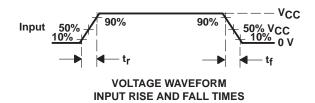
PARAMETER S1 S2 Open Closed ^tPZH ten Closed **tPZL** Open ^tPHZ Open Closed tdis Closed Open **tPLZ** tpd or tt Open Open





VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f = 6 ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



PACKAGE OPTION ADDENDUM

30-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD54HC160F3A	OBSOLETE	CDIP	J	16	TBD	Call TI	Call TI
CD54HC162F3A	OBSOLETE	CDIP	J	16	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

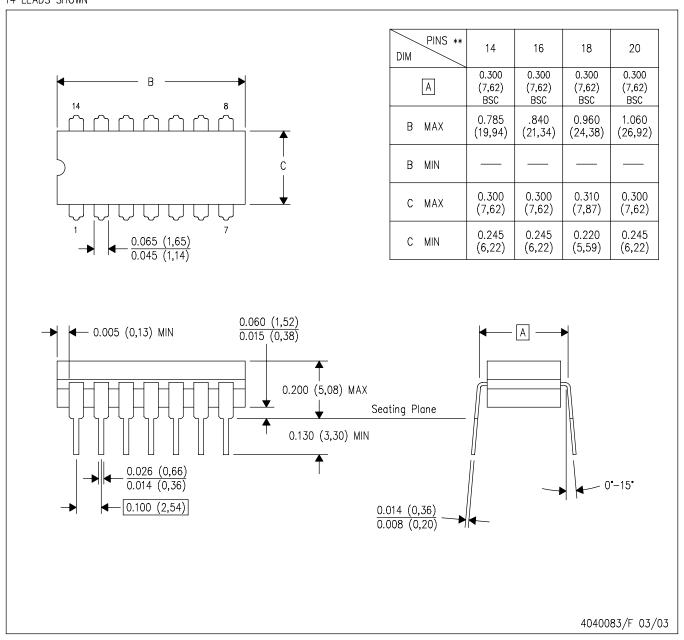
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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