Ordering Information		
Part Numbers	**Description**	**Module Speed**
SG572568FG8D6DB	256Mx72 (2GB), DDR2, 240-pin DIMM, Unbuffered, ECC, 128Mx8 Based, DDR2-400-333, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-3200 @ CL 3.0
SG572568FG8D6DG	256Mx72 (2GB), DDR2, 240-pin DIMM, Unbuffered, ECC, 128Mx8 Based, DDR2-533-444, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-4200 @ CL 4.0
SG572568FG8D6IL	256Mx72 (2GB), DDR2, 240-pin DIMM, Unbuffered, ECC, 128Mx8 Based, DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-5300 @ CL 5.0
SG572568FG8D6IR	256Mx72 (2GB), DDR2, 240-pin DIMM, Unbuffered, ECC, 128Mx8 Based, DDR2-800-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-6400 @ CL 5.0
SG572568FG8D6KF	256Mx72 (2GB), DDR2, 240-pin DIMM, Unbuffered, ECC, 128Mx8 Based, DDR2-800-666, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-6400 @ CL 6.0

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Revision History

- **September 28, 2008**
  Added SG572568FG8D6IR & SG572568FG8D6KF to the Ordering Information on page 1.

- **May 17, 2006**
  Corrected the OCD Program in the EMRS on page 14.
  Changed the Ambient Operating temperature to 0 to +65°C on page 16.
  Added the Case Operating temperature on page 16.

- **September 13, 2005**
  Corrected the DLL Enable in the EMRS on page 14.

- **July 28, 2005**
  Changed datasheet part number from SG572568FG8D6DU to SG572568FG8D6UU because of the addition of a new option in CAS Latency.
  Added SG572568FG8D6IL to the Ordering Information on page 1.

- **May 10, 2005**
  Datasheet released.

2GByte (256Mx72) DDR2 SDRAM Module - 128Mx8 Based 240-pin DIMM, Unbuffered, ECC

Features

- Standard : JEDEC
- Configuration : ECC
- Cycle Time : 5.0ns (DDR2-400)
  3.75ns (DDR2-533)
  3.0ns (DDR2-667)
  2.5ns (DDR2-800
- CAS# Latency : 3.0, 4.0 (-DB/-DG)
  4.0, 5.0 (-IL/-IR)
  5.0, 6.0 (-KF)
- Posted CAS#/Additive Latency (AL) : 0, 1.0, 2.0, 3.0 & 4.0
- Write Latency (WL) : Read (CAS#) Latency - 1
- Burst Length : 4, 8
- Burst Type : Sequential/Interleave
- Module Ranks : 2 Ranks of x8 devices
- No. of Devices : 18
- No. of Internal Banks per SDRAM : 8
- Operating Voltage : 1.8V
- Refresh : 8K/64ms
- Device Physicals : FBGA
- Lead Finish : Gold
- Length x Height : 133.35mm x 30.00mm
- No. of sides : Double-sided
- Mating Connector (Examples)
  Vertical : Molex - 87705-0021

DDR2 240-Pin DIMM Pin List

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	V_{REF}	31	DQ19	61	A4	91	V_{SS}	121	V_{SS}	151	V_{SS}	181	V_{DDQ}	211	DM5
2	V_{SS}	32	V_{SS}	62	V_{DDQ}	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	V_{SS}
4	DQ1	34	DQ25	64	V_{DD}	94	V_{SS}	124	V_{SS}	154	V_{SS}	184	V_{DD}	214	DQ46
5	V_{SS}	35	V_{SS}	65	V_{SS}	95	DQ42	125	DM0	155	DM3	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	V_{SS}	96	DQ43	126	NC	156	NC	186	CK0#	216	V_{SS}
7	DQS0	37	DQS3	67	V_{DD}	97	V_{SS}	127	V_{SS}	157	V_{SS}	187	V_{DD}	217	DQ52
8	V_{SS}	38	V_{SS}	68	NC	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	V_{DD}	99	DQ49	129	DQ7	159	DQ31	189	V_{DD}	219	V_{SS}
10	DQ3	40	DQ27	70	A10/AP	100	V_{SS}	130	V_{SS}	160	V_{SS}	190	BA1	220	CK2
11	V_{SS}	41	V_{SS}	71	BA0	101	SA2	131	DQ12	161	CB4	191	V_{DDQ}	221	CK2#
12	DQ8	42	CB0	72	V_{DDQ}	102	NC	132	DQ13	162	CB5	192	RAS#	222	V_{SS}
13	DQ9	43	CB1	73	WE#	103	V_{SS}	133	V_{SS}	163	V_{SS}	193	CS0#	223	DM6
14	V_{SS}	44	V_{SS}	74	CAS#	104	DQS6#	134	DM1	164	DM8	194	V_{DDQ}	224	NC
15	DQS1#	45	DQS8#	75	V_{DDQ}	105	DQS6	135	NC	165	NC	195	ODT0	225	V_{SS}
16	DQS1	46	DQS8	76	CS1#	106	V_{SS}	136	V_{SS}	166	V_{SS}	196	A13	226	DQ54
17	V_{SS}	47	V_{SS}	77	ODT1	107	DQ50	137	CK1	167	CB6	197	V_{DD}	227	DQ55
18	NC	48	CB2	78	V_{DDQ}	108	DQ51	138	CK1#	168	CB7	198	V_{SS}	228	V_{SS}
19	NC	49	CB3	79	V_{SS}	109	V_{SS}	139	V_{SS}	169	V_{SS}	199	DQ36	229	DQ60
20	V_{SS}	50	V_{SS}	80	DQ32	110	DQ56	140	DQ14	170	V_{DDQ}	200	DQ37	230	DQ61

DDR2 240-pin DIMM Pin List (Contd.)

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
21	DQ10	51	V_{DDQ}	81	DQ33	111	DQ57	141	DQ15	171	CKE1	201	V_{SS}	231	V_{SS}
22	DQ11	52	CKE0	82	V_{SS}	112	V_{SS}	142	V_{SS}	172	V_{DD}	202	DM4	232	DM7
23	V_{SS}	53	V_{DD}	83	DQS4#	113	DQS7#	143	DQ20	173	A15 (NC)	203	NC	233	NC
24	DQ16	54	BA2	84	DQS4	114	DQS7	144	DQ21	174	A14 (NC)	204	V_{SS}	234	V_{SS}
25	DQ17	55	NC	85	V_{SS}	115	V_{SS}	145	V_{SS}	175	V_{DDQ}	205	DQ38	235	DQ62
26	V_{SS}	56	V_{DDQ}	86	DQ34	116	DQ58	146	DM2	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NC	177	A9	207	V_{SS}	237	V_{SS}
28	DQS2	58	A7	88	V_{SS}	118	V_{SS}	148	V_{SS}	178	V_{DD}	208	DQ44	238	V_{DDSPD}
29	V_{SS}	59	V_{DD}	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	V_{SS}	240	SA1

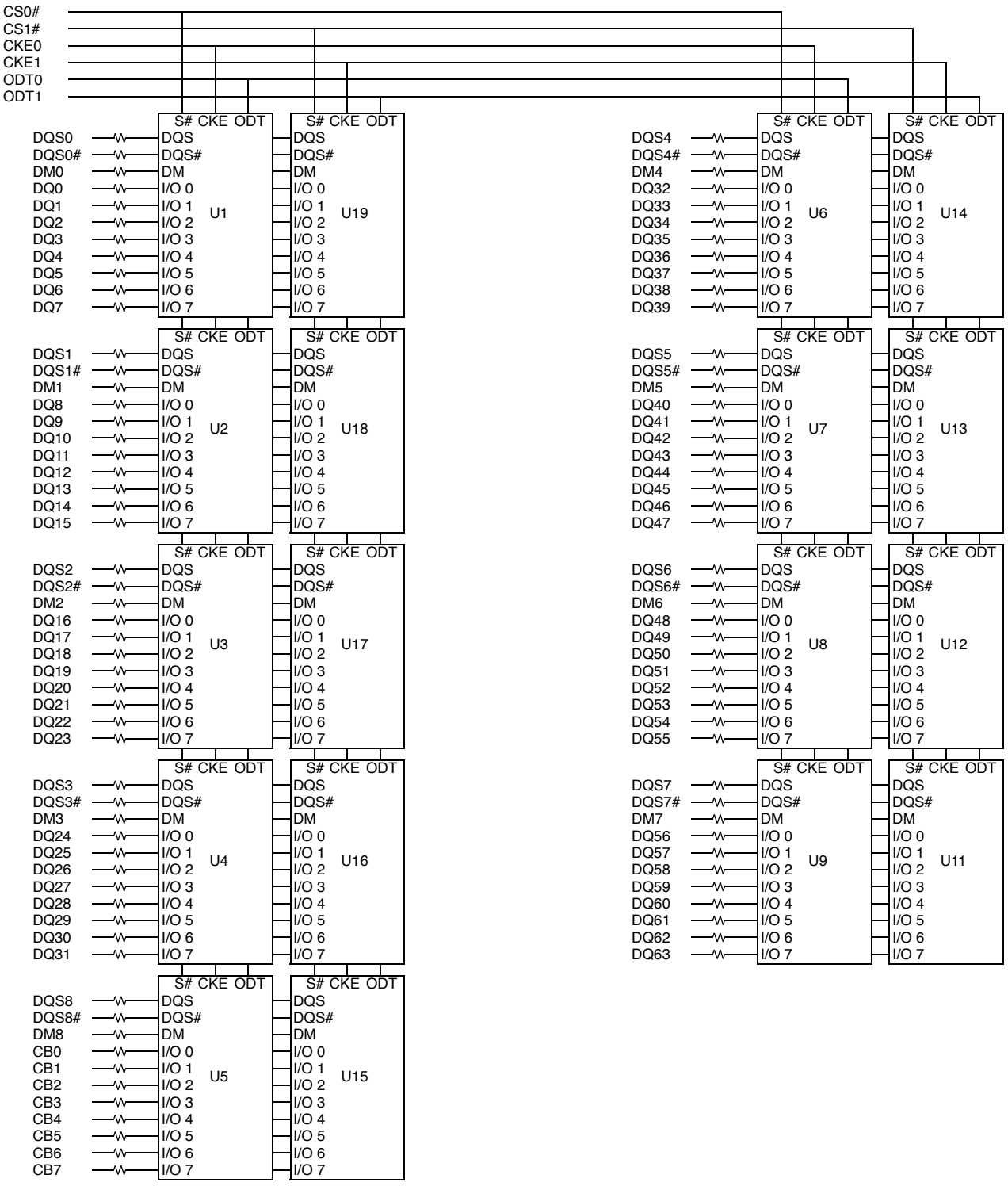
Pin Description Table

Symbol	Type	Polarity	Function
CK0~CK2	SSTL_18	Positive Edge	Positive line of the differential pair of system clock inputs. (All DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks. Output data is referenced at the crossings of the clocks.)
CK0#~CK2#	SSTL_18	Negative Edge	Negative line of the differential pair of system clock inputs.
ODT0, ODT1	SSTL_18	Active High	On-Die Termination: ODT when high enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, and DM. The ODT input will be ignored if disabled in Extended Mode Register (EMRS).
CKE0, CKE1	SSTL_18	Active High	Activates the DDR2 SDRAM CLK signal when high and deactivates the CLK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CS0#, CS1#	SSTL_18	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	SSTL_18	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operations to be executed by the SDRAM.
BA0~BA2	SSTL_18	-	Bank Address define to which bank an Activate, Read, Write or Precharge command is being applied. Bank address also determines if the Mode Register or Extended Mode Register is to be accessed during a MRS or EMRS cycle.

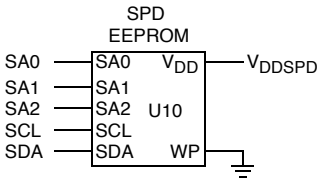
Pin Description Table (Contd.)

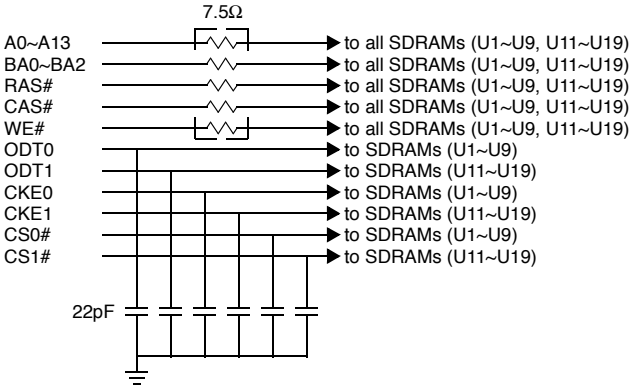
Symbol	Type	Polarity	Function
A0~A9, A10/AP, A11~A13	SSTL_18	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0~BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0~BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0~BA2. If AP is low, BA0~BA2 are used to define which bank to precharge. The address inputs also provide the op-code during Mode Register Set commands.
DQ0~DQ63 CB0~CB7	SSTL_18	-	Data and Check Bit Input/Output pins.
DQS0~DQS8	SSTL_18	Positive Edge	SDRAM differential data strobe for input and output data.
DQS0#~DQS8#	SSTL_18	Negative Edge	SDRAM differential data strobe for input and output data.
DM0~DM8	SSTL_18	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ/DQS loading.
SA0~SA2	LVTTL	-	Slave Address Select for EEPROM. These pins are used to configure the presence-detect device.
SDA	LVTTL	-	Serial Bus Data Line for EEPROM. SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. A resistor must be connected from the SDA bus line to V_{DDSPD} to act as pull up on the system board.
SCL	LVTTL	-	Serial Bus Clock for EEPROM. SCL is used to synchronize the presence-detect data transfer to and from the module. A resistor may be connected from the SCL bus line to V_{DDSPD} to act as pull up on the system board.
V_{DD}	Supply	-	SDRAM positive power supply. 1.8V±0.1V
V_{SS}	Supply	-	Power supply return (ground).
V_{REF}	Supply	-	SDRAM I/O reference supply.
V_{DDQ}	Supply	-	SDRAM I/O Driver positive power supply. 1.8V±0.1V
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports operation from 1.7V to 3.6V).
NC	-	-	No Connect.
DU	-	-	Do not use.

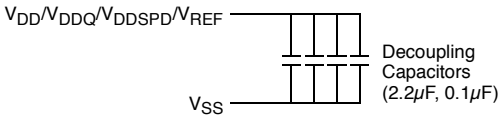
Block Diagram



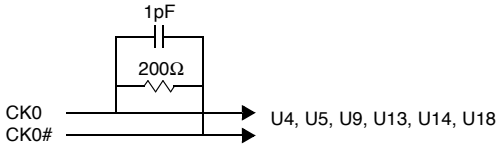
Note: Unless otherwise noted, data resistor values are 22Ω ± 5%.

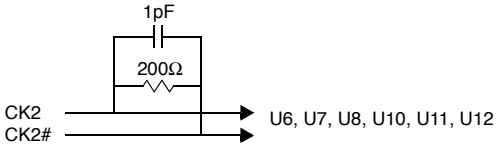


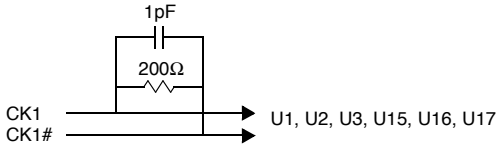




Clock Wiring	
CK0/CK0#	6 SDRAMs
CK1/CK1#	6 SDRAMs
CK2/CK2#	6 SDRAMs



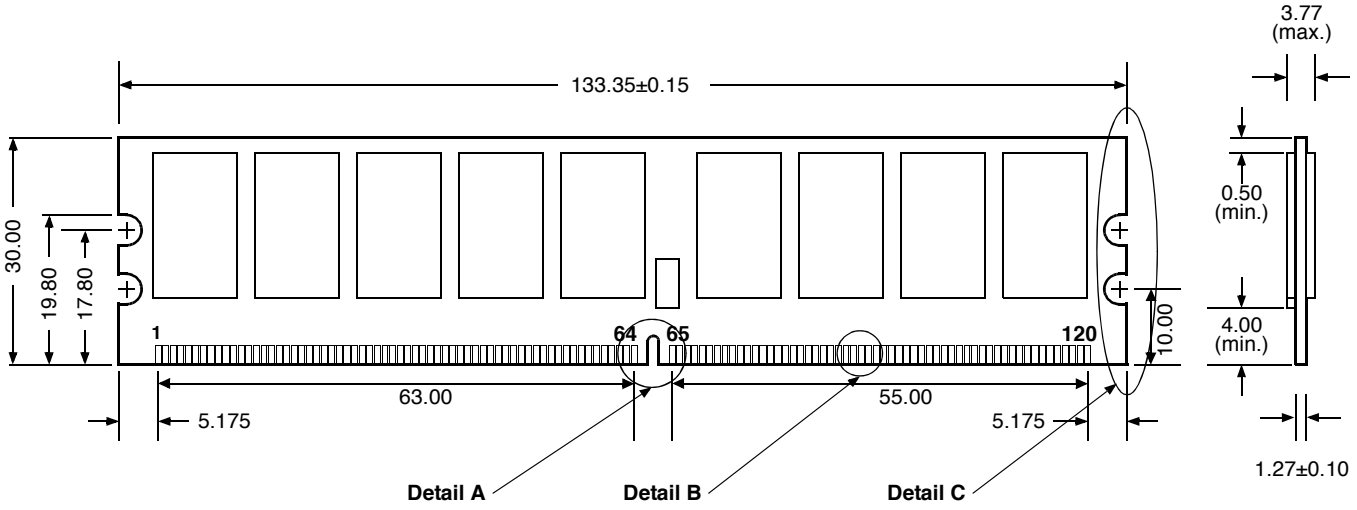




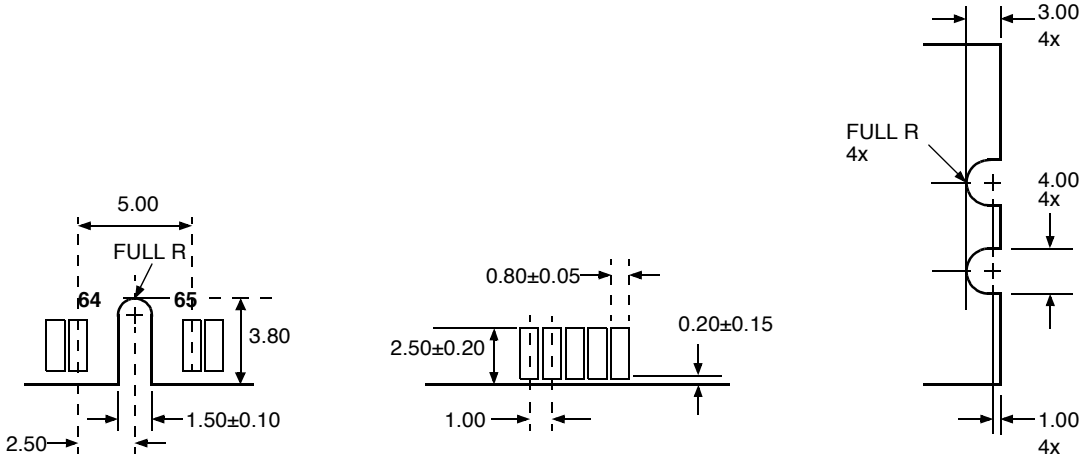
Notes:
1. Ax, BAx, RAS#, CAS#, WE# resistors: 7.5Ω±5%.
2. Data bits may be swapped within a device. However, DQ/DQS relationship is maintained as shown.

Physical Dimensions

240-pin DIMM Module



Front View



Detail A **Detail B** **Detail C**

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Serial Presence Detect Table

Byte No.	Byte Description	Speed	Value Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	All	128 Bytes	80h
1	Total # of bytes of SPD memory device	All	256 Bytes	08h
2	Fundamental memory type	All	SDRAM DDR2	08h
3	# of row address on this assembly	All	14	0Eh
4	# of column address on this assembly	All	10	0Ah
5	# of Ranks, Package and Height	All	2, Planar, 30.00mm	61h
6	Data width of this assembly	All	72	48h
7	Reserved	All	-	00h
8	Voltage interface standard of this assembly	All	SSTL_18	05h
9	SDRAM cycle time @ CAS latency of X	-DB -DG -IL -IR/KF	5.0ns 3.75ns 3.0ns 2.5ns	50h 3Dh 30h 25h
10	SDRAM access time @ CAS latency of X	-DB -DG -IL -IR/KF	0.60ns 0.50ns 0.45ns 0.40ns	60h 50h 45h 40h
11	DIMM configuration type	All	ECC	02h
12	Refresh rate & type	All	SR, 7.8	82h
13	Primary SDRAM width	All	8	08h
14	Error checking SDRAM width	All	8	08h
15	Reserved	All	-	00h
16	SDRAM device attributes : Burst lengths supported	All	4, 8	0Ch
17	SDRAM device attributes : # of banks on SDRAM device	All	8	08h
18	SDRAM device attributes : CAS latency	-DB/DG -IL/IR -KF	3.0, 4.0 4.0, 5.0 5.0, 6.0	18h 30h 60h
19	DIMM Mechanical Characteristics	-DB -DG/IL/IR/KF	- 3.77mm	00h 01h
20	DIMM type information	All	UDIMM	02h
21	SDRAM module attributes	All	None	00h

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
22	SDRAM device attributes : General	-DB/DG -IL/IR/KF	Weak Driver Weak Driver, 50Ω ODT	01h 03h
23	SDRAM cycle time @ CAS latency of X-1	-DB/DG -IL/IR -KF	5.0ns 3.75ns 3.0ns	50h 3Dh 30h
24	SDRAM access time @ CAS latency of X-1	-DB -DG/IR -IL/KF	0.60ns 0.50ns 0.45ns	60h 50h 45h
25	SDRAM cycle time @ CAS latency of X-2	All	-	00h
26	SDRAM access time @ CAS latency of X-2	All	-	00h
27	Minimum row precharge time (=tRP)	-DB/DG/IL/KF -IR	15ns 12.5ns	3Ch 32h
28	Minimum row active to row active delay (=tRRD)	All	7.5ns	1Eh
29	Minimum RAS to CAS delay (=tRCD)	-DB/DG/IL/KF -IR	15ns 12.5ns	3Ch 32h
30	Minimum activate precharge time (=tRAS)	-DB -DG/IL/IR/KF	40ns 45ns	28h 2Dh
31	Module row density	All	1GB	01h
32	Command and Address signal input setup time	-DB -DG -IL -IR/KF	0.35ns 0.25ns 0.20ns 0.17ns	35h 25h 20h 17h
33	Command and Address signal input hold time	-DB -DG -IL -IR/KF	0.47ns 0.37ns 0.27ns 0.25ns	47h 37h 27h 25h
34	Data signal input setup time	-DB -DG/IL -IR/KF	0.15ns 0.10ns 0.05ns	15h 10h 05h
35	Data signal input hold time	-DB -DG -IL -IR/KF	0.27ns 0.22ns 0.17ns 0.12ns	27h 22h 17h 12h
36	Write recovery time (=tWR)	All	15ns	3Ch

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
37	Internal write to read command delay (=tWTR)	-DB -DG/IL/IR/KF	10ns 7.5ns	28h 1Eh
38	Internal read to precharge delay (=tRTP)	All	7.5ns	1Eh
39	Memory Analysis Probe Characteristics	All	-	00h
40	Extension of tRC and tRFC	-DB/DG/IL/KF -IR	Extension of tRFC Ext. of tRC & tRFC	06h 36h
41	Device Minimum activate/auto-refresh time (=tRC)	-DB/DG -IL/KF -IR	55ns 60ns 57.5ns	37h 3Ch 39h
42	Device Minimum auto-refresh to active/ auto-refresh time (=tRFC)	All	127.5ns	7Fh
43	Maximum device cycle time (=tCK max)	All	8ns	80h
44	Device DQS-DQ skew for DQS and associated DQ signals (=tDQSQ max)	-DB -DG -IL -IR/KF	0.35ns 0.30ns 0.24ns 0.20ns	23h 1Eh 18h 14h
45	Device read data hold skew factor (=tQHS)	-DB -DG -IL -IR/KF	0.45ns 0.40ns 0.34ns 0.30ns	2Dh 28h 22h 1Eh
46	PLL relock time	All	-	00h
47~61	Reserved	All	-	00h
62	SPD data revision code	-DB -DG/IL -IR/KF	1.0 1.2 1.3	10h 12h 13h
63	Checksum for bytes 0~62	-DB -DG -IL -IR -KF		0Eh AAh 62h 54h 53h
64	Manufacturer JEDEC ID code	All	Continuation Code	7Fh
65	.....Manufacturer JEDEC ID code	All	SMART's ID	94h
66~71	.....Manufacturer JEDEC ID code	-DB -DG/IL/IR/KF	- -	FFh 00h
72	Manufacturing location	All	See Note 2	01h

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
73~90	Manufacturer part #	-DB -DG -IL -IR -KF	SG572568FG8D6DB SG572568FG8D6DG SG572568FG8D6IL SG572568FG8D6IR SG572568FG8D6KF	Part No.
91	Manufacturer revision code	All	Rev. 0	00h
92	.....Manufacturer revision code	-DB -DG/IL/IR/KF	- -	FFh 00h
93	Manufacturing data (Year)	All	Date	Date
94	Manufacturing data (Week)	All	Date	Date
95~98	Assembly serial #	All	Serial Number	00h
99~125	Manufacturer specific data	All	SMART Modular Technologies	
126~255	Unused storage locations	-DB -DG/IL/IR/KF	- -	FFh 00h

Note:

1. X represents the maximum CAS Latency.
   For DDR2-400-333, X = CL 4.0
   For DDR2-533-444, X = CL 4.0
   For DDR2-667-555, X = CL 5.0
   For DDR2-800-555, X = CL 5.0
   For DDR2-800-666, X = CL 6.0
2. Manufacturing Location:
   00h - Undefined,
   01h - Fremont, USA,
   02h - Aguada, Puerto Rico,
   03h - East Kilbride, Scotland,
   04h - Penang, Malaysia,
   05h - Bangalore, India,
   06h - Sao Paulo, Brazil,
   07h - Aguadilla, Puerto Rico,
   08h - Mayaguez, Puerto Rico,
   09h - Santo Domingo, Dominican Republic,
   0Ah - Dongguan, China,

Mode Register Table Definition

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, t_{WR} and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0 and BA1, while controlling the state of address pins A0~A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0~A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4~A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time t_{WR} is defined by A9~A11.

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
M18	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	Mode Register
0[1]	MR		0[1]	0[1]	0[1]	PD	WR			DLL	TM	CAS Latency			BT	Burst Length			

M8	DLL Reset
0	No
1	Yes

M7	Mode
0	Normal
1	Test

M3	Burst Type
0	Sequential
1	Interleave

Burst Length

M2	M1	M0	BL
0	1	0	4
0	1	1	8

M12	Active power down exit time
0	Fast exit (t_{XARD})
1	Slow exit (t_{XARDS})

Write recovery for autoprecharge

M11	M10	M9	WR (cycles)[2]
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

DDR2-400, DDR2-533, DDR2-667, DDR2-800

CAS Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2.0 (optional)
0	1	1	3.0 (optional)
1	0	0	4.0 (optional)
1	0	1	5.0 (optional)
1	1	0	6.0 (optional)
1	1	1	Reserved

M17	M16	MRS mode
0	0	MRS
0	1	EMRS (1)
1	0	EMRS (2): Reserved
1	1	EMRS (3): Reserved

Notes:
1. BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.
2. WR min is determined by t_{CK} max and WR max is determined by t_{CK} min. WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer. The mode register must be programmed to this value.

Extended Mode Register Table Definition

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ODT (R_{TT}), Posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and OUTPUT enable/disable. The extended mode register is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Notes:
1. BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.
2. When the adjust mode of the OCD Calibration Program is issued, AL from previously set value must be applied.
3. After setting the OCD Calibration Program to default, OCD mode needs to be exited by setting A9-A7 to 000.
4. Outputs disabled - DQs, DQSs, DQS#s, RDQSs, RDQS#s. This feature is used in conjunction with DIMM I_{DD} measurements when I_{DDQ} is not desired to be included.
5. If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.
6. Supported for DDR2-667 and DDR2-800 speeds only.

Extended Mode Register Table

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	Extended Mode Register
0[1]	EMR		0[1]	0[1]	0[1]	Q_{off}	RDQS	DQS#	OCD Program			R_{TT}	AL			R_{TT}	D.I.C	DLL	

E17	E16	MRS mode
0	0	MRS
0	1	EMRS (1)
1	0	EMRS (2)
1	1	EMRS (3): Reserved

E6	E2	R_{TT} (Nominal)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	50 ohm[6] (See page 15)

E0	DLL Enable
0	Enable
1	Disable

E9	E8	E7	OCD Calibration Program
0	0	0	OCD calibration mode exit; maintain setting
0	0	1	Drive (1)
0	1	0	Drive (0)
0	1	1	Adjust mode[2] (See page 15)
1	1	1	OCD calibration default[3] (See page 15)

E5	E4	E3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

E12	Q_{off} (Optional)[4] (See page 15)
0	Output buffer enabled
1	Output buffer disabled

E1	Output Driver Impedence Control	Driver Size
0	Normal	100%
1	Weak	60%

E10	DQS#
0	Enable
1	Disable

E11	RDQS
0	Disable
1	Enable[5] (See page 15)

E11 (RDQS Enable)	E10 (DQS# Enable)	Strobe Function Matrix			
		RDQS/DM	RDQS#	DQS	DQS#
0 (Disable)	0 (Enable)	DM	Hi-z	DQS	DQS#
0 (Disable)	1 (Disable)	DM	Hi-z	DQS	Hi-z
1 (Enable)	0 (Enable)	RDQS	RDQS#	DQS	DQS#
1 (Enable)	1 (Disable)	RDQS	Hi-z	DQS	Hi-z

Commands

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

Truth Table - Commands

Function	CKE		CS#	RAS#	CAS#	WE#	BA0~BAn[9]	An[8]~A11	A10	A9~A0	Notes
	Previous cycle	Current cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1, 2
Refresh	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1, 7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1, 2
Precharge All Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1, 2
Write	H	H	L	H	L	L	BA	Column	L	Column	1, 2, 3
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	1, 2, 3
Read	H	H	L	H	L	H	BA	Column	L	Column	1, 2, 3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1, 2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					

Notes:

1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
3. Burst reads or writes at BL = 4 cannot be terminated or interrupted.
4. The Power Down Mode does not perform any refresh operations. The duration of power down is therefore limited by the refresh requirements.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6. “X” means “H or L (but a defined logic level)”.
7. Self Refresh Exit is asynchronous.
8. An = A12 for 256Mb, A13 for 512Mb & 1 Gb, A14 for 2Gb.
9. BAn = BA1 for up to 512Mb , BA2 for 1 Gb & 2Gb.

DC Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Notes
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0 ~ 2.3	V	
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.3	V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.3	V	
Voltage on V_{DDSPD} relative to V_{SS}	V_{DDSPD}	1.7 ~ 3.6	V	
Operating Temperature (Ambient)	T_{OPR}	0 to +65	°C	
Operating Temperature (Case)	T_{CASE}	0 to +85	°C	1, 2
Storage Temperature	T_{STG}	-55 to +100	°C	

Notes:

1. It is possible to operate the DRAM, Register & PLL up to 95°C.
2. Above 85°C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9μs.

Recommended DC Operating Conditions (T_A = 0 to +65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	
I/O Reference Voltage	V_{REF}	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1, 2
I/O Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	3
SPD Voltage	V_{DDSPD}	1.7	-	3.6	V	
Input High Voltage	$V_{IH(DC)}$	V_{REF} + 0.125	-	V_{DDQ} + 0.3	V	
Input Low Voltage	$V_{IL(DC)}$	-0.3	-	V_{REF} - 0.125	V	
Input Voltage Level, CK/CK#	$V_{IN(DC)}$	-0.3	-	V_{DDQ} + 0.3	V	
Input Differential Voltage, CK/CK#	$V_{ID(DC)}$	0.25	-	V_{DDQ} + 0.6	V	
Ground	V_{SS}	0	0	0	V	

Notes:

1. V_{REF} is expected to track variation in V_{DDQ}.
2. Peak to peak noise (non-common mode) on V_{REF} may not exceed ±1% of the DC value. Peak to peak AC noise on V_{REF} may not exceed ±2% of V_{REF} (DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not used on the module. It is the voltage used on the system board to terminate all the signals. However, this supply should track the variations in DC level of V_{REF}.

Capacitance
(V_{DD} = 1.8V±0.1V, T_{Case} = +25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (CKn, CKn#)	C_{CK}	6.0	12.0	pF
Input Capacitance delta (CKn, CKn#)	C_{DCK}	-	1.5	pF
Input Capacitance (all other input-only pins)	C_I	18.0	36.0	pF
Input Capacitance delta (all other input-only pins)	C_{DI}	-	4.5	pF
Input/Output Capacitance (DQ, DM, DQS, DQS#, CB)	C_{IO1}	5.0	8.0	pF
Input/Output Capacitance (DQ, DM, DQS, DQS#, CB)	C_{IO2}	5.0	7.0	pF
Input/Output Capacitance delta (DQ, DM, DQS, DQS#, CB)	C_{DIO}	-	1.0	pF

Notes:
1. C_{IO1} is for DDR2-400 and DDR2-533.
2. C_{IO2} is for DDR2-667 and DDR2-800.

AC Operating Conditions
(V_{DD} = 1.8V±0.1V, V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Notes
Input High Logic Voltage	$V_{IH(AC)}$	V_{REF} + 0.250	-	V	1, 2
Input Low Logic Voltage	$V_{IL(AC)}$	-	V_{REF} - 0.250	V	1, 2
Input differential voltage, CK and CK# inputs	$V_{ID(AC)}$	0.5	V_{DDQ} + 0.6	V	1, 2, 3
Input crossing point voltage, CK and CK# inputs	$V_{IX(AC)}$	0.5*V_{DDQ} - 0.175	0.5*V_{DDQ} + 0.175	V	1, 2, 3
AC differential crossing point voltage	$V_{OX(AC)}$	0.5*V_{DDQ} - 0.125	0.5*V_{DDQ} + 0.125	V	3

Notes:
1. Input slew rate is 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
4. The value of V_{IX}/V_{OX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

ODT DC Electrical Characteristics

Parameter	Symbol	Min	Nom	Max	Unit	Notes
R_{TT} effective impedence value for 75Ω setting EMR (A6, A2) = 0, 1	$R_{TT1(EFF)}$	60	75	90	Ω	1
R_{TT} effective impedence value for 150Ω setting EMR (A6, A2) = 1, 0	$R_{TT2(EFF)}$	120	150	180	Ω	1
R_{TT} effective impedence value for 50Ω setting EMR (A6, A2) = 1, 1	$R_{TT3(EFF)}$	40	50	60	Ω	1, 3
Deviation of VM with respect to $V_{DDQ}/2$	ΔVM	-6		+6	%	2

Notes:

1. $R_{TT1(EFF)}$ and $R_{TT2(EFF)}$ are determined by applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to pin under test separately, then measure current $I(V_{IH(AC)})$ and $I(V_{IL(AC)})$ respectively. $R_{TT(EFF)} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$
2. Measured voltage (VM) at tested pin with no load.
$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1\right) \times 100\,\%$$
3. Supported for DDR2-667 and DDR2-800 speeds only.

Output DC Current Drive

Parameter	Symbol	Min	Max	Unit	Notes
Output Minimum Source DC Current	I_{OH}	-13.4	-	mA	1, 3, 4
Output Minimum Sink DC Current	I_{OL}	13.4	-	mA	2, 3, 4

Notes:

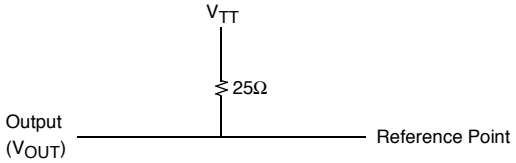
1. For I_{OH} (DC); V_{DDQ} = 1.7V, V_{OUT} = 1420mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV.
2. For I_{OL} (DC); V_{DDQ} = 1.7V, V_{OUT} = 280mV. V_{OUT}/I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.
3. The DC value of V_{REF} applied to the receiving device is set to V_{TT}.
4. The values of I_{OH} (DC) and I_{OL} (DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point along a 21Ω load line to define a convenient driver current for measurement.

OCD Default Output Characteristics
(V_{DD} = 1.8V±0.1V, V_{SS} = 0V, T_A = 0 to +65°C)

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Output Impedance		12.6	18	23.4	Ω	1, 2
Pull-up and Pull-down mismatch		0		4	Ω	1, 2, 3
Output Slew Rate	S_{OUT}	1.5		5	V/ns	1, 4, 5, 7
Output Step Size for Calibration		0		1.5	Ω	6

Notes:
1. Absolute specifications: 0°C ≤ T_{case} ≤ +85°C; V_{DDQ} = +1.8V±0.1V, V_{DD} = +1.8V±0.1V.
2. Impedance measurement condition for output source DC current: V_{DDQ} = 1.7V; V_{OUT} = 1420mV; (V_{OUT} - V_{DDQ})/I_{OH} must be less than 23.4Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV. Impedance measurement condition for output sink DC current: V_{DDQ} = 1.7V; V_{OUT} = 280mV; V_{OUT}/I_{OL} must be less than 23.4Ω for values of V_{OUT} between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between V_{TT} - 250mV and V_{TT} + 250mV for single ended signals. For differential signals output slew rate is measured between DQS - DQS# = -500mV and DQS# - DQS = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.
5. The absolute value of the slew rate as measured from V_{IL} (DC) max to V_{IH} (DC) min is equal to or greater than the slew rate as measured from V_{IL} (AC) max to V_{IH} (AC) min. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18Ω at nominal conditions across all process and represent only the DRAM uncertainty.
7. Timing skew due to DRAM output slew rate mis-match between DQS/DQS# and associated DQs is included in t_{DQSQ} and t_{QHS} specification.

Output Slew Rate Load Diagram



IDD Specification Parameters and Test Conditions (V_{DD} = 1.8V±0.1V, V_{SS} = 0V, T_A = 0 to +65°C)

Symbol	Parameter		5.0ns CL 3.0	3.75ns CL 4.0	3.0ns CL 5.0	2.5ns CL 5.0	2.5ns CL 6.0	Unit
IDD0	**Operating one bank active–precharge current;** $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE and CS# are HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		990	1035	1260	1350	1350	mA
IDD1	**Operating one bank active–read–precharge current;** I_{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE and CS# are HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		1170	1260	1395	1530	1530	mA
IDD2P	**Precharge power–down current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		126	126	126	126	126	mA
IDD2Q	**Precharge quiet standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		630	720	720	900	900	mA
IDD2N	**Precharge standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		630	720	720	900	900	mA
IDD3P	**Active power–down current;** All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	630	675	765	900	900	mA
		Slow PDN Exit MRS(12) = 1	450	495	585	630	630	mA
IDD3N	**Active standby current;** All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		720	810	990	1080	1080	mA
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1305	1530	1710	1980	1980	mA
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		1305	1530	1710	1980	1980	mA
IDD5B	**Burst refresh current;** $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		2205	2295	2430	2655	2655	mA
IDD6	**Self refresh current;** CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		126	126	126	126	126	mA
IDD7	**Operating bank interleave read current;** All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$, t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R		2700	2835	3015	3555	3555	mA

IDD Specification Parameters and Test Conditions (Contd.)

Notes:

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Parametric Test Condition.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#. IDD values must be met with all combinations of ERMS bits 10 and 11.
5. Definitions for IDD

LOW	=	$V_{in} \leq V_{IL(AC)}$(max)
HIGH	=	$V_{in} \geq V_{IH(AC)}$(min)
STABLE	=	inputs stable at a HIGH or LOW level
FLOATING	=	inputs at $V_{REF} = V_{DDQ}/2$
SWITCHING	=	inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks of strobes.

IDD Testing Parameters

	DDR2-400	DDR2-533	DDR2-667	DDR2-800	DDR2-800	
Parameter	**3-3-3**	**4-4-4**	**5-5-5**	**5-5-5**	**6-6-6**	**Units**
CL(IDD)	3	4	5	5	6	t_{CK}
$t_{RCD(IDD)}$	15	15	15	12.5	15	ns
$t_{RC(IDD)}$	55	60	60	57.5	60	ns
$t_{RRD(IDD)}$	7.5	7.5	7.5	7.5	7.5	ns
$t_{CK(IDD)}$	5	3.75	3	2.5	2.5	ns
$t_{RASmin(IDD)}$	40	45	45	45	45	ns
$t_{RASmax(IDD)}$	70000	70000	70000	70000	70000	ns
$t_{RP(IDD)}$	15	15	15	12.5	15	ns
$t_{RFC(IDD)}$	127.5	127.5	127.5	127.5	127.5	ns

Device AC Operating Conditions

Parameter		Symbol	5.0ns @ CL 3.0 DDR2-400-333		3.75ns @ CL 4.0 DDR2-533-444		3.0ns @ CL 5.0 DDR2-667-555		2.5ns @ CL 5.0 DDR2-800-555		2.5ns @ CL 5.0 DDR2-800-666		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock cycle time	CL=6.0	t_{CK}	-	-	-	-	-	-	-	-	2500	8000	ps	12, 20
	CL=5.0		-	-	-	-	3000	8000	2500	8000	3000	8000	ps	12, 20
	CL=4.0		5000	8000	3750	8000	3750	8000	3750	8000	-	-	ps	12, 20
	CL=3.0		5000	8000	5000	8000	-	-	-	-	-	-	ps	12, 20
Clock high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	14
Clock low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	14
Clock half period		t_{HP}	Min (t_{CL}, t_{CH})	-	Min (t_{CL}, t_{CH})	-	Min (t_{CL}, t_{CH})	-	Min (t_{CL}, t_{CH})	-	Min (t_{CL}, t_{CH})	-	ps	15
DQ output access time from CK/CK#	CL=6.0	t_{AC}	-	-	-	-	-	-	-	-	-400	+400	ps	
	CL=5.0		-	-	-	-	-450	+450	-400	+400	-450	+450	ps	
	CL=4.0		-600	+600	-500	+500	-450	+450	-500	+500	-	-	ps	
	CL=3.0		-600	+600	-500	+500	-	-	-	-	-	-	ps	
Data-out high-impedence window from CK/CK#		t_{HZ}	-	t_{AC} (max)	-	t_{AC} (max)	-	t_{AC} (max)	-	t_{AC} (max)	-	t_{AC} (max)	ps	4, 5
Data-out low-impedence window from CK/CK#		t_{LZ}	t_{AC} (min)	t_{AC} (max)	t_{AC} (min)	t_{AC} (max)	t_{AC} (min)	t_{AC} (max)	t_{AC} (min)	t_{AC} (max)	t_{AC} (min)	t_{AC} (max)	ps	4, 6
DQ & DM input setup time relative to DQS		t_{DS}	150	-	100	-	100	-	50	-	50	-	ps	3, 11, 17
DQ & DM input hold time relative to DQS		t_{DH}	275	-	225	-	175	-	125	-	125	-	ps	3, 11, 17
DQ & DM input pulse width (for each input)		t_{DIPW}	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	t_{CK}	
Data hold skew factor		t_{QHS}	-	450	-	400	-	340	-	300	-	300	ps	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	ps	11,13
DQS input high pulse width		t_{DQSH}	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	t_{CK}	
DQS input low pulse width		t_{DQSL}	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	t_{CK}	
DQS output access time from CK/CK#		t_{DQSCK}	-500	+500	-450	+450	-400	+400	-350	+350	-350	+350	ps	
DQS falling edge to CK rising - setup time		t_{DSS}	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	t_{CK}	
DQS falling edge from CK rising - hold time		t_{DSH}	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	t_{CK}	
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	-	350	-	300	-	240	-	200	-	200	ps	11,13

Device AC Operating Conditions (Contd.)

Parameter	Symbol	5.0ns @ CL 3.0 DDR2-400-333		3.75ns @ CL 4.0 DDR2-533-444		3.0ns @ CL 5.0 DDR2-667-555		2.5ns @ CL 5.0 DDR2-800-555		2.5ns @ CL 5.0 DDR2-800-666		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	18
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS write preamble setup time	t_{WPRES}	0	-	0	-	0	-	0	-	0	-	ps	8, 9
DQS write preamble	t_{WPRE}	0.25	-	0.25	-	0.35	-	0.35	-	0.35	-	t_{CK}	
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	7
Write command to first DQS latching transition	t_{DQSS}	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t_{CK}	
Address & control input pulse width for each input	t_{IPW}	0.6	-	0.6	-	0.6	-	0.6	-	0.6	-	t_{CK}	
Address and control input setup time	t_{IS}	350	-	250	-	200	-	175	-	175	-	ps	2, 17
Address and control input hold time	t_{IH}	475	-	375	-	275	-	250	-	250	-	ps	2, 17
CAS# to CAS# command delay	t_{CCD}	2	-	2	-	2	-	2	-	2	-	t_{CK}	
OCD Drive mode delay	t_{OIT}	0	12	0	12	0	12	0	12	0	12	ns	
CKE low to CK, CK# uncertainity	t_{DELAY}	5.825	5.825	4.375	4.375	3.475	3.475	2.925	2.925	2.925	2.925	ns	24
ACTIVE to ACTIVE (same bank) command	t_{RC}	55	-	60	-	60	-	57.5	-	60	-	t_{CK}	
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	t_{CK}	
ACTIVE to READ or WRITE delay	t_{RCD}	15	-	15	-	15	-	12.5	-	15	-	ps	11,13
ACTIVE to PRECHARGE command	t_{RAS}	40	70000	45	70000	45	70000	45	70000	45	70000	t_{CK}	18
Internal READ to precharge command delay	t_{RTP}	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	t_{CK}	
Write recovery time	t_{WR}	15	-	15	-	15	-	15	-	15	-	ps	8, 9
Auto precharge write recovery + Precharge time	t_{DAL}	t_{WR} + t_{RP}	-	t_{WR} + t_{RP}	-	t_{WR} + t_{RP}	-	t_{WR} + t_{RP}	-	t_{WR} + t_{RP}	-	t_{CK}	
Internal WRITE to READ command delay	t_{WTR}	10	-	7.5	-	7.5	-	7.5	-	7.5	-	t_{CK}	7
PRECHARGE command period	t_{RP}	15	-	15	-	15	-	12.5	-	15	-	t_{CK}	
LOAD MODE command cycle time	t_{MRD}	2	-	2	-	2	-	2	-	2	-	t_{CK}	

Device AC Operating Conditions (Contd.)

Parameter	Symbol	5.0ns @ CL 3.0 DDR2-400-333		3.75ns @ CL 4.0 DDR2-533-444		3.0ns @ CL 5.0 DDR2-667-555		2.5ns @ CL 5.0 DDR2-800-555		2.5ns @ CL 5.0 DDR2-800-666		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
REFRESH to REFRESH command interval	t_{RFC}	127.5	-	127.5	-	127.5	-	127.5	-	127.5	-	ps	2, 17
Average periodic refresh Interval	t_{REFI}	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	ps	2, 17
Exit self refresh to non-READ command	t_{XSNR}	t_{RFC} (min) + 10	-	t_{RFC} (min) + 10	-	t_{RFC} (min) + 10	-	t_{RFC} (min) + 10	-	t_{RFC} (min) + 10	-	t_{CK}	
Exit self refresh to READ command	t_{XSRD}	200	-	200	-	200	-	200	-	200	-	ns	
ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	2	2	2	2	t_{CK}	
ODT turn-on	t_{AON}	t_{AC} (min)	t_{AC} (max) + 1000	t_{AC} (min)	t_{AC} (max) + 1000	t_{AC} (min)	t_{AC} (max) + 700	t_{AC} (min)	t_{AC} (max) + 700	t_{AC} (min)	t_{AC} (max) + 700	t_{CK}	
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ps	11,13
ODT turn-off	t_{AOF}	t_{AC} (min)	t_{AC} (max) + 600	t_{AC} (min)	t_{AC} (max) + 600	t_{AC} (min)	t_{AC} (max) + 600	t_{AC} (min)	t_{AC} (max) + 600	t_{AC} (min)	t_{AC} (max) + 600	t_{CK}	18
ODT turn-on (power-down mode)	t_{AONPD}	t_{AC} (min) + 2000	$2*t_{CK}$ + t_{AC} (max) + 1000	t_{AC} (min) + 2000	$2*t_{CK}$ + t_{AC} (max) + 1000	t_{AC} (min) + 2000	$2*t_{CK}$ + t_{AC} (max) + 1000	t_{AC} (min) + 2000	$2*t_{CK}$ + t_{AC} (max) + 1000	t_{AC} (min) + 2000	$2*t_{CK}$ + t_{AC} (max) + 1000	t_{CK}	
ODT turn-off (power-down mode)	t_{AOFPD}	t_{AC} (min) + 2000	$2.5*t_{CK}$ + t_{AC} (max) + 1000	t_{AC} (min) + 2000	$2.5*t_{CK}$ + t_{AC} (max) + 1000	t_{AC} (min) + 2000	$2.5*t_{CK}$ + t_{AC} (max) + 1000	t_{AC} (min) + 2000	$2.5*t_{CK}$ + t_{AC} (max) + 1000	t_{AC} (min) + 2000	$2.5*t_{CK}$ + t_{AC} (max) + 1000	ps	8, 9
ODT to power-down entry latency	t_{ANPD}	3	-	3	-	3	-	3	-	3	-	t_{CK}	
ODT power-down exit latency	t_{AXPD}	8	-	8	-	8	-	8	-	8	-	t_{CK}	7
Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2	-	2	-	2	-	2	-	2	-	t_{CK}	
Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	6 - AL	-	6 - AL	-	7 - AL	-	8 - AL	-	8 - AL	-	t_{CK}	
Exit precharge power down to any non-read command	t_{XP}	2	-	2	-	2	-	2	-	2	-	ps	2, 17
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	-	3	-	3	-	3	-	3	-	ps	2, 17

Notes:

1. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level.
2. Command/Address minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of CK/CK#. t_{IS} timing is referenced to $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a fallng signal. t_{IH} timing is referenced to $V_{IH(DC)}$ for a rising signal and $V_{IL(DC)}$ for a fallng signal. Derating values for Command/Address input signal slew rates < 1.0V/ns are TBD.
3. Data minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of DQS/DQS# if differential strobe feature is enabled. t_{DS} timing is referenced to $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a fallng signal. t_{DH} timing is referenced to $V_{IH(DC)}$ for a rising signal and $V_{IL(DC)}$ for a fallng signal. Derating values for Data input signal slew rates < 1.0V/ns are TBD.
4. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (t_{HZ}) or begins driving (t_{LZ}).
5. This maximum value is derived from the reference test load. $t_{HZ(MAX)}$ will prevail over a $t_{DQSCK(MAX)} + t_{RPST(MAX)}$ condition.
6. $t_{LZ(MIN)}$ will prevail over a $t_{DQSCK(MIN)} + t_{RPRE(MAX)}$ condition.
7. The intent of the Don't Care state after completion of the postamble is the DQS driven signal should be high, low or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high [above $V_{IHDC(MIN)}$] then it must not transition low (below V_{IHDC}) prior to $t_{DQSH(min)}$.
8. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
9. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during his time depending on t_{DQSS}.
10. The refresh period is 64ms. This equates to an average refresh rate of 7.8125μs. However, an REFRESH comand must be asserted at least once every 70.3μs or $t_{RFC(MAX)}$; issuing more than eight REFRESH commands back to back at $t_{RFC(min)}$ is not allowed.
11. Each byte lane has a corresponding DQS.
12. CK and CK# input slew rate must be ≥ 1 V/ns (≥ 2 V/ns if measured differentially).
13. The data valid window is derived by achieving other specifications: t_{HP}, (t_{CK}/2), t_{DQSQ}, and t_{QH} ($t_{QH} = t_{HP} - t_{QHS}$). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
14. MIN(t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
15. $t_{HP(MIN)}$ is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CK and CK# inputs.
16. READs and WRITEs with no auto precharge are allowed to be issued before $t_{RAS(MIN)}$ is satisfied since t_{RAS} lockout feature is supported in DDR2 SDRAM.
17. V_{IL}/V_{IH} DDR2 overshoot/undershoot. Refer to 256MB, 512MB, or 1GB DDR2 SDRAM component data sheet for more detailed information.
18. $t_{DAL} = (n_{WR}) + (t_{RP}/t_{CK})$: For each of the terms above, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period; n_{WR} refers to the t_{WR} parameter stored in the MR[11,10,9].
19. This is a minimum requirement. Minimum READ to internal PRECHARGE timing is AL + BL/2 providing the t_{RTP} and $t_{RAS(MIN)}$ have been satisfied. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until $t_{RAS(MIN)}$ has been satisfied.
20. Operating frequency is only allowed to change during self refresh mode or precharge power-down mode. Anytime the operating frequency is changed, not including jitter, the DLL is required to be reset followed by 200 clock cycles.
21. ODT turn-on time $t_{AON(MIN)}$ is when the device leaves high impedence and ODT resistance begins to turn-on. ODT turn-on time $t_{AON(MAX)}$ is when the resistance is fully on. Both are measured from t_{AOND}.
22. ODT turn-off time $t_{AOF(MIN)}$ is when the device starts to turn-off ODT resistance. ODT turn-off time $t_{AOF(MAX)}$ is when the bus is in high impedence. Both are measured from t_{AOFD}.
23. This parameter has a two clock minimum requirement at any t_{CK}.
24. t_{DELAY} is calculated from $t_{IS} + t_{CK} + t_{IH}$ so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system reset condition.

Part Number Decode

S	G	5	72	56	8	F	G	8	D	6	U	U
1	2	3	4	5	6	7	8	9	10	11	12	13

1 **SMART Modular Technologies**

2 **Module Process Technology**
G: Green Module (RoHS Compliant)

3 **Product Category**
5: SDRAM DIMM

4 **Module Data Bus Width**
72: x72

5 **Module Address Depth**
56: 256M

6 **Device Data Width**
8: x8

7 **Special Device Feature**
F: Standard FBGA (4 Bank SDRAM)

8 **Technology**
G: DDR2 SDRAM

9 **Refresh/Power**
8: 8K Refresh/Standard Power

10 **Module Configuration**
D: 240-pin DIMM Unbuffered, ECC

11 **Device Physicals**
6: 1Gbit Device Based

12 **CAS Latency**
D: 3.0, 4.0
I: 4.0, 5.0
K: 5.0, 6.0

13 **Cycle Time (Clock Speed)**
B: 5.0ns (200MHz, PC2-3200, DDR2-400-333)
G: 3.75ns (267MHz, PC2-4200, DDR2-533-444)
L: 3.0ns (333MHz, PC2-5300, DDR2-667-555)
R: 2.5ns (400MHz, PC2-6400, DDR2-800-555)
F: 2.5ns (400MHz, PC2-6400, DDR2-800-666)

Note : “U” in the part number should be replaced by user specified option.

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