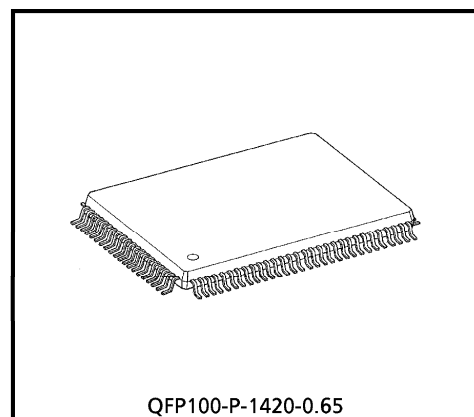


TC9283F

CD SINGLE-CHIP PROCESSOR

The TC9283F is a single chip processor for sync separation protection / synchronization, EFM demodulation, error correction / interpolation, microcomputer interface, CLV servo and focus tracking servo in CD player system.

In combination with the TA8190F / TA8191F / TA2031F / TA2035F / TA2065F, which are focus tracking servo LSI, a CD player system can be composed very simply.



Weight : 1.6g (Typ.)

FEATURES

- Sync pattern detection, sync signal protection and synchronization can be made correctly.
- Built-in EFM demodulation and subcode demodulation circuit.
- Has the correction capacity of double and triple correction for C1 and C2 each correcting units, respectively, using CIRC correction theoretical format.
- Jitter absorbing capacity of ± 6 frames.
- Built-in 16k RAM.
- Built-in digital out circuit.
- Built-in variable pitch control circuit.
- Built-in digital level meter and peak meter circuit.
- The output circuit of each channel (Left/Right) has the independent digital attenuation circuit.
- Audio-out circuit is apply to bilingual output.
- Read timing free subcode Q data.
- Built-in the output circuit for CD-ROM (CD-I)
- Built-in data slicer and analog PLL (free-adjustment VCO adopted) circuit.
- Focus/Tracking loop gain auto adjusting function incorporated.
- Built-in AFC and APC circuit for disc motor CLV servo.
- Built-in focus tracking servo control circuit.
- Tracking search control apply to all modes.
- Double and Quadruple speed play is possible.
- Built-in microcomputer interface circuit.
- In CMOS structure, high speed and low power dissipation.
- 100 pin flat package.

980910EBA2

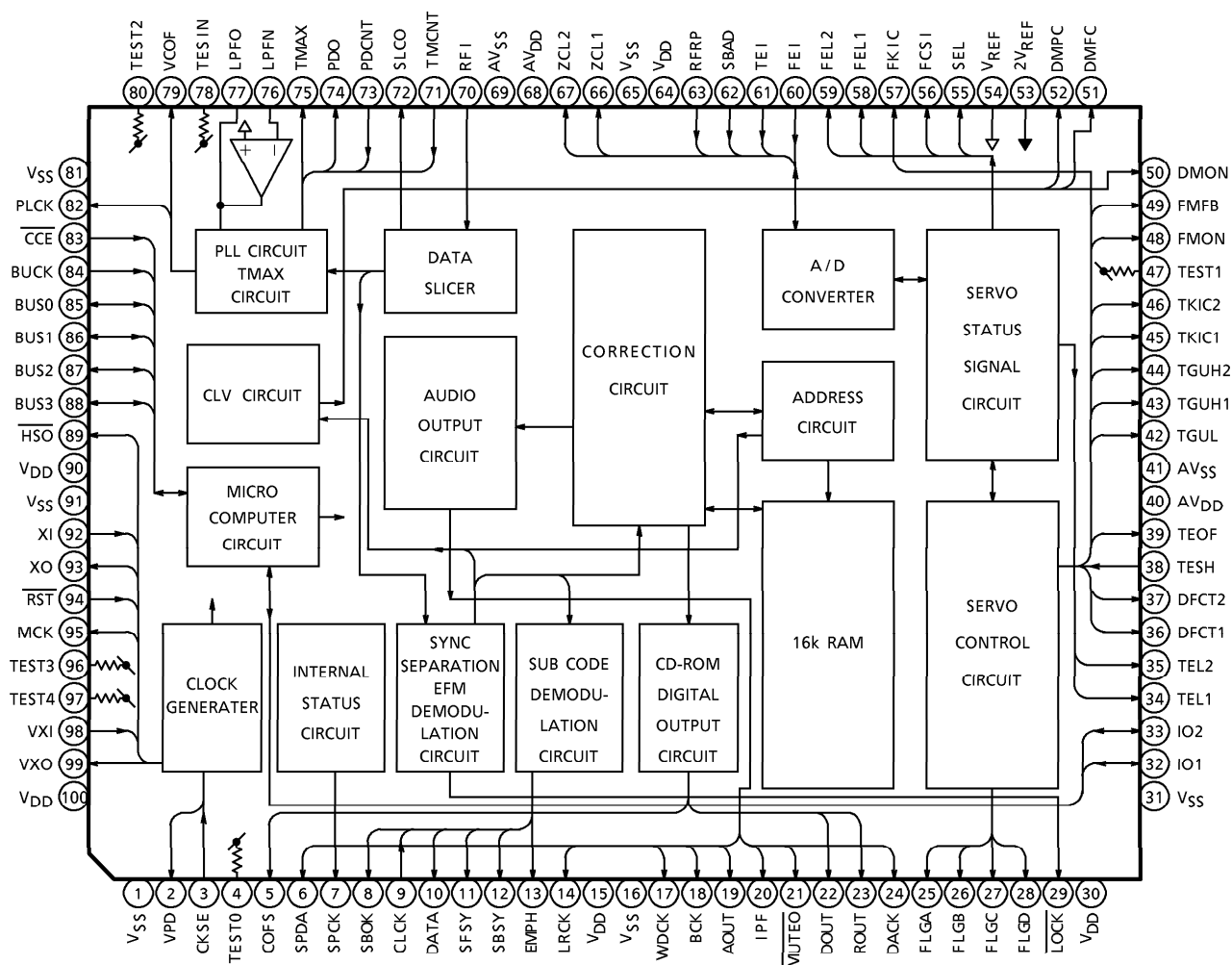
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BLOCK DIAGRAM (TOP VIEW)



FUNCTION OF EACH PIN

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARK
1	V _{SS}	—	Digital ground terminal.	—
2	VPD	O	Phase compare (XI and VXI signal) output terminal for variable-pitch.	3-state output (V _{DD} , HiZ, V _{SS})
3	CKSE	I	Internal clock selection terminal.	—
4	TEST0	I	Test terminal. Normally, keep at "H" level or open.	With pull-up resistor
5	COFS	O	Correction system frame periodic signal output terminal. 7.35kHz	—
6	SPDA	O	Processor status signal output terminal.	—
7	SPCK	O	Processor status signal read clock output terminal. 176.4kHz	—
8	SBOK	O	Subcode Q data CRC checking result output terminal. The checking result is OK at "H" level.	—
9	CLCK	I	Subcode P-W data readout clock input terminal.	—
10	DATA	O	Subcode P-W data output terminal.	—
11	SFSY	O	Play-back frame periodic signal output terminal.	—
12	SBSY	O	Subcode block sync signal output terminal. The subcode sync is detect, output "H" level at S1 position.	—
13	EMPH	O	Subcode Q data emphasis status signal output terminal. Emphasis ON at "H" level, OFF at "L" level. Output polarity can change by command.	—
14	LRCK	O	Channel clock output terminal. Normally, 44.1kHz. Output L-channel at "L" level, R-channel at "H" level. Output polarity can change by command.	—
15	V _{DD}	—	Digital power supply voltage terminal. (+5V)	—
16	V _{SS}	—	Digital ground terminal.	—
17	WDCK	O	Word clock output terminal. Normally, 88.2kHz.	—
18	BCK	O	Bit clock output terminal. Normally, 1.4112MHz.	—
19	AOUT	O	Audio data output terminal.	—
20	IPF	O	Interpolation status signal output terminal. Output "H" level at C2 correcting unit unable error correction.	—
21	MUTE $\overline{O}$	O	Audio mute signal output terminal. Mute ON at "L" level.	—
22	DOUT	O	Digital data output terminal.	—
23	ROUT	O	Digital data for CD-ROM output terminal.	—
24	DACK	O	ROUT signal read clock output terminal. It is possible to select 2.8MHz or 5.6MHz by command.	—
25	FLGA	O	Internal status monitor terminal. It is possible to select TEZC, $\overline{FOON}$, $\overline{FOK}$, RFZC signal by command.	—
26	FLGB	O	Internal status monitor terminal. It is possible to select $\overline{TRON}$, $\overline{FOON}$, $\overline{FDON}$, RFZC signal by command.	—

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARK
27	FLGC	O	Internal status monitor terminal. It is possible to select $\overline{\text{TRON}}$, $\overline{\text{TSSR}}$, $\overline{\text{FOK}}$, $\overline{\text{SRCH}}$ signal by command.	—
28	FLGD	O	Internal status monitor terminal. It is possible to select $\overline{\text{TRON}}$, $\overline{\text{DMON}}$, $\overline{\text{HYS}}$, $\overline{\text{SHC}}$ signal by command.	—
29	$\overline{\text{LOCK}}$	O	Lock status output terminal. If sync pattern under EFM signal cannot be detector for 17ms continuously by runway detection information, this terminal is put at "H" level.	—
30	V _{DD}	—	Digital power supply voltage terminal. (+ 5V)	—
31	V _{SS}	—	Digital ground terminal.	—
32	IO1	I/O	Command controllable I/O port terminals.	—
33	IO2			
34	TEL1	O	Tracking gain adjusting analog switch output terminals. V _{REF} or HiZ. It is possible to select Normally mode or Command control mode.	—
35	TEL2			—
36	DFCT1	O	Defect (drop-out of data) detection signal output terminal. V _{REF} when defect is detected. Normally, HiZ.	—
37	DFCT2	O	Black-dot (drop-out of data) detection signal output terminal. V _{REF} when defect is detected. Normally, HiZ.	—
38	TESH	I	Tracking error signal sample holding analog switch input terminal.	Analog input
39	TEOF	O	Tracking servo operation ON/OFF analog switch output terminal. V _{REF} when the tracking servo is OFF.	Analog output
40	AV _{DD}	—	Analog power supply voltage terminal. (+ 5V)	—
41	AV _{SS}	—	Analog ground terminal.	—
42	TGUL	O	Tracking servo gain up analog switch output terminal. V _{REF} or HiZ. It is possible to select Normally mode or Command control mode.	—
43	TGUH1	O	Tracking servo gain up analog switch output terminals. HiZ when gain is up. Normally, V _{REF} . TGUH1 is used at normal play and TGUH2 is used at high (Double and Quadruple) speed play.	—
44	TGUH2			
45	TKIC1	O	Tracking actuator kick signal output terminal. It used NKIC, CKIC and tracking gain adjusting mode. Kicks in the outer direction at "2V _{REF} " level and in the inner direction at "AV _{SS} " level. Normally, HiZ.	3-state output (2V _{REF} , HiZ, AV _{SS})
46	TKIC2	O	Tracking actuator kick signal output terminal. It used FVKIC. It is possible to polarity change. Output signal form is PWM. (3-state 2V _{REF} , V _{REF} , AV _{SS} at 132kHz). Normally, HiZ.	3-state output (2V _{REF} , HiZ, AV _{SS})
47	TEST1	I	Test terminal. Normally, keep at "H" level or open.	With pull-up resistor

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION			REMARK																				
48	FMON	O	Feed servo ON/OFF analog switch output terminal. The feed servo is ON at “HiZ” level, and OFF at “VREF” level.			—																				
49	FMFB	O	Feed motor FWD/BWD feeding control signal output terminal. Output signal form is PWM. (3-state 2VREF, VREF, AVSS at 132kHz) Feed in the outer direction at “2VREF” level and in the inner direction at “AVSS” level. Normally, HiZ.			4-state output (2VREF, VREF, AVSS, HiZ)																				
50	DMON	O	Disc motor driving circuit gain change-over analog switch output terminal. The CLV servo is OFF at “HiZ” level. It is possible to select “HiZ” or “VREF” level, when CLV servo is ON.			—																				
51	DMFC	O	<table border="1"><thead><tr><th colspan="2">OPERATION</th><th>COMMAND</th><th>DMFC OUTPUT</th></tr></thead><tbody><tr><td colspan="2">Motor acceleration</td><td>DMFK</td><td>“2VREF”</td></tr><tr><td colspan="2">CLV servo ON</td><td>DMSV</td><td>AFC Signal (PWM)</td></tr><tr><td colspan="2">Motor deceleration</td><td>DMBK</td><td>“AVSS”</td></tr><tr><td colspan="2">CLV servo OFF</td><td>DMOFF</td><td>“VREF”</td></tr></tbody></table>			OPERATION		COMMAND	DMFC OUTPUT	Motor acceleration		DMFK	“2VREF”	CLV servo ON		DMSV	AFC Signal (PWM)	Motor deceleration		DMBK	“AVSS”	CLV servo OFF		DMOFF	“VREF”	3-state output (2VREF, VREF, AVSS)
OPERATION		COMMAND	DMFC OUTPUT																							
Motor acceleration		DMFK	“2VREF”																							
CLV servo ON		DMSV	AFC Signal (PWM)																							
Motor deceleration		DMBK	“AVSS”																							
CLV servo OFF		DMOFF	“VREF”																							
52	DMPC	O	Disc motor CLV servo APC signal output terminal.			3-state output (2VREF, HiZ, AVSS)																				
53	2VREF	—	Double times reference voltage input terminal. (VREF×2)			—																				
54	VREF	—	Reference voltage input terminal.			—																				
55	SEL	O	<table border="1"><thead><tr><th>SEL</th><th>LD</th><th>FOCUS SERVO</th><th>OPERATION</th></tr></thead><tbody><tr><td>“AVSS”</td><td>OFF</td><td>OFF</td><td>LD OFF</td></tr><tr><td>“HiZ”</td><td>ON</td><td>OFF</td><td>Focus search</td></tr><tr><td>“AVDD”</td><td>ON</td><td>ON</td><td>Focus ON</td></tr></tbody></table>			SEL	LD	FOCUS SERVO	OPERATION	“AVSS”	OFF	OFF	LD OFF	“HiZ”	ON	OFF	Focus search	“AVDD”	ON	ON	Focus ON	3-state output (AVDD, HiZ, AVSS)				
SEL	LD	FOCUS SERVO	OPERATION																							
“AVSS”	OFF	OFF	LD OFF																							
“HiZ”	ON	OFF	Focus search																							
“AVDD”	ON	ON	Focus ON																							
56	FCSI	O	Focus actuator driving signal output terminal in the focus serach adjust mode. Lens gets for away from disc at “AVDD”, Lens gets near disc at “AVSS”. Normally, “HiZ”.			3-state output (AVDD, HiZ, AVSS)																				
57	FKIC	O	Focus actuator driving signal output terminal in the focus gain adjust mode. Lens gets for away from disc at “AVDD”, Lens gets near disc at “AVSS”. Normally, “HiZ”.			3-state output (AVDD, HiZ, AVSS)																				
58	FEL1	O	Focus gain adjusting analog switch output terminals. VREF or HiZ. It is possible to select Normally mode or Command control mode.			—																				
59	FEL2																									
60	FEI	I	Focus error signal input terminal.			Analog input																				
61	TEI	I	Tracking error signal input terminal.			Analog input																				
62	SBAD	I	Sub-beam adding signal input terminal.			Analog input																				

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARK								
63	RFRP	I	RF ripple signal input terminal.	Analog input								
64	V _{DD}	—	Digital power supply voltage terminal. (+ 5V)	—								
65	V _{SS}	—	Digital ground terminal.	—								
66	ZCL1	O	Focusing and tracking signal output terminal. (Internal 5 bits DAC output) Usually use for monitoring of internal signal.	Analog output								
67	ZCL2	O	SBAD and RFRP signal output terminal. (Internal 5 bits DAC output) Usually use for monitoring of internal signal. (SBAD : sub-beam additional signal, RFRP : RF ripple signal)	Analog output								
68	AV _{DD}	—	Analog power supply voltage terminal. (+ 5V)	—								
69	AV _{SS}	—	Analog ground terminal.	—								
70	RFI	I	RF signal input terminal.	Analog input								
71	TMCNT	I	TMAX output control terminal. When input level is “L”, TMAX terminal output fixes “HiZ”. Normally, input level is “H”.	—								
72	SLCO	O	Data slice level output terminal. (Internal DAC output)	Analog output								
73	PDCNT	I	PDO output control terminal. When input level is “L”, PDO terminal output fixes “HiZ”, Normally, input level is “H”.	—								
74	PDO	O	Phase comparator error signal output terminal between EFM signal and PLCK.	3-state output (2V _{REF} , HiZ, AV _{SS})								
75	TMAX	O	TMAX signal output terminal. TMAX is frequency information of RF signal. <table><tr><td>TMAX PERIOD</td><td>TMAX OUTPUT</td></tr><tr><td>Longer than specified period</td><td>“AV_{SS}”</td></tr><tr><td>Shorter than specified period</td><td>“2V_{REF}”</td></tr><tr><td>Specified period</td><td>“HiZ”</td></tr></table>	TMAX PERIOD	TMAX OUTPUT	Longer than specified period	“AV _{SS} ”	Shorter than specified period	“2V _{REF} ”	Specified period	“HiZ”	3-state output (2V _{REF} , HiZ, AV _{SS})
TMAX PERIOD	TMAX OUTPUT											
Longer than specified period	“AV _{SS} ”											
Shorter than specified period	“2V _{REF} ”											
Specified period	“HiZ”											
76	LPFN	I	LPF amplifier negative input terminal for PLL.	Analog input								
77	LPFO	O	LPF amplifier output terminal for PLL.	Analog output								
78	TESIN	I	Test terminal. Normally, keep at “H” level or open.	With pull-up resistor								
79	VCOF	O	VCO noise filter terminal.	—								
80	TEST2	I	Test terminal. Normally, keep at “H” level or open.	With pull-up resistor								
81	V _{SS}	—	Digital ground terminal.	—								
82	PLCK	O	PLCK signal output terminal. It is possible to select PLCK, 17MCK (VCO), EFMS (EFM slice data), fixes “H” level by command.	—								
83	$\overline{\text{CCE}}$	I	Command and data sending /receiving chip enable signal input terminal. The bus line becomes active at “L” level.	Schmitt trigger input								
84	BUCK	I	Command and data sending /receiving clock input terminal.	Schmitt trigger input								

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARK
85	BUS0	I/O	Command and data sending /receiving input/output terminals.	Schmitt trigger input. Open drain output, With pull-up resistor
86	BUS1			
87	BUS2			
88	BUS3			
89	$\overline{\text{HSO}}$	O	High speed play monitor output terminal. Double and Quadruple speed play at "L" level. Normally, "H".	—
90	V _{DD}	—	Digital power supply voltage terminal. (+ 5V)	—
91	V _{SS}	—	Digital ground terminal.	—
92	XI	I	Crystal oscillator input terminal.	—
93	XO	O	Crystal oscillator output terminal.	—
94	$\overline{\text{RST}}$	I	Reset input terminal. The internal system is reset at "L" level.	With pull-up resistor
95	MCK	O	Master clock output terminal.	—
96	TEST3	I	Test terminal. Normally, keep at "H" level or open.	With pull-up resistor
97	TEST4	I	Test terminal. Normally, keep at "H" level or open.	With pull-up resistor
98	VXI	I	External VCO clock input terminal for variable-pitch.	Alanlog input
99	VXO	O	Buffer output terminal at VXI signal.	—
100	V _{DD}	—	Digital power supply voltage terminal. (+ 5V)	—

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V _{DD}	− 0.3~6.0	V
Input Voltage	V _{IN}	− 0.3~V _{DD} + 0.3	V
Power Dissipation	P _D	1,250	mW
Operating Temperature	T _{opr}	− 35~85	°C
Storage Temperature	T _{stg}	− 55~150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, $V_{DD} = 5V$, $2V_{REF} = 4.2V$, $V_{REF} = 2.1V$, $T_a = 25^\circ C$)

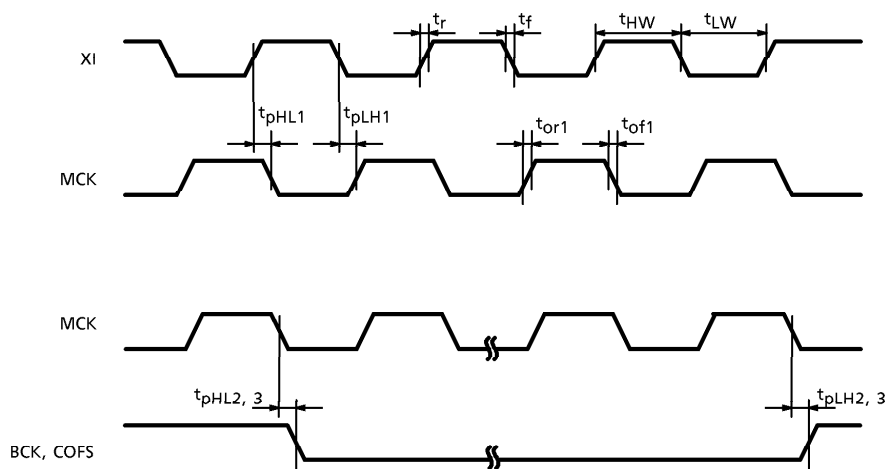
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	—	$T_a = -35 \sim 85^\circ C$		4.75	5.0	5.25	V
Operating Supply Current		I_{DD}	—	$XI = 16.9344MHz$, In normal mode		—	40	70	mA
Input Voltage	"H" Level	$V_{IH}(1)$	—	Whole input terminals except $BUS0 \sim 3$, BUCK and $\overline{CCE}$		3.5	—	$V_{DD} + 0.3$	V
	"L" Level	$V_{IL}(1)$				0	—	1.5	
	"H" Level	$V_{IH}(2)$	—	$BUS0 \sim 3$, BUCK, $\overline{CCE}$ (Schmitt Input)		4.0	—	$V_{DD} + 0.3$	
	"L" Level	$V_{IL}(2)$				0	—	1.0	
Input Current	"H" Level	I_{TH}	—	$V_{IH} = 5V$	CMOS input terminals except analog input terminal.	—	—	1.0	μA
	"L" Level	I_{TL}		$V_{IL} = 0V$		-1.0	—	—	
Try State Leak Current	"H" Level	I_{TLH}	—	$V_{IH} = 5V$		—	—	1.0	
	"L" Level	I_{TLL}		$V_{IL} = 0V$		-1.0	—	—	
Output Current	"H" Level	$I_{OH}(1)$	—	$V_{OH} = 4.6V$	VPD, COFS, SPDA, SPCK, SBOK, CLCK, DATA, SEL, FCSI, FKIC, PDCNT $V_{OUT} = V_{DD}$	—	—	-1.0	mA
	"L" Level	$I_{OL}(1)$		$V_{OL} = 0.4V$		2.5	—	—	
	"H" Level	$I_{OH}(2)$	—	$V_{OH} = 4.6V$	SFSY, SBSY, EMPH $V_{OUT} = V_{DD}$	—	—	-1.0	
	"L" Level	$I_{OL}(2)$		$V_{OL} = 0.4V$		1.5	—	—	
	"H" Level	$I_{OH}(3)$	—	$V_{OH} = 4.6V$	WDCK, IPF, MUTE0, DOUT, DACK, FLGA, FLGB, FLGC, FLGD, $\overline{LOCK}$, IO1, IO2, ROUT, LRCK, BCK, AOUT, PLCK $V_{OUT} = V_{DD}$	—	—	-2.0	
	"L" Level	$I_{OL}(3)$		$V_{OL} = 0.4V$		4.0	—	—	
	"H" Level	$I_{OH}(4)$	—	$V_{OH} = 4.6V$	MCK, VXO, XO $V_{OUT} = V_{DD}$	—	—	-2.0	
	"L" Level	$I_{OL}(4)$		$V_{OL} = 0.4V$		3.0	—	—	
	"H" Level	$I_{OH}(5)$	—	$V_{OH} = 3.8V$	TKIC1, TKIC2, FMFB, DMFC, DMPC $V_{OUT} = 2V_{REF}$	—	—	-0.4	
	"L" Level	$I_{OL}(5)$		$V_{OL} = 0.4V$		2.5	—	—	
	"H" Level	$I_{OH}(6)$	—	$V_{OH} = 3.8V$	PDO, TMAX $V_{OUT} = 2V_{REF}$	—	—	-1.5	
	"L" Level	$I_{OL}(6)$		$V_{OL} = 0.4V$		2.5	—	—	

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Analog Switch OFF Current	"H" Level	I _{OFH}	—	V _{IH} = 5V	—	—	1.0	μ A
	"L" Level	I _{OFL}	—	V _{IL} = 0V	- 1.0	—	—	
Analog Switch ON Resistance	R _{ON} (1)	—	—	FEL1, FEL2, TEL1, TEL2, FMON, TGUL, TGUH1, TGUH2, FMFB, DFCT1, DFCT2, TEOF, DMON, DMFC	—	—	0.6	k Ω
	R _{ON} (2)			TESH	—	—	1.2	
Pull-Up Resistance	R _{UP} (1)	—	—	$\overline{\text{RST}}$	—	65	—	k Ω
	R _{UP} (2)			$\overline{\text{TEST}}$, $\overline{\text{TEST1}} \sim \overline{5}$	—	45	—	
	R _{UP} (3)			BUS0~3	8	—	—	
Oscillation Amplifier Feedback Resistance	R _N (1)	—	—	XI-XO	2.0	3.5	5.0	M Ω
	R _N (2)			VXI-VXO, TESIN	0.25	0.5	1.0	
Operating Frequency Ratio	f _{OP}	—	—	XI	6	—	28	MHz

AC characteristics

(1) Clock system timing

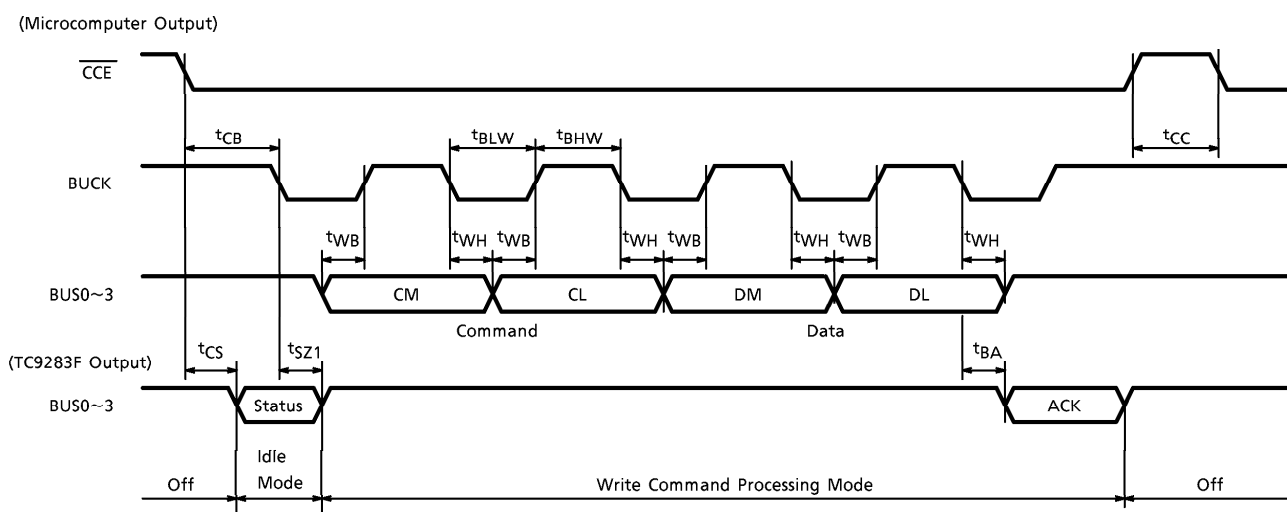
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	"H" Level	t_{HW}	XI input	18	—	—	ns
	"L" Level	t_{LW}		18	—	—	
Input Rising Time		t_r		—	—	10	
Input Falling Time		t_f		—	—	10	
Transfer Time (1)	"H" Level	t_{pHL1}	XI→MCK	—	—	60	ns
	"L" Level	t_{pLH1}		—	—	60	
Transfer Time (2)	"H" Level	t_{pHL2}	MCK→BCK	—	—	60	
	"L" Level	t_{pLH2}		—	—	60	
Transfer Time (3)	"H" Level	t_{pHL3}	MCK→COFS	—	—	100	
	"L" Level	t_{pLH3}		—	—	100	
Output Rising Time (1)		t_{or1}	MCK, BCK	—	—	15	ns
Output Falling Time (1)		t_{of1}		—	—	15	
Output Rising Time (2)		t_{or2}	COFS	—	—	40	ns
Output Falling Time (2)		t_{of2}		—	—	40	



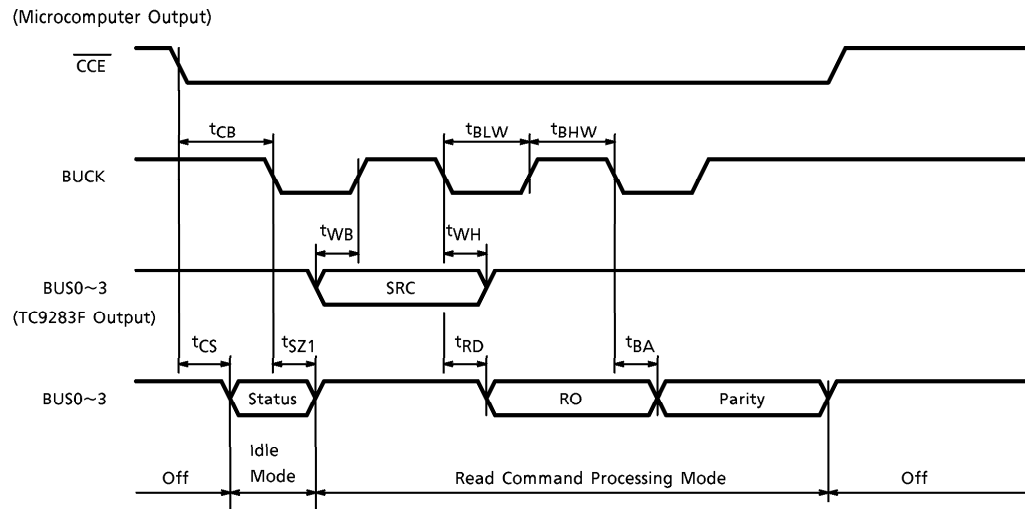
(2) Microcomputer interface timing

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width (1)	"H" Level	t _{BHW}	BUCK	10	—	—	μs
	"L" Level	t _{BLW}		10	—	—	
Clock Pulse Width (2)		t _{CC}	$\overline{CCE}$	6	—	—	
Delay Time (1)		t _{CB}	$\overline{CCE} \rightarrow$ BUCK	—	—	6	μs
Delay Time (2)		t _{WB}	Command Data→BUCK	0	—	—	
Delay Time (3)		t _{CS}	$\overline{CCE} \rightarrow$ Status Output	—	—	6	
Set-Up Time (1)		t _{RD}	BUCK→Read Data Output	—	—	6	μs
Set-Up Time (2)		t _{BA}	BUCK→ACK, Parity Output	—	—	6	
Hold Time (1)		t _{SZ1}	BUCK→ACK, Parity, Status Output	—	—	6	μs
Hold Time (2)		t _{SZ2}	$\overline{CCE} \rightarrow$ Status Output	—	—	6	
Hold Time (3)		t _{WH}	BUCK→Command Data	6	—	—	

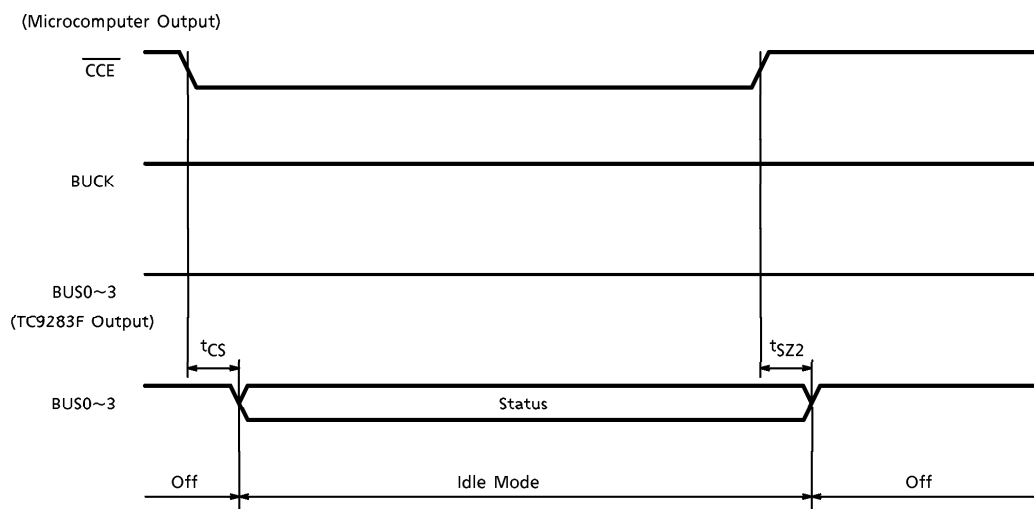
(a) Write command processing mode



(b) Read command processing mode

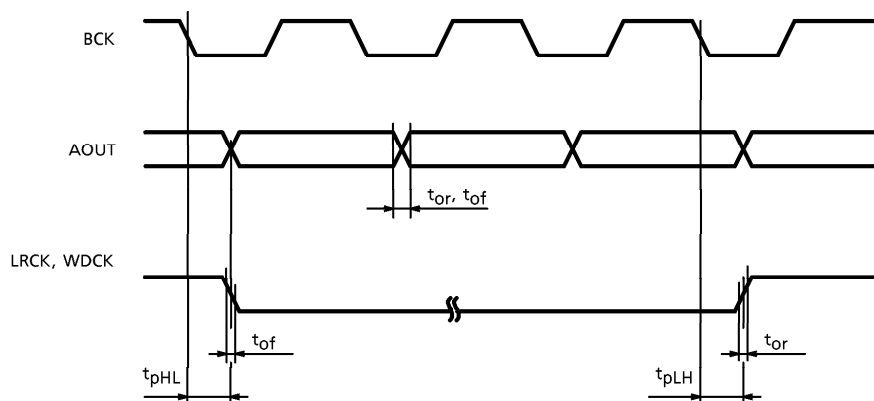


(c) Idle mode



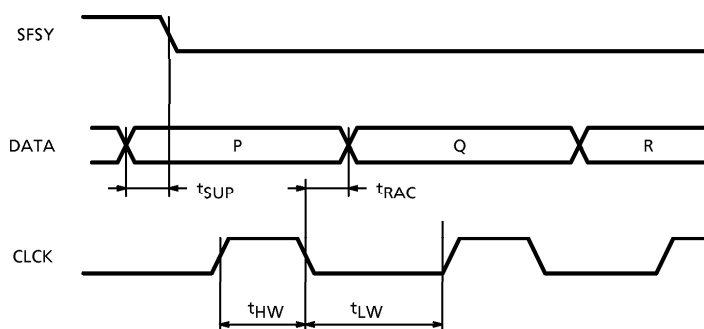
(3) Data output system timing

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{pHL}	BCK→AOUT, WDCK, LRCK	—	—	30	ns
	"L" Level	t_{pLH}		—	—	30	
Output Rising Time		t_{or}	AOUT, WDCK, LRCK	—	—	15	ns
Output Falling Time		t_{of}		—	—	15	



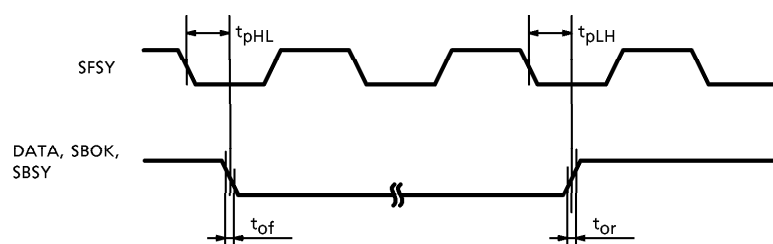
(4) Output timing for subcode P~W

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	"H" Level	t_{HW}	CLK	2	—	—	ns
	"L" Level	t_{LW}		2	—	—	
Set-Up Time		t_{SUP}	SFSY→DATA	0.4	—	—	ns
Read Access Time		t_{RAC}	CLK→DATA	1.2	—	—	



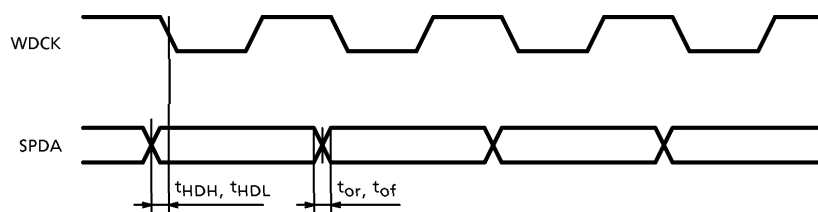
(5) Output time for subcode Q

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{pHL}	SFSY→SBOK, SBSY	- 50	—	200	ns
	"L" Level	t_{pLH}		- 50	—	200	
Output Rising Time		t_{or}	SBOK, SBSY	—	—	40	ns
Output Falling Time		t_{of}		—	—	40	



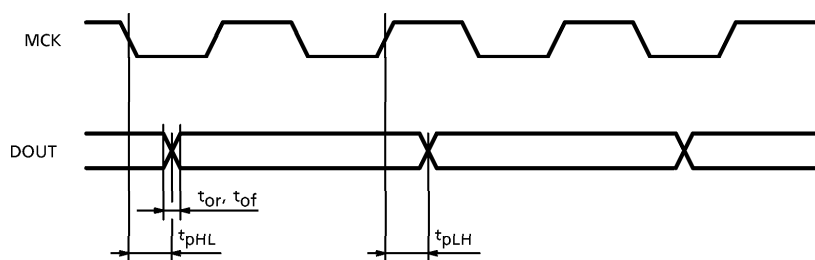
(6) Status signal output timing

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Hold Time	"H" Level	t_{HDH}	WDCK→SPDA	—	—	200	ns
	"L" Level	t_{HDL}		—	—	200	
Output Rising Time		t_{or}	SPDA	—	—	40	ns
Output Falling Time		t_{of}		—	—	40	



(7) Digital output timing

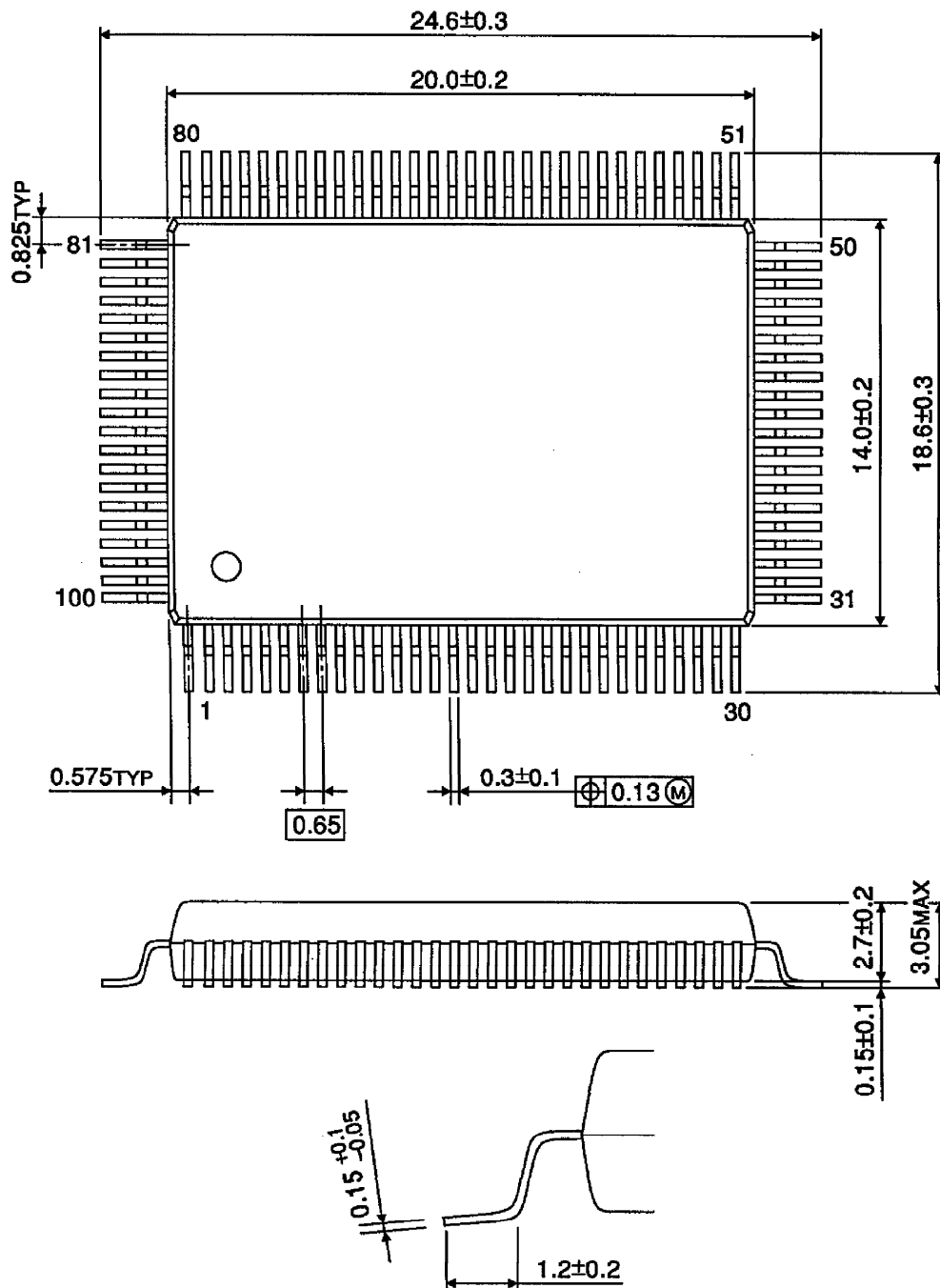
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{pHL}	MCK→DOUT	—	—	60	ns
	"L" Level	t_{pLH}		—	—	60	
Output Rising Time		t_{or}	DOUT	—	—	14	ns
Output Falling Time		t_{of}		—	—	14	



OUTLINE DRAWING

QFP100-P-1420-0.65

Unit : mm



Weight : 1.6g (Typ.)