

Triple ECL to PECL Translator

The MC100LVEL/EL90 is a triple ECL to PECL translator. The device receives either standard or low voltage differential ECL signals and translates them to either standard or low voltage differential PECL output signals. The LVEL device can handle the low voltage signals while the EL device is designed for the standard signals. It is possible to have low voltage signals on one side and standard signals on the other if the LVEL90 is used.

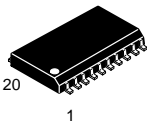
- 500ps Propagation Delays
- Fully Differential Design
- Supports both Standard and Low Voltage Operation
- 20-Lead SOIC Packaging

A V_{BB} output is provided for interfacing with single ended ECL signals at the input. If a single ended input is to be used the V_{BB} output should be connected to the D input. The active signal would then drive the D input. When used the V_{BB} output should be bypassed to ground via a $0.01\mu F$ capacitor. The V_{BB} output is designed to act as the switching reference for the EL90 under single ended input switching conditions, as a result this pin can only source/sink up to 0.5mA of current.

To accomplish the level translation the EL/LVEL90 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins as expected are connected to the system ground plain. Both V_{EE} and V_{CC} should be bypassed to ground via $0.01\mu F$ capacitors.

Under open input conditions, the \overline{D} input will be biased at $V_{EE}/2$ and the D input will be pulled to V_{EE} . This condition will force the Q output to a LOW, ensuring stability.

MC100LVEL90
MC100EL90

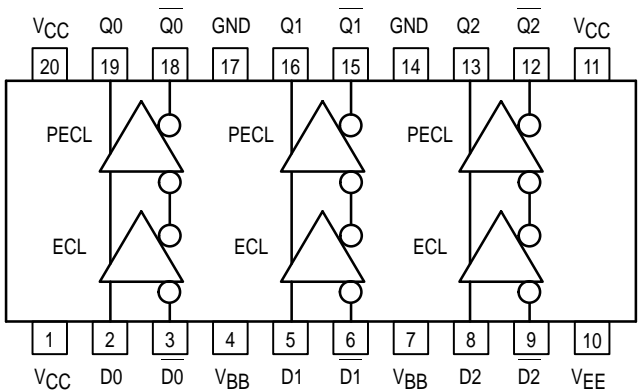


DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-04

PIN NAMES

Pins	Function
Dn	ECL Inputs
Qn	PECL Outputs
V_{BB}	ECL Reference Voltage Output

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



ECL INPUT DC CHARACTERISTICS

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
V _{EE}	Power Supply Voltage EL90 LVEL90	-4.2 -3.0	-5.5 -3.8	-4.2 -3.0	-5.5 -3.8	-4.2 -3.0		-5.5 -3.8	-4.2 -3.0	-5.5 -3.8	V	
I _{IH}	Input HIGH Current		150		150			150		150	μA	
I _{IL}	Input LOW Current	0.5		0.5		0.5			0.5		μA	
V _{PP}	Minimum Peak-to-Peak Input ¹	150		150		150			150		mV	
V _{IH}	Input HIGH Voltage	-1165	-880	-1165	-880	-1165		-880	-1165	-880	V	
V _{IL}	Input LOW Voltage	-1810	-1475	-1810	-1475	-1810		-1475	-1810	-1475	V	
V _{BB}	Reference Output	-1.38	-1.26	-1.38	-1.26	-1.38		-1.26	-1.38	-1.26	V	
I _{EE}	Power Supply Current		8.0		8.0		6.0	8.0		8.0	mA	

1. 150mV input guarantees full logic swing at the output.

LVPECL OUTPUT DC CHARACTERISTICS

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
V _{CC}	Power Supply Voltage	3.0	3.8	3.0	3.8	3.0	3.3	3.8	3.0	3.8	V	
V _{OH}	Output HIGH Voltage ¹	2.215	2.42	2.275	2.42	2.275	2.35	2.42	2.275	2.42	V	V _{CC} = 3.3V
V _{OL}	Output LOW Voltage ¹	1.47	1.745	1.49	1.68	1.49	1.60	1.68	1.49	1.68	V	V _{CC} = 3.3V
I _{IGND}	Power Supply Current		24		24		20	24		26	mA	

1. Levels will vary 1:1 with V_{CC}.

PECL OUTPUT DC CHARACTERISTICS

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
V _{CC}	Power Supply Voltage	4.75	5.25	4.75	5.25	4.75		5.25	4.75	5.25	V	
V _{OH}	Output HIGH Voltage ¹	3.915	4.12	3.975	4.12	3.975	4.05	4.12	3.975	4.12	V	V _{CC} = 5.0V
V _{OL}	Output LOW Voltage ¹	3.17	3.445	3.19	3.38	3.19	3.30	3.38	3.19	3.38	V	V _{CC} = 5.0V
I _{IGND}	Power Supply Current		24		24		20	24		26	mA	

1. Levels will vary 1:1 with V_{CC}.

MC100LVEL90**AC CHARACTERISTICS** ($V_{EE} = -3.0V$ to $-3.8V$; $V_{CC} = 3.0V$ to $3.8V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{PLH} t _{PHL}	Propagation Delay Diff D to Q S.E.	390 340		590 640	410 360		610 660	420 370		620 670	460 410		660 710	ps
t _{SKEW}	Skew Output-to-Output ¹ Part-to-Part (Diff) ¹ Duty Cycle (Diff) ²		20 25	100 200		20 25	100 200		20 25	100 200		20 25	100 200	ps
V _{PP}	Minimum Input Swing ³	150			150			150			150			mV
V _{CMR}	Common Mode Range ⁴	See ⁴		-0.4	See ⁴		-0.4	See ⁴		-0.4	See ⁴		-0.4	V
t _r t _f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	230		500	ps

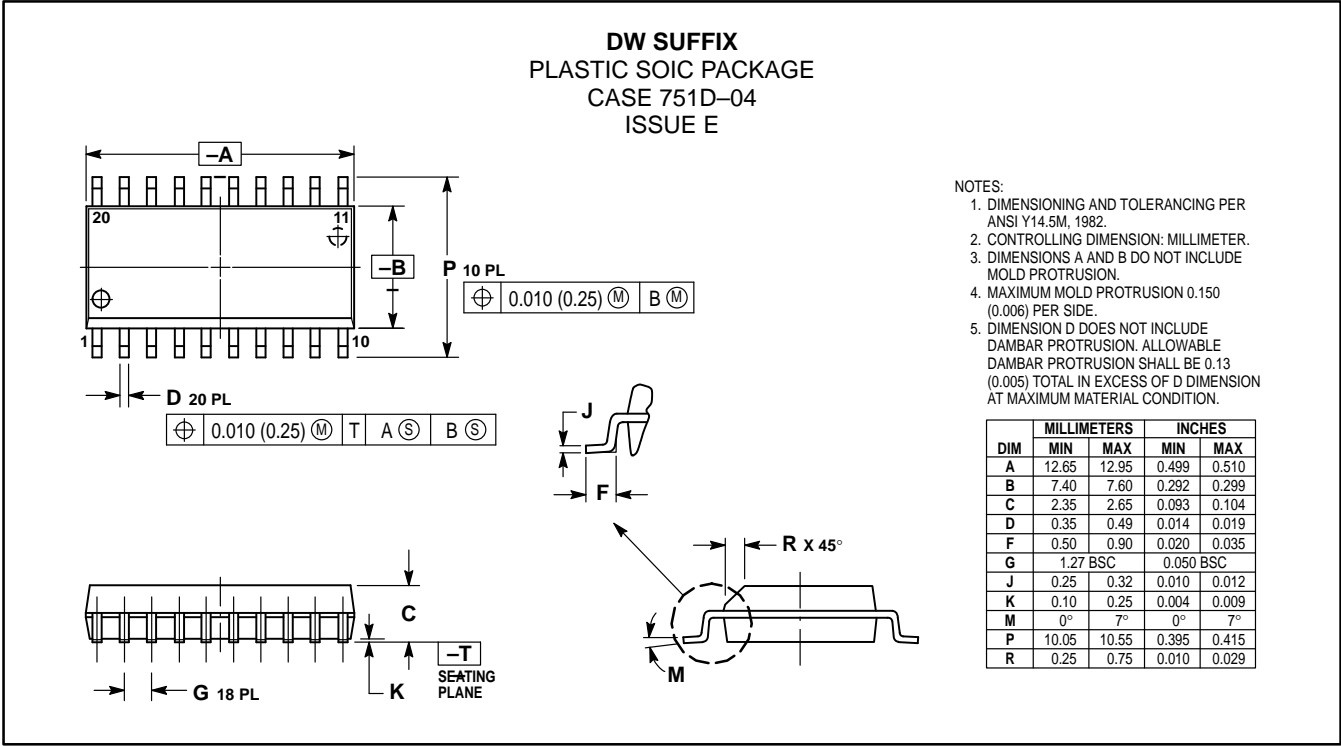
1. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
2. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
3. Minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40 .
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1V. V_{CMRmin} depends on V_{EE} , V_{PP} and temperature. At $V_{PP} < 500mV$ and $-40^\circ C$, V_{CMR} is $V_{EE} + 1.3V$; and for $0-85^\circ C$, V_{CMR} is $V_{EE} + 1.2V$. At $V_{PP} \geq 500mV$ and $-40^\circ C$, V_{CMR} is $V_{EE} + 1.5V$; and for $0-85^\circ C$, V_{CMR} is $V_{EE} + 1.4V$.


MC100EL90**AC CHARACTERISTICS** ($V_{EE} = -4.20V$ to $-5.5V$; $V_{CC} = 4.5V$ to $5.5V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{PLH} t _{PHL}	Propagation Delay Diff D to Q S.E.	390 340		590 640	410 360		610 660	420 370		620 670	460 410		660 710	ps
t _{SKEW}	Skew Output-to-Output ¹ Part-to-Part (Diff) ¹ Duty Cycle (Diff) ²		20 25	100 200		20 25	100 200		20 25	100 200		20 25	100 200	ps
V _{PP}	Minimum Input Swing ³	150			150			150			150			mV
V _{CMR}	Common Mode Range ⁴	See ⁴		-0.4	See ⁴		-0.4	See ⁴		-0.4	See ⁴		-0.4	V
t _r t _f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	230		500	ps

1. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
2. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
3. Minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40 .
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1V. V_{CMRmin} depends on V_{EE} , V_{PP} and temperature. At $V_{PP} < 500mV$ and $-40^\circ C$, V_{CMR} is $V_{EE} + 1.3V$; and for $0-85^\circ C$, V_{CMR} is $V_{EE} + 1.2V$. At $V_{PP} \geq 500mV$ and $-40^\circ C$, V_{CMR} is $V_{EE} + 1.5V$; and for $0-85^\circ C$, V_{CMR} is $V_{EE} + 1.4V$.

OUTLINE DIMENSIONS



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