

1.1 Scope.

This specification covers the device requirements for a hybrid quad 12-bit voltage output D/A converter with double buffered latches.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD390SD/883B
-2	AD390TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-28.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

$+V_S$ to DGND	0 to +18V
$-V_S$ to DGND	0 to -18V
Digital Inputs (Pins 1-12, 23-28) to DGND	-1.0V to +7V
Ref In to DGND	$\pm V_S$
AGND to DGND	$\pm 0.6V$
Analog Outputs (Pins 16, 18-21)	Infinite
Short to AGND or DGND, Momentary Shorts to $\pm V_S$	
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 8^\circ\text{C/W}$
 $\theta_{JA} = 25^\circ\text{C/W}$

AD390 — SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C (−55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Data Input Voltage High End Point Electrical	V _{IH}	−1, 2 −1, 2	2.0 (2.0) 5.5 (5.5)	2.0		2.0	Test Limits Apply to Pins 1–12. Design Limits Apply to Pins 23–28.	V min V max V min
Data Input Voltage Low End Point Electrical	V _{IL}	−1, 2 −1, 2	0.0 (0.0) 0.8 (0.8)	0.8		0.8	Test Limits Apply to Pins 1–12. Design Limits Apply to Pins 23–28.	V min V max V max
Input Current High End Point Electrical	I _{IH}	−1, 2 −1, 2	1200 (1200)	1200			Test Limits Apply to Pins 1–12. Design Limits Apply to Pins 23–28, Except for Pin 24 Which is 3X.	μA max
Input Current Low End Point Electrical	I _{IL}	−1, 2 −1, 2	400 (400)	400				μA max
Output Voltage Range	V _{OUT}	−1, 2	10 (10) 10 (10)			10 10		+ V max − V min
Output Current Range	I _{OR}	−1, 2	5 (5)				@ ±10V Output	mA min
Gain Error End Point Electrical	A _E	−1 −2 −1, 2	0.1 0.05	0.1 0.2		0.05	With External +10,000 Ref	± % FSR max ²
Gain Error Temperature Coefficient	TC _{AE}	−1 −2	(40) (20)				With Internal Reference	± ppm/°C max
		−1 −2	(10) (5)		10 5		With External Reference	± ppm/°C max
Offset Error End Point Electrical	V _{OS}	−1 −2 −1, 2	0.05 0.025	0.05 0.1		0.025		± % FSR max
Bipolar Zero Temperature Coefficient	TCB _{PZ}	−1 −2	(10) (5)		10 5		V _{BPFS} = ±10V	± ppm/°C max
Differential Linearity ³ Error End Point Electrical	DLE	−1 −2 −1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Linearity Error ⁴ End Point Electrical	LE	−1 −2 −1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Linearity Error Temperature Coefficient	TC _{LE}	−1 −2	(3/4) (1/2)		3/4 1/2			± LSB max
Positive Summation Error End Point Electrical	E _{PE}	−1 −2 −1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Negative Summation Error End Point Electrical	E _{NE}	−1 −2 −1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Reference Output	REF _{OUT}	−1, 2	9.997 10.003	9.997 10.003			R _L = 6.8kΩ	V min V max
Power Supply Voltages ³	V _S	−1, 2 −1, 2	13.5 16.5					± V min ± V max

Table 1. (Continued on next page)

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Test	Symbol	Device	Design Limit @ +25°C (-55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Power Supply Currents	I_{EE} I_{CC}	-1, 2	100 35	100 35	120 35		No Load	- mA max + mA max
Power Supply Gain Sensitivity Delta Gain/ Delta V_S (+ V_S and - V_S)	PSRR	-1, 2	0.0067			0.0067	Input Bits = 1111 1111 1111	± % FS/%
Timing Specifications Chip Select Pulse Width	t_{AW}	-1 -2	100				See Figure 2	ns min
Address Select Low Time	t_{WP}	-1 -2	100				See Figure 2	ns min
Data Valid Before $\overline{A0}$ Rising Edge	t_{OW}	-1 -2	50				See Figure 2	ns min
Data Valid After $\overline{A0}$ Rising Edge	t_{DH}	-1 -2	10				See Figure 2	ns min
Chip Select Valid Before $\overline{A1}$ Low	t_{AS}	-1 -2	0				See Figure 2	ns min
Output Voltage Settling Time	t_{SETT}	-1 -2	8				See Figure 2	μs max

NOTES

¹ T_A = +25°C and $\pm V_S$ = ±15V unless otherwise specified.

AD390 can be used with supplies as low as ±11.4V (see AD390 commercial data sheet).

²FSR means Full-Scale Range and is equal to 20V for a ±10V bipolar range.

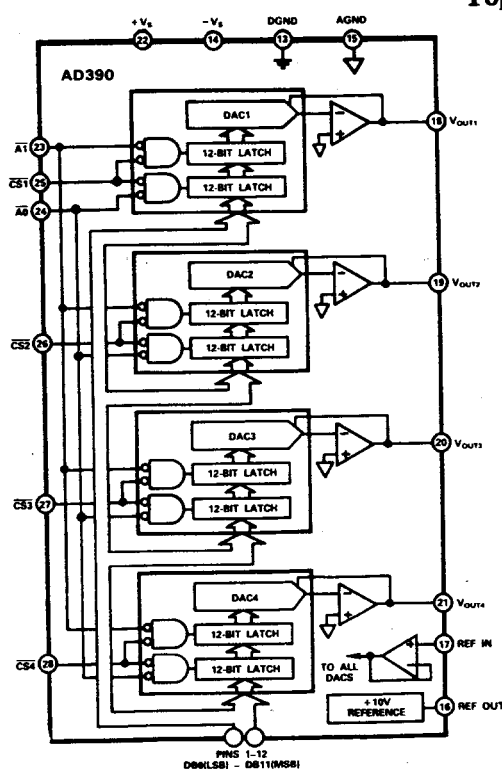
³Monotonicity is tested for over the full military temperature.

⁴Integral Nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the transfer function.

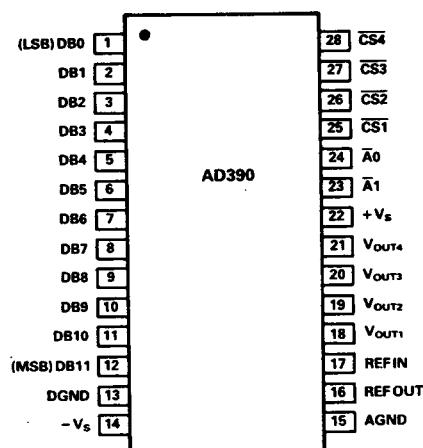
Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View



DH-28 Package

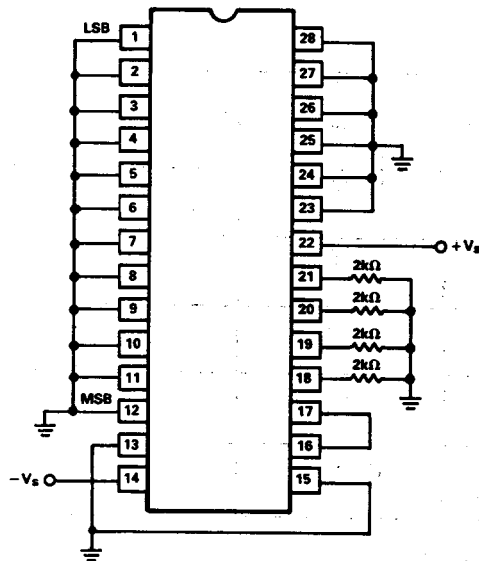


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (1).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



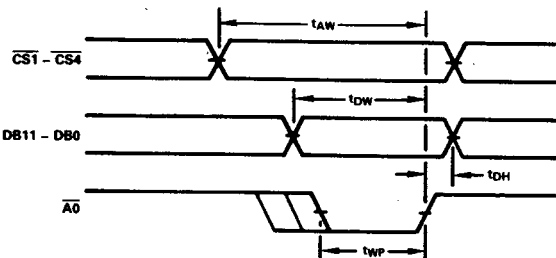
CS1	CS2	CS3	CS4	A1	A0	Operation
1	1	1	1	X	X	No Operation
X	X	X	X	1	1	No Operation
0	1	1	1	1	0	Enable 1st rank of DAC 1
1	0	1	1	1	0	Enable 1st rank of DAC 2
1	1	0	1	1	0	Enable 1st rank of DAC 3
1	1	1	0	1	0	Enable 1st rank of DAC 4
0	1	1	1	0	1	Load DAC 1 second rank from first rank
1	0	1	1	0	1	Load DAC 2 second rank from first rank
1	1	0	1	0	1	Load DAC 3 second rank from first rank
1	1	1	0	0	1	Load DAC 4 second rank from first rank
0	0	0	0	0	0	All latches transparent

Table 2. AD390 Truth Table

Digital Input Code	Analog Output Voltage
0000 0000 0000	- 10.000V - Full Scale
0100 0000 0000	- 5.000V - 1/2 Scale
1000 0000 0000	0.000V Zero
1000 0000 0001	+ 4.88mV + 1LSB
1100 0000 0000	+ 5.000V + 1/2 Scale
1111 1111 1111	+ 9.9951V + Full Scale - 1LSB

Table 3. AD390 Analog Output vs. Digital Input ($\pm V$ Scale)

Write Cycle #1 (Load First Rank from Data Bus; $\overline{A1} = 1$)



Write Cycle #2 (Load Second Rank from First Rank; $\overline{A0} = 1$)

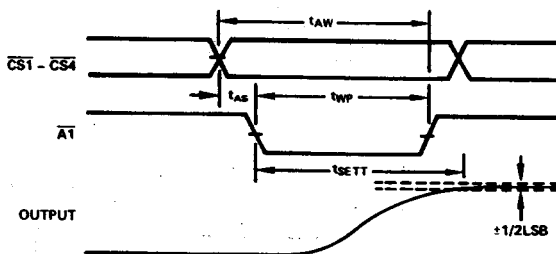


Figure 1. Timing Diagram