

SN54AS286, SN74AS286
9-BIT PARITY GENERATORS/CHECKERS
WITH BUS-DRIVER PARITY I/O PORT

SDAS050B – DECEMBER 1983 – REVISED DECEMBER 1994

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity
- Direct Bus Connection for Parity Generation or Checking by Using the Parity I/O Port
- Glitch-Free Bus During Power Up/Down
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

The SN54AS286 and SN74AS286 universal 9-bit parity generators/checkers feature a local output for parity checking and a 48-mA bus-driving parity input/output (I/O) port for parity generation/checking. The word-length capability is easily expanded by cascading.

The transmit ($\overline{\text{XMIT}}$) control input is implemented specifically to accommodate cascading. When $\overline{\text{XMIT}}$ is low, the parity tree is disabled and PARITY ERROR remains at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high, the parity tree is enabled. PARITY ERROR indicates a parity error when either an even number of inputs (A–I) are high and PARITY I/O is forced to a low logic level, or when an odd number of inputs are high and PARITY I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port remains in the high-impedance state during power up or power down to prevent bus glitches.

The SN54AS286 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS286 is characterized for operation from 0°C to 70°C .

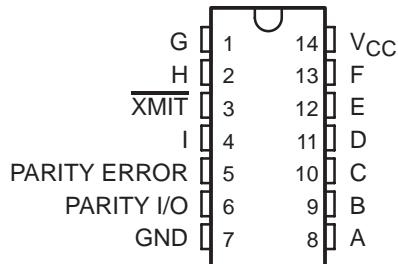
FUNCTION TABLE

| NUMBER OF INPUTS (A–I) THAT ARE HIGH | $\overline{\text{XMIT}}$ | PARITY I/O | PARITY ERROR |
|--|--------------------------|---------------|-----------------|
| 0, 2, 4, 6, 8 | I | H | H |
| 1, 3, 5, 7, 9 | I | L | H |
| 0, 2, 4, 6, 8 | h | h | H |
| 0, 2, 4, 6, 8 | h | I | L |
| 1, 3, 5, 7, 9 | h | h | L |
| 1, 3, 5, 7, 9 | h | I | H |

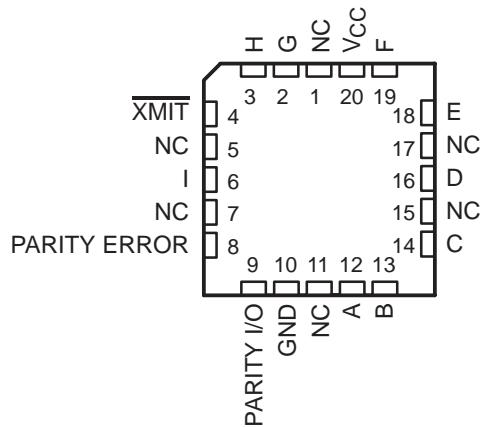
h = high input level
H = high output level

I = low input level
L = low output level

SN54AS286 . . . J PACKAGE
SN74AS286 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS286 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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 **TEXAS
INSTRUMENTS**

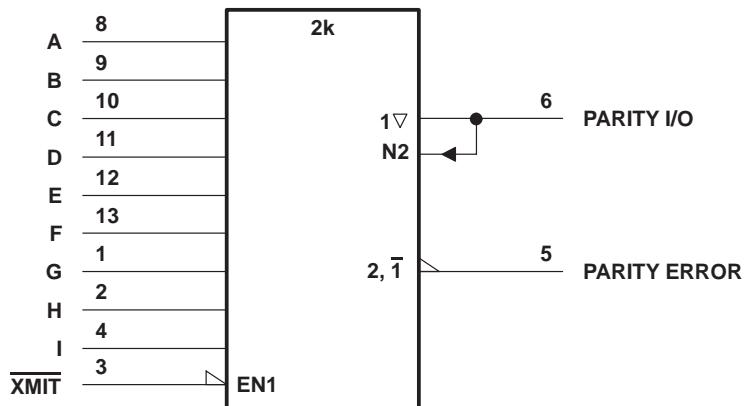
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**SN54AS286, SN74AS286
9-BIT PARITY GENERATORS/CHECKERS
WITH BUS-DRIVER PARITY I/O PORT**

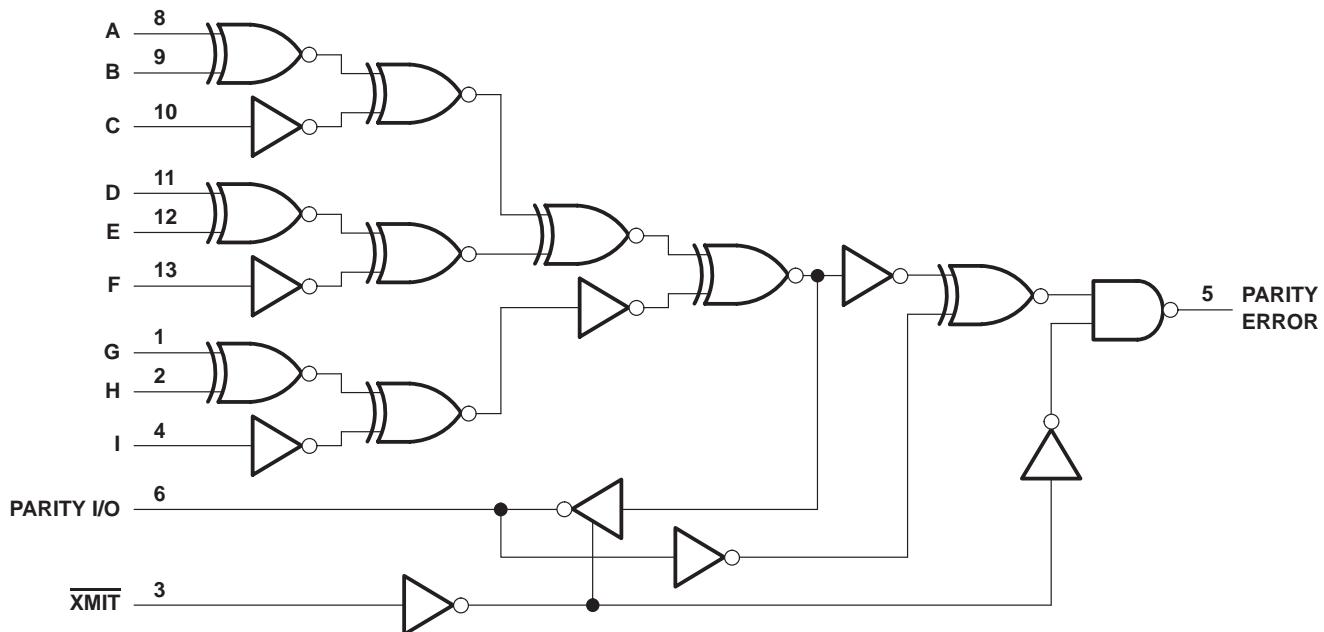
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN54AS286 | | | SN74AS286 | | | UNIT |
|-----------------|--------------------------------|--------------|-----|-----|-----------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} | High-level output current | PARITY ERROR | | | -2 | | -2 | mA |
| | | PARITY I/O | | | -12 | | -15 | |
| I _{OL} | Low-level output current | PARITY ERROR | | | 20 | | 20 | mA |
| | | PARITY I/O | | | 32 | | 48 | |
| T _A | Operating free-air temperature | | -55 | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54AS286 | | | SN74AS286 | | | UNIT | |
|---------------|--|--|--------------------------|--------------|-----------|--------------|------|---------------|--|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | | | -1.2 | V | |
| V_{OH} | All outputs | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -2\text{ mA}$ | | $V_{CC} - 2$ | | $V_{CC} - 2$ | | V | |
| | PARITY I/O | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -3\text{ mA}$ | 2.4 | 2.9 | | 2.4 | | |
| | | | $I_{OH} = -12\text{ mA}$ | 2.4 | | | | | |
| | | | $I_{OH} = -15\text{ mA}$ | | | 2.4 | | | |
| V_{OL} | PARITY ERROR | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 20\text{ mA}$ | 0.35 | 0.5 | | 0.35 | 0.5 | |
| | PARITY I/O | | $I_{OL} = 32\text{ mA}$ | | 0.5 | | | V | |
| | | | $I_{OL} = 48\text{ mA}$ | | | | 0.5 | | |
| I_I | PARITY I/O | $V_{CC} = 5.5\text{ V}$ | $V_I = 5.5\text{ V}$ | | 0.1 | | 0.1 | mA | |
| | All other inputs | | $V_I = 7\text{ V}$ | | 0.1 | | 0.1 | | |
| I_{IH} | PARITY I/O\$ | $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$ | | | 50 | | 50 | μA | |
| | All other inputs | | | | 20 | | 20 | | |
| I_{IL} | PARITY I/O\$ | $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$ | | | -0.5 | | -0.5 | mA | |
| | All other inputs | | | | -0.5 | | -0.5 | | |
| $I_O\ddagger$ | $V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$ | | -30 | -112 | -30 | -112 | -30 | mA | |
| I_{CC} | Transmit | $V_{CC} = 5.5\text{ V}$ | | | 30 | 43 | | mA | |
| | Receive | | | | 35 | 50 | 35 | | |

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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switching characteristics (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $R1 = 500\text{ }\Omega,$ $R2 = 500\text{ }\Omega,$ $T_A = \text{MIN to MAX}^\dagger$ | | | | UNIT | |
|-----------|--------------------------|----------------|--|-----|-----------|------|------|--|
| | | | SN54AS286 | | SN74AS286 | | | |
| | | | MIN | MAX | MIN | MAX | | |
| t_{PLH} | Any A - I | PARITY I/O | 3 | 17 | 3 | 15 | ns | |
| t_{PHL} | | | 3 | 15 | 3 | 14 | | |
| t_{PLH} | Any A - I | PARITY ERROR | 3 | 20 | 3 | 16.5 | ns | |
| t_{PHL} | | | 3 | 18 | 3 | 16.5 | | |
| t_{PLH} | PARITY I/O | PARITY ERROR | 3 | 10 | 3 | 9 | ns | |
| t_{PHL} | | | 3 | 10 | 3 | 9 | | |
| t_{PZH} | $\overline{\text{XMIT}}$ | PARITY I/O | 3 | 14 | 3 | 13 | ns | |
| t_{PZL} | | | 3 | 17 | 3 | 16 | | |
| t_{PHZ} | $\overline{\text{XMIT}}$ | PARITY I/O | 3 | 13 | 3 | 11.5 | ns | |
| t_{PLZ} | | | 3 | 11 | 3 | 10 | | |

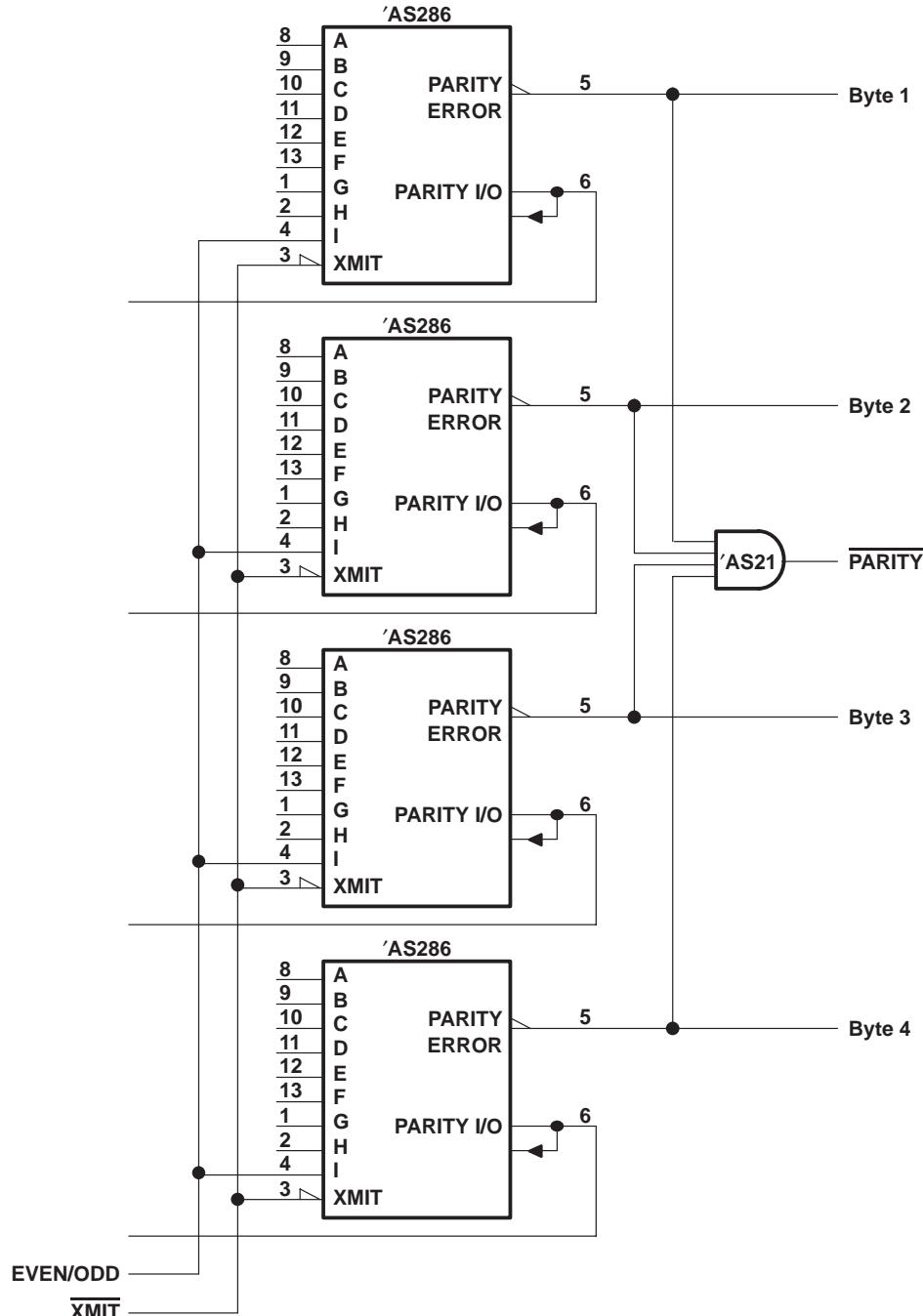
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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APPLICATION INFORMATION

Figure 1 shows a 32-bit parity generator/checker with output polarity switching, parity-error detection, and parity on every byte.



Pin numbers shown are for the D, J, and N packages.

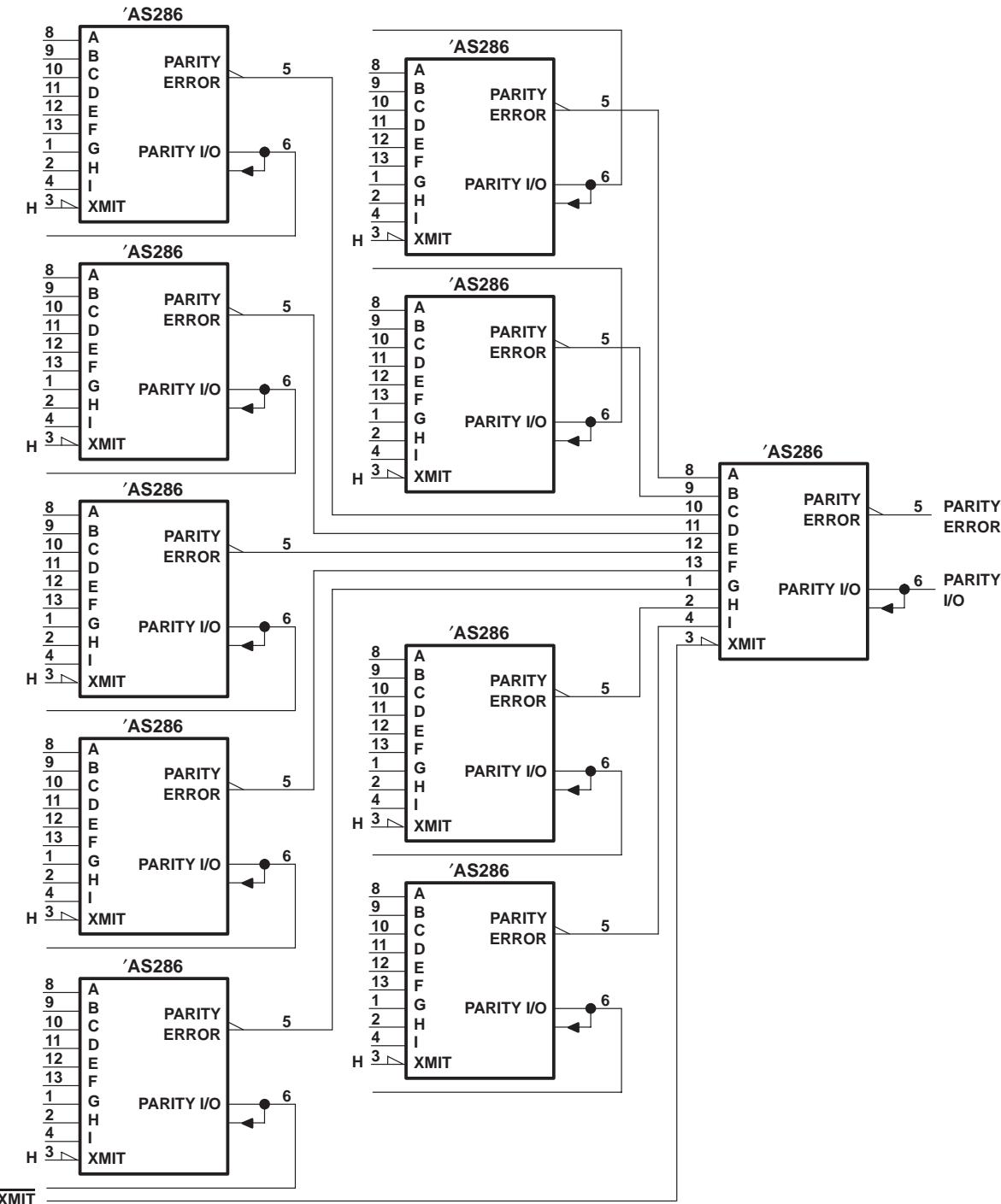
Figure 1. 32-Bit Parity Generator/Checker

SN54AS286, SN74AS286 9-BIT PARITY GENERATORS/CHECKERS WITH BUS-DRIVER PARITY I/O PORT

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APPLICATION INFORMATION

Figure 2 shows a 90-bit parity generator/checker with $\overline{\text{XMIT}}$ on the last stage available for use with parity detection.

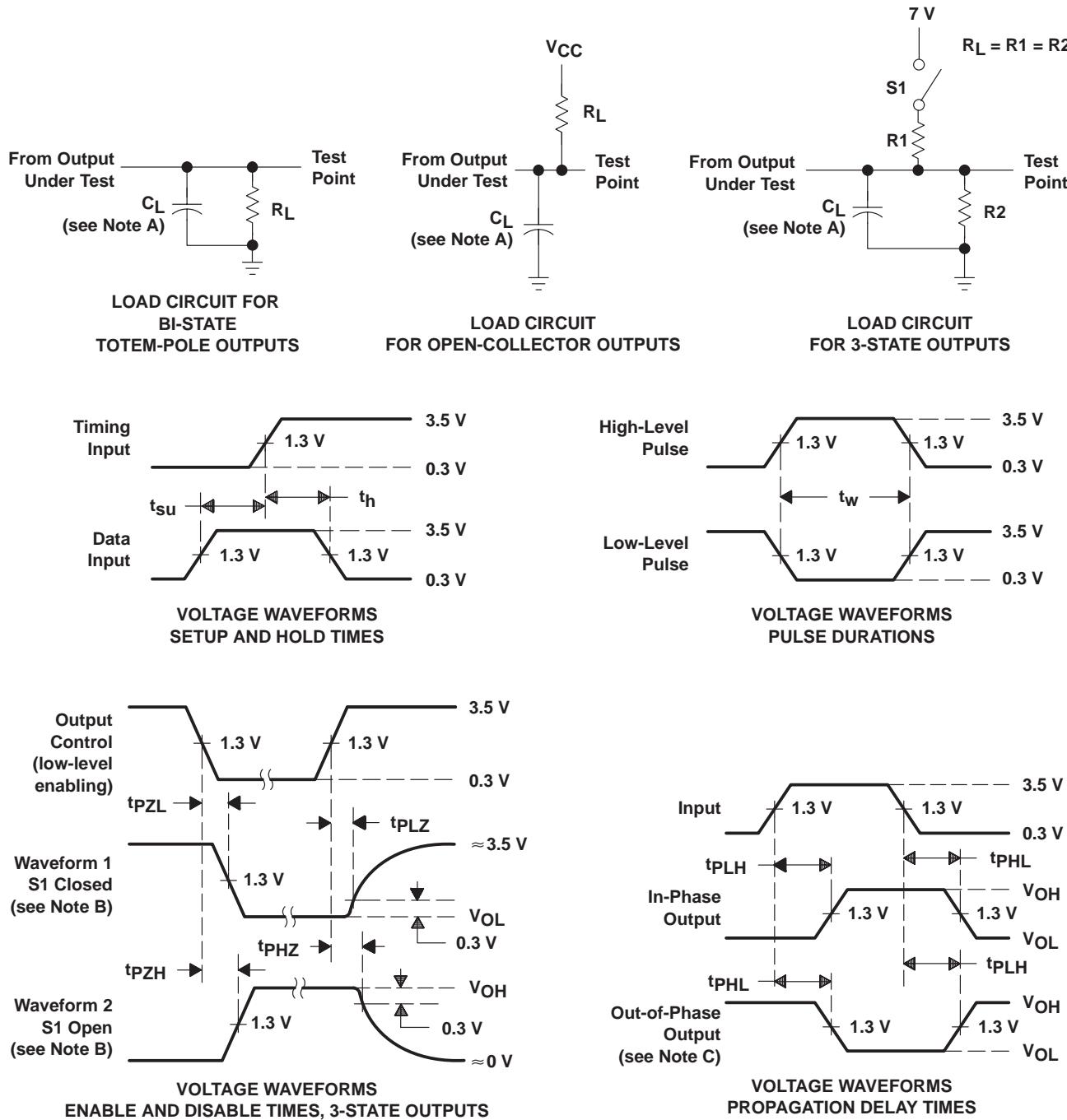


Pin numbers shown are for the D, J, and N packages.

Figure 2. 90-Bit Parity Generator/Checker With Parity-Error Detection



PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|---|
| 5962-8966301CA | ACTIVE | CDIP | J | 14 | | TBD | Call TI | Call TI | -55 to 125 | | Samples |
| SN54AS286J | OBsolete | CDIP | J | 14 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SN74AS286D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS286 | Samples |
| SN74AS286DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS286 | Samples |
| SN74AS286DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS286 | Samples |
| SN74AS286DR | OBsolete | SOIC | D | 14 | | TBD | Call TI | Call TI | 0 to 70 | AS286 | |
| SN74AS286DRE4 | OBsolete | SOIC | D | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74AS286DRG4 | OBsolete | SOIC | D | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74AS286N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS286N | Samples |
| SN74AS286NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS286N | Samples |
| SNJ54AS286FK | OBsolete | LCCC | FK | 20 | | TBD | Call TI | Call TI | -55 to 125 | | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54AS286, SN74AS286 :

- Catalog: [SN74AS286](#)
- Military: [SN54AS286](#)

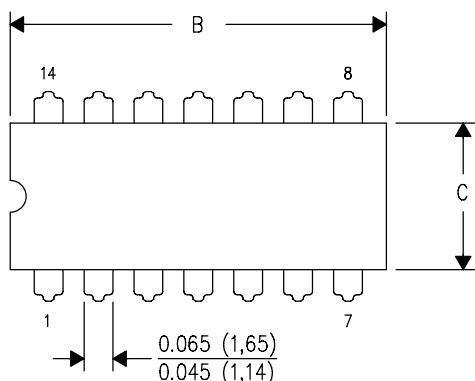
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

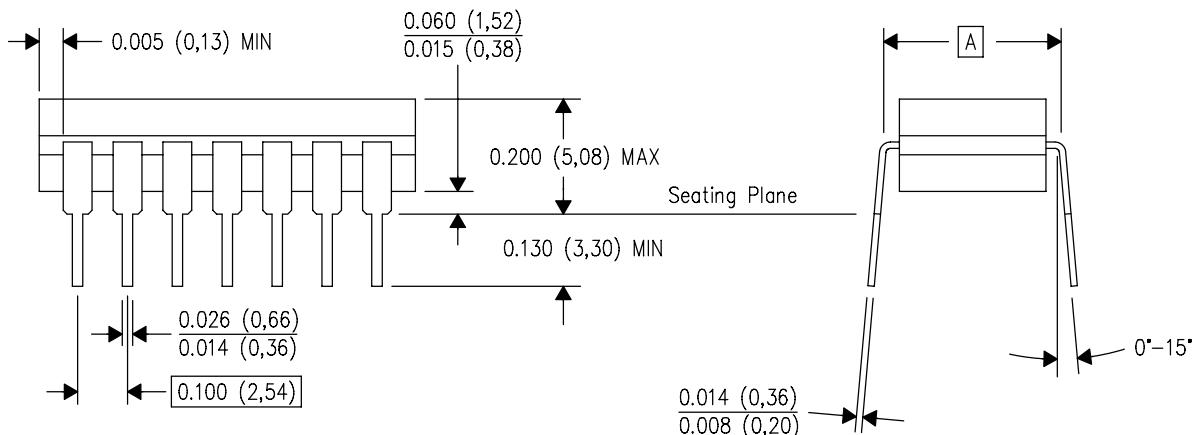
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



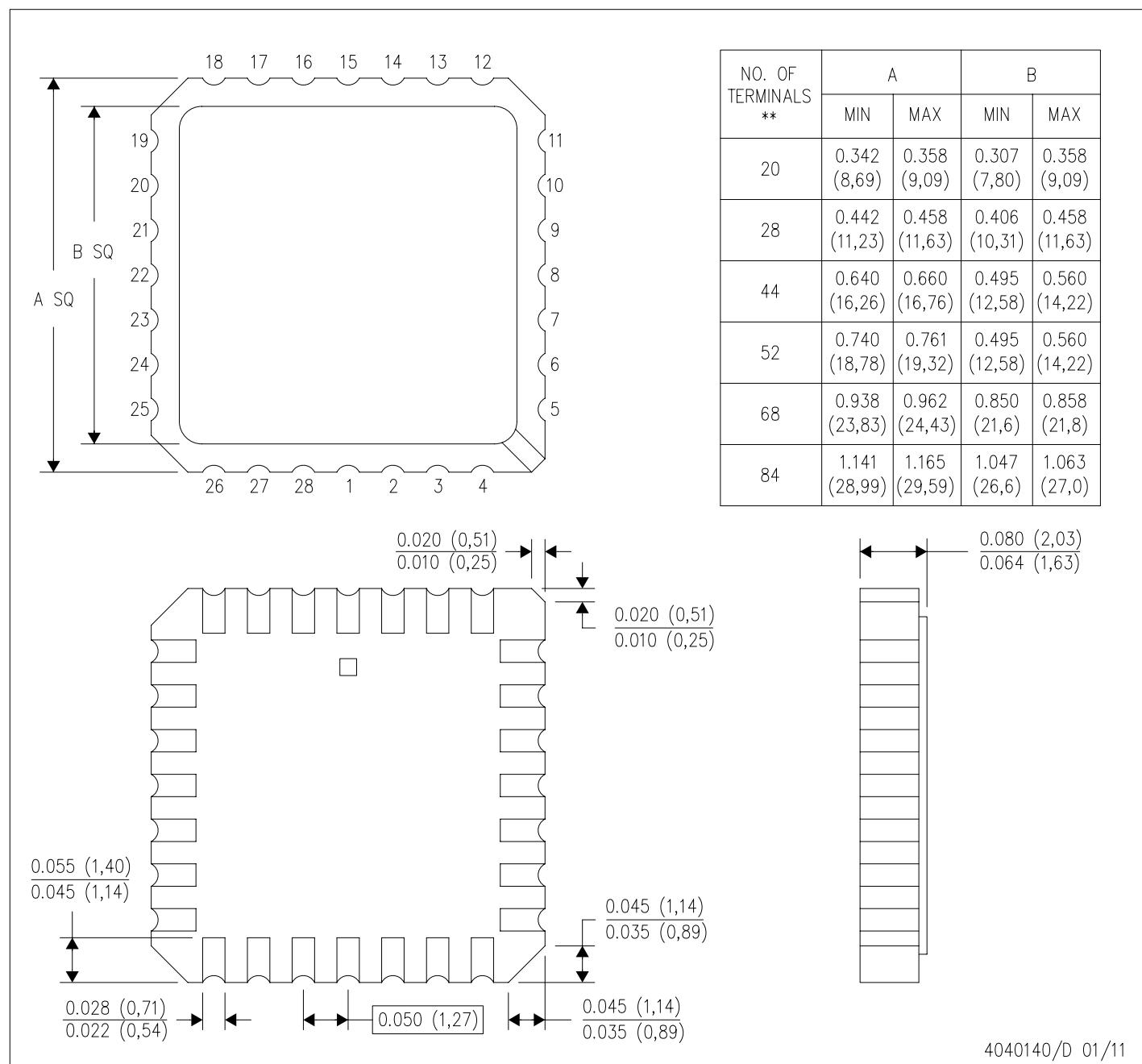
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- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



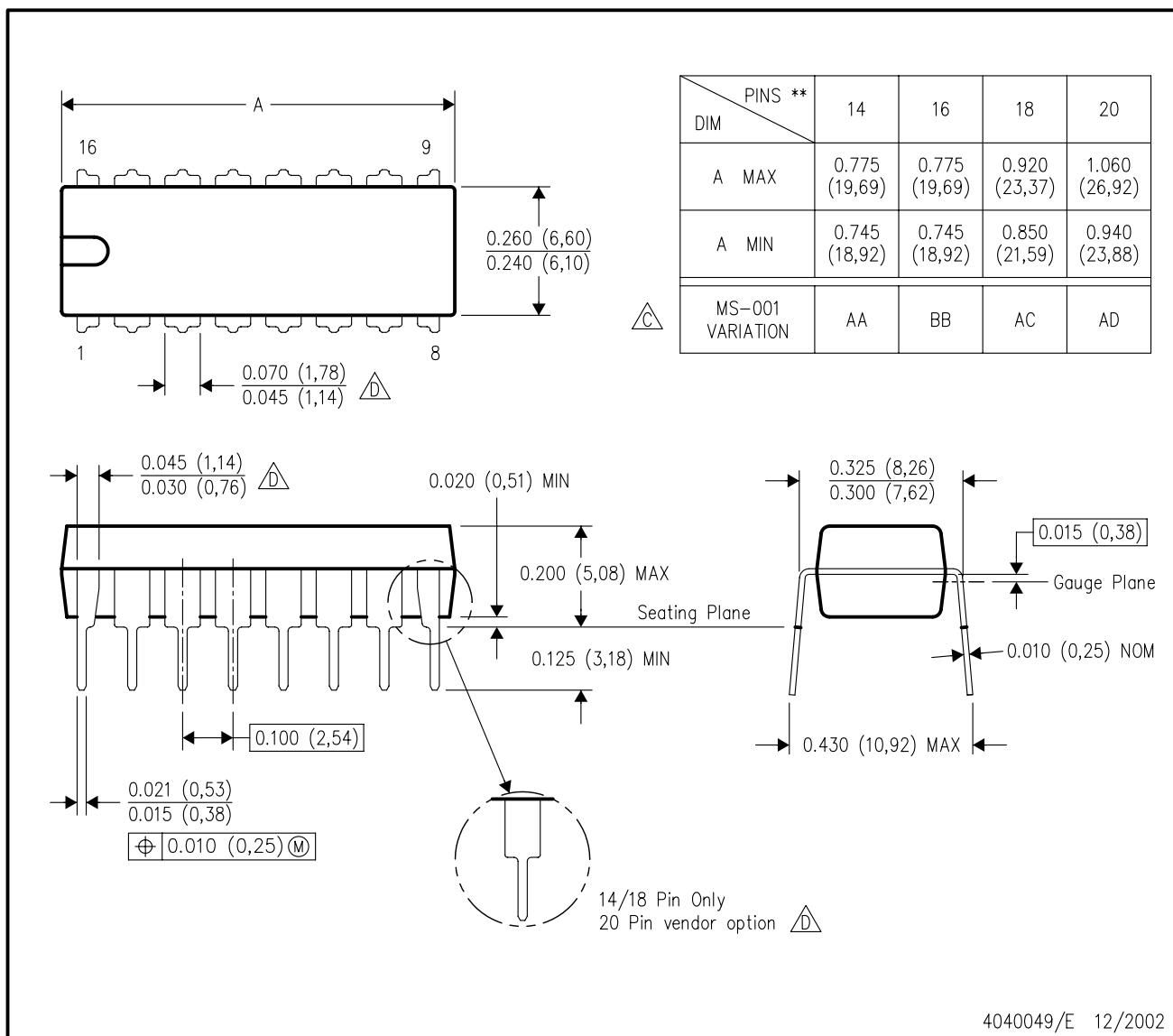
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

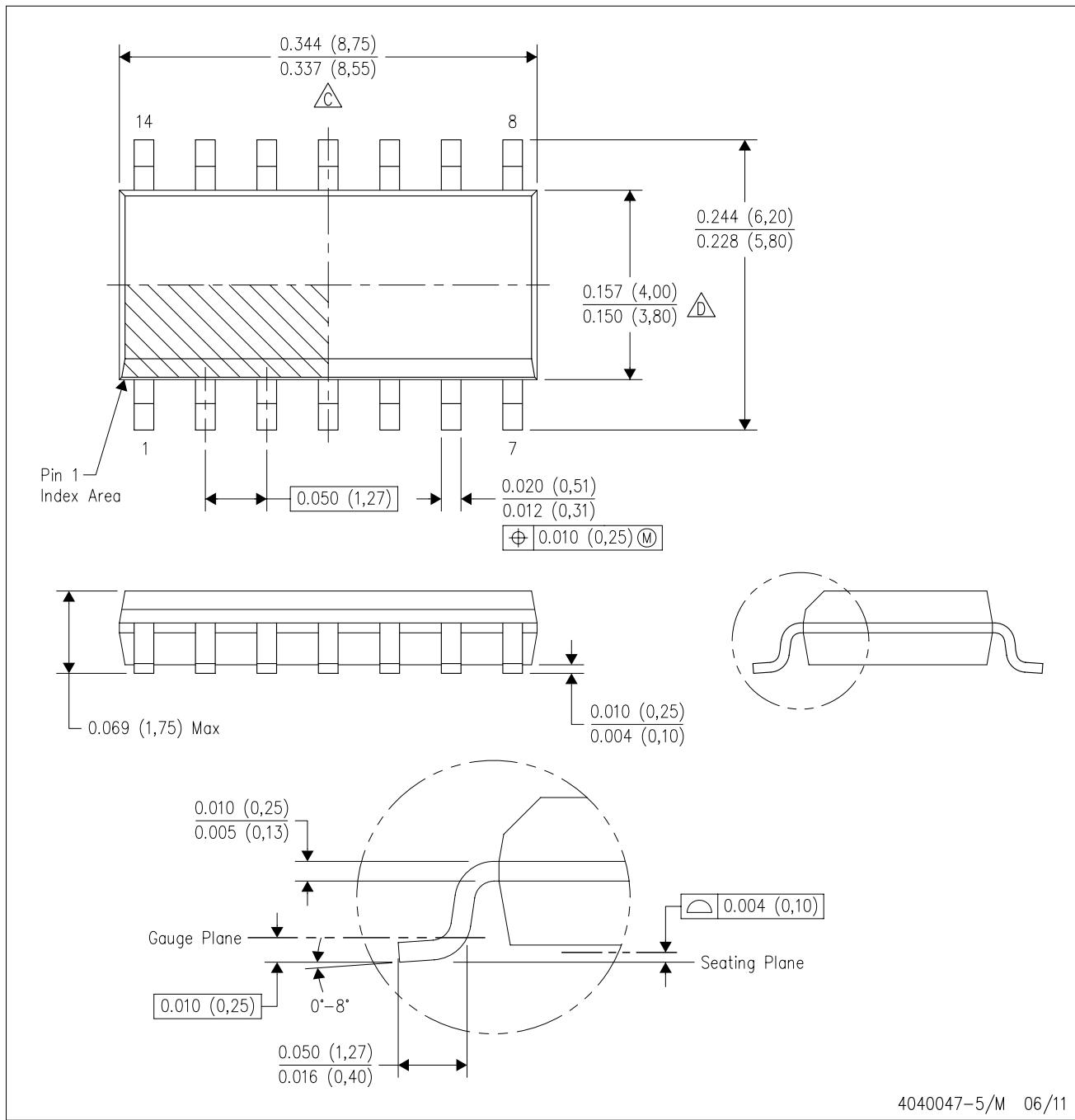
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

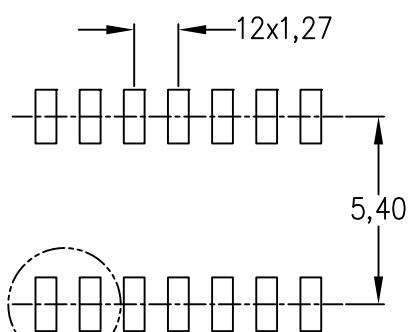
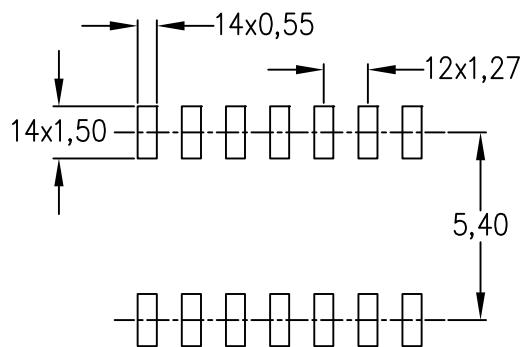
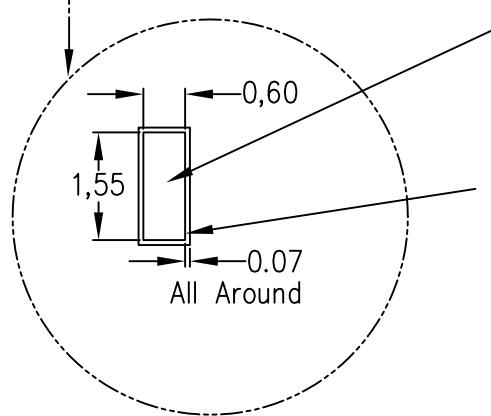
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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