SC4612
Wide Input Range High Performance Synchronous Buck Switching Controller

POWER MANAGEMENT

Description

SC4612 is a high performance synchronous buck controller that can be configured for a wide range of applications. The SC4612 utilizes synchronous rectified buck topology where high efficiency is the primary consideration. SC4612 is optimized for applications requiring wide input supply range and low output voltages down to 500mV.

SC4612 implements an asynchronous soft-start mode, which keeps the lower side MOSFET off during soft-start, a desired feature when a converter turns on into a preset external voltage or pre-biased output voltage. With the lower MOSFET off, the external bus is not discharged, preventing any disturbances in the start up slope and any latch-up of modern day ASIC circuits.

SC4612 comes with a rich set of features such as regulated DRV supply, programmable soft-start, high current gate drivers, internal bootstrapping for driving high side N-channel MOSFET, shoot through protection, R_{DS-ON} sensing with hiccup over current protection, and asynchronous start up with over current protection.

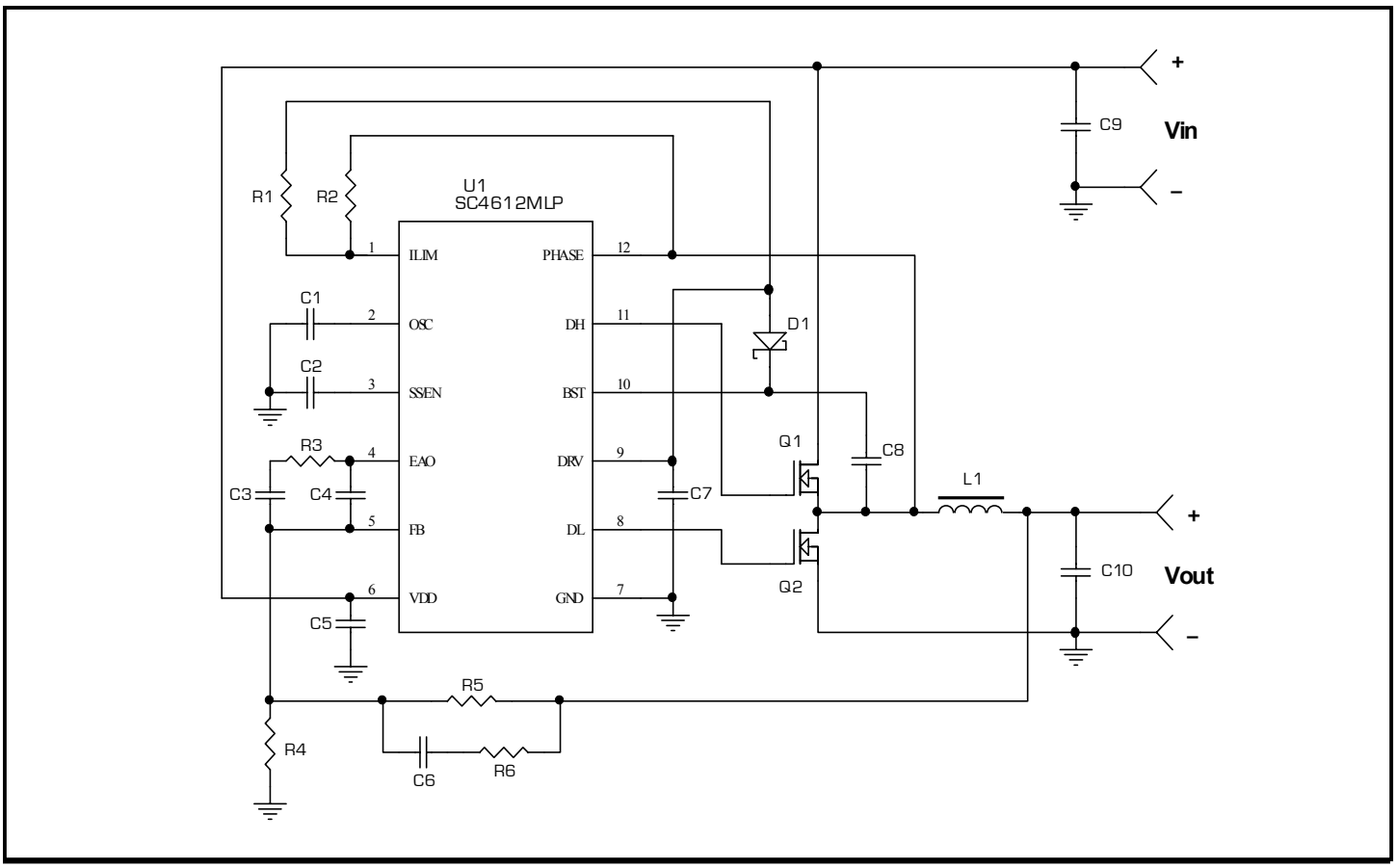
Features

- Wide input voltage range, up to 28V
- Internally regulated DRV
- Output voltage as low as 0.5V
- 1.7A gate drive capability
- Asynchronous start up mode
- Low side R_{DS-ON} sensing with hiccup mode current limit
- Programmable current limit
- Programmable frequency up to 1.2 MHz
- Available in MLPD-12 and SOIC-14 Lead-free packages. This product is fully WEEE and RoHS compliant

Applications

- Distributed power architectures
- Telecommunication equipment
- Servers/work stations
- Mixed signal applications
- Base station power management
- Point of use low voltage high current applications

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Bias Supply Voltage to GND	VDD	-0.3 to 30	V
DRV to GND		-0.3 to 10	V
DRV Source Current (peak)		± 75	mA
ILIM, to GND		-0.3 to 10	V
EAO, SS/EN, FB, OSC to GND		-0.3 to +5	V
DL to GND		-0.3 to +10	V
BST to PHASE		-0.3 to +10	V
PHASE to GND	VIN	-2 to +40	V
DH to PHASE		-0.3 to +10	V
Thermal Resistance Junction to Ambient (MLPD) (1)	θ_{JA}	45.3	°C/W
Thermal Resistance Junction to Ambient (SOIC)	θ_{JA}	115	°C/W
Thermal Resistance Junction to Case (SOIC)	θ_{JC}	45	°C/W
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Peak IR Reflow Temperature (10-40s), (MLP-12)	$T_{IR\ Reflow}$	260	°C
Lead Temperature (10s), (SOIC-14)	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

All voltages with respect to GND. Positive currents are into, and negative currents are out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns. Consult Packaging Section of Data sheet for thermal limitations and considerations of packages.

Note:
(1). 1 sq. inch of FR-4, double-sided, 1 oz copper weight.

Electrical Characteristics

Unless otherwise specified:
VIN = VDD = 12V, F_{OSC} = 600kHz, $T_A = T_J$ = -40°C to 125°C.

Parameter	Test Conditions	Min	Typ	Max	Units
Bias Supply					
VDD				28	V
Quiescent Current	V_{DD} = 28V, No load, SS/EN = 0		5	7	mA
VDD Undervoltage Lockout					
Start Threshold		4.20	4.50	4.75	V
UVLO Hysteresis			400		mV
Drive Regulator					
DRV	10V ≤ V_{DD} ≤ 28V, I_{OUT} ≤ 1mA	7.3	7.8	8.3	V
Load Regulation	1mA ≤ I_O ≤ 100mA			100	mV
Oscillator					
Operation Frequency Range		100		1200	kHz
Initial Accuracy (1)	C_{OSC} = 160pF (Ref only)	540	600	660	kHz
Maximum Duty Cycle (2)		85			%
Ramp Peak to Valley (1)			850		mV
Oscillator Charge Current		90		110	µA
Current Limit (Low Side Rdson)					
Current Limit Threshold Voltage	V_{OUT} = 500mV, 3.3V, 5V		100		mV
Error Amplifier					
Feedback Voltage	T_A = 25°C	0.495	0.500	0.505	V
	T_J = -40 to +125°C	0.488	0.500	0.512	V
Input Bias Current	FB = 0.5V			200	nA
Open Loop Gain (1)			60		dB
Unity Gain Bandwidth (1)		7	10		MHz
Output Sink Current	Open Loop, FB = 0V		900		µA
Output Source Current	Open Loop, FB = 0.6V		1100		µA
Slew Rate (1)			1		V/µs

Electrical Characteristics (Cont.)

Unless otherwise specified:

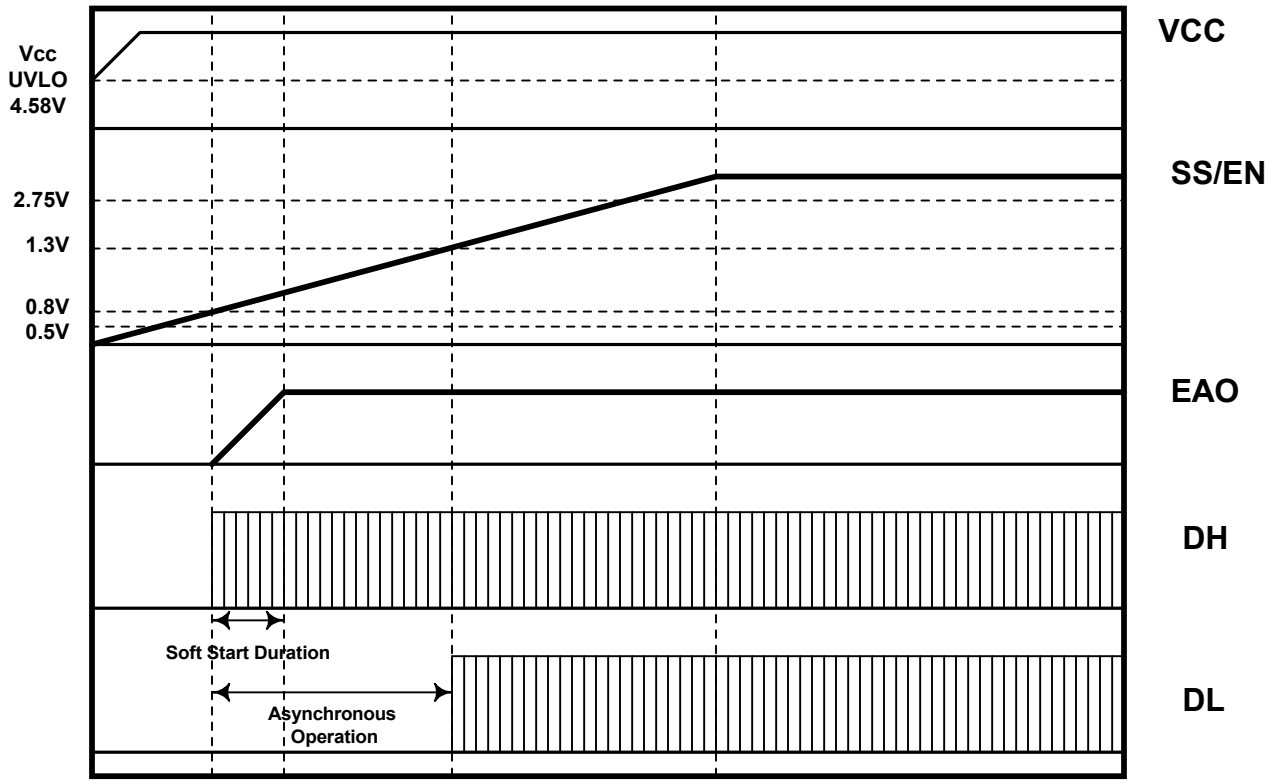
VIN = VDD = 12V, F_{OSC} = 600kHz, $T_A = T_J$ = -40°C to 125°C.

Parameter	Test Conditions	Min	Typ	Max	Units
SS/EN					
Disable Threshold Voltage				500	mV
Soft Start Charge Current			25		µA
Soft Start Discharge Current (1)			1		µA
Disable Low to Shut Down (1)			50		ns
Hiccup					
Hiccup duty cycle	C_{SS} = 0.1, current limit condition		1		%
Gate Drive					
Gate Drive On-Resistance (H)(2)	I_{SOURCE} = 100mA			4	Ω
Gate Drive On-Resistance (L)(2)	I_{SINK} = 100mA			4	Ω
DL Source/Sink Peak Current(2)	COUT = 2000pF	±1.4	1.7		A
DH Source/Sink Peak Current(2)	COUT = 2000pF	±1.4	1.7		A
Output Rise Time	COUT = 2000pF		20		ns
Output Fall Time	COUT = 2000pF		20		ns
Minimum Non-Overlap (1)			30		ns
Minimum On Time(2)				110	ns

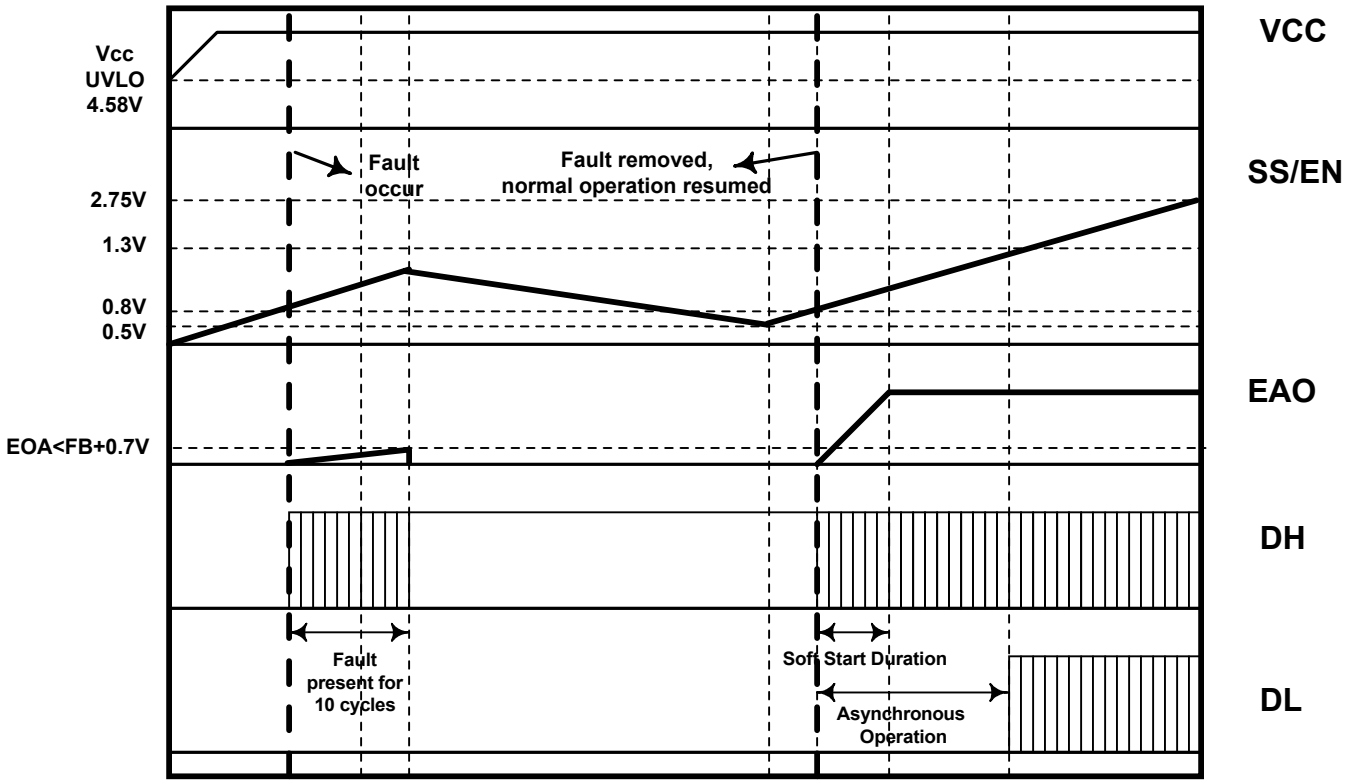
Notes:
(1) Guaranteed by design.
(2) Guaranteed by characterization.

Timing Diagrams

No fault start up sequence

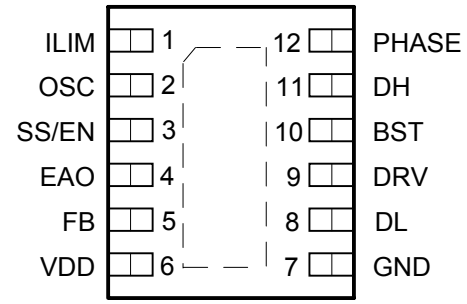


Over current fault at Asynchronous start up sequence



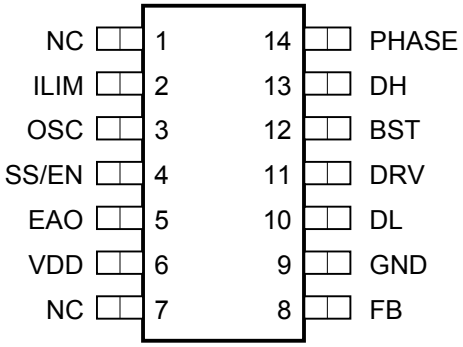
Pin Configurations

TOP VIEW



(12 Pin MLPD)

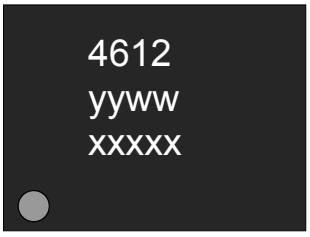
TOP VIEW



(14 Pin SOIC)

Marking Information

Top Mark



nnnn = Part Number (Example: 1531)
yyww = Date Code (Example: 0012)
xxxxx = Semtech Lot No. (Example:E9010)

Ordering Information

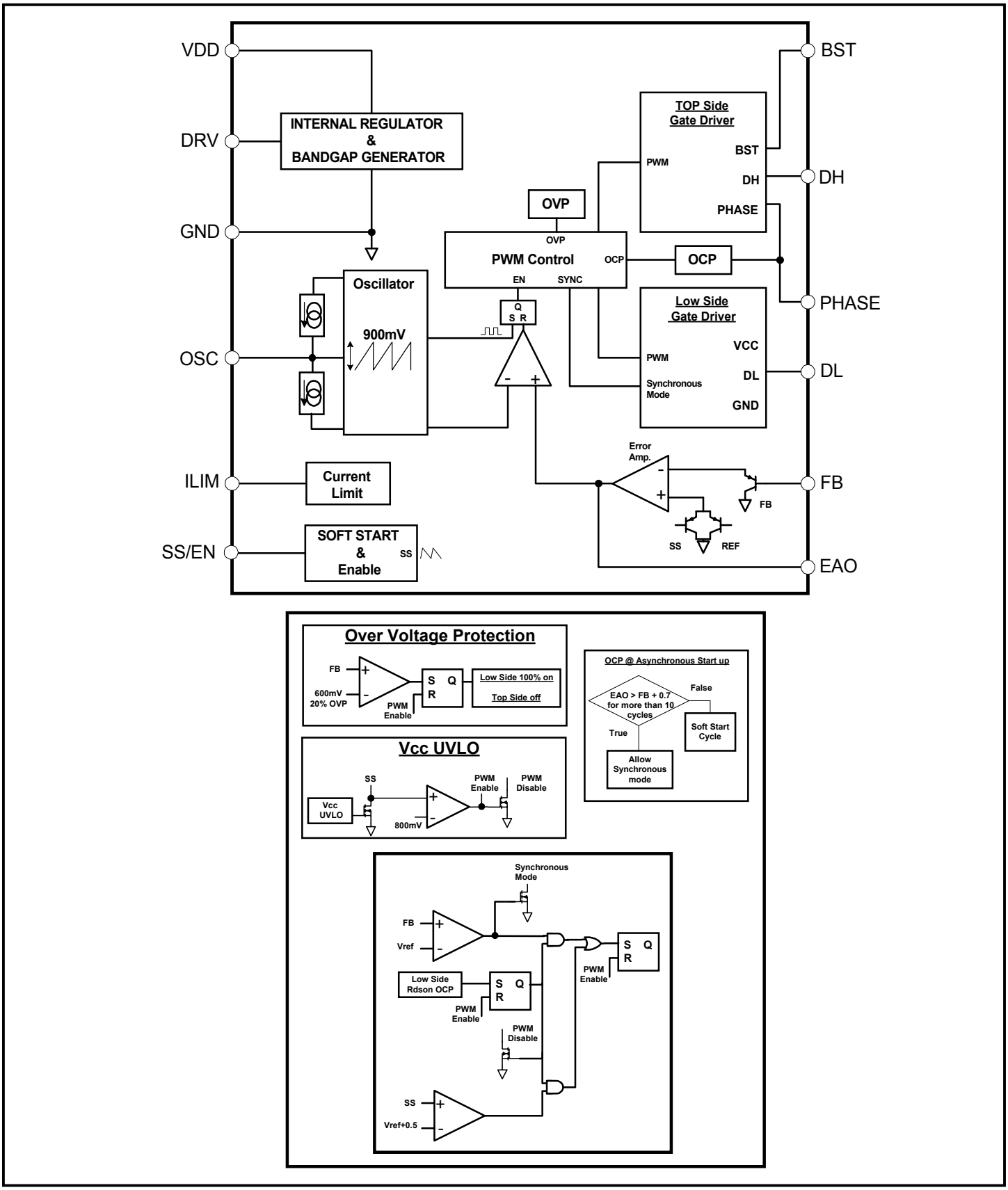
Part Number[3]	Package[2]	Temp. Range (T_J)
SC4612MLTRT	MLPD-12	-40°C to +125°C
SC4612STRT	SOIC-14	
SC4612EVB[1]	EVALUATION BOARD	

Notes:
(1) When ordering please specify MLPD or SOIC package.
(2) Only available in tape and reel packaging. A reel contains 2500 devices.
(3) Lead-free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin # MLPD	Pin# SOIC	Pin Name	Pin Function
	1, 7	NC	No connection.
1	2	ILIM	The current limit programing resistors (R2 & R3) in conjunction with an internal current source, program the current limit threshold for the low side MOSFET RDS-ON sensing. Once the voltage drop across the Low side MOSFET is larger than the drop across the programmed value, current limit condition occurs, and the hiccup current limit protection is activated.
2	3	OSC	Oscillator Frequency set pin. An external capacitor to GND will program the oscillator frequency. See Table "Frequency vs. C_{OSC}" on page 14 to determine oscillator frequency.
3	4	SS/EN	Soft start pin. Internal current source connected to a single external capacitor will determine the soft-start duration for the output. Inhibits the chip if pulled down. $T_{SS} \approx \frac{C_{SS} X 1.2}{I_{SS}}$
4	5	EAO	Error Amplifier output. A compensation network is connected from this pin to FB.
5	8	FB	The inverting input of the error amplifier. Feedback pin is used to sense the output voltage via a resistive divider.
6	6	VDD	Bias supply ranging from 4.5V to 28V, VDD pin is initially used to provide the base drive to the internal pass transistor to regulate the DRV.
7	9	GND	Ground.
8	10	DL	DL signal (Drive Low). Gate drive for bottom MOSFET.
9	11	DRV	DRV supplies the output MOSFETs gate drive, and the chip analog circuitry. This pin should be bypassed with a 2.2µF ceramic capacitor to GND. DRV is internally regulated from the external supply connected to VDD. If VDD is below 10V , the supply could be directly connected to the DRV pin.
10	12	BST	BST signal. Supply for high side driver; can be directly connected to an external supply or to a bootstrap circuit.
11	13	DH	DH signal (Drive High). Gate drive for top MOSFET.
12	14	PHASE	The return path for the high side gate drive, also used to sense the voltage at the phase node for adaptive gate drive protection, and the low-side RDS-ON voltage sensing.
X	-	THERMAL PAD (GND)	Pad for heatsinking purposes. Connect to ground plane using multiple vias.

Block Diagram



INTRODUCTION

The SC4612 is a versatile voltage mode synchronous rectified buck PWM convertor, with an input supply (VIN) ranging from 4.5V to 28V designed to control and drive N-channel MOSFETs.
The power dissipation is controlled using a novel low voltage supply technique, allowing high speed and integration with the high drive currents to ensure low MOSFET switching loss. The synchronous buck configuration also allows converter sinking current from load without losing output regulation.

The internal reference is trimmed to 500mV with ± 1% accuracy, and the output voltage can be adjusted by two external resistors.

A fixed oscillator frequency (up to 1.2MHz) can be programmed by an external capacitor for an optimized design.
During the Asynchronous start up, the SC4612 provides a top MOSFET shut down over current protection, while under normal operating conditions a low side MOSFET R_{DS-ON} current sensing with hiccup mode over current protection, minimizes power dissipation and provides further protection.
Other features of the SC4612 include:

Wide input power voltage range (from 4.5V to 28V), low output voltages down to 500mV, externally programmable soft-start, hiccup over current protection, wide duty cycle range, thermal shutdown, asynchronous start-up protection, and a -40 to 125°C junction operating temperature range.

THEORY OF OPERATION

SUPPLIES

Two pins (VDD and DRV) are used to power up the SC4612. If input supply (VDD) is less than 10V (MAX), tie DRV and VDD together.

This supply should be bypassed with a low ESR 2.2uF (or greater) ceramic capacitor directly at the DRV to GND pins of the SC4612.

The DRV supply also provides the bias for the low and the high side MOSFET gate drive.

The maximum rating for DRV supply is 10V and for applications where input supply is below 10V, it may be connected directly to VDD.

START UP SEQUENCE

Start up is inhibited until VDD input reaches its UVLO threshold. The UVLO limit is 4.5V (TYP).
Meanwhile, the high side and low side gate drivers DH, and DL, are kept low. Once VDD exceeds the UVLO threshold, the external soft-start capacitor starts to be charged by a 25µA current source. If an over current condition occurs, the SS/EN pin will discharge to 500mV by an internal switch. During this time, both DH and DL will be turned off.

When the SS pin reaches 0.8V, the converter will start switching. The reference input of the error amplifier is ramped up with the soft-start signal. Initially only the high side driver is enabled. Keeping the low side MOSFET off during start up is useful where multiple convertors are operating in parallel. It prevents forward conduction in the freewheeling MOSFET which might otherwise cause a dip in the common output bus.

In case of over current condition which is longer than 10 cycles during the asynchronous start up, SC4612 will turn off the high side MOSFET gate drive, and the soft-start sequence will repeat.
When the SS pin reaches 1.3V, the low side MOSFET will begin to switch and the convertor is fully operational in the synchronous mode. The soft-start duration is controlled by the value of the SS cap. If the SS pin is pulled below 0.5V, the SC4612 is disabled and draws a typical quiescent current of 5mA.

Bias Generation

A 4.5V to 10V (MAX) supply voltage is required to power up the SC4612. This voltage could be provided by an external power supply or derived from VDD (VDD >10V) through an internal pass transistor.

The internal pass transistor will regulate the DRV from an external supply >10V connected to VDD to produce 7.8V (TYP) at the DRV pin.

Soft start / Shut down

An external capacitor at the SS/EN pin is used to set up the soft-start duration. The capacitor value in conjunction with the internal current source, controls the duration of soft-start time. If the SS/EN pin is pulled down to GND, the SC4612 is disabled. The soft-start pin is charged by a 25µA current source and discharged by an internal switch. When SS/EN is released it charges up to 0.5V as the control circuit starts up.

Applications Information (Cont.)

The reference input of the error amplifier is effectively ramped up with the soft-start signal. The error amp output will vary between 100mV and 1.2V, depending on the duty cycle. The error amp will be off until SS/EN reaches 0.7V (TYP) and will move the output up to its desired voltage by the time SS/EN reaches 1.3V. The gate drivers will be in asynchronous mode until the FB pin reaches 500mV.

The intention for the asynchronous start up is to keep the low side MOSFET from being switched on which forces the low side MOSFETs body diode or the parallel Schottky diode to conduct. The conduction by the diode prevents any dips in an existing output voltage that might be present, allowing for a glitch free start up in applications that are sensitive to any bus disturbances.

During the asynchronous start up SC4612 monitors the output and if within 10 cycles the FB has not reached the internal soft start ramp level, the device switches to synchronous mode. This provides an added protection in case of short circuit at the output during the asynchronous start when the bottom MOSFET is not being switched to provide the R_{DS-ON} sensing current limit protection.

In case of a current limit, the gate drives will be held off until the soft-start is initiated. The soft-start cycle defined by the SS cap being charged from 800mV to 1.3V and slowly discharged to achieve an approximate hiccup duty cycle of 1% to minimize excessive power dissipation.

The part will try to restart on the next softstart cycle. If the fault has cleared, the outputs will start . If the fault still remains, the part will repeat the soft-start cycle above indefinitely until the fault has been removed.

The soft-start time is determined by the value of the softstart capacitor (see formula below).

$$T_{SS} \approx \frac{C_{SS} \times 1.2}{I_{SS}}$$

Oscillator Frequency Selection

The internal oscillator sawtooth signal is generated by charging an external capacitor with a current source of 100µA charge current.

See Table 1 “Frequency vs. C_{OSC}” on page 14 to determine oscillator frequency.

OVERCURRENT PROTECTION

SC4612 features low side MOSFET on-state Rds current sensing and hiccup mode over current protection. ILIM pin would be connected to DRV or PHASE via programming resistors to adjust the over current trip point to meet different customer requirements.

The sampling of the current thru the bottom FET is set at ~150ns after the bottom FET drive comes ON. It is done to prevent a false tripping of the current limit circuit due to the ringing at the phase node when the top FET is turned OFF.

Internally overcurrent threshold is set to 100mV_typ. If voltage magnitude at the phase node during sampling is such that the current comparator meets this condition then the OCP occurs.

Connecting a resistor from external voltage source such as VDD, DRV, etc. to ILIM increases the current limit. Connecting a resistor from ILIM to PHASE lowers the current limit (see the block diagram in page 9).

Internal current source at ILIM node is ~20µA. External programming resistors add to or subtract from that source and hence vary the threshold.

The tolerance of the collective current sink at ILIM node is fairly loose when combined with variations of the FET’s Rds(on). Therefore when setting current limit some iteration might be required to get to the wanted trip point. Nonetheless, this circuit does serve the purpose of a hard fault protection of the power switches. When choosing the current limit one should consider the cumulative effect of the load and inductor ripple current. As a rule of thumb, the limit should be set at least x10 greater then the pk-pk ripple current. Whenever a high current peak is detected, SC4612 would first block the driving of the high side and low side MOSFET, and then discharge the soft-start capacitor. Discharge rate of the SS capacitor is 1/25 of the charge rate.

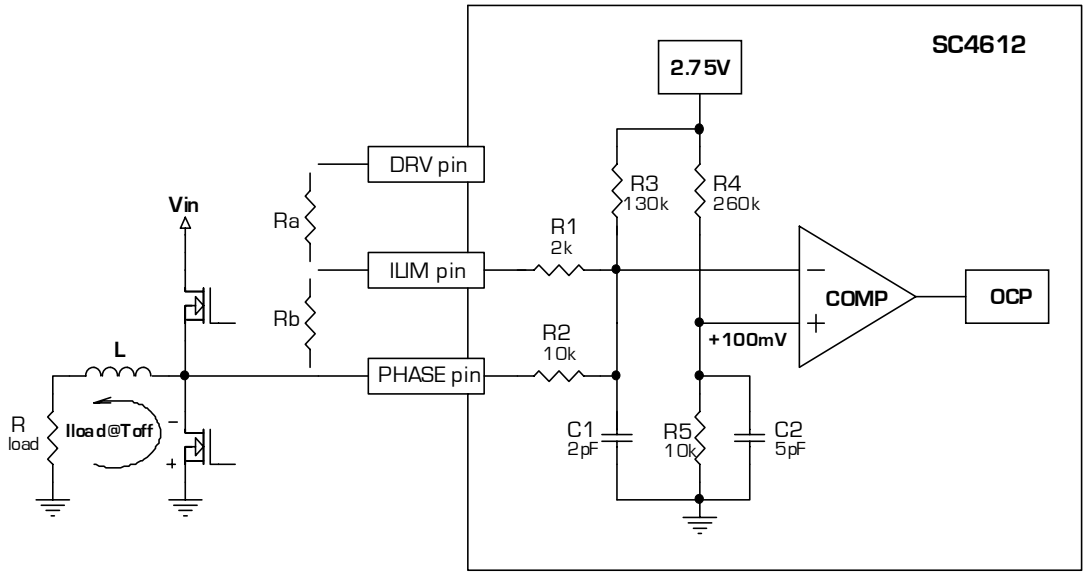
Under Voltage Lock Out

Under Voltage Lock Out (UVLO) circuitry senses the VDD through a voltage divider. If this signal falls below 4.5V (typical) with a 400mV hysteresis (typical), the output drivers are disabled . During the thermal shutdown, the output drivers are disabled.

Applications Information (Cont.)

Below are examples of calculating the OCP trip voltages.

Low Side R_{DS_ON} Current Limit



1. Ra, Rb - Not installed:

$$\frac{2.75V - 100mV}{R3} = \frac{100mV - Vphase}{R2}$$

solving for: V_{PHASE} = -100mV, therefore the circuit will trip @ R_{DS_ON} x I_{LOAD} = 100mV

2. To lower trip voltage - install Rb. For example: Rb = 8k

$$\frac{2.75V - 100mV}{R3} = \frac{100mV - Vphase}{R2 \,||\, (Rb + R1)}$$

solving for: V_{PHASE} = -20mV, obviously more sensitive! R_{DS_ON} x I_{LOAD} = 20mV

3. To increase trip voltage - install Ra. For example: Ra = 800k; V_{DRIVE} = 7.8V typ.

$$\frac{2.75V - 100mV}{R3} + \frac{Vdrive}{Ra + R1} = \frac{100mV - Vphase}{R2}$$

solving for: V_{PHASE} = -200mV. Current limit has doubled compared to original conditions.

NOTE! Allow for tempco and R_{DS_ON} variation of the MOSFET - see “overcurrent protection” information on page 11 in the datasheet.

Applications Information (Cont.)

Gate Drive/Control

The SC4612 also provides integrated high current gate drives for fast switching of large MOSFETs. The high side and low side MOSFET gates could be switched with a peak gate current of 1.7A. The higher gate current will reduce switching losses of the larger MOSFETs.

The low side gate drives are supplied directly from the DRV. The high side gate drives could be provided with the classical bootstrapping technique from DRV.

Cross conduction prevention circuitry ensures a non overlapping (30ns typical) gate drive between the top and bottom MOSFETs. This prevents shoot through losses which provides higher efficiency. Typical total minimum off time for the SC4612 is about 30ns which will cause the maximum duty cycle at higher frequencies to be limited to lower than 100%.

OVERVOLTAGE PROTECTION

If the FB pin ever exceeds 600mV, the top side driver is latched OFF, and the low side driver is latched ON. This mode can only be reset by power supply cycling.

ERROR AMPLIFIER DESIGN

The SC4612 is a voltage mode buck controller that utilizes an externally compensated high bandwidth error amplifier to regulate output voltage. The power stage of the synchronous rectified buck converter control-to-output transfer function is as shown below:

$$G_{VD}(s) = \frac{V_{IN}}{V_S} \times \left(\frac{1 + sESR_C C}{1 + s\frac{L}{R_L} + s^2 LC} \right)$$

where,

V_{IN} – Input voltage

R_L – Load resistance

L – Output inductance

C – Output capacitance

ESR_C – Output capacitor ESR

V_S – Peak to peak ramp voltage

The classical Type III compensation network can be built around the error amplifier as shown below:

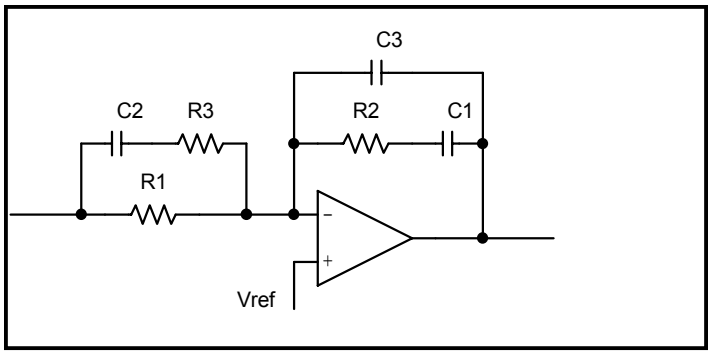


Figure 1. Voltage mode buck converter compensation network

The transfer function of the compensation network is as follows:

$$G_{COMP}(s) = \frac{\omega_I}{s} \cdot \frac{(1 + \frac{s}{\omega_{Z1}})(1 + \frac{s}{\omega_{Z2}})}{(1 + \frac{s}{\omega_{P1}})(1 + \frac{s}{\omega_{P2}})}$$

where,

$$\omega_{Z1} = \frac{1}{R_2 C_1}, \quad \omega_{Z2} = \frac{1}{(R_1 + R_3)C_2}, \quad \omega_o = \frac{1}{\sqrt{Lout \times Cout}}$$

$$\omega_I = \frac{1}{R_1(C_1 + C_3)}, \quad \omega_{P1} = \frac{1}{R_3 C_2}, \quad \omega_{P2} = \frac{1}{R_2 \frac{C_1 C_3}{C_1 + C_3}}$$

Application Information (Cont.)

The design guidelines are as following:

1. Set the loop gain crossover frequency w_C for given switching frequency.

2. Place an integrator at the origin to increase DC and low frequency gains.

3. Select w_{Z1} and w_{Z2} such that they are placed near w_0 to dampen peaking; the loop gain should cross 0dB at a rate of -20dB/dec.

4. Cancel w_{ESR} with compensation pole w_{P1} ($w_{P1} = w_{ESR}$).

5. Place a high frequency compensation pole w_{P2} at half the switching frequency to get the maximum attenuation of the switching ripple and the high frequency noise with adequate phase lag at w_C.

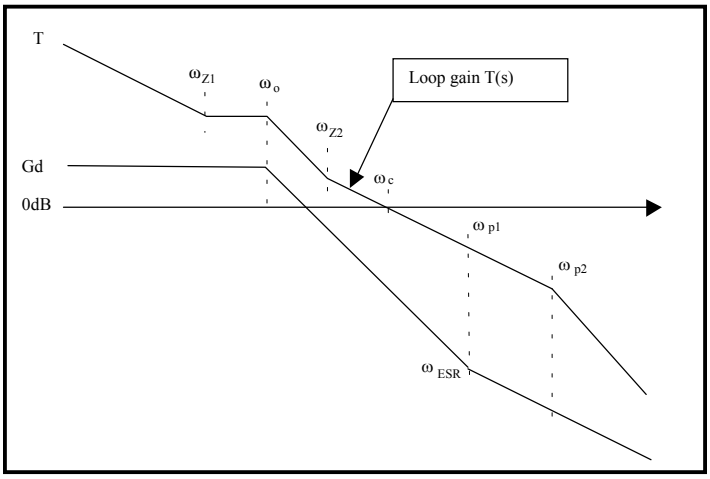


Figure 2. Simplified asymptotic diagram of buck power stage and its compensated loop gain.

Switching Frequency, F_{SW} vs. C_{OSC}.

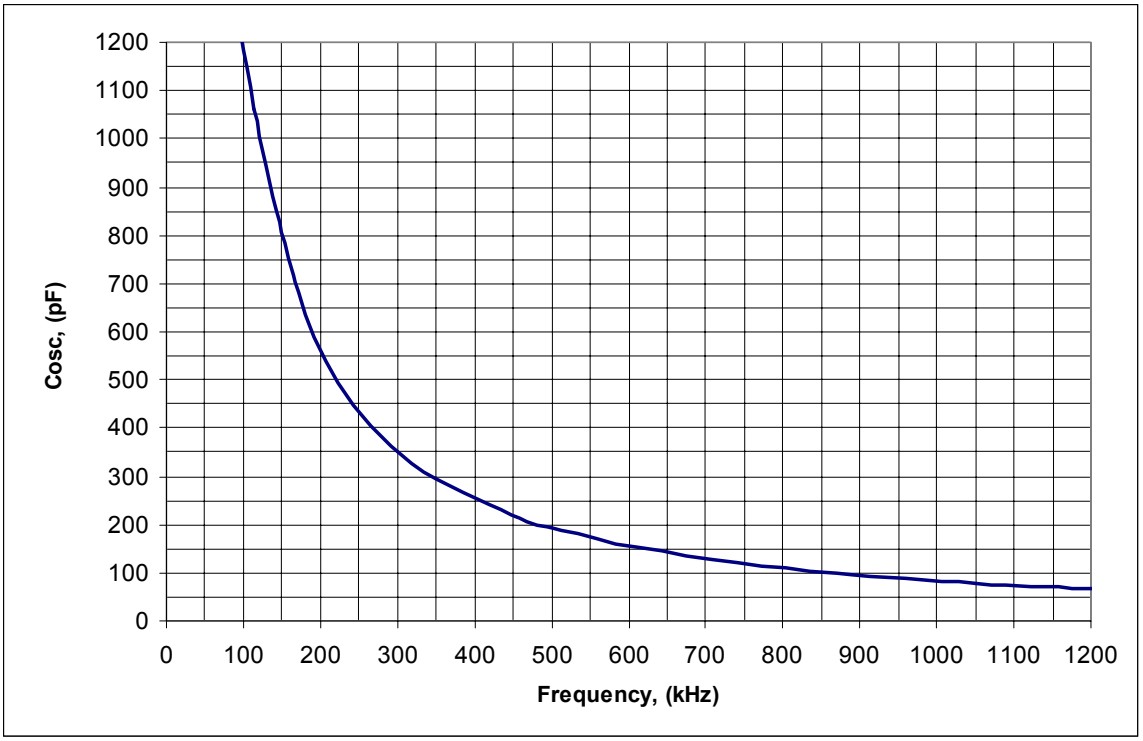


Table 1

Application Information (Cont.)

PCB LAYOUT GUIDELINES

Careful attention to layout is necessary for successful implementation of the SC4612 PWM controller. High switching currents are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1) The high power section of the circuit should be laid out first. A ground plane should be used. The number and position of ground plane interruptions should not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas; for example, the input capacitor and bottom FET ground.

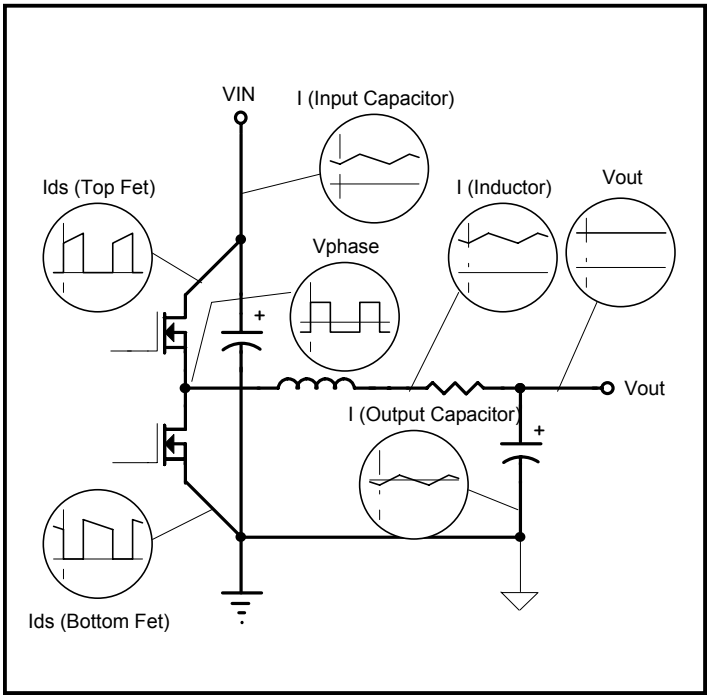
2) The loop formed by the Input Capacitor(s) (Cin), the Top FET (M1), and the Bottom FET (M2) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3) The connection between the junction of M1, M2 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. Also keep the Phase connection to the IC short. Top FET gate charge currents flow in this trace.

4) The Output Capacitor(s) (Cout) should be located as close to the load as possible. Fast transient load currents are supplied by Cout only, and therefore, connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC4612 is best placed over a quiet ground plane area. Avoid pulse currents in the Cin, M1, M2 loop flowing in this area. GND should be returned to the ground plane close to the package and close to the ground side of (one of) the output capacitor(s). If this is not possible, the GND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, M1, M2 loop. Under no circumstances should GND be returned to a ground inside the Cin, M1, M2 loop.

6) Allow adequate heat sinking area for the power components. If multiple layers will be used, provide sufficent vias for heat ransfer



Voltage and current waveforms of buck power stage .

Application Information (Cont.)

COMPONENT SELECTION:

SWITCHING SECTION

OUTPUT CAPACITORS - Selection begins with the most critical component. Because of fast transient load current requirements in modern microprocessor core supplies, the output capacitors must supply all transient load current requirements until the current in the output inductor ramps up to the new level. Output capacitor ESR is therefore one of the most important criteria. The maximum ESR can be simply calculated from:

$$R_{ESR} \leq \frac{V_t}{I_t}$$

Where

V_t = Maximum transient voltage excursion

I_t = Transient current step

For example, to meet a 100mV transient limit with a 10A load step, the output capacitor ESR must be less than 10mΩ. To meet this kind of ESR level, there are three available capacitor technologies.

Technology	Each Capacitor		Qty Rqd.	Total	
	C (uF)	ESR (mΩ)		C (uF)	ESR (mΩ)
Low ESR Tantalum	330	60	6	2000	10
OS-CON	330	25	3	990	8.3
Low ESR Aluminum	1500	44	5	7500	8.8

The choice of which to use is simply a cost/performance issue, with low ESR Aluminum being the cheapest, but taking up the most space.

INDUCTOR - Having decided on a suitable type and value of output capacitor, the maximum allowable value of inductor can be calculated. Too large an inductor will produce a slow current ramp rate and will cause the output capacitor to supply more of the transient load current for longer - leading to an output voltage sag below the ESR excursion calculated above.

The maximum inductor value may be calculated from:

$$L \leq \frac{R_{ESR}\ C}{I_t}(V_{IN} - V_O)$$

The calculated maximum inductor value assumes 100% duty cycle, so some allowance must be made. Choosing an inductor value of 50 to 75% of the calculated maximum will guarantee that the inductor current will ramp fast enough to reduce the voltage dropped across the ESR at a faster rate than the capacitor sags, hence ensuring a good recovery from transient with no additional excursions. We must also be concerned with ripple current in the output inductor and a general rule of thumb has been to allow 10% of maximum output current as ripple current. Note that most of the output voltage ripple is produced by the inductor ripple current flowing in the output capacitor ESR. Ripple current can be calculated from:

$$I_{L_{RIPPLE}} = \frac{V_{IN}}{4 \cdot L \cdot f_{OSC}}$$

Ripple current allowance will define the minimum permitted inductor value.

POWER FETS - The FETs are chosen based on several criteria with probably the most important being power dissipation and power handling capability.

TOP FET - The power dissipation in the top FET is a combination of conduction losses, switching losses and bottom FET body diode recovery losses.

a) Conduction losses are simply calculated as:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot D$$

where

$$D = \text{duty cycle} \approx \frac{V_O}{V_{IN}}$$

b) Switching losses can be estimated by assuming a switching time, If we assume 100ns then:

$$P_{SW} = I_O \cdot V_{IN} \cdot \frac{100ns}{T_{SW}}$$

or more generally,

$$P_{SW} = \frac{I_O \cdot V_{IN} \cdot (t_r + t_f) \cdot f_{OSC}}{2}$$

c) Body diode recovery losses are more difficult to estimate, but to a first approximation, it is reasonable to assume

Application Information (Cont.)

that the stored charge on the bottom FET body diode will be moved through the top FET as it starts to turn on. The resulting power dissipation in the top FET will be:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot f_{OSC}$$

To a first order approximation, it is convenient to only consider conduction losses to determine FET suitability. For a 5V in, 2.8V out at 14.2A requirement, typical FET losses would be:

FET Type	$R_{DS(on)}$ (mΩ)	PD(W)	Package
IRL3402S	15	1.69	D²PAK
IRL2203	10.5	1.19	D²PAK
Si4410	20	2.26	SO-8

Using 1.5X Room temp $R_{DS(ON)}$ to allow for temperature rise.

BOTTOM FET - Bottom FET losses are almost entirely due to conduction. The body diode is forced into conduction at the beginning and end of the bottom switch conduction period, so when the FET turns on and off, there is very little voltage across it resulting in very low switching losses. Conduction losses for the FET can be determined by:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot (1-D)$$

For the example above:

FET Type	$R_{DS(on)}$ (mΩ)	P_D(W)	Package
IRL3402S	15	1.33	D²PAK
IRL2203	10.5	0.93	D²PAK
Si4410	20	1.77	SO-8

Each of the package types has a characteristic thermal impedance, for the TO-220 package, thermal impedance is mostly determined by the heatsink used. For the surface mount packages on double sided FR4, 2 oz printed circuit board material, thermal impedances of 40°C/W for the D²PAK and 80°C/W for the SO-8 are readily achievable. The corresponding temperature rise is detailed below:

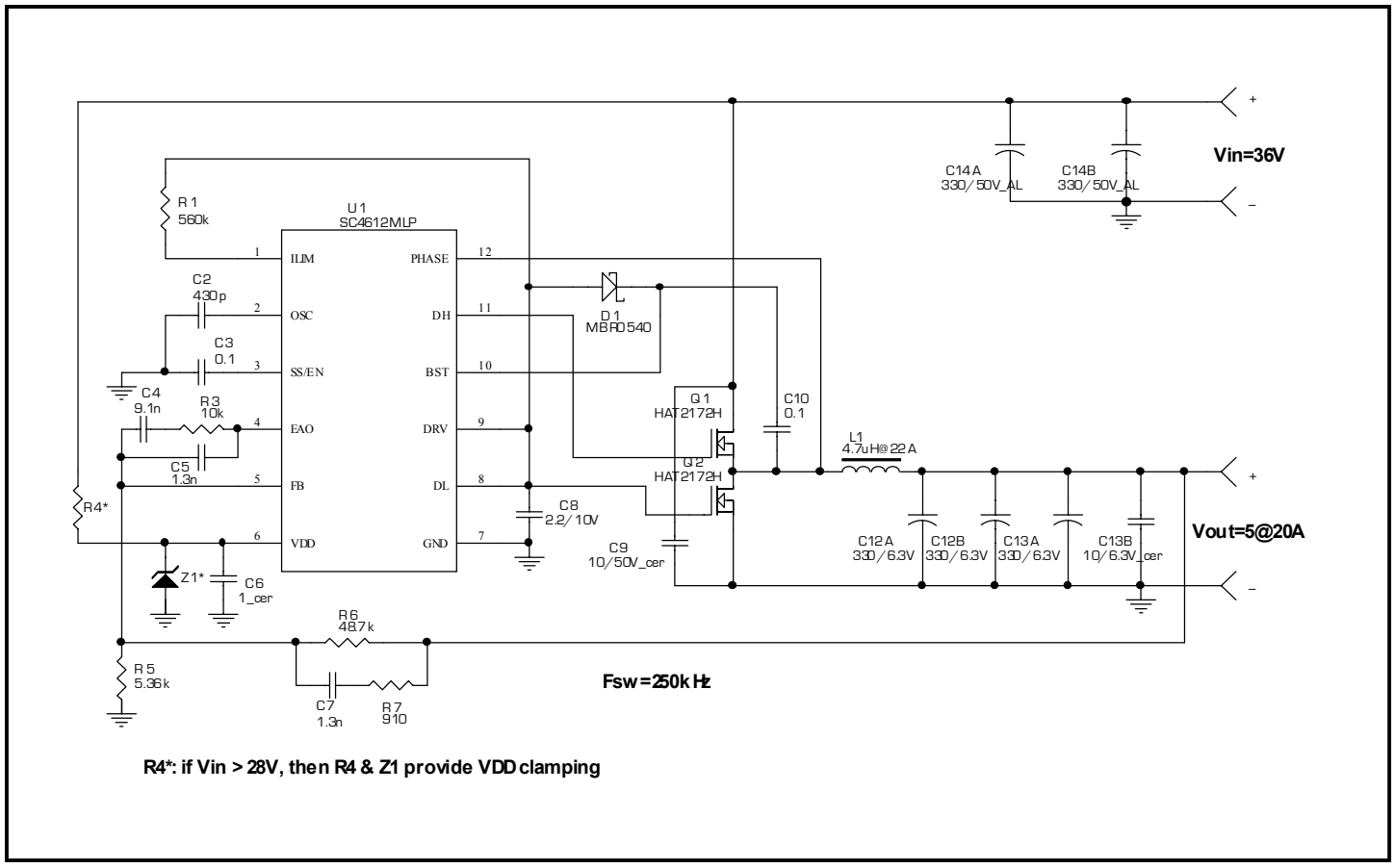
	Temperature rise (°C)	
FET Type	Top FET	Bottom FET
IRL3402S	67.6	53.2
IRL2203	47.6	37.2
Si4410	180.8	141.6

It is apparent that single SO-8 Si4410 are not adequate for this application, By using parallel pairs in each position, power dissipation will be approximately halved and temperature rise reduced by a factor of 4.

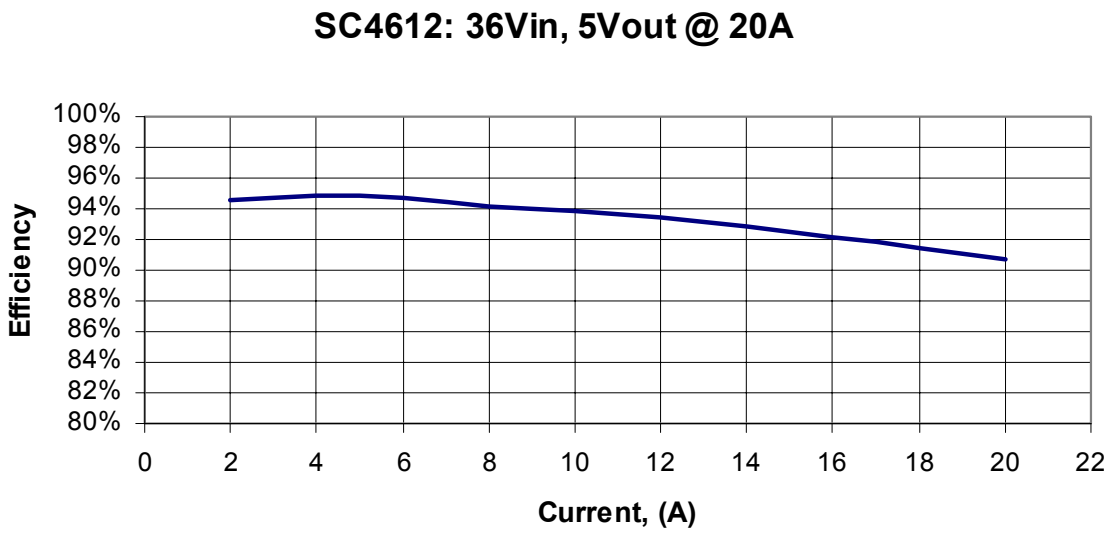
INPUT CAPACITORS - Since the RMS ripple current in the input capacitors may be as high as 50% of the output current, suitable capacitors must be chosen accordingly. Also, during fast load transients, there may be restrictions on input di/dt. These restrictions require useable energy storage within the converter circuitry, either as extra output capacitance or, more usually, additional input capacitors. Choosing low ESR input capacitors will help maximize ripple rating for a given size.

Application Information (Cont.)

Application Circuit 1: Vin = 36V; Vout = 5V @ 20A, Fsw = 250kHz.

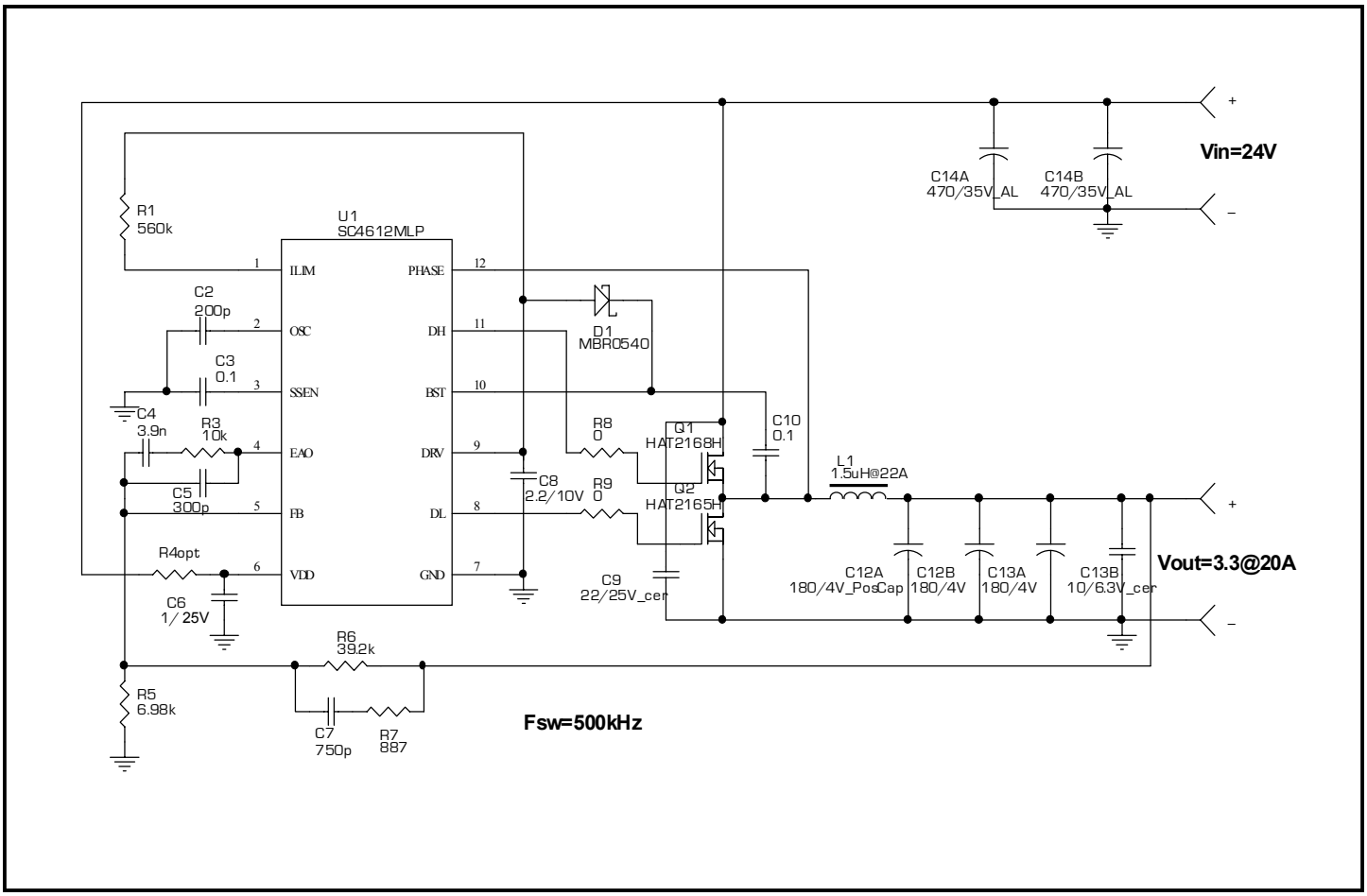


Efficiency:

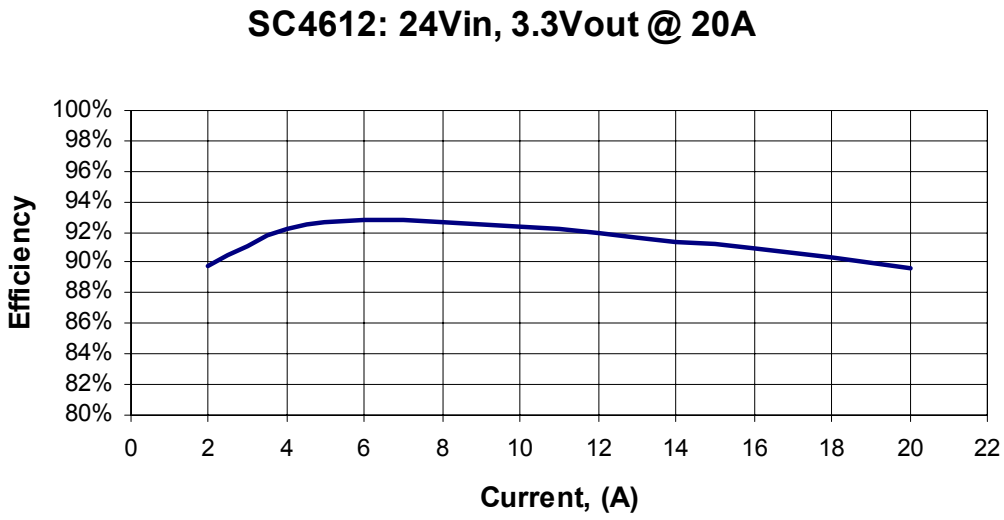


Application Information (Cont.)

Application Circuit 2: Vin = 24V; Vout = 3.3V @ 20A, Fsw = 470kHz.

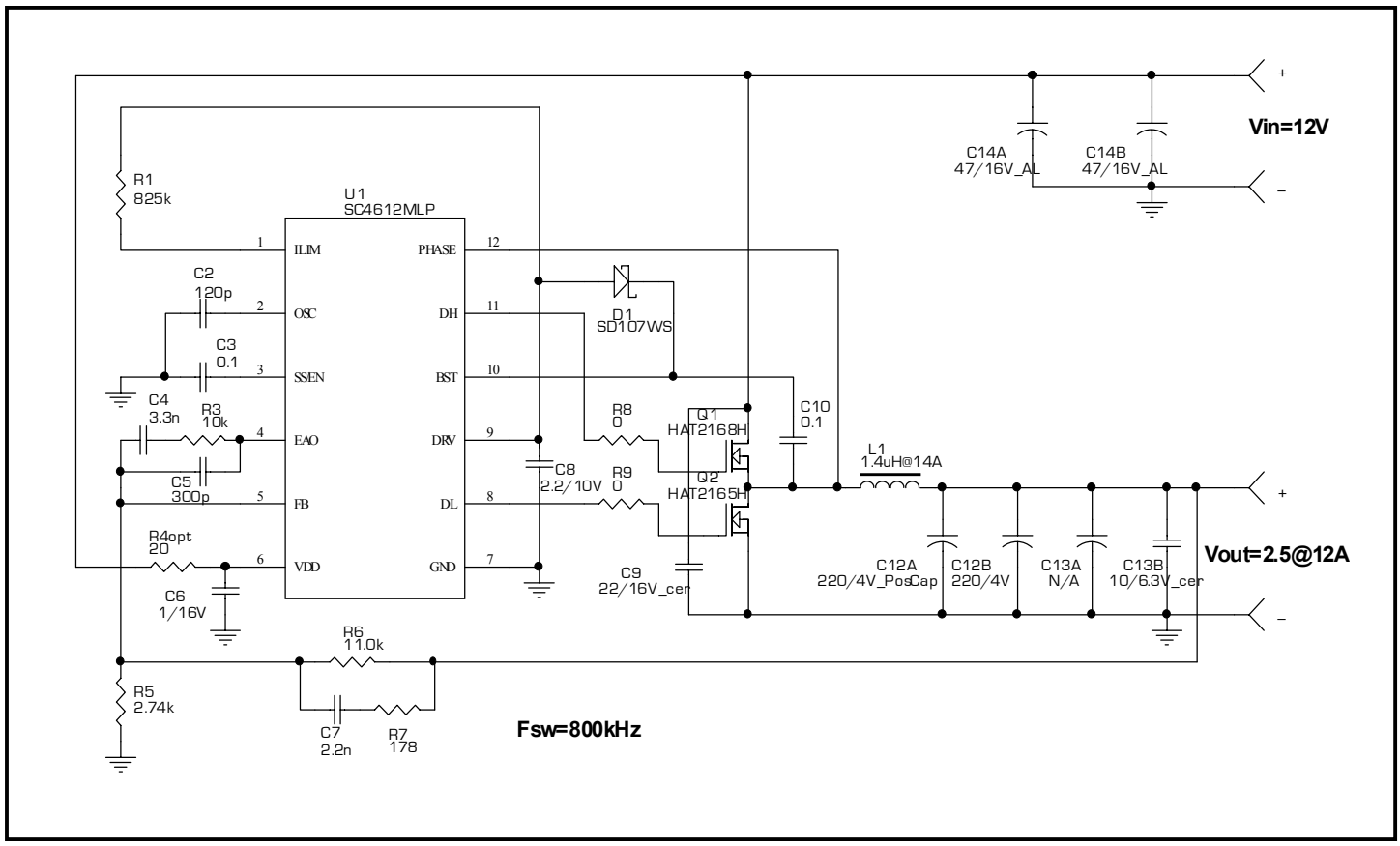


Efficiency:

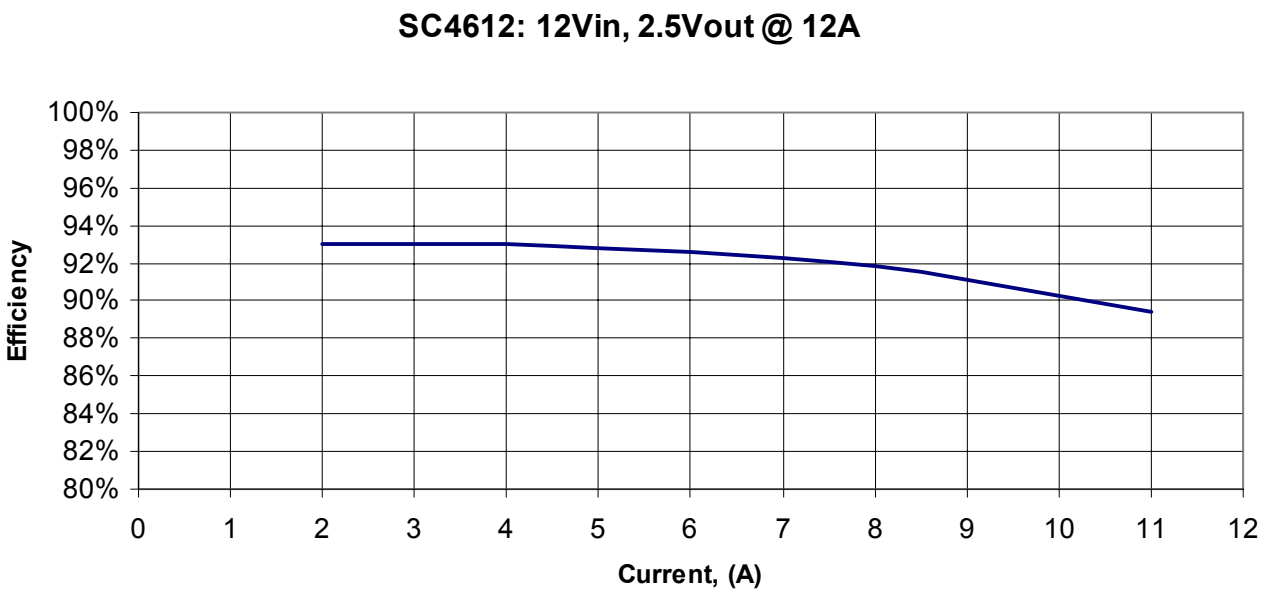


Application Information (Cont.)

Application Circuit 3: Vin = 12V; Vout = 2.5V @ 12A, Fsw = 770kHz

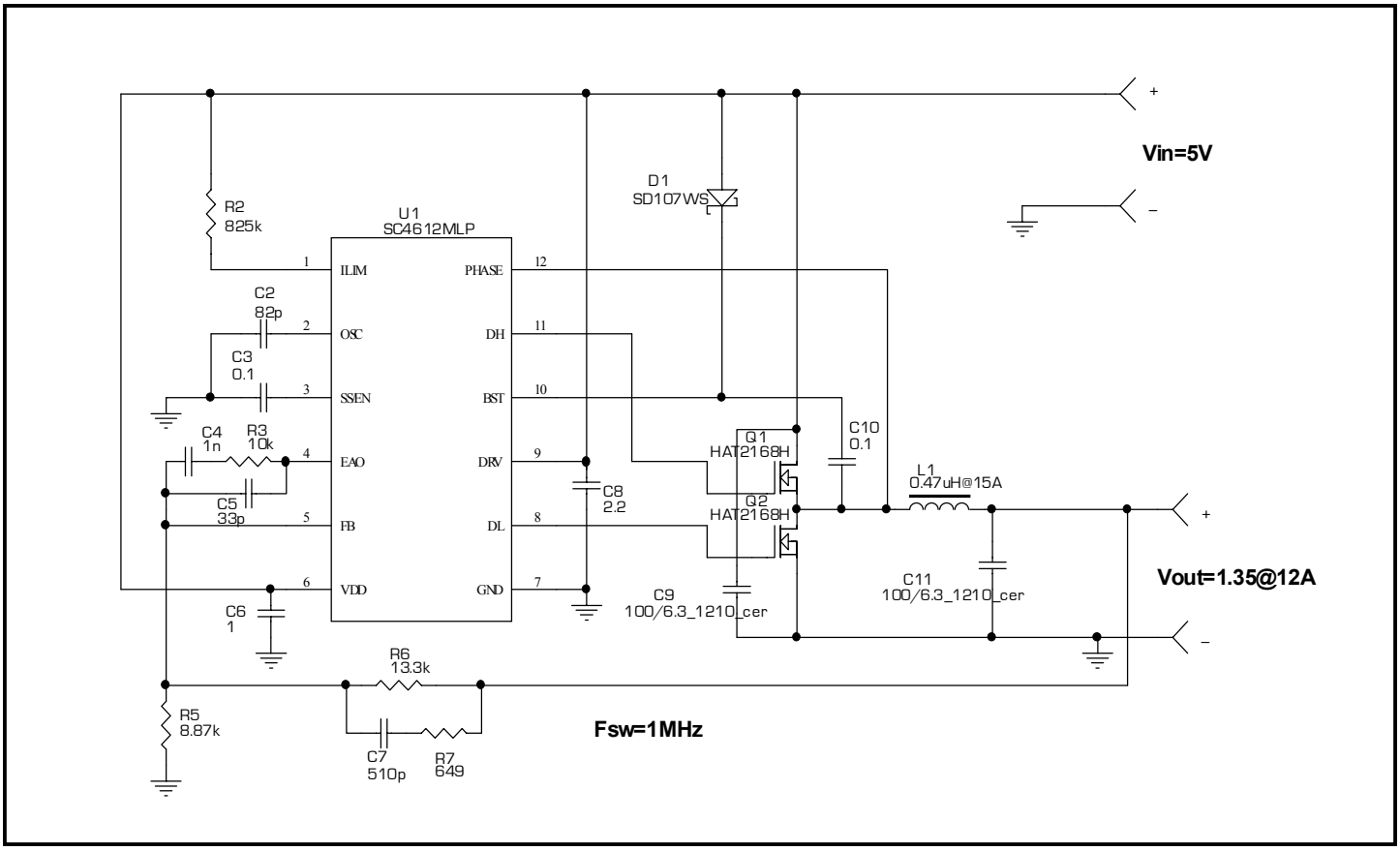


Efficiency:

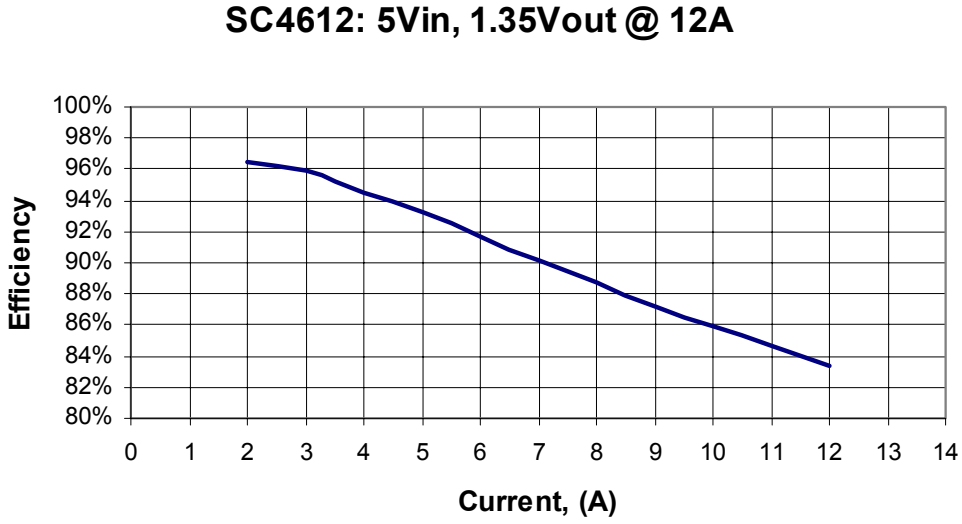


Application Information (Cont.)

Application Circuit 4: Vin = 5V; Vout = 1.35V @ 12A, Fsw = 960kHz.

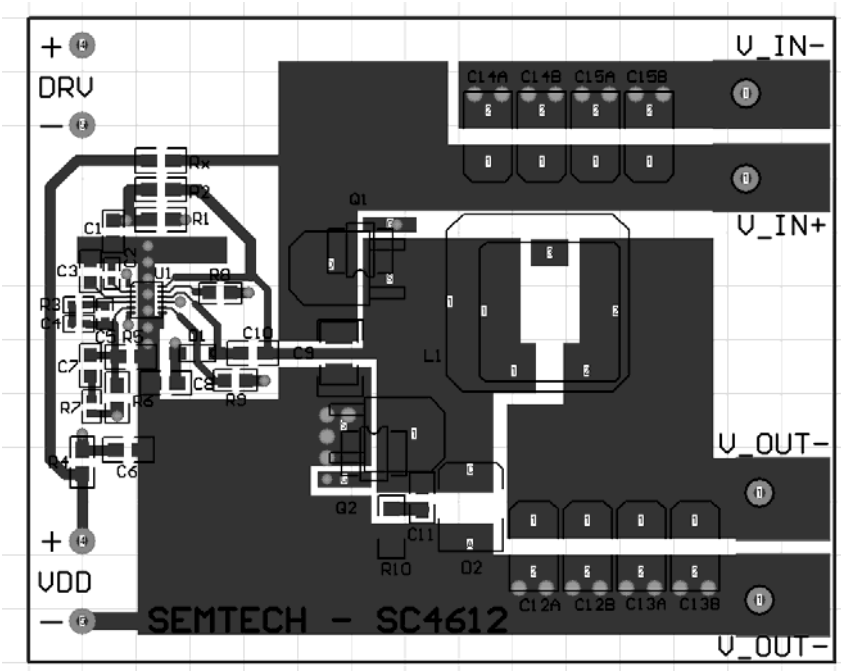


Efficiency:

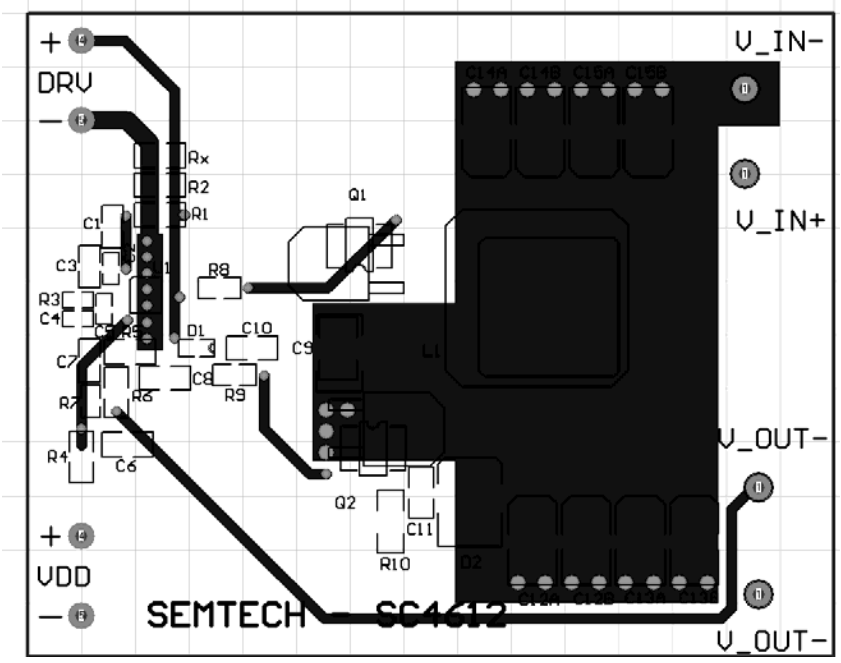


Evaluation Board 1:

Top layer and components view

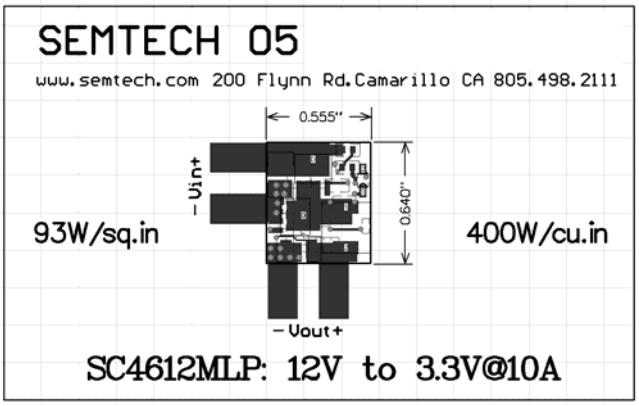


Bottom Layer:

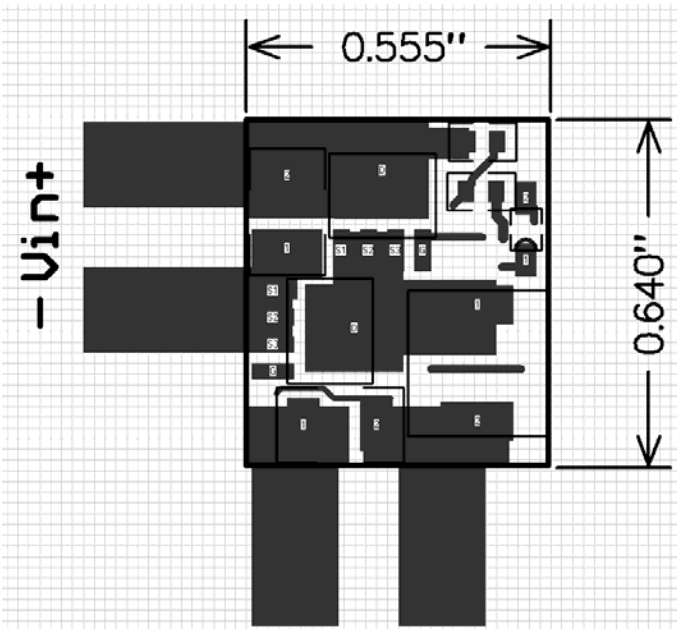


Application Information (Cont.)

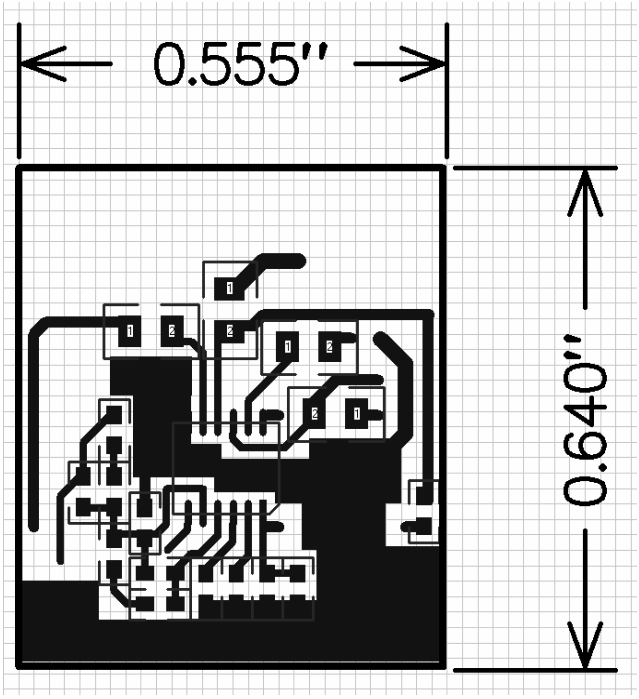
Evaluation Board 2 (actual size):



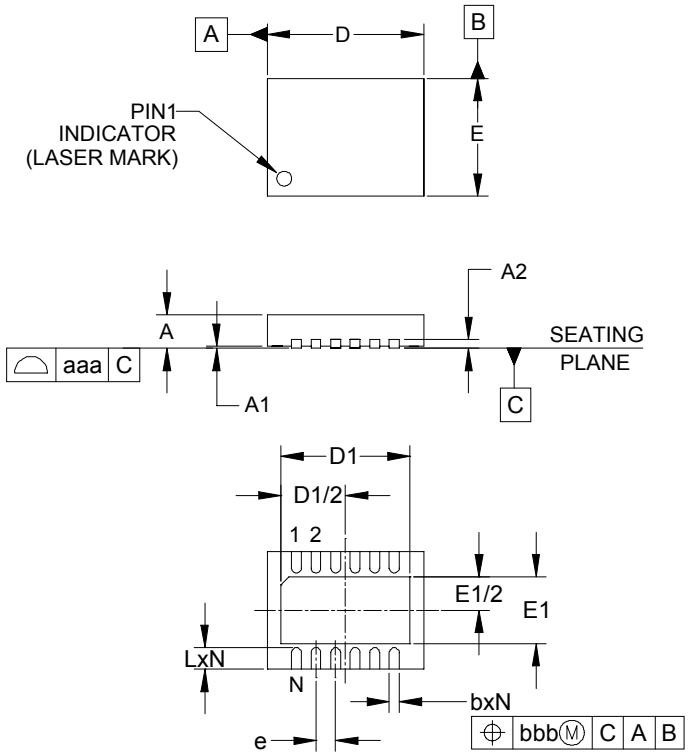
Top layer:



Bottom layer:



Outline Drawing - MLPD - 12

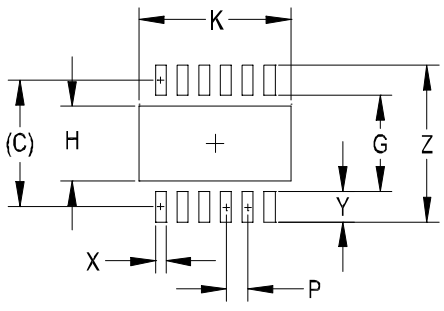


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.040	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.154	.157	.161	3.90	4.00	4.10
D1	.124	.130	.134	3.15	3.30	3.40
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	12			12		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLPD - 12

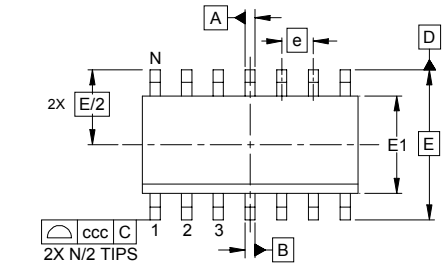


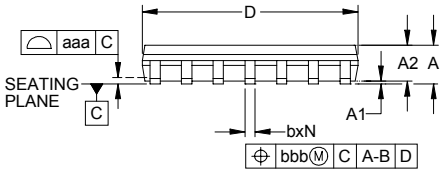
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.087	2.20
H	.067	1.70
K	.138	3.50
P	.020	0.50
X	.012	0.30
Y	.028	0.70
Z	.142	3.60

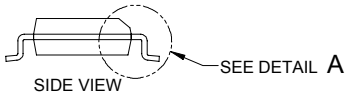
NOTES:

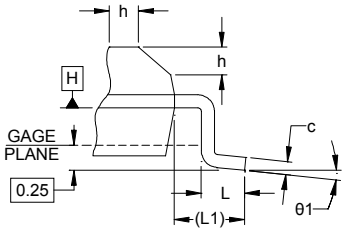
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Outline Drawing - SOIC - 14







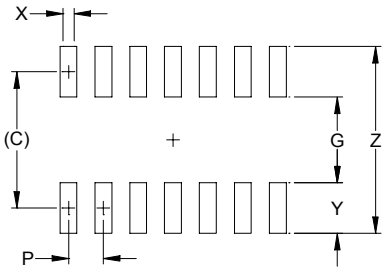


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.337	.341	.344	8.55	8.65	8.75
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	14			14		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AB.

Land Pattern - SOIC - 14



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 302A.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804