BGSX210MA18

DP10T Diversity Cross Switch for Carrier Aggregation

Data Sheet

Revision 3.1 - 2016-11-03

Power Management & Multimarket

Edition 2016-11-03

Published by Infineon Technologies AG
81726 Munich, Germany

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Revision History

Document No.: BGSX210MA18__v3.1.pdf	
Revision History: Rev. v3.1	
Previous Version: 3.0	
Page	**Subjects (major changes since last revision)**
9	RF performance updated in Table 5
13	Application information updated in Table 12

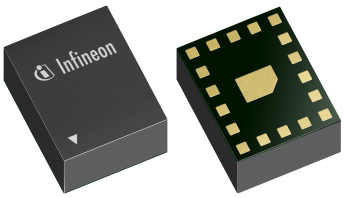
Contents

List of Figures

List of Tables

BGSX210MA18 DP10T Diversity Cross Switch for Carrier Aggregation

1 Features



- RF CMOS DP10T diversity switch with power handling capability of up to 27 dBm
- Industry's first flexible carrier aggregation switch via cross switch functionality of two ports
- Device configurations SP5T/SP5T, SP4T/SP6T, and SP6T/SP4T featured via cross switch functionality
- Suitable for LTE carrier aggregation applications
- Ultra-low insertion loss and harmonics generation
- 0.1 to 3.8 GHz coverage
- High port-to-port-isolation
- No decoupling capacitors required if no DC applied on RF lines
- Integrated MIPI RFFE interface operating in 1.1 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- Leadless and halogen free package ATSLP-18 with lateral size of 2.0 mm x 2.4 mm and thickness of 0.6 mm
- No power supply blocking required
- High EMI robustness
- RoHS and WEEE compliant package

RoHS

2 Product Description

The BGSX210MA18 RF CMOS switch is specifically designed for LTE carrier aggregation applications. This DP10T offers low insertion loss and low harmonic generation. In addition, two ports feature cross functionality enabling higher flexibility for carrier aggregation applications.

The switch is controlled via a MIPI RFFE controller. The on-chip controller allows power-supply voltages from 1.1 to 1.95 V. The switch features direct-connect-to-battery functionality and DC-free RF ports. Unlike GaAs technology, external DC blocking capacitors at the RF Ports are only required if DC voltage is applied externally. The BGSX210MA18 RF Switch is manufactured in Infineon's patented MOS technology, offering the performance of GaAs with the economy and integration of conventional CMOS including the inherent higher ESD robustness. The device has a very small size of only 2.0 x 2.4 mm^2 and a maximum thickness of 0.6 mm.

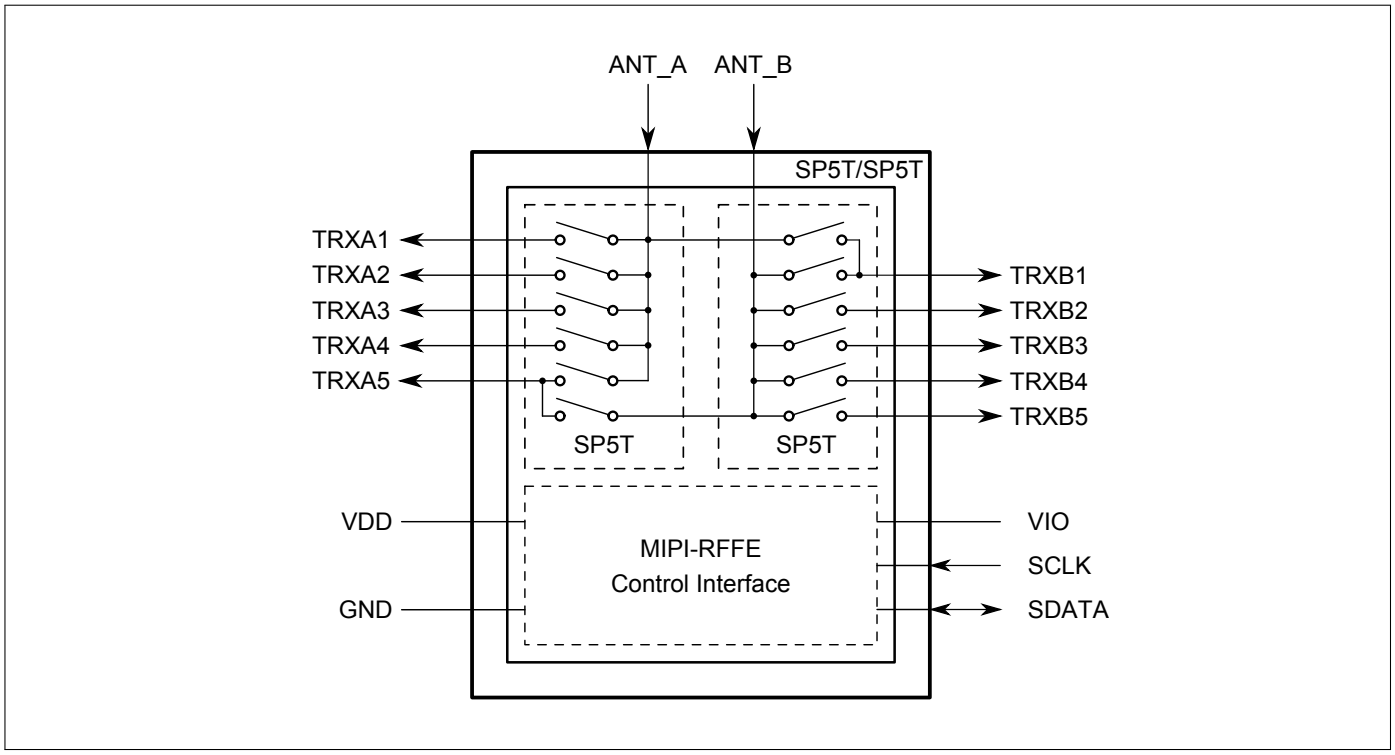


Figure 1: BGSX210MA18 Block diagram

3 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.1	–	3.8	GHz	[1]
Supply voltage	V_{DD}	-0.5	–	3.6	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–
RF input power at all TRX ports	P_{RF}	–	–	32	dBm	CW
ESD capability, HBM[2]	$V_{ESD_{HBM}}$	-1	–	+1	kV	
ESD capability, system level[3]	$V_{ESD_{ANT}}$	-8	–	+8	kV	ANT versus system GND, with 27 nH shunt inductor

[1] Switch has no highpass response. There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] ANSI/ESDA/JEDEC JS-001-2012 (R=1.5 kΩ, C=100 pF).
[3] IEC 61000-4-2 (R=330 Ω, C=150 pF), contact discharge.

Table 2: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
RFFE Supply Voltage	V_{IO}	-0.5	–	3.6	V	–
RFFE Control Voltage Levels	V_{SCLK}, V_{SDATA}	-0.7	–	V_{IO}+0.7 (max. 3.6)	V	–

4 Operation Ranges

Table 3: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	2.5	–	3.4	V	–
Supply current[2]	I_{DD}	–	90	200	µA	–
Supply current in standby mode[2]	I_{DD}	–	0.5	1	µA	VIO=low or MIPI low-power mode
RFFE supply voltage	V_{IO}	1.1	1.8	1.95	V	–
RFFE input high voltage[1]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	15	–	µA	Idle State
Ambient temperature	T_A	-30	25	85	°C	–

[1] SCLK and SDATA
[2] T_A = –30 °C ... 85 °C, V_{DD} = 2.5 ... 3.4 V

Table 4: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TRX ports (50 Ω)	P_{RF}	–	–	27	dBm	–

5 RF Characteristics

Table 5: RF Characteristics at T_A = –30 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{DD}= 2.5 V...3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1]						
All TRX ports	IL	–	0.30	0.45	dB	100 to 960MHz
		–	0.45	0.75	dB	960 to 2170MHz
		–	0.65	0.90	dB	2170 to 2700MHz[2]
		–	0.90	1.35	dB	3400 to 3800MHz[3]
Insertion Loss						
All TRX ports	IL	–	0.30	0.50	dB	100 to 960MHz
		–	0.45	0.85	dB	960 to 2170MHz
		–	0.65	1.00	dB	2170 to 2700MHz[2]
		–	0.90	1.45	dB	3400 to 3800MHz[3]
Return Loss						
All TRX ports	RL	17	24	–	dB	100 to 960MHz
		14	21	–	dB	960 to 2170MHz
		12	16	–	dB	2170 to 2700MHz[2]
		10	15	–	dB	3400 to 3800MHz[3]
Isolation						
Adjacent TRX ports A-A/B-B	ISO	26	36	–	dB	100 to 960MHz
		19	26	–	dB	960 to 2170MHz
		16	21	–	dB	2170 to 2700MHz
Opposite TRX ports A-B/B-A	ISO	38	48	–	dB	100 to 960MHz
		31	41	–	dB	960 to 2170MHz
		29	39	–	dB	2170 to 2700MHz
Harmonic Generation[4]						
All TRX ports, H2	P_{Harm}	80	90	–	dBc	25 dBm, 50 Ω, CW mode
All TRX ports, H3	P_{Harm}	80	90	–	dBc	25 dBm, 50 Ω, CW mode
Intermodulation Distortion in Rx Band[1] [4] (T_A = 25 °C, V_{DD}= 3.0 V)						
IMD2, low	$IMD2_{low}$	–	-105	-100	dBm	Tx = 20 dBm, Interferer = –15 dBm, 50 Ω
IMD3	IMD3	–	-115	-110	dBm	
IMD2, high	$IMD2_{high}$	–	-105	-100	dBm	
Switching Time						
MIPI to RF time[1]	t_{INT}	–	1.5	3	µs	50 % last SCLK falling edge to 90 % ON
Power up settling time[1]	t_{PUP}	–	10	25	µs	After power down mode

[1] Measured at 25°C.
[2] On application board with application circuit according to Fig. 2 and Tab. 12.
[3] On application board with application circuit according to Fig. 2 and Tab. 13.
[4] Measured at Band 5.

6 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011.

Table 6: MIPI Features

Feature	Supported	Comment
Register write command sequence	Yes	
Register read command sequence	Yes	
Extended register write command sequence	No	Up to 4 Bytes
Extented register read command sequence	No	Up to 4 Bytes
Register 0 write command sequence	Yes	
Trigger function	Yes	Trigger assignment to each control register is supported
Programmable USID	Yes	3 register command sequence
Status Register	Yes	Register for debugging
Reset	Yes	By VIO, Power Mode and RFFE_STATUS
Group SID	Yes	
USID_Sel pin	No	External pin for changing USID is not implemented
Full speed write	Yes	
Half speed read	Yes	
Full speed read	Yes	

Table 7: Startup Behavior

Feature	State	Comment
Power status	LOW POWER	The chip is in low power mode after startup
Trigger function	ENABLED	Trigger function is enabled after startup. Trigger function can be disabled via PM_TRIG register.

Table 8: Register Mapping

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x0000	REGISTER_0	7:0	MODE_CTRL	Switch control	00000000	No	Yes	R/W
0x0001	REGISTER_1	7:0	MODE_CTRL	Switch control	00000000	No	Yes	R/W
0x001D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	11100000	No	No	R
0x001E	MANUFACTURER_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R

Continued on next page

Table 8: Register Mapping – Continued from previous page

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x001C	PM_TRIG	7:6	PWR_MODE	00: Normal operation 01: Default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved	10	Yes	No	R/W
		5	TRIGGER_MASK_2	If this bit is set, trigger 2 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 2, the data goes directly to the destination register.	0	No	No	
		4	TRIGGER_MASK_1	If this bit is set, trigger 1 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 1, the data goes directly to the destination register.	0	No	No	
		3	TRIGGER_MASK_0	If this bit is set, trigger 0 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 0, the data goes directly to the destination register.	0	No	No	
		2	TRIGGER_2	A write of a one to this bit loads trigger 2's registers.	0	Yes	No	
		1	TRIGGER_1	A write of a one to this bit loads trigger 1's registers.	0	Yes	No	R/W
		0	TRIGGER_0	A write of a one to this bit loads trigger 0's registers.	0	Yes	No	
0x001F	MAN_USID	7:6	SPARE	These are read-only bits that are reserved and yield a value of 0b00 at readback.	00	No	No	R/W
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	1010			
0x001A	RFFE_STATUS	7	SOFTWARE RESET	0: Normal operation 1: Software reset	0	No	No	R/W
		6	COMMAND_FRAME_ PARITY_ERR	Command sequence received with parity error - discard command.	0	No	No	R
		5	COMMAND_LENGTH_ERR	Command length error	0			
		4	ADDRESS_FRAME_ PARITY_ERR	Address frame parity error = 1	0			
		3	DATA_FRAME_ PARITY_ERR	Data frame with parity error	0			
		2	READ_UNUSED_REG	Read command to an invalid address	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_SID	0			
0x001B	GROUP_SID	7:4	RESERVED		0	No	No	R/W
		3:0	GROUP_SID	Group slave ID	0			

Table 9: Modes of Operation (Truth Table, Switch A)

		REGISTER_1 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	All Isolation	0	0	0	0	0	0	0	0
2	TRXA1	x	x	x	0	0	0	0	1
3	TRXA2	x	x	x	0	0	0	1	0
4	TRXA3	x	x	x	0	0	0	1	1
5	TRXA4	x	x	x	0	0	1	0	0
6	TRXA5	x	x	x	0	0	1	0	1
7	TRXA5+TRXA4	x	x	x	0	1	1	0	0
8	TRXA5+TRXA3	x	x	x	0	1	1	0	1
9	TRXA5+TRXA2	x	x	x	0	1	1	1	0
10	TRXA5+TRXA1	x	x	x	0	1	1	1	1
11	TRXA4+TRXA3	x	x	x	1	0	0	0	0
12	TRXA4+TRXA2	x	x	x	1	0	0	0	1
13	TRXA4+TRXA1	x	x	x	1	0	0	1	0
14	TRXA3+TRXA2	x	x	x	1	0	0	1	1
15	TRXA3+TRXA1	x	x	x	1	0	1	0	0
16	TRXA2+TRXA1	x	x	x	1	0	1	0	1
17-26	All Isolation	0x16 - 0x1F							

Table 10: Modes of Operation (Truth Table, Switch B)

		REGISTER_0 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
27	All Isolation	0	0	0	0	0	0	0	0
28	TRXB1	x	x	x	0	0	0	0	1
29	TRXB2	x	x	x	0	0	0	1	0
30	TRXB3	x	x	x	0	0	0	1	1
31	TRXB4	x	x	x	0	0	1	0	0
32	TRXB5	x	x	x	0	0	1	0	1
33	TRXB5+TRXB4	x	x	x	0	1	1	0	0
34	TRXB5+TRXB3	x	x	x	0	1	1	0	1
35	TRXB5+TRXB2	x	x	x	0	1	1	1	0
36	TRXB5+TRXB1	x	x	x	0	1	1	1	1
37	TRXB4+TRXB3	x	x	x	1	0	0	0	0
38	TRXB4+TRXB2	x	x	x	1	0	0	0	1
39	TRXB4+TRXB1	x	x	x	1	0	0	1	0
40	TRXB3+TRXB2	x	x	x	1	0	0	1	1
41	TRXB3+TRXB1	x	x	x	1	0	1	0	0
42	TRXB2+TRXB1	x	x	x	1	0	1	0	1
43-52	All Isolation	0x16 - 0x1F							

Table 11: Modes of Operation (Truth Table, Cross Ports)

		REGISTER_2 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
53	ANT_A-TRXB1	x	x	x	x	x	x	x	1
54	ANT_B-TRXA5	x	x	x	x	x	x	1	x

7 Application Information

Application Board Configuration

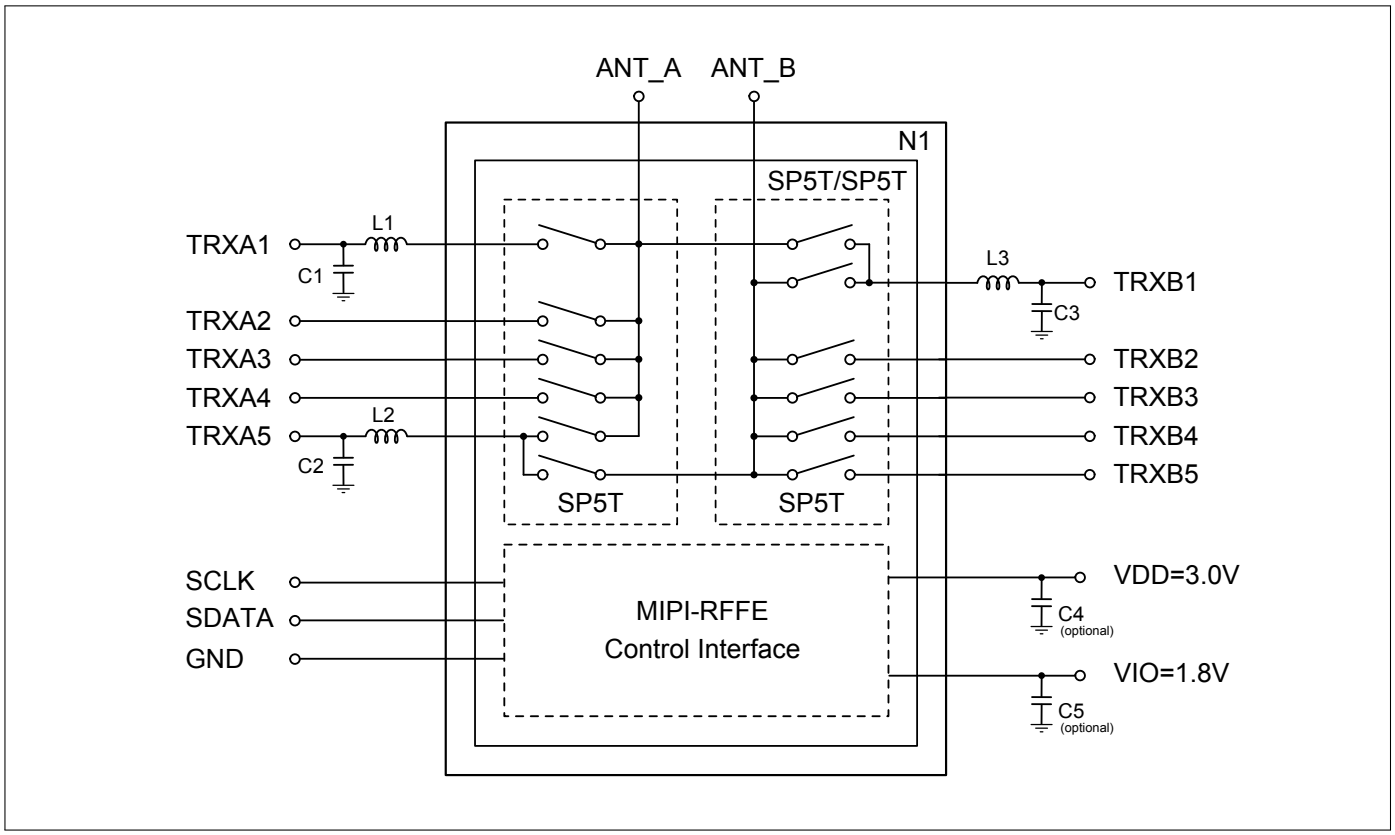


Figure 2: BGSX210MA18 Application Schematic

Table 12: Bill of Materials Table for frequency range 2500 to 2700MHz

Name	Value	Package	Manufacturer	Function
C1=C2=C3	0.8 pF	0402	Various	Impedance Matching
C4=C5 (optional)	1 nF	0402	Various	Impedance Matching
L1=L2=L3	2.1 nH	0402	Various	Impedance Matching
N1	BGSX210MA18	ATSLP-18	Infineon	RF CMOS Switch

Table 13: Bill of Materials Table for frequency range 3400 to 3800MHz

Name	Value	Package	Manufacturer	Function
C1=C2=C3	0.8 pF	0402	Various	Impedance Matching
C4=C5 (optional)	1 nF	0402	Various	Impedance Matching
L1=L2=L3	1 nH	0402	Various	Impedance Matching
N1	BGSX210MA18	ATSLP-18	Infineon	RF CMOS Switch

8 Package Information

Pin Configuration and Function

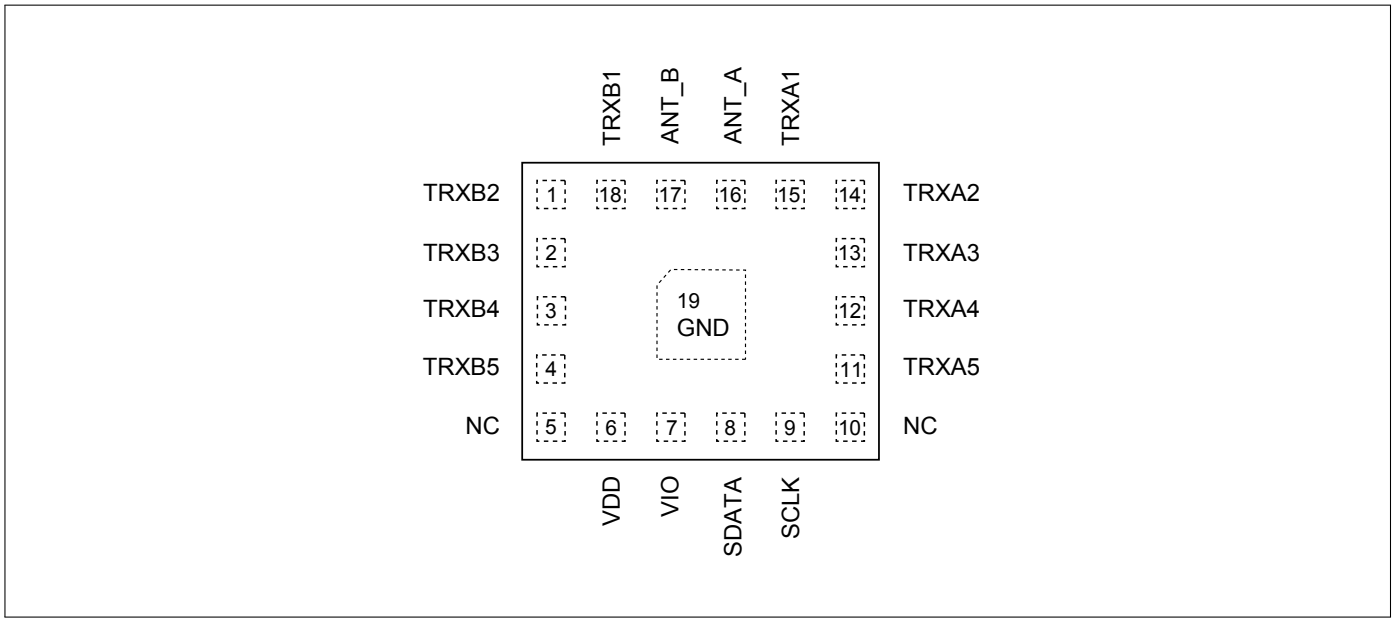


Figure 3: BGSX210MA18 Pin Configuration (top view)

Table 14: Pin Definition and Function

Pin No.	Name	Function
1	TRXB2	TRX port B2
2	TRXB3	TRX port B3
3	TRXB4	TRX port B4
4	TRXB5	TRX port B5
5	NC	Not connected
6	VDD	Power supply
7	VIO	MIPI RFFE power supply
8	SDATA	MIPI RFFE data
9	SCLK	MIPI RFFE clock
10	NC	Not connected
11	TRXA5	TRX port A5
12	TRXA4	TRX port A4
13	TRXA3	TRX port A3
14	TRXA2	TRX port A2
15	TRXA1	TRX port A1
16	ANT_A	Antenna port A
17	ANT_B	Antenna port B
18	TRXB1	TRX port B1
19	GND	RF ground

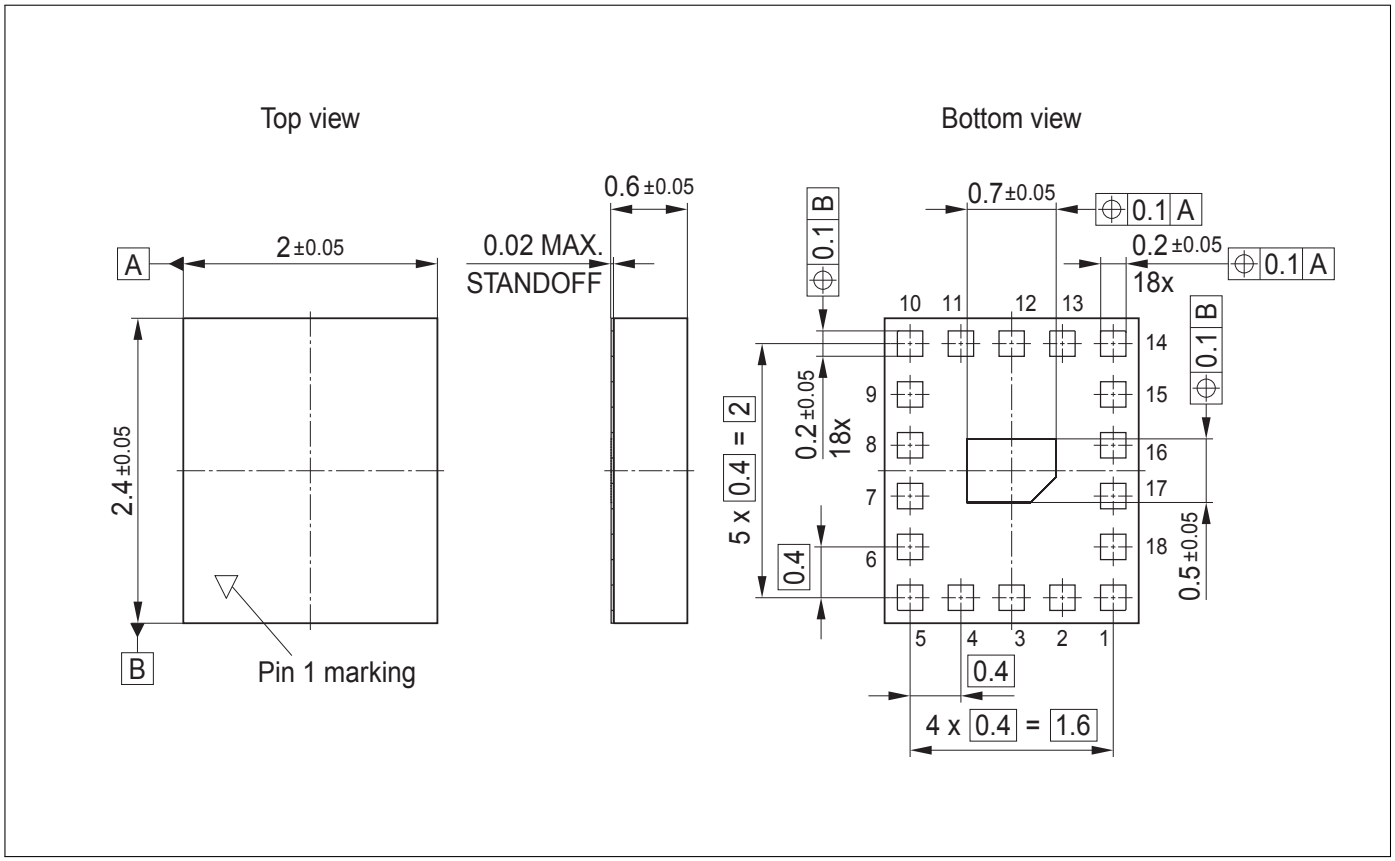


Figure 4: ATSLP-18 Package Outline (top, side and bottom views)

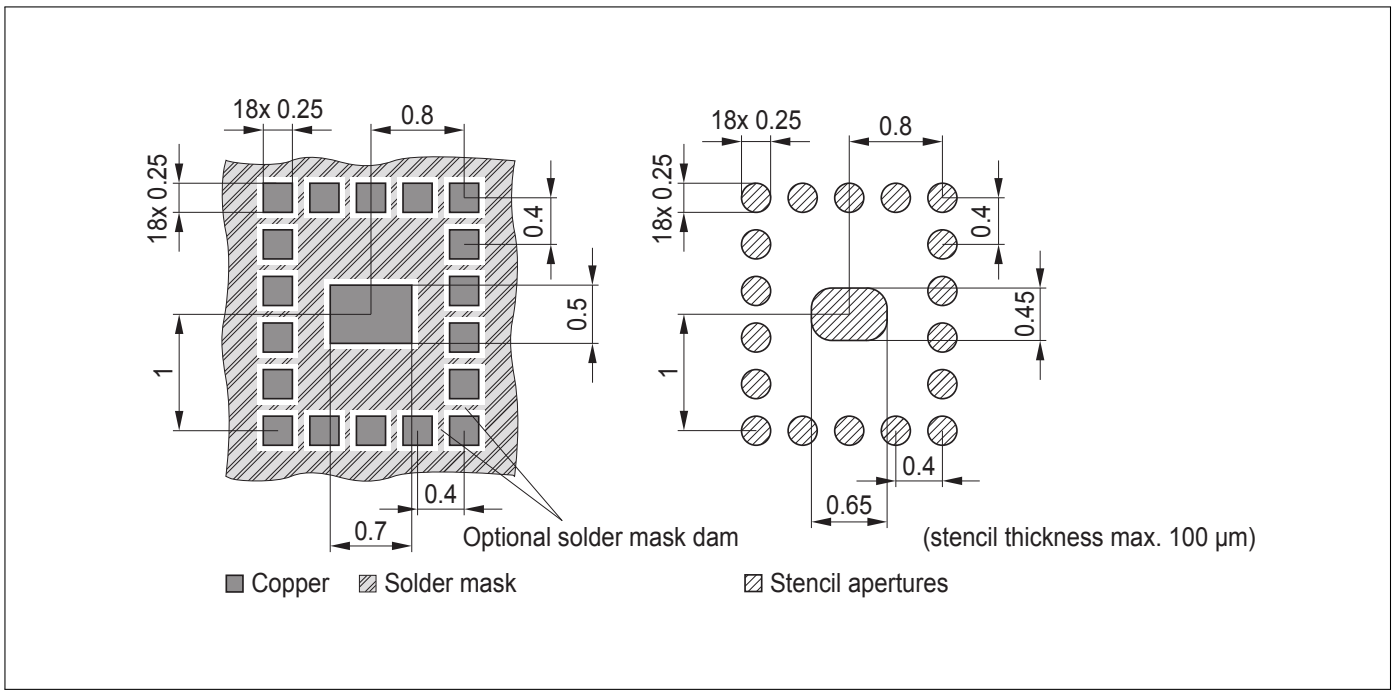


Figure 5: Land Pattern and Stencil Mask

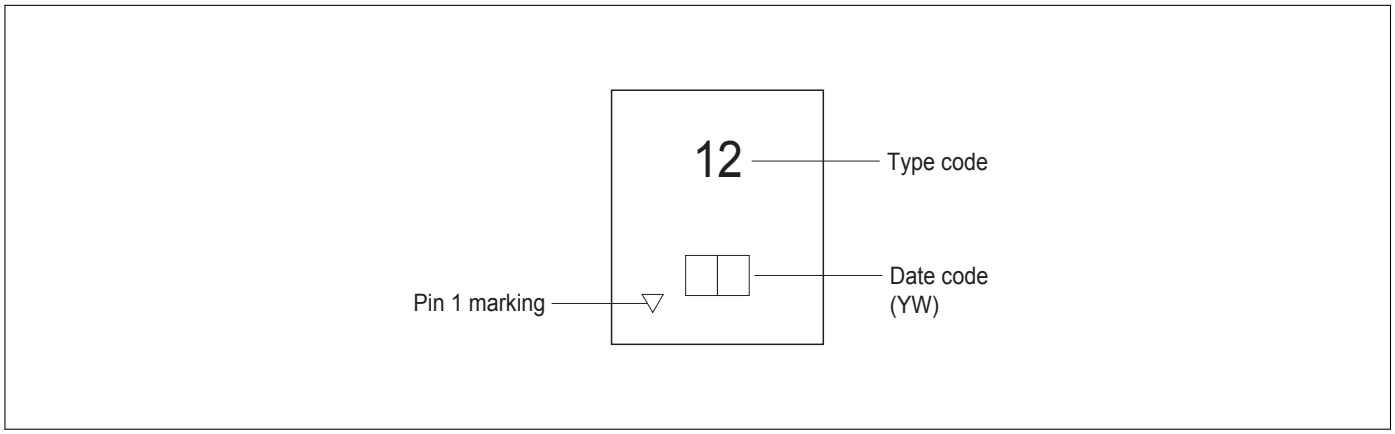


Figure 6: Laser Marking (top view)

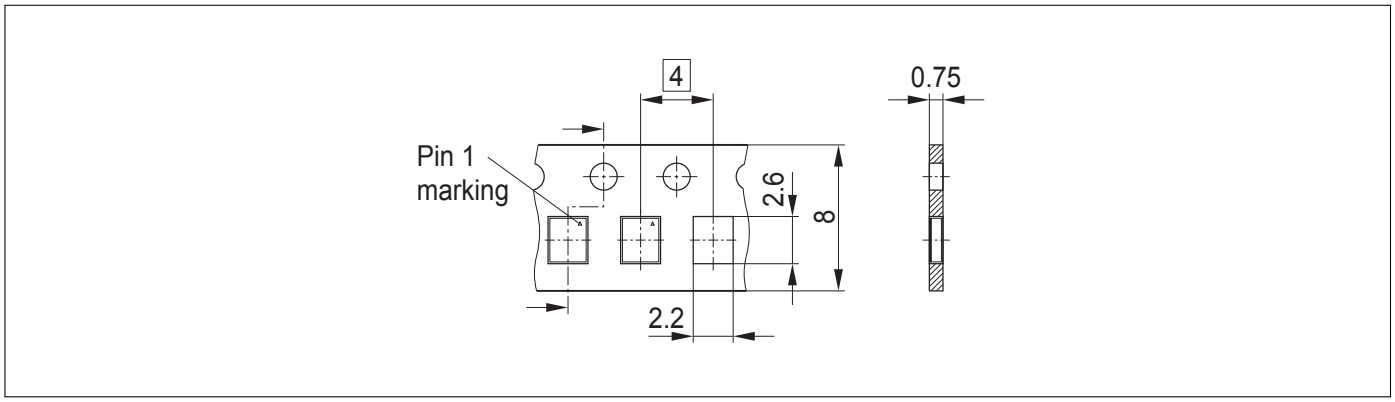


Figure 7: Carrier Tape

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