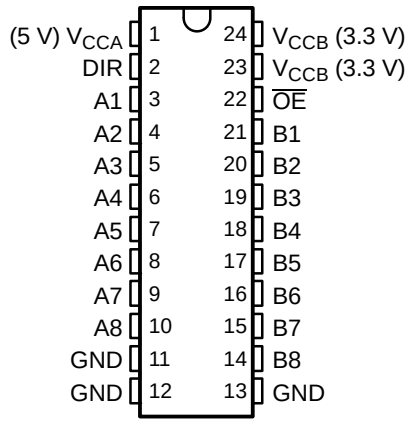
SN74LVC4245A
OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

SCAS375H – MARCH 1994 – REVISED MARCH 2005

FEATURES

- **Bidirectional Voltage Translator**
- **5.5 V on A Port and 2.7 V to 3.6 V on B Port**
- **Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DB, DW, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB}, which is set at 3.3 V, and A port has V_{CCA}, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, $\overline{OE}$) is powered by V_{CCA}.

The SN74LVC4245A pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional '245 pinout.

ORDERING INFORMATION

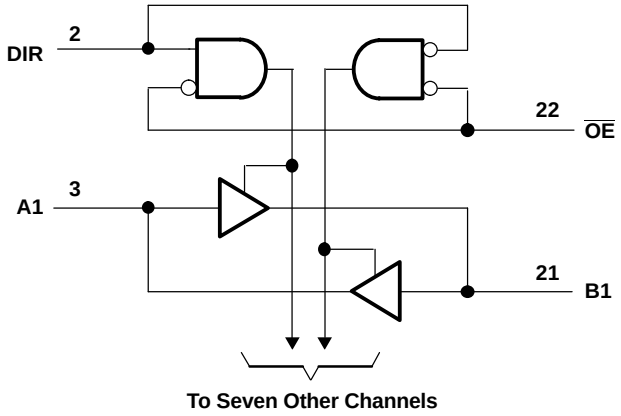
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube of 25	SN74LVC4245ADW	LVC4245A
		Reel of 2000	SN74LVC4245ADWR	
	SSOP – DB	Reel of 2000	SN74LVC4245ADBR	LJ245A
	TSSOP – PW	Tube of 60	SN74LVC4245APW	LJ245A
		Reel of 2000	SN74LVC4245APWR	
		Reel of 250	SN74LVC4245APWT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings[1]

over operating free-air temperature range for V_{CCA} = 4.5 V to 5.5 V (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range	A port[2]	–0.5	V_{CCA} + 0.5	V
		Control inputs	–0.5	6	
V_O	Output voltage range	A port[2]	–0.5	V_{CCA} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA} or GND			±100	mA
θ_{JA}	Package thermal impedance[3]	DB package		63	°C/W
		DW package		46	
		PW package		88	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 6 V maximum.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Absolute Maximum Ratings(1)

over operating free-air temperature range for V_{CCB} = 2.7 V to 3.6 V (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range	B port(2)	–0.5	V_{CCB} + 0.5	V
V_O	Output voltage range	B port(2)	–0.5	V_{CCB} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCB} or GND			±100	mA
θ_{JA}	Package thermal impedance(3)	DB package		63	°C/W
		DW package		46	
		PW package		88	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 4.6 V maximum.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

for V_{CCA} = 4.5 V to 5.5 V

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_{IA}	Input voltage	0	V_{CCA}	V
V_{OA}	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions(1)

for V_{CCB} = 2.7 V to 3.6 V

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCB} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CCB} = 2.7 V to 3.6 V		0.8	V
V_{IB}	Input voltage		0	V_{CCB}	V
V_{OB}	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	V_{CCB} = 2.7 V		–12	mA
		V_{CCB} = 3 V		–24	
I_{OL}	Low-level output current	V_{CCB} = 2.7 V		12	mA
		V_{CCB} = 3 V		24	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics(1)

over recommended operating free-air temperature range for V_{CCA} = 4.5 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP(2)	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		4.5 V	4.3			V
				5.5 V	5.3			
		I_{OH} = –24 mA		4.5 V	3.7			
				5.5 V	4.7			
V_{OL}		I_{OL} = 100 μA		4.5 V			0.2	V
				5.5 V			0.2	
		I_{OL} = 24 mA		4.5 V			0.55	
				5.5 V			0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		5.5 V			±1	μA
I_{OZ}(3)	A port	$V_O = V_{CCA}$ or GND		5.5 V			±5	μA
I_{CCA}		$V_I = V_{CCA}$ or GND,	I_O = 0	5.5 V			80	μA
ΔI_{CCA}(4)		One input at 3.4 V,	Other inputs at V_{CCA} or GND	5.5 V			1.5	mA
C_i	Control inputs	$V_I = V_{CCA}$ or GND		Open		5		pF
C_{io}	A port	$V_O = V_{CCA}$ or GND		5 V		11		pF

(1) V_{CCB} = 2.7 V to 3.6 V
(2) All typical values are measured at V_{CC} = 5 V, T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.

Electrical Characteristics(1)

over recommended operating free-air temperature range for V_{CCB} = 2.7 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCB}	MIN	TYP(2)	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		2.7 V to 3.6 V	V_{CC} – 0.2			V
		I_{OH} = –12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2			
V_{OL}		I_{OL} = 100 μA		2.7 V to 3.6 V			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_{OZ}(3)	B port	$V_O = V_{CCB}$ or GND		3.6 V			±5	μA
I_{CCB}		$V_I = V_{CCB}$ or GND,	I_O = 0	3.6 V			50	μA
ΔI_{CCB}(4)		One input at V_{CCB} – 0.6 V,	Other inputs at V_{CCB} or GND	2.7 V to 3.6 V			0.5	mA
C_{io}	B port	$V_O = V_{CCB}$ or GND		3.3 V		11		pF

(1) V_{CCA} = 5 V ± 0.5 V
(2) All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 2.7 V to 3.6 V		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	$\overline{OE}$	A	1	9	ns
t_{PZH}			1	8.1	
t_{PZL}	$\overline{OE}$	B	1	8.8	ns
t_{PZH}			1	9.8	
t_{PLZ}	$\overline{OE}$	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	$\overline{OE}$	B	1	7.7	ns
t_{PHZ}			1	7.8	

Operating Characteristics

V_{CCA} = 4.5 V to 5.5 V, V_{CCB} = 2.7 V to 3.6 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 0,	f = 10 MHz	39.5	pF
		Outputs disabled			5	

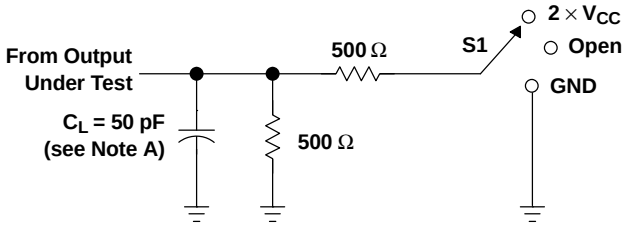
Power-Up Considerations(1)

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

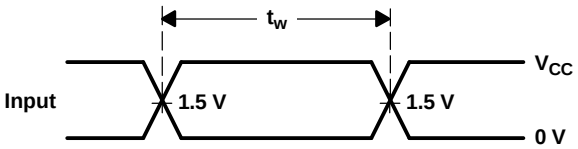
(1) Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

PARAMETER MEASUREMENT INFORMATION
A PORT

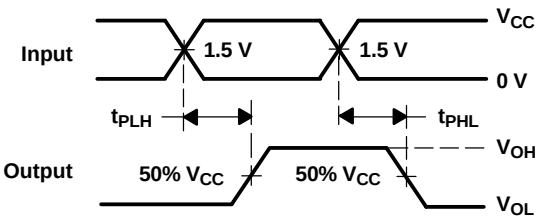


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

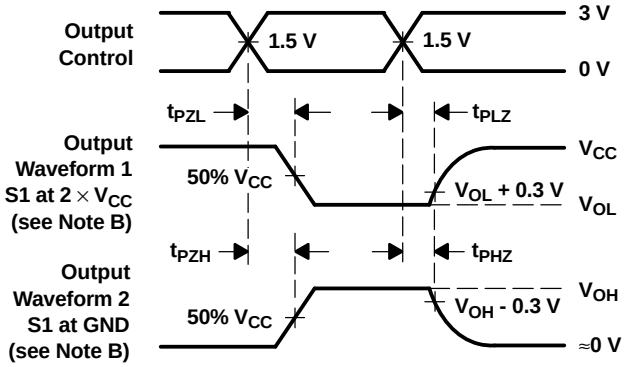
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

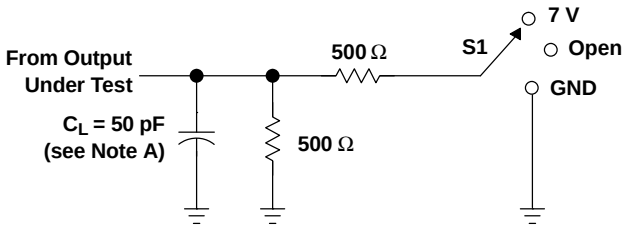


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

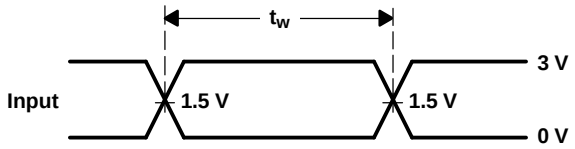
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
B PORT

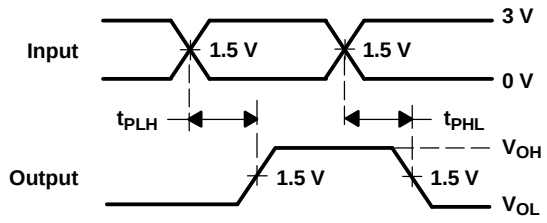


LOAD CIRCUIT

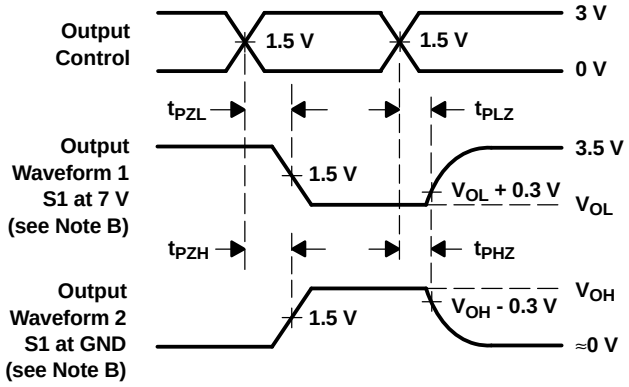
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC4245ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWTG4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVC4245A :

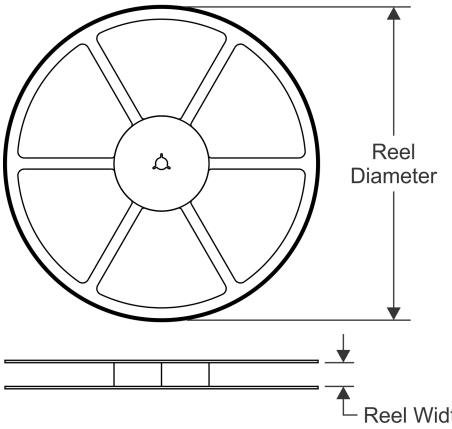
- Enhanced Product: SN74LVC4245A-EP

NOTE: Qualified Version Definitions:

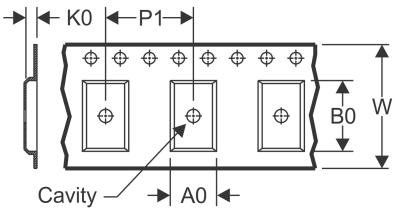
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

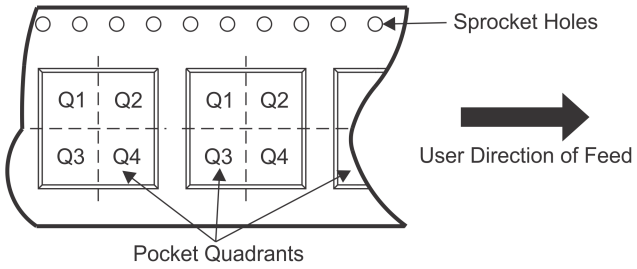


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

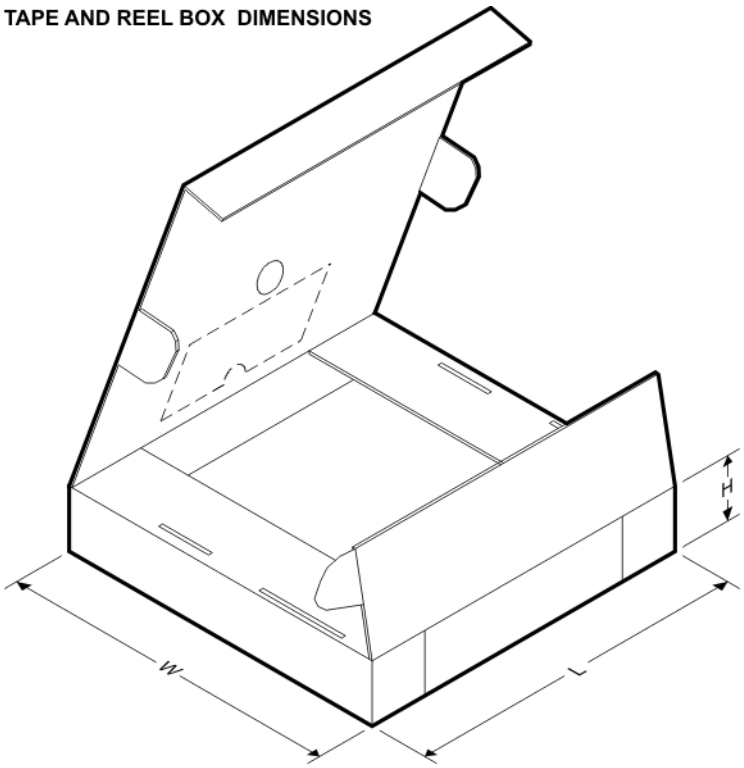
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC4245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVC4245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC4245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC4245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC4245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC4245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

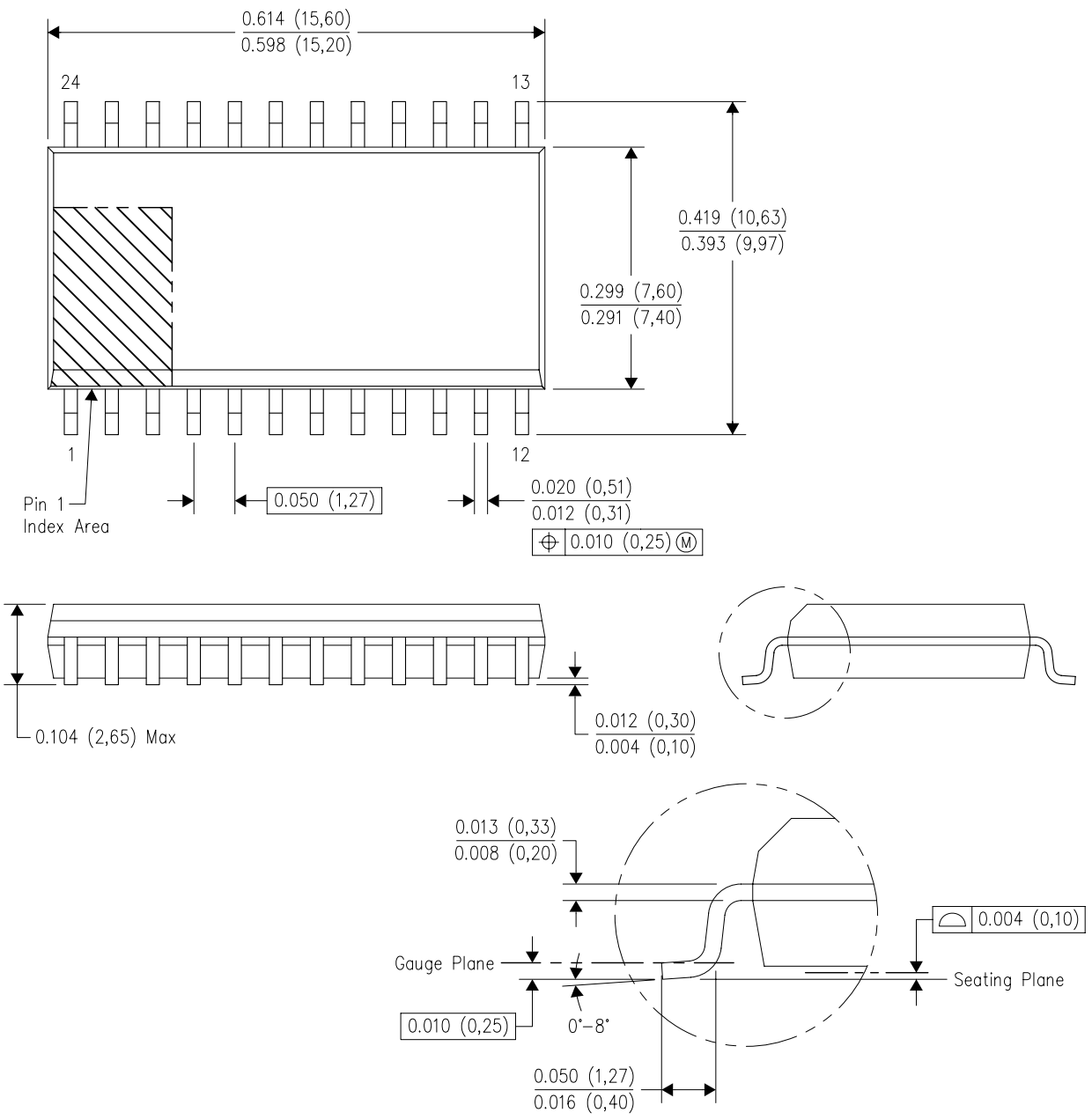
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

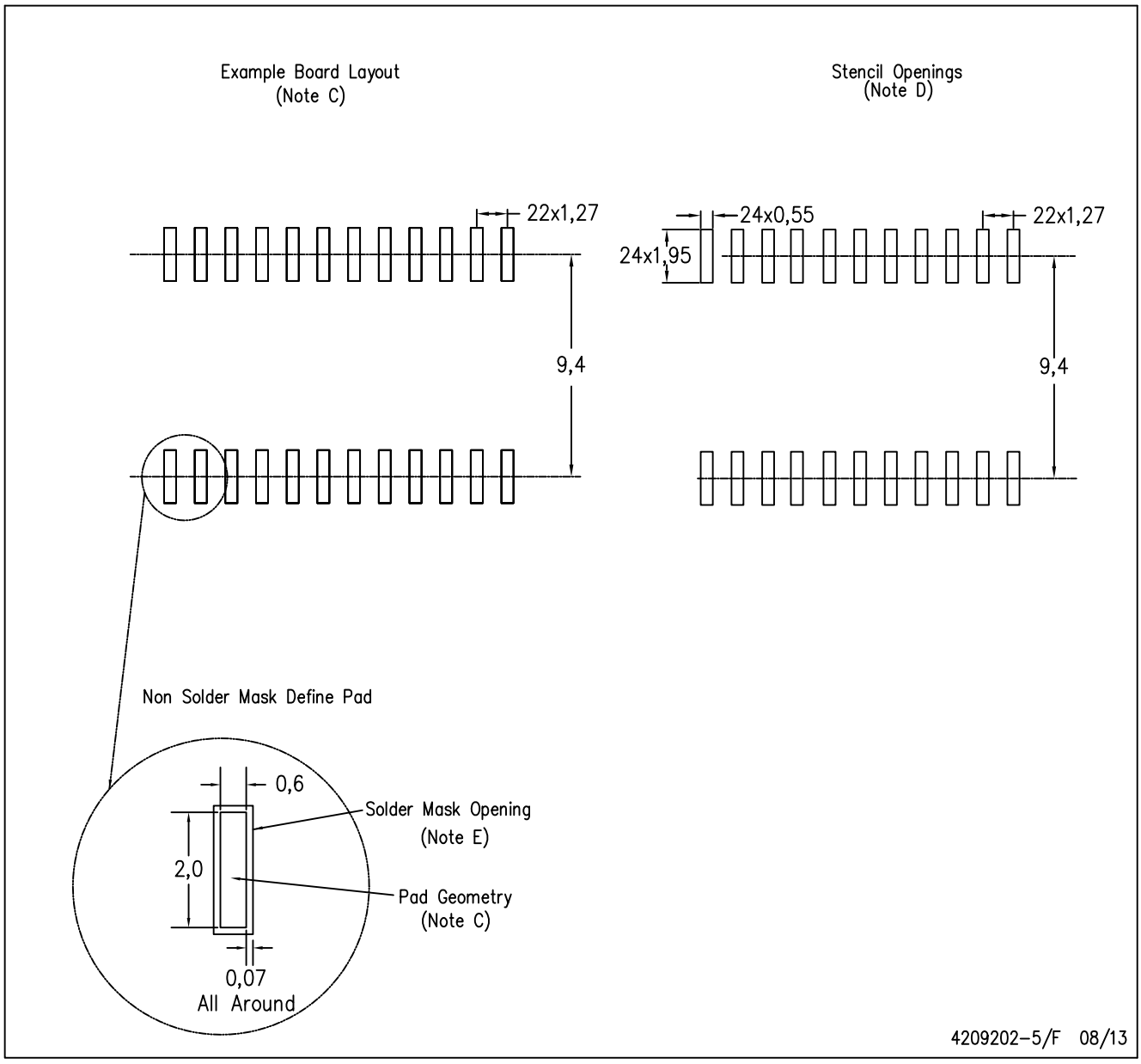
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC4245ADBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74LVC4245ADWR	SOIC	DW	24	2000	366.0	364.0	50.0
SN74LVC4245ADWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74LVC4245ADWRG4	SOIC	DW	24	2000	367.0	367.0	45.0
SN74LVC4245APWR	TSSOP	PW	24	2000	367.0	367.0	38.0
SN74LVC4245APWT	TSSOP	PW	24	250	367.0	367.0	38.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



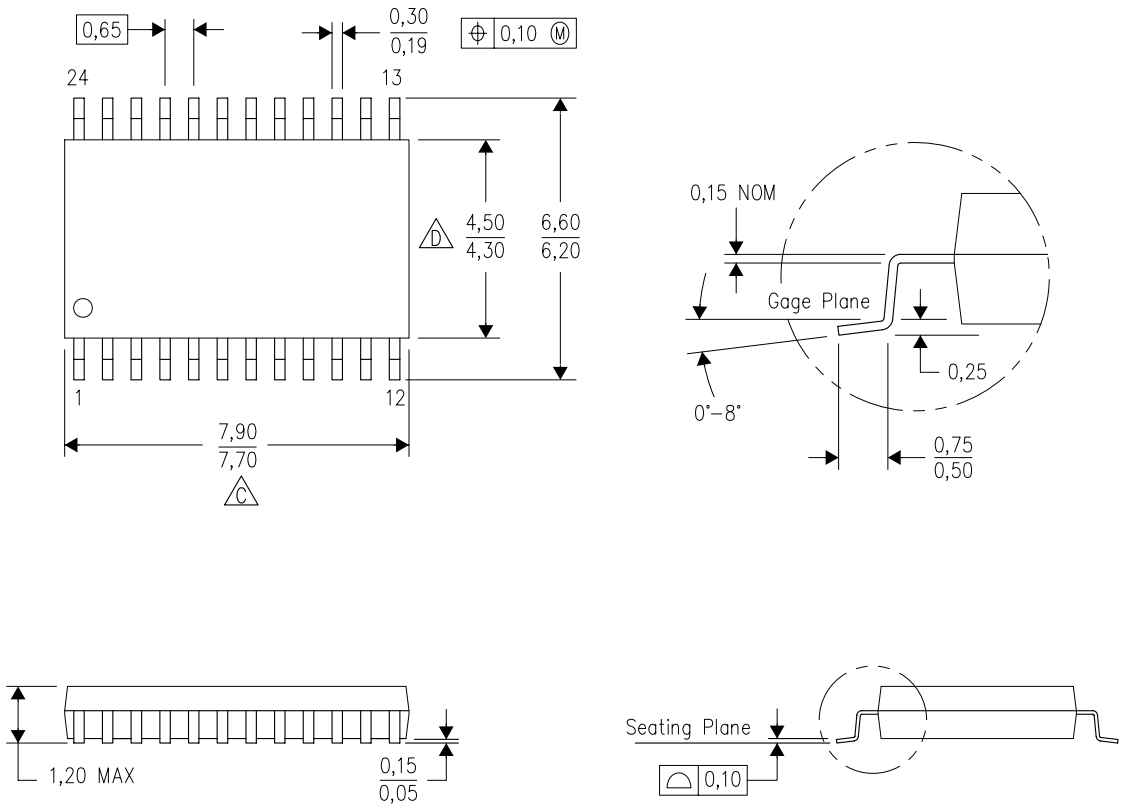
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

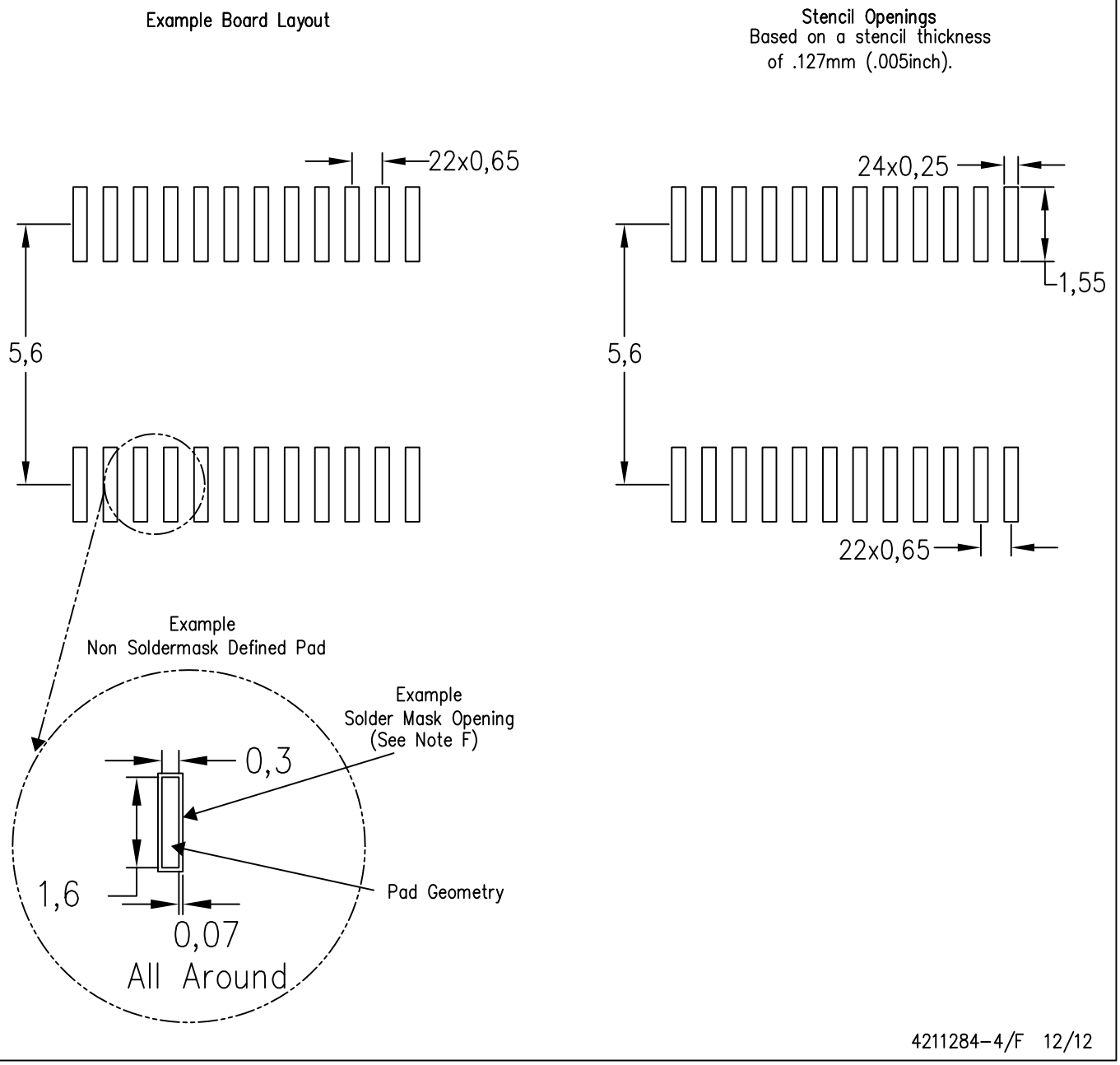
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE

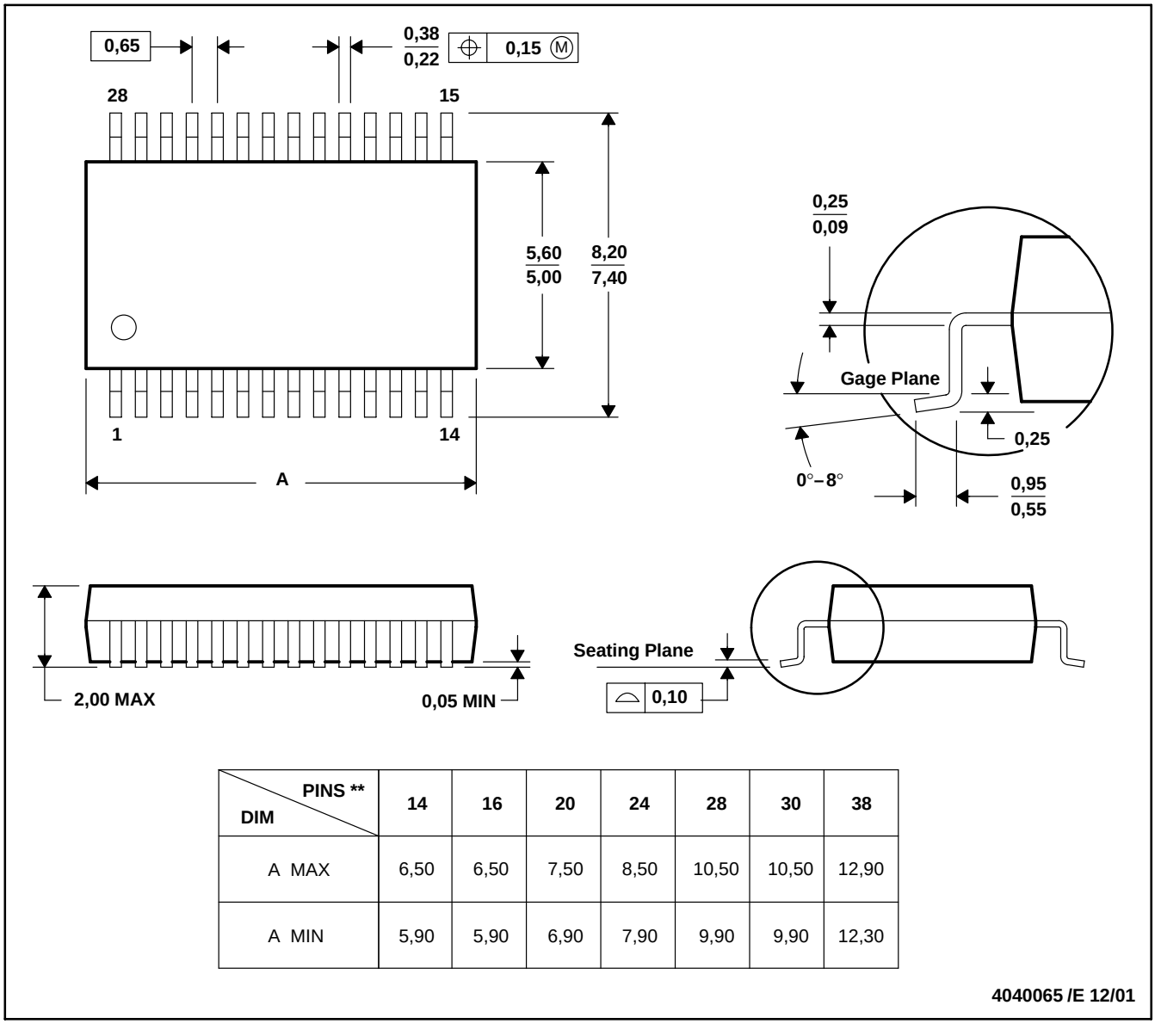


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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