



3.3V CMOS 1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

IDT74ALVC162344

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4 μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVC162344:

- *Balanced Output Drivers: $\pm 12\text{mA}$*
- *Low switching noise*

APPLICATIONS:

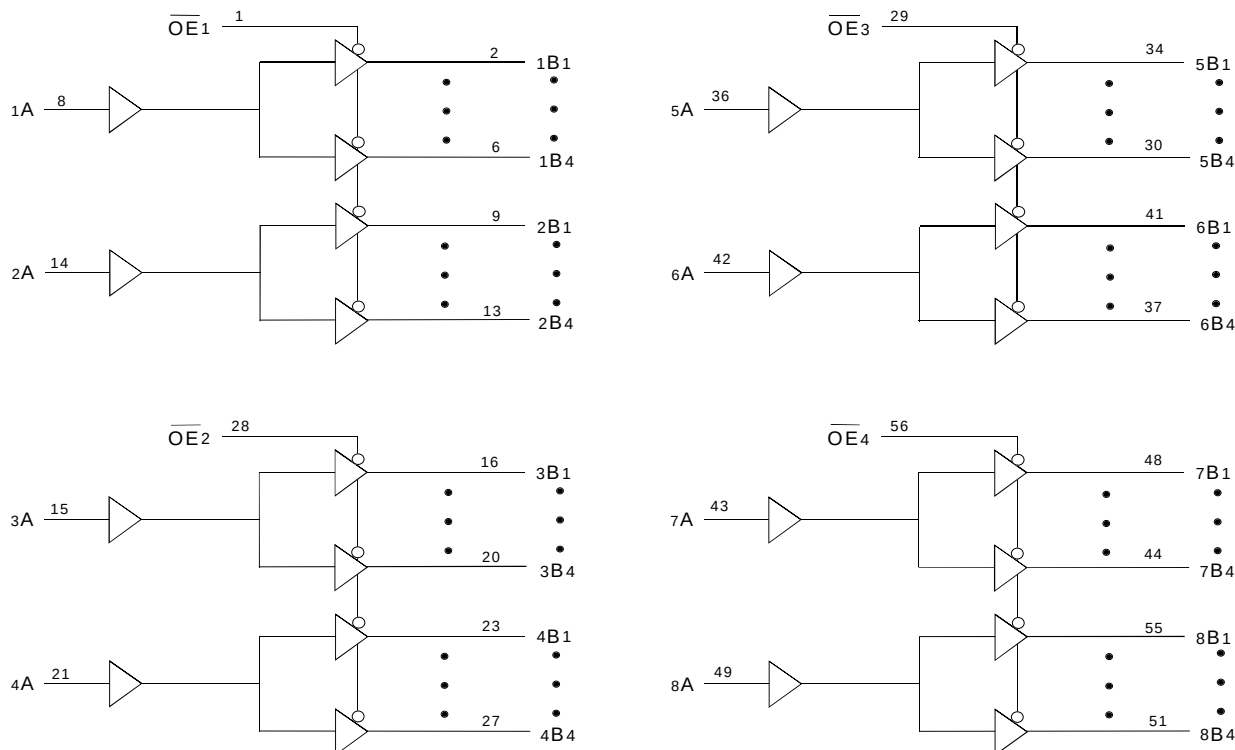
- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

This 1-bit to 4-bit address driver is built using advanced dual metal CMOS technology. The ALVC162344 device is used in applications in which four separate memory locations must be addressed by a single address.

The ALVC162344 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12\text{mA}$ at the designated threshold levels.

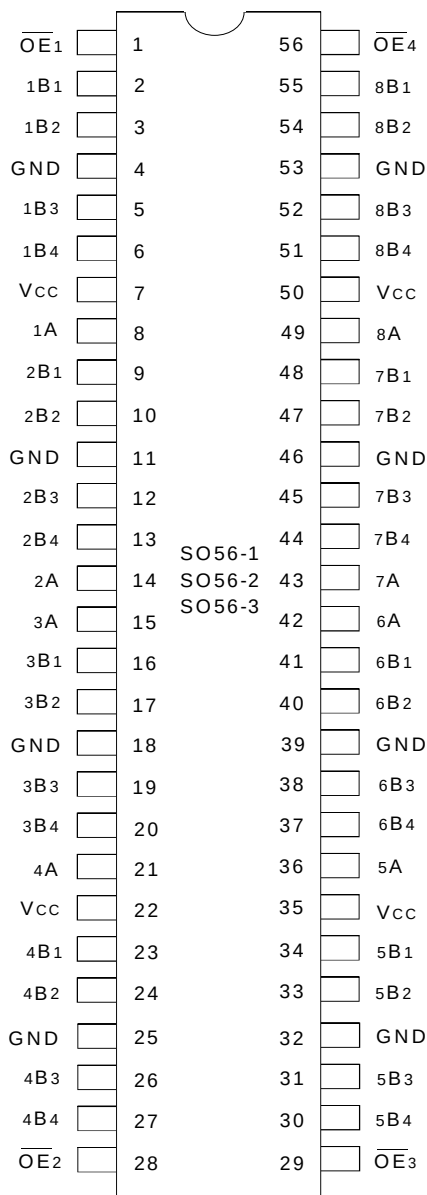
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

JANUARY 1999

PIN CONFIGURATION



SSOP/
TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	- 0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	- 65 to + 150	°C
I _{OUT}	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I _{OK}	Continuous Clamp Current, $V_O < 0$	- 50	mA
I _{CC}	Continuous Current through each Vcc or GND	±100	mA

NEW16link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0V$	5	7	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0V$	7	9	pF
C _{I/O}	I/O Port Capacitance	$V_{IN} = 0V$	7	9	pF

NEW16link

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_x$	3-State Output Enable Inputs (Active LOW)
xA	Data Inputs
xBx	3-State Outputs

FUNCTION TABLE (1)

Inputs		Outputs
$\overline{OE}_x$	xA	xBx
L	H	H
L	L	L
H	X	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V	Vi = VCC	—	—	± 5	μA
IiL	Input LOW Current	VCC = 3.6V	Vi = GND	—	—	± 5	
IoZH IoZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	Vo = VCC	—	—	± 10	μA
			Vo = GND	—	—	± 10	μA
Vik	Clamp Diode Voltage	VCC = 2.3V, IIN = – 18mA		—	– 0.7	– 1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
IcCL IcCH IcCZ	Quiescent Power Supply Current	VCC = 3.6V		—	0.1	40	μA
		VIN = GND or VCC					
ΔIcc	Quiescent Power Supply Current Variation	One input at VCC – 0.6V, other inputs at VCC or GND		—	—	750	μA

NEW16link

NOTE:

- Typical values are at VCC = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
			IOH = – 4mA	1.9	—	
		VCC = 2.3V	IOH = – 6mA	1.7	—	
			IOH = – 4mA	2.2	—	
		VCC = 2.7V	IOH = – 8mA	2	—	
			IOH = – 6mA	2.4	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOH = – 12mA	2	—	V
			IOH = – 0.1mA	—	0.2	
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	—	0.6	
		VCC = 3.0V	IOL = 6mA	—	0.55	
			IOL = 12mA	—	0.8	

NEW16link

NOTE:

- VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	VCC = 2.5V $\pm$ 0.2V	VCC = 3.3V $\pm$ 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	68	82	pF
CPD	Power Dissipation Capacitance Outputs disabled		12	14	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	VCC = 2.5V $\pm$ 0.2V		VCC = 2.7V		VCC = 3.3V $\pm$ 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay xA to xBx	1	4.9	—	5.1	1.4	4.4	ns
tPZH tPZL	Output Enable Time $\overline{\text{OE}}$ to xBx	1	6.4	—	6.6	1.2	5.7	ns
tPHZ tPLZ	Output Disable Time $\overline{\text{OE}}$ to xBx	1	5.4	—	4.7	1.2	4.5	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps
tsk(b)	Output Skew ⁽²⁾	—	—	—	—	—	350	ps

NOTES:

- See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
- Skew between any two outputs of the same package and switching in the same direction. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank of the same package; this parameter is guaranteed but not production tested.

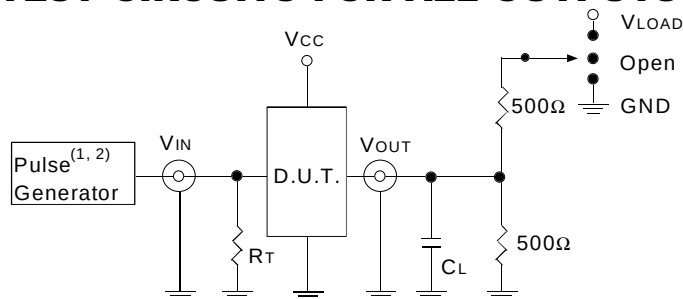
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

NEW16link

TEST CIRCUITS FOR ALL OUTPUTS



ALVC Link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

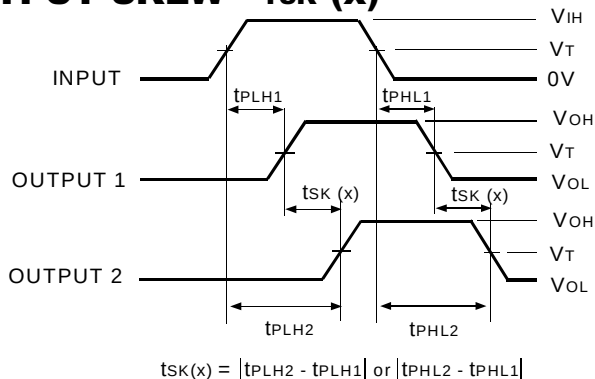
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

NEW16link

OUTPUT SKEW - t_{SK} (x)



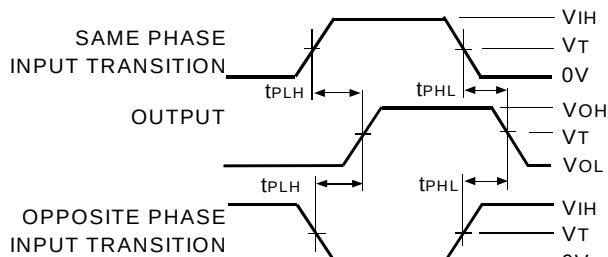
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

ALVC Link

NOTES:

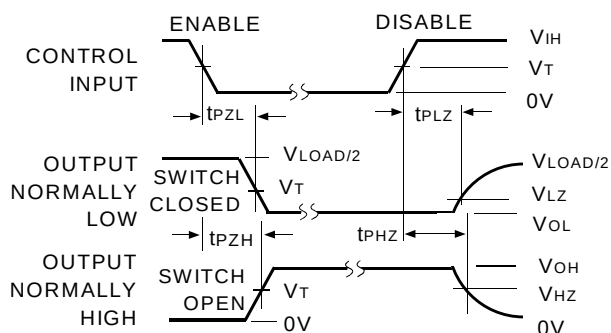
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



ALVC Link

ENABLE AND DISABLE TIMES

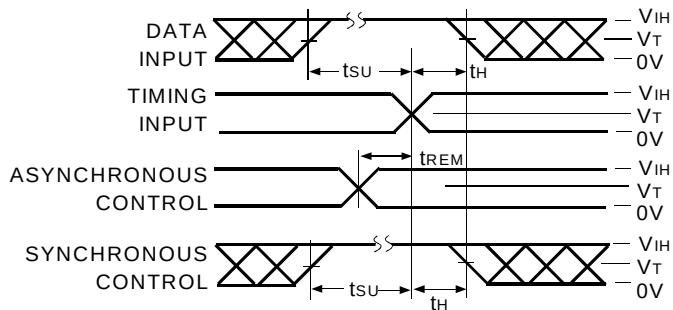


ALVC Link

NOTE:

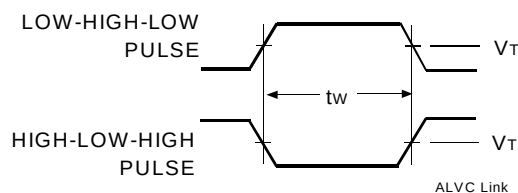
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



ALVC Link

PULSE WIDTH



ALVC Link

ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
						344	1-Bit to 4-Bit Address Driver with 3-State Outputs
						162	Double-Density with Resistors, $\pm 12\text{mA}$
						Blank	No Bus-Hold
						74	-40°C to $+85^{\circ}\text{C}$

**CORPORATE HEADQUARTERS**

2975 Stender Way
Santa Clara, CA 95054

for SALES:

800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.
The IDT logo is a registered trademark of Integrated Device Technology, Inc.