

# SN54LS323, SN74LS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

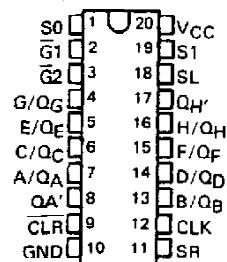
SDLS160

OCTOBER 1976 - REVISED MARCH 1988

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
  - Hold (Store) Shift Left
  - Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Typical Power Dissipation . . . 175 mW
- Exceptionally Stable Shift (Clock) Frequency . . . 25 MHz
- Applications:
  - Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- SN54LS299 and SN74LS299 Are Similar But Have Direct Overriding Clear

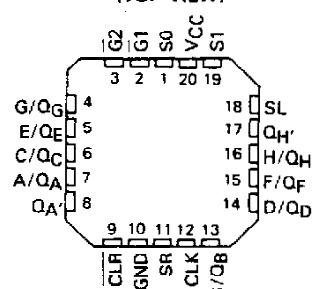
SN54LS323 . . . J OR W PACKAGE  
SN74LS323 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS323 . . . FK PACKAGE

(TOP VIEW)



## description

These Low-Power Schottky eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table. Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

## FUNCTION TABLE

MODE	INPUTS					INPUTS/OUTPUTS								OUTPUTS				
	CLR	FUNCTION		CLK	SERIAL	A/QA B/QB C/QC D/QD E/QE F/QF G/QG H/QH								QA' QH'				
		SELECT	OUTPUT CONTROL			S1	S0	G1 <sup>t</sup>	G2 <sup>t</sup>	SL	SR	a	b	c	d	e	f	g
Clear	L	X	L	L	†	X	X	L	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	†	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	†	X	X	X	X	X	X	X	X	X	X	X	L
Hold	H	L	L	L	L	X	X	QA <sub>0</sub>	QA <sub>0</sub>	QC <sub>0</sub>	QD <sub>0</sub>	QE <sub>0</sub>	QF <sub>0</sub>	QG <sub>0</sub>	QH <sub>0</sub>	QA <sub>0</sub>	QA <sub>0</sub>	
	H	X	X	L	L	L	X	X	QA <sub>0</sub>	QA <sub>0</sub>	QC <sub>0</sub>	QD <sub>0</sub>	QE <sub>0</sub>	QF <sub>0</sub>	QG <sub>0</sub>	QH <sub>0</sub>	QA <sub>0</sub>	QA <sub>0</sub>
Shift Right	H	L	H	L	L	†	X	H	H	QA <sub>n</sub>	QA <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	H	QG <sub>n</sub>
	H	L	H	L	L	†	X	L	L	QA <sub>n</sub>	QA <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	L	QG <sub>n</sub>
Shift Left	H	H	L	L	L	†	H	X	QA <sub>n</sub>	QA <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	H	QA <sub>n</sub>	H
	H	H	L	L	L	†	L	X	QA <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	QH <sub>n</sub>	L	QA <sub>n</sub>	L
Load	H	H	H	X	X	†	X	X	a	b	c	d	e	f	g	h	a	h

<sup>t</sup>When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

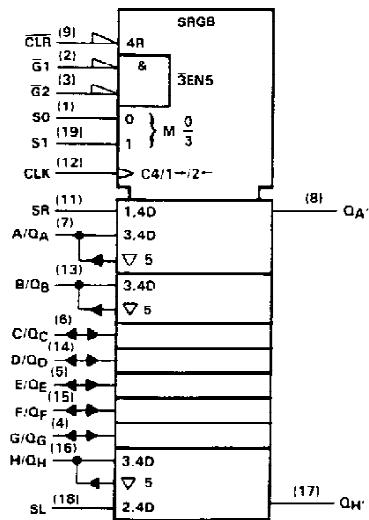
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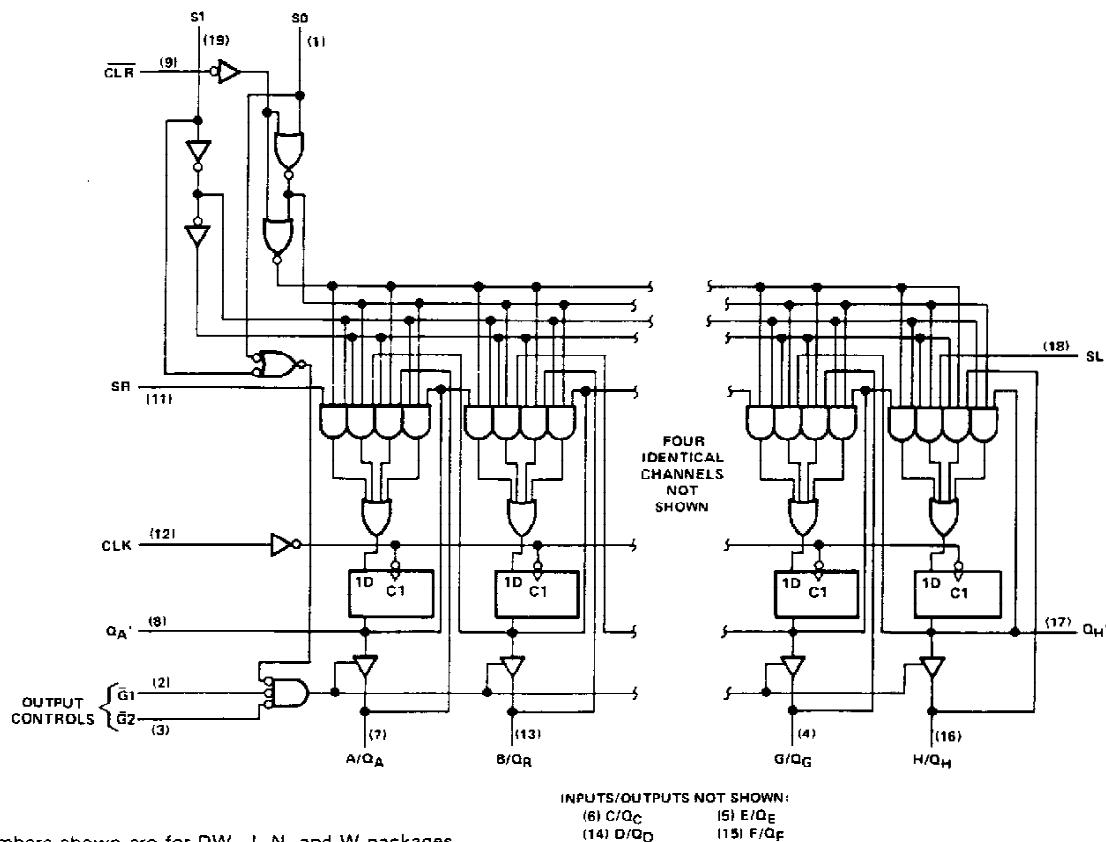
# SN54LS323, SN74LS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

## logic symbol<sup>†</sup>



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for DW, J, N, and W packages.

## logic diagram (positive logic)



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**SN54LS323, SN74LS323**  
**8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS**

**schematics of inputs and outputs, absolute maximum ratings, recommended operating conditions, and electrical characteristics**

Same as SN54LS299 and SN74LS299, except  $t_{SU}$  (Clear Inactive) does not apply.

**switching characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ C$**

PARAMETER <sup>†</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$			See Note 1	25	35		MHz
$t_{PLH}$	CLK	$Q_A'$ or $Q_H'$	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$	22	33		
$t_{PHL}$				26	39		ns
$t_{PLH}$	CLK	$Q_A$ thru $Q_H$	$C_L = 45 \text{ pF}, R_L = 665 \Omega$	17	25		
$t_{PHL}$				25	39		ns
$t_{PZH}$	$\bar{G}_1, \bar{G}_2$	$Q_A$ thru $Q_H$	$C_L = 5 \text{ pF}, R_L = 665 \Omega$	14	21		
$t_{PZL}$				20	30		ns
$t_{PHZ}$	$\bar{G}_1, \bar{G}_2$	$Q_A$ thru $Q_H$	$C_L = 5 \text{ pF}, R_L = 665 \Omega$	10	20		
$t_{PLZ}$				10	15		ns

<sup>†</sup> $t_{max}$  = maximum clock frequency

$t_{PLH}$  = Propagation delay time, low-to-high-level output

$t_{PHL}$  = Propagation delay time, high-to-low-level output

$t_{PZH}$  = Output enable time to high level

$t_{PZL}$  = Output enable time to low level

$t_{PHZ}$  = Output disable time from high level

$t_{PLZ}$  = Output disable time from low level

NOTE 1: For testing  $f_{max}$ , all outputs are loaded simultaneously, each with  $C_L$  and  $R_L$  as specified for the propagation times. Load circuits and voltage waveforms are shown in Section 1.

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN54LS323J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SN74LS323DW	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI
SN74LS323DW	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI
SN74LS323DWR	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI
SN74LS323DWR	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI
SN74LS323N	OBsolete	PDIP	N	20		TBD	Call TI	Call TI
SN74LS323N	OBsolete	PDIP	N	20		TBD	Call TI	Call TI
SNJ54LS323FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS323FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS323J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SNJ54LS323J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SNJ54LS323W	OBsolete	CFP	W	20		TBD	Call TI	Call TI
SNJ54LS323W	OBsolete	CFP	W	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

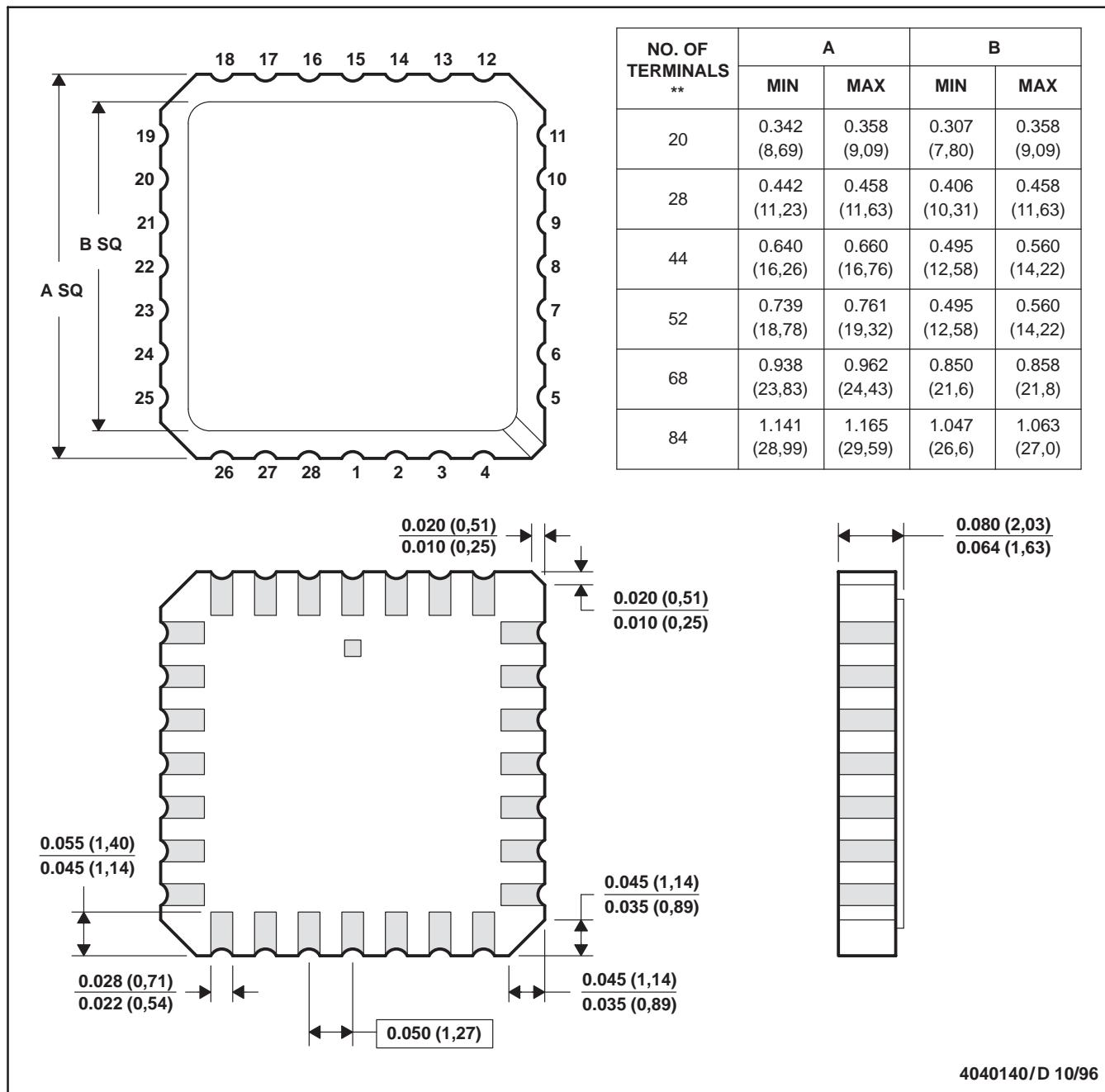
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## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

## 28 TERMINAL SHOWN



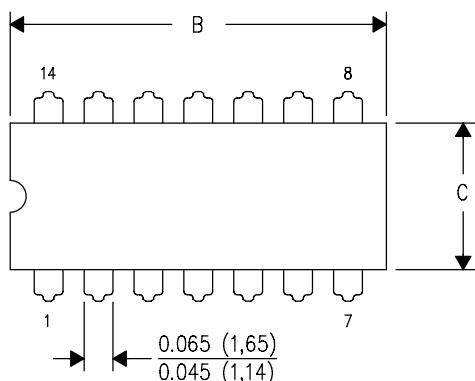
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

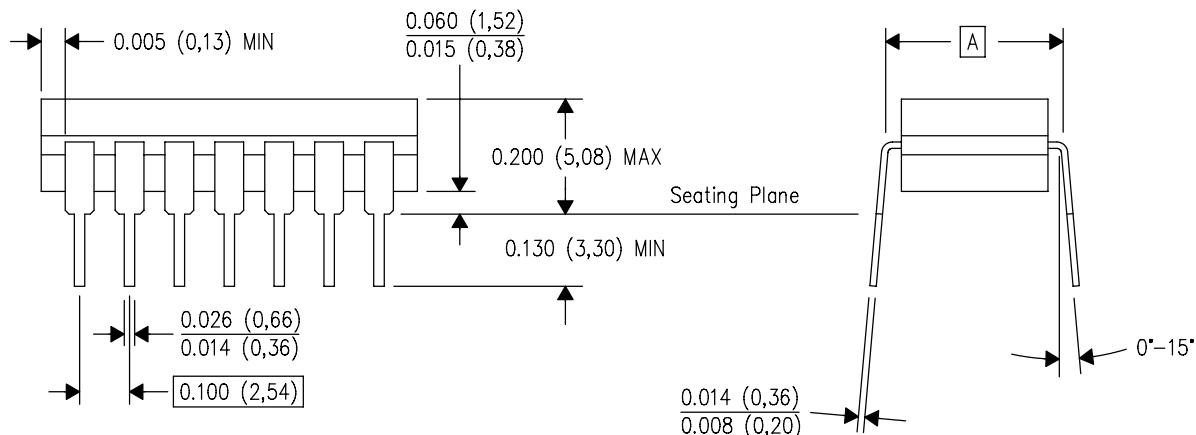
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

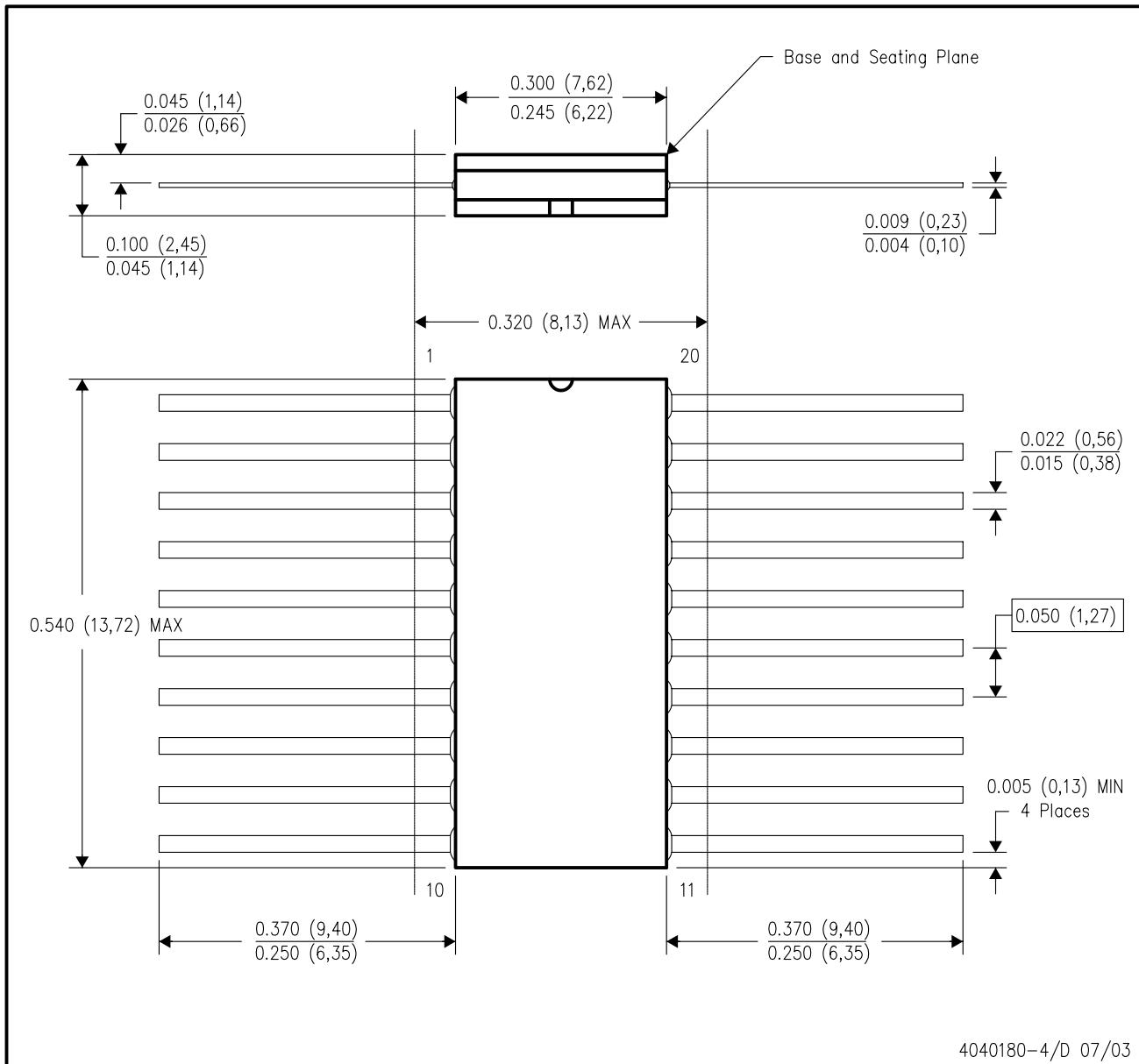


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NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

## CERAMIC DUAL FLATPACK

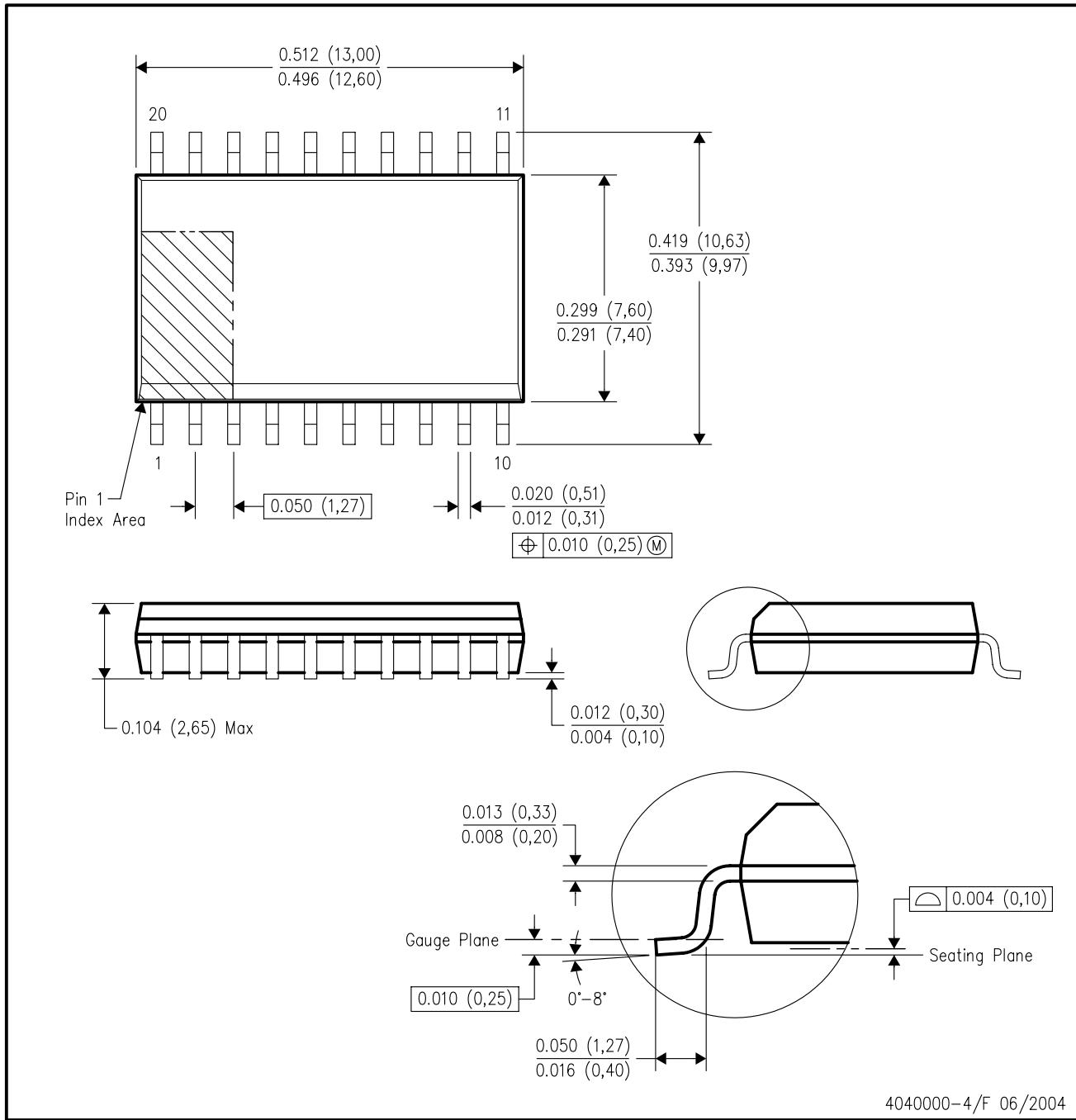


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



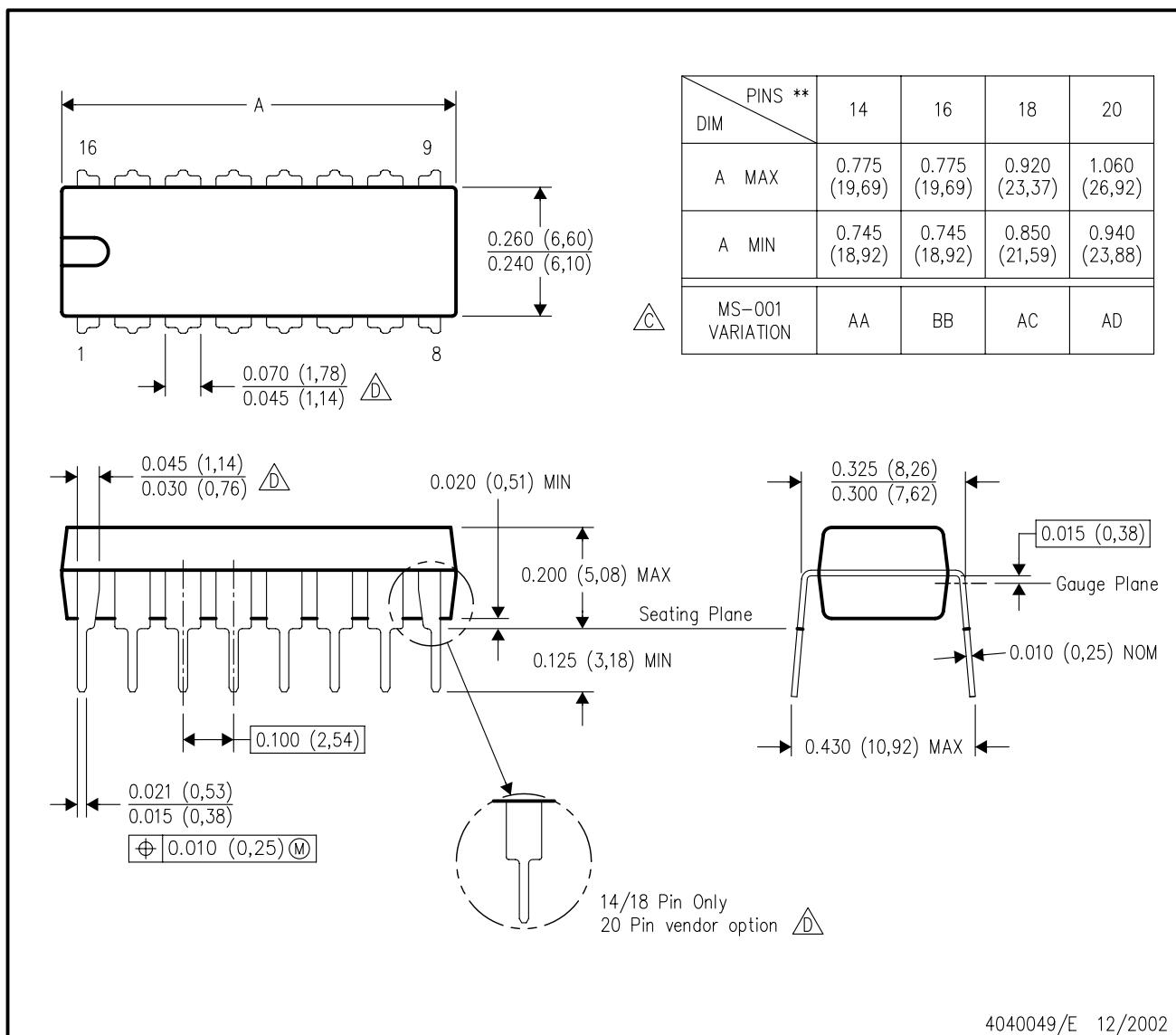
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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