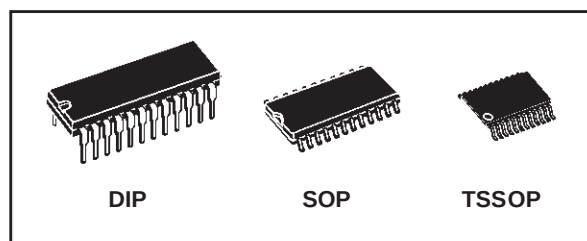




M74HC646

OCTAL BUS TRANSCEIVER/REGISTER WITH 3 STATE OUTPUTS

- HIGH SPEED:
 $f_{MAX} = 79 \text{ MHz (TYP.) at } V_{CC} = 6V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu A(\text{MAX.}) \text{ at } T_A = 25^\circ C$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} (\text{MIN.})$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 6mA (\text{MIN})$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 $V_{CC} (\text{OPR}) = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE WITH
74 SERIES 646



ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC646B1R	
SOP	M74HC646M1R	M74HC646RM13TR
TSSOP		M74HC646TTR

DESCRIPTION

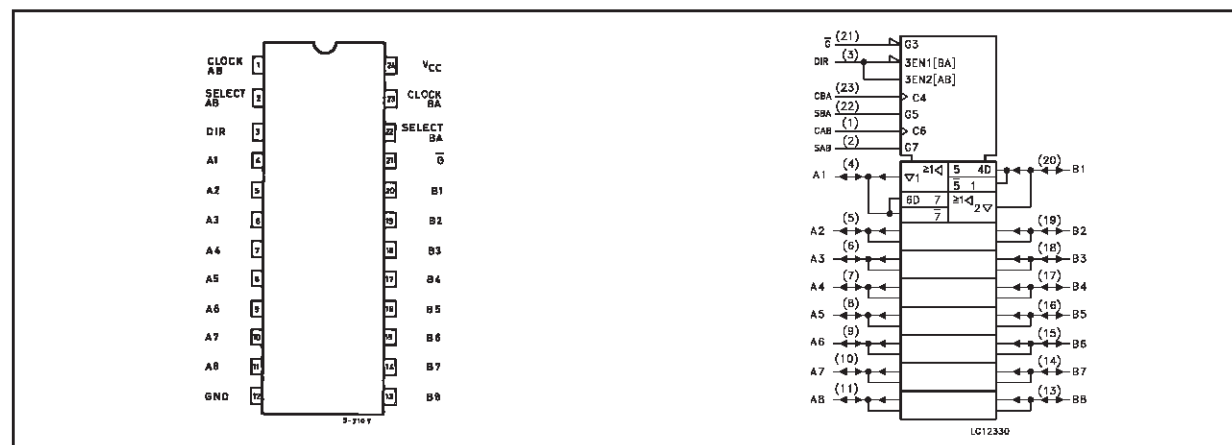
The 74HC646 is an advanced high-speed CMOS OCTAL BUS TRANSCEIVER AND REGISTER (3-STATE) fabricated with silicon gate C²MOS technology.

This device consists of bus transceiver circuits with 3 state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into register on the low to high transition of the appropriate clock pin (Clock AB or Clock BA). Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either

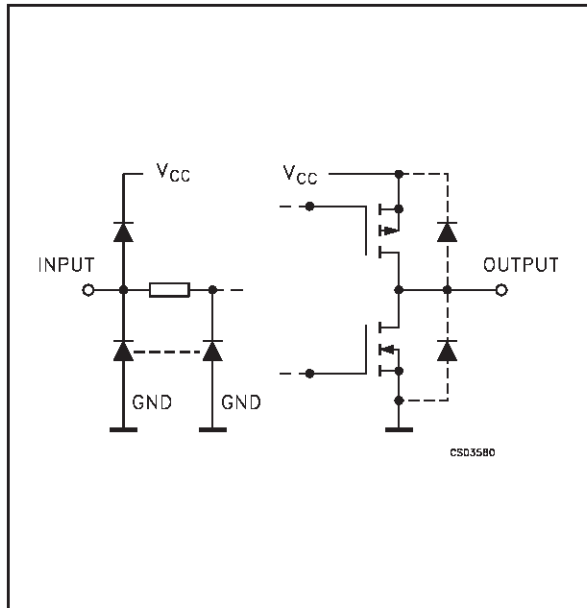
register or in both. The select controls (Select AB select BA) can multiplex stored and real time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (enable $\overline{G}$ high), "A" data may be stored in one register and/or "B" data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK AB (CAB)	A to B Clock Input (LOW to HIGH, Edge-Triggered)
2	SELECT AB (SAB)	Select A to B Source Input
3	DIR	Direction Control Input
4, 5, 6, 7, 8, 9, 10, 11	A1 to A8	A Data Inputs/Outputs
20, 19, 18, 17, 16, 15, 14, 13	B1 to B8	B Data Inputs/Outputs
21	$\overline{G}$	Output Enable Input (Active LOW)
22	SELECT BA (SBA)	Select B to A Source Input
23	CLOCK BA (CBA)	B to A Clock Input (LOW to HIGH, Edge Triggered)
12	GND	Ground (0V)
24	V _{CC}	Positive Supply Voltage

TRUTH TABLE

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	FUNCTION
H	X					INPUTS	INPUTS	Both the A bus and the B bus are inputs
		X	X	X	X	Z	Z	The Output functions of the A and B bus are disabled
				X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs
		X	X*	L	X	L	L	The data at the A bus are displayed at the B bus
						H	H	
			X*	L	X	L	L	The data at the A bus are displayed at the B bus. The data of the A bus are stored to internal flip-flop on low to high transition of the clock pulse
						H	H	
		X	X*	H	X	X	Qn	The data stored to the internal flip-flop are displayed at the B bus.
			X*	H	X	L	L	The data at the A bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
						H	H	
L	L					OUTPUTS	INPUTS	The B bus are inputs and the A bus are outputs.
		X*	X	X	L	L	L	The data at the B bus are displayed at the A bus
						H	H	
		X*		X	L	L	L	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flop on low to high transition of the clock pulse.
						H	H	
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are displayed at the A bus
			X*	X	H	L	L	The data at the B bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
						H	H	

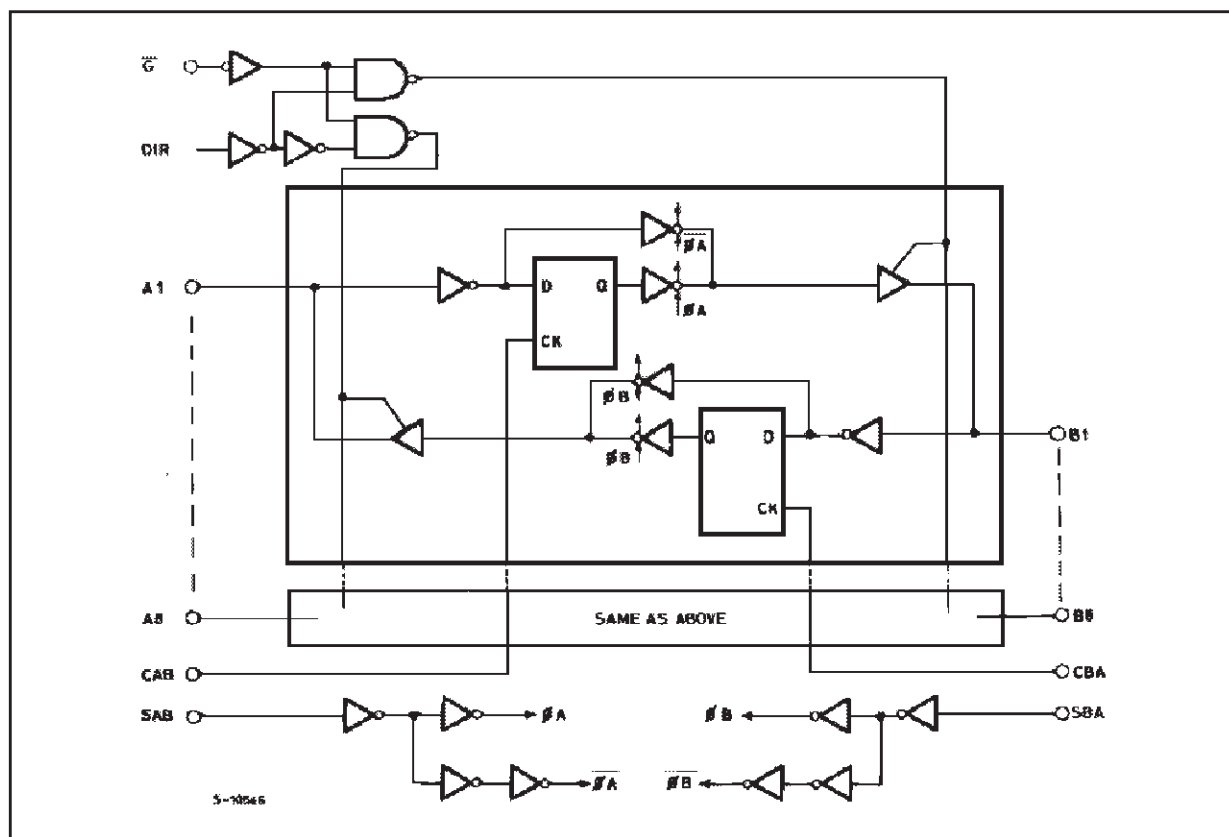
X : Don't Care

Z : High Impedance

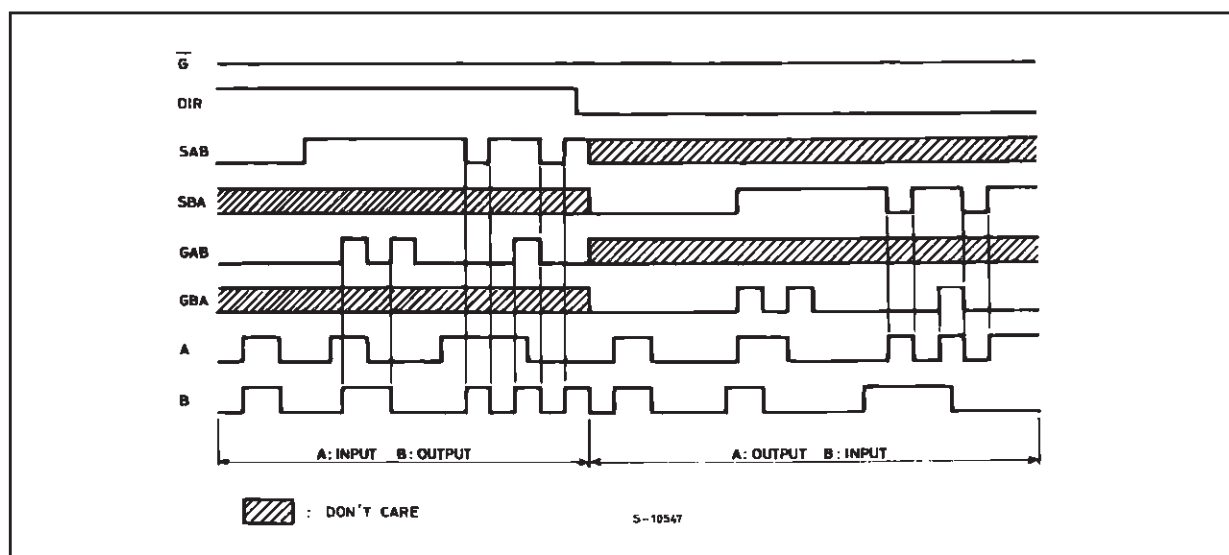
Qn : The data stored to the internal flip-flops by most recent low to high transition of the clock inputs

* : The data at the A and B bus will be stored to the internal flip-flops on every low to high transition of the clock inputs.

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V _{CC}	Supply Voltage		2 to 6	V
V _I	Input Voltage		0 to V _{CC}	V
V _O	Output Voltage		0 to V _{CC}	V
T _{op}	Operating Temperature		-55 to 125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2.0V	0 to 1000	ns
		V _{CC} = 4.5V	0 to 500	ns
		V _{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High Level Output Voltage	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		V	
		4.5	I _O =-20 μA	4.4	4.5		4.4		4.4			
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9			
		4.5	I _O =-6.0 mA	4.18	4.31		4.13		4.10			
		6.0	I _O =-7.8 mA	5.68	5.8		5.63		5.6			
V _{OL}	Low Level Output Voltage	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	V	
		4.5	I _O =20 μA		0.0	0.1		0.1		0.1		
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1		
		4.5	I _O =6.0 mA		0.17	0.26		0.37		0.37		
		6.0	I _O =7.8 mA		0.18	0.26		0.37		0.37		
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA	
I _{OZ}	High Impedance Output Leakage Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			± 0.5		± 5		± 10	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

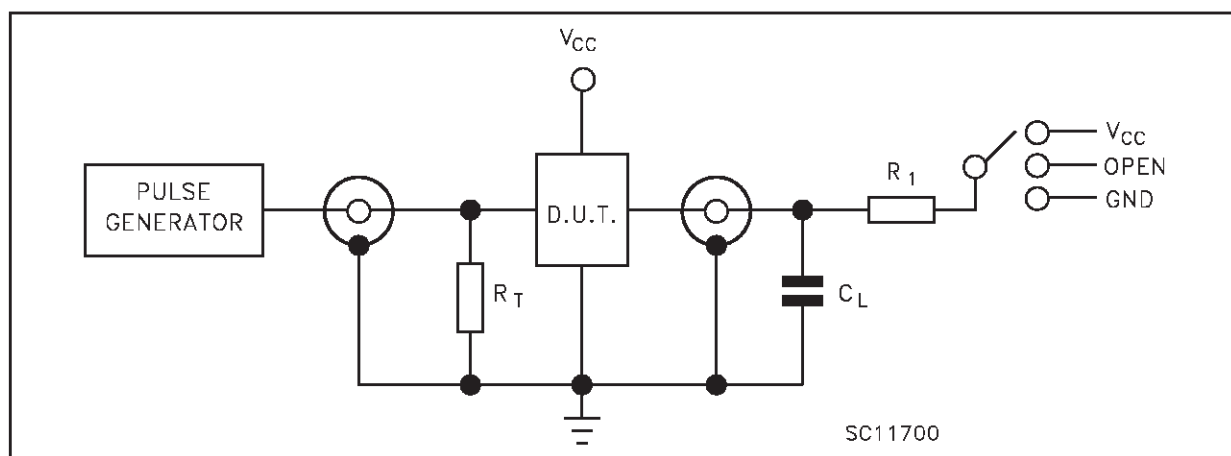
Symbol	Parameter	Test Condition			Value							Unit
		V _{CC} (V)	C _L (pF)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transition Time	2.0	50			25	60		75		80	ns
		4.5				7	12		15		20	
		6.0				6	10		13		15	
t _{PLH} t _{PHL}	Propagation Delay Time (BUS - BUS)	2.0	50			74	150		190		195	ns
		4.5				21	30		38		42	
		6.0				18	26		32		35	
		2.0	150			91	190		240		245	ns
		4.5				26	38		48		52	
		6.0				22	32		41		48	
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK - BUS)	2.0	50			98	210		265		275	ns
		4.5				28	42		53		60	
		6.0				24	36		45		50	
		2.0	150			116	250		315		325	ns
		4.5				33	50		63		75	
		6.0				28	43		54		60	
t _{PLH} t _{PHL}	Propagation Delay Time (SELECT - BUS)	2.0	50			81	170		215		225	ns
		4.5				23	34		43		56	
		6.0				20	29		37		45	
		2.0	150			98	210		265		275	ns
		4.5				28	42		53		60	
		6.0				24	36		45		50	
t _{PZL} t _{PZH}	High Impedance Output Enable Time (G, DIR)	2.0	50	R _L = 1 KΩ		84	175		220		225	ns
		4.5				24	35		44		50	
		6.0				20	30		37		45	
		2.0	150	R _L = 1 KΩ		102	215		270		280	ns
		4.5				29	43		54		60	
		6.0				25	37		46		55	
t _{PLZ} t _{PHZ}	High Impedance Output Disable Time (G, DIR)	2.0	50	R _L = 1 KΩ		60	175		220		230	ns
		4.5				23	35		44		50	
		6.0				20	30		37		45	
f _{MAX}	Maximum Clock Frequency	2.0	50		6	19		4.8		4.0		MHz
		4.5			30	67		24		20		
		6.0			35	79		28		25		
t _{W(H)} t _{W(L)}	Minimum Pulse Width	2.0	50			30	75		95		100	ns
		4.5				7	15		19		22	
		6.0				6	13		16		18	
t _s	Minimum Set-Up Time	2.0	50			16	50		65		70	ns
		4.5				4	10		13		15	
		6.0				3	9		11		13	
t _h	Minimum Hold Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance				5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)				39						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per bit)

TEST CIRCUIT

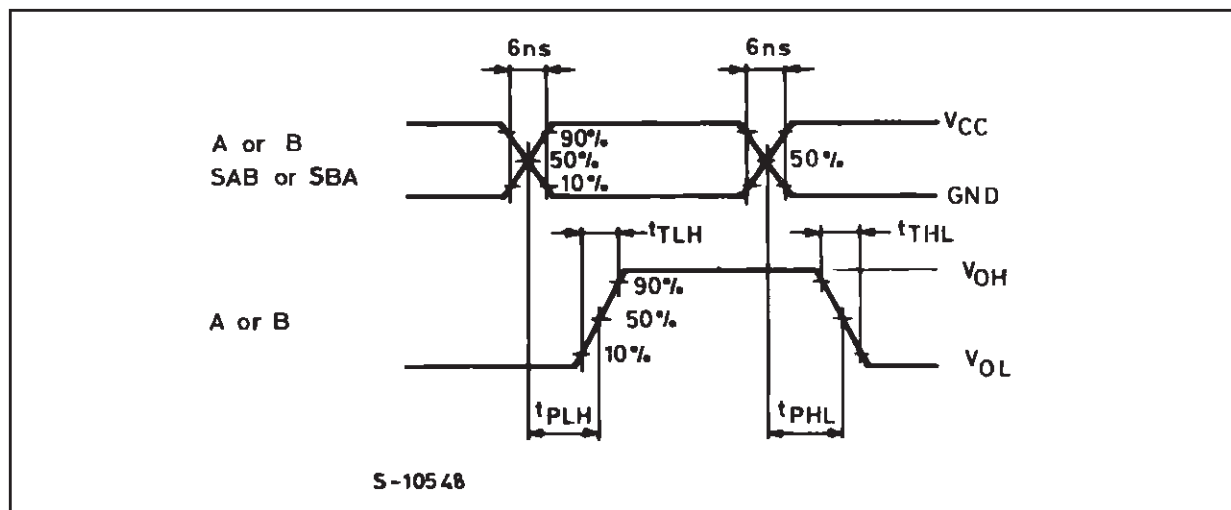
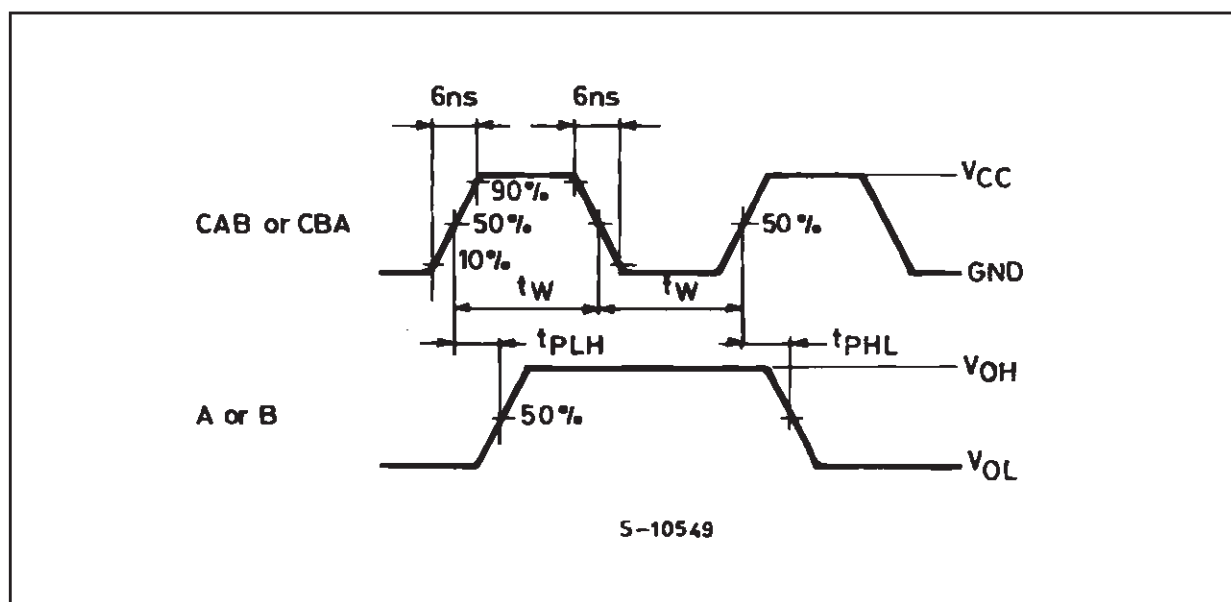


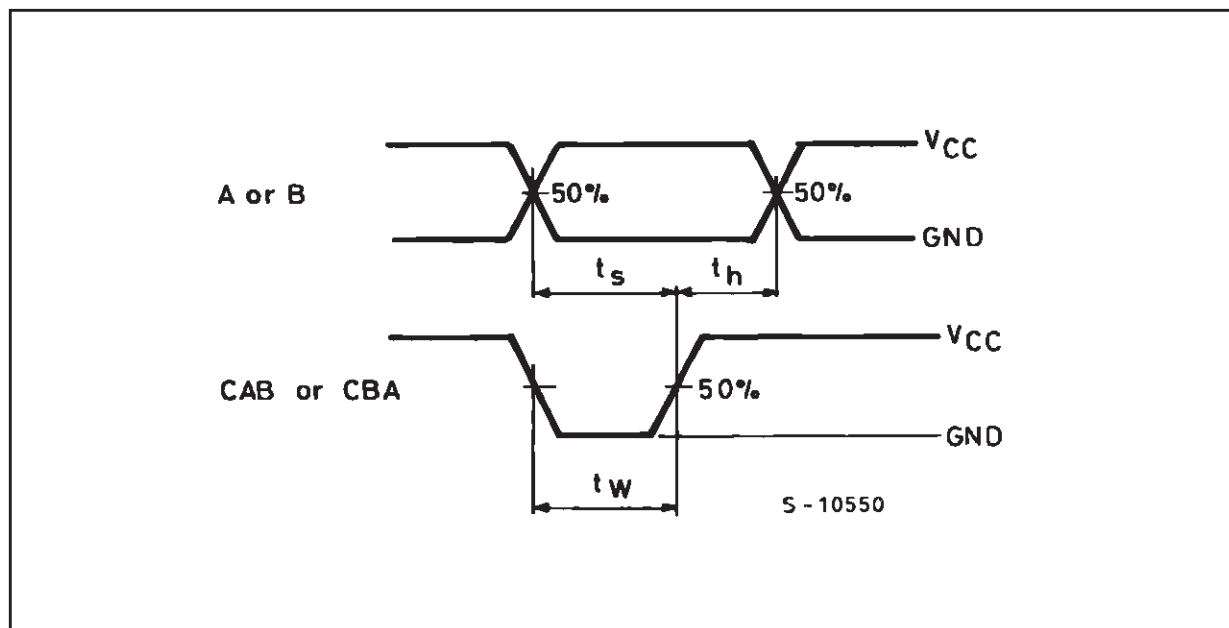
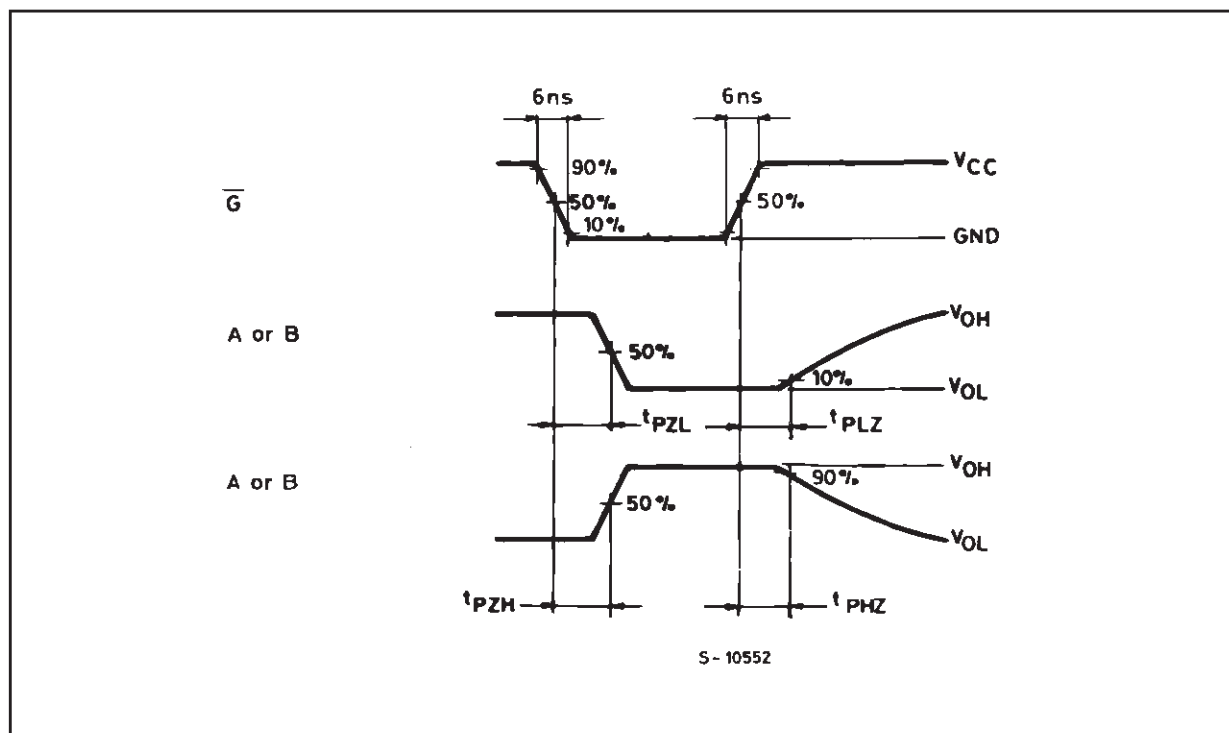
TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	V _{CC}
t _{PZH} , t _{PHZ}	GND

C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)

R₁ = 1KΩ or equivalent

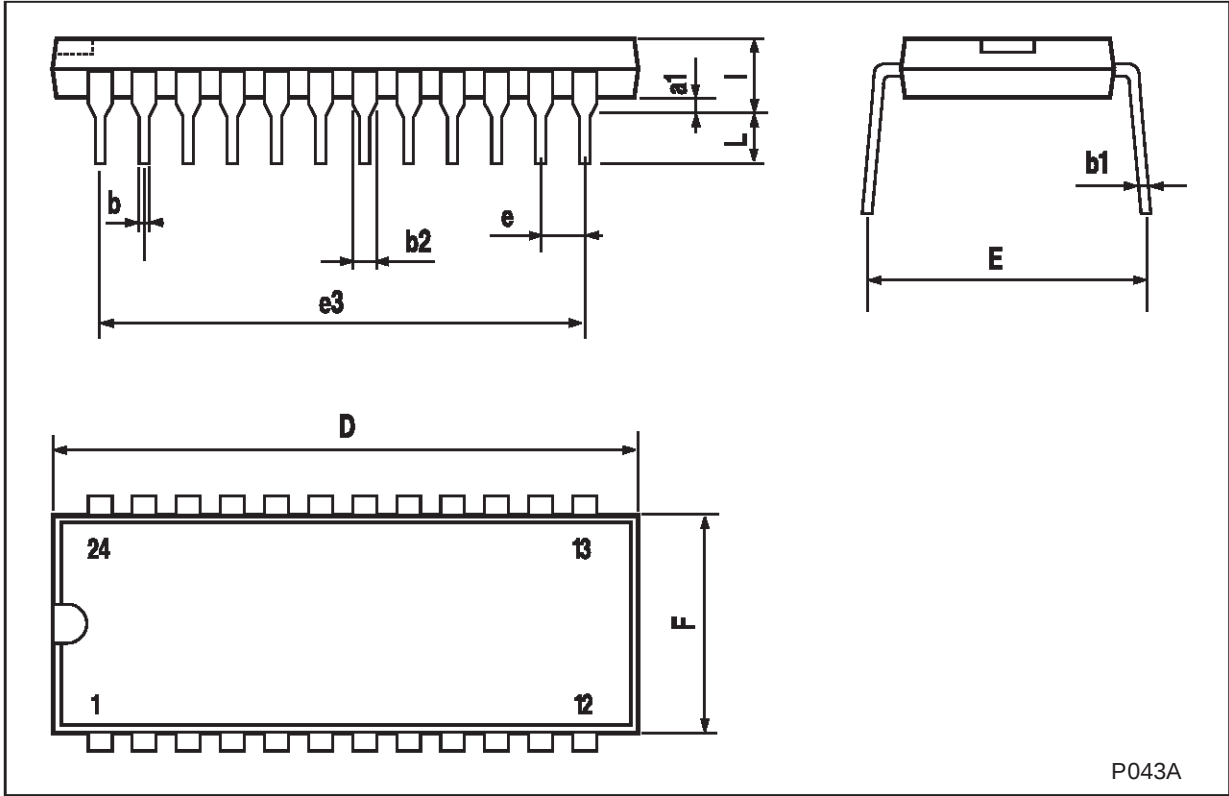
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1 : PROPAGATION DELAY TIME ($f=1\text{MHz}$; 50% duty cycle)WAVEFORM 2 : PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH ($f=1\text{MHz}$; 50% duty cycle)

WAVEFORM 3 : MINIMUM PULSE WIDTH, SETUP AND HOLD TIME ($f=1\text{MHz}$; 50% duty cycle)WAVEFORM 4 : OUTPUT ENABLE AND DISABLE TIME ($f=1\text{MHz}$; 50% duty cycle)

Plastic DIP-24 (0.25) MECHANICAL DATA

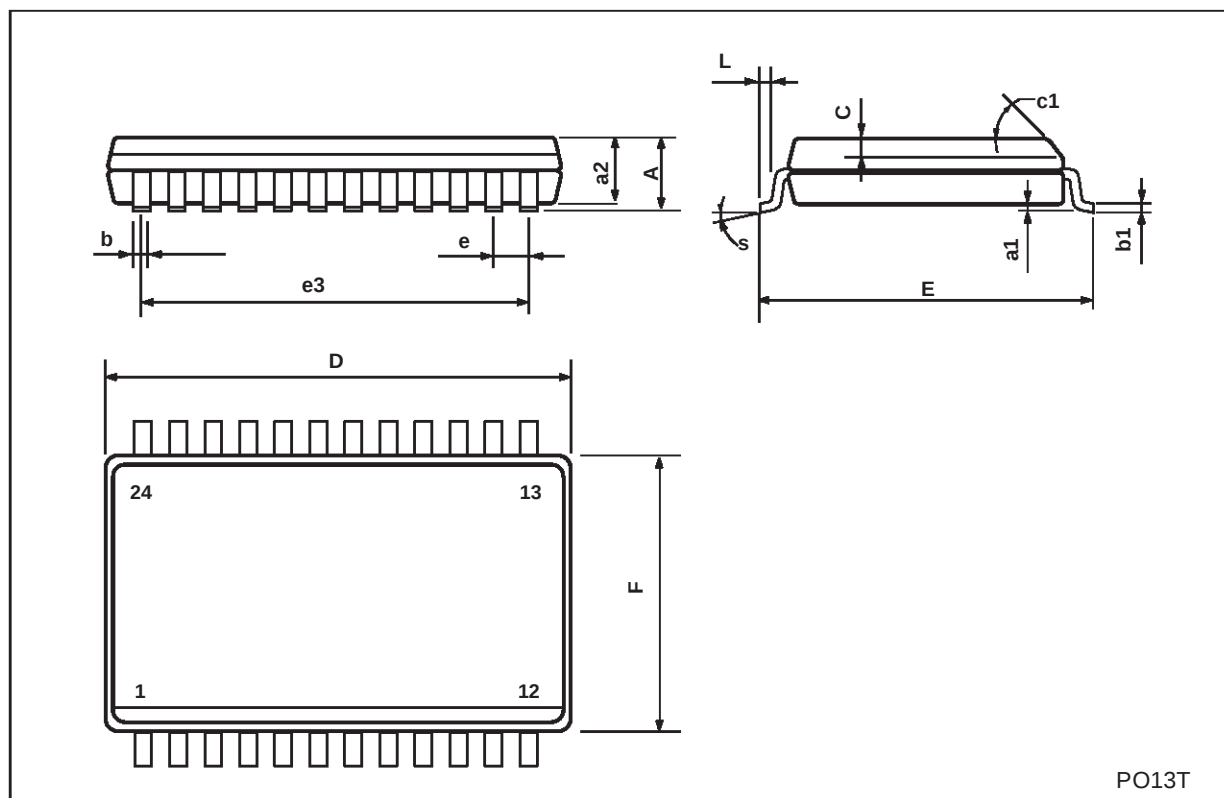
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.500	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



P043A

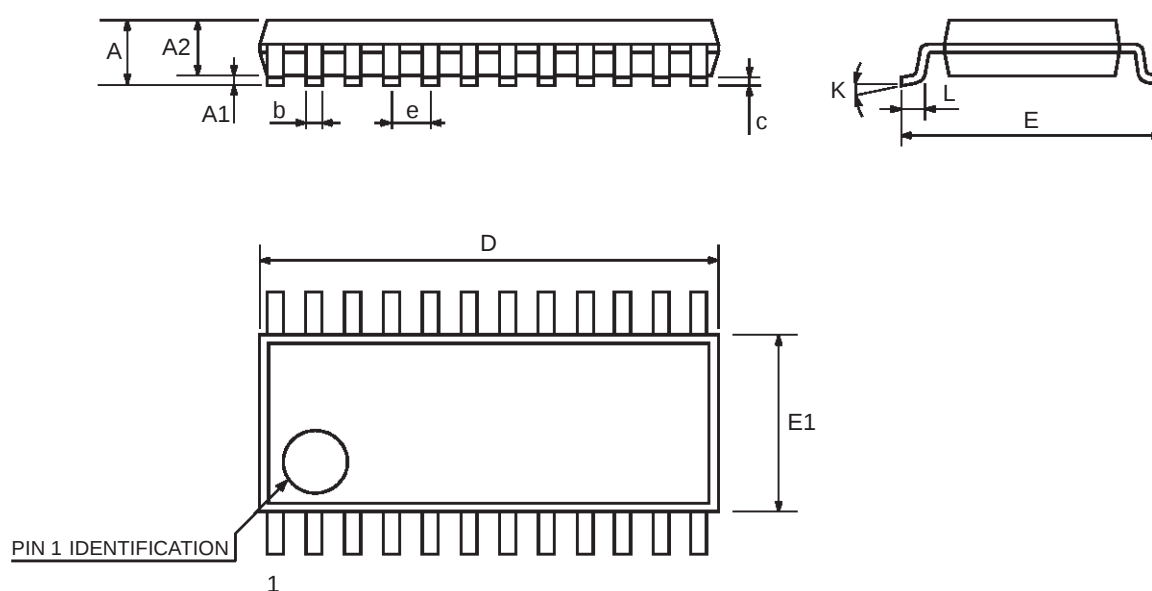
SO-24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max.)					



TSSOP24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	6.25		6.5	0.246		0.256
E1	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028



7047476A

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

