**Melexis**
Microelectronic Integrated Systems

## Features and Benefits

Complies with ISO 14443A/B, 15693 standards
Provision for new ISO18000-3 Mode 1 standard compliance
Programmable encoder for custom protocols
Low external component count
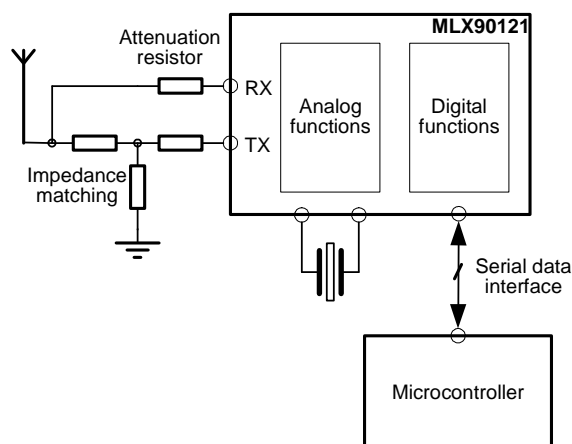Short to medium reading range applications

## Applications

Freight identification systems
Smart labels and write systems
Access control systems

## Ordering Information

| Part No. | Temperature Suffix | Package Code | Option code |
|----------|-------------------|--------------|-------------|
| MLX90121 | C (0℃ to 70℃) | FR (SSOP20) | -- |
| MLX90121 | E (-40℃ to 85℃) | FR (SSOP20) | -- |

## 1. Functional Diagram



## 2. Description

The MLX90121 is an ISO compliant contact-less smart labels and smart cards transceiver circuit. Applications range from freight identification systems to access control. The main features include user selectable modulation depth in write mode, whereas single sub-carrier ASK, FSK and PSK modulations are recognized in the read mode. The receiver is based on a diode envelope detector, followed by an IF filter and amplifier. A logarithmic amplifier is used for single sub-carrier ASK detection, ensuring fast and clean data recovery. The limiting output of the log amp is used for FSK and PSK recovery. The transmitter uses a built in open drain output transistor, which can provide up to 200 miliwatts of RF power to a 50 ohms load with a 5 volts power supply using the recommended matching network. This is suitable for most short to mid range applications. A simplified antenna and matching network can be used, at the expense of a reduced reading range, for example in hand-held reader applications. The chip is configured with a serial interface. A synchronization signal is available when the majority voting is used. Digital part contains ASK, FSK (423 / 484kHz) and PSK (847kHz) decoders and a programmable encoder to facilitate data handling with a low cost microcontroller. The encoder can be programmed with 6 different patterns. The chip can also be used as an analog front-end, in direct mode.

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## 3. Absolute Maximum Ratings

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage ($V_{DD}$ with respect to $V_{SS}$) | $V_{DD}$ | DC | -0.3 | 6 | V |
| Input voltage on any pin (except TX) | $V_{in}$ | | -0.3 | $V_{DD}$+0.3 | V |
| | | | | | |
| Maximum power dissipation | $P_{max}$ | | | 500 | mW |
| Maximum junction temperature | $T_j$ | | | +150 | ºC |
| Storage temperature | $T_{stor}$ | | -55 | +150 | ºC |

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 4. MLX90121 Electrical Specifications

$T_A$ = -40 ºC to +85 ºC, or 0ºC to +70 ºC according to the version, $V_{DD}$ = 5Volts, unless otherwise noted. On board resonator is used.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **General DC Parameters** | | | | | | |
| Operating supply voltage range | $V_{DD}$ | $V_{DD}$ with respect to $V_{SS}$ | 2.7 | 5 | 5.5 | V |
| Standby current consumption | $I_{stb}$ | $V_{DD}$ = 5.5 V – $T_A$ = +85 ºC | | 3 | 30 | µA |
| | | $T_A$ = +25 ºC | | 0.1 | 10 | µA |
| Idle mode current consumption | $I_{dle2}$ | $V_{DD}$ = 5.5V - Analog section off | | 3.5 | 8 | mA |
| Operating current | $I_{op}$ | | | 11 | 16 | mA |
| Transmit current | $I_{tr}$ | | | 80 | 120 | mA |

## 5. MLX90121 Specific Specifications

DC Operating Parameters $T_A$ = -40ºC to 85ºC, or 0ºC to +70ºC according to the version, $V_{DD}$ = 5V (unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Transmitter specifications** | | | | | | |
| Max peak voltage applied on drain of output transistor | | | | | 32 | V |
| Max output transistor power dissipation | | | | 500 | 600 | mW |
| Output transistor ON resistance | | Id = 50 mA | | 2 | 5 | Ω |
| Output power for five volts operation | | See note 1 | 180 | 200 | | mW |
| Amplitude modulation depth adjustment range in 10% mode, with external resistor connected between R_MOD pin and ground. | | See note 1 | 0 | | 90 | % |

| | | | | | | |
|---|---|---|---|---|---|---|
| Amplitude modulation depth in 10% mode with nominal external resistor (12Ω) | | See note 1 | 10 | 12 | 16 | % |
| Minimum depth for 100% ASK | | See note 1 | 40 | | | dB |
| Rise and fall time for 100% ASK | | See note 1 | | 2.5 | 4 | µs |
| Rise and fall time for 10% modulation depth ( nominal external resistor used) | | See note 1 | | 1 | 1.5 | µs |
| | | | | | | |
| **Receiver specifications** | | | | | | |
| Small signal input impedance (RX) | | | | 100 | | kΩ |
| Input RF voltage range (RX – $V_{SS}$) | | With 1k series external resistor | | ± 3 | | V |
| Receiver sensitivity (FSK) | | See note 2 | -40 | -60 | | dBm |
| Base-band receiver sensitivity (FSK) | | See note 3 | -40 | -60 | | dBm |
| FSK IF filter cut off points | | | | 200-1400 | | kHz |
| Total gain, in FSK mode | | | | 120 | | dB |
| | | | | | | |
| **Log amplifier section** | | | | | | |
| Limiting gain | | | 70 | 80 | | dB |
| Sensitivity for ASK recovery | | | | -60 | | dBm |
| Sensitivity for FSK recovery | | | | -60 | | dBm |
| | | | | | | |
| **Serial link and digital I/O** | | | | | | |
| Output voltage low | $V_{ol}$ | $I_{ol}$max=1mA | 0 | 0.2 | 0.4 | V |
| Output voltage high | $V_{oh}$ | | 4.6 | 4.8 | 5 | V |
| Output current drive | $I_{ol}$ | $V_{ol} \leq 0.4$ Volt | 1 | | | mA |
| Input voltage high | $V_{ih}$ | | $0.7 * V_{DD}$ | | $V_{DD} + 0.3$ | V |
| Input voltage low | $V_{il}$ | | -0.3 | | $0.3 * V_{DD}$ | V |
| CK frequency | $F_{CK}$ | | | | 1 | MHz |
| General setup time | $T_s$ | | 60 | | | ns |
| General setup time | $T_h$ | | 60 | | | ns |
| Pulse time between successive registers writing | $T_{mw}$ | | 5 | | | µs |
| | | | | | | |

| Crystal Oscillator | | | | | | | |
|---|---|---|---|---|---|---|---|
| Frequency range | $F_{xtal}$ | | | 4 | 13.56 | 16 | MHz |
| Start-up time | $T_{start}$ | | | | 2 | 5 | ms |
| Xtal series resistance | | | | | 50 | 100 | $\Omega$ |
| | | | | | | | |
| **External clock signal specifications** | | **see note 4** | | | | | |
| Min sine wave amplitude, AC coupled Input on pin XTAL2 | | | | 1 | | $V_{DD}$ | $V_{PP}$ |
| Min sine wave amplitude, DC coupled Input on pin XTAL2 | | Input has to be centered around Vdd/2 | | 1 | | $V_{DD}$ | $V_{PP}$ |
| | | | | | | | |
| **XBUF output specifications** | | | | | | | |
| XBUF Low Level (Col) | | 1K load resistor | | | 0.1 | | V |
| XBUF High Level (Coh) | | 1K load resistor | | | 4.8 | | V |
| Rise and fall times (10%-90%) | | 1K load resistor//12pF | | | 3 | | ns |
| | | | | | | | |

*Notes*

1. Parameter measured using recommended output matching network.

2. This parameter is specified with the chip wired as specified in the typical application circuit provided below, with the transmitter switched on. It cannot be measured during the final test.

3. This parameter is measured at base band for all specified modulation modes. The measurement is made at a test pin output with the input diode detector bypassed.

4. The external clock symmetry is of paramount importance. It has a direct influence on the transmitter output power. When using a sine wave as external clock input, it must not show visible distortion. In case a square wave is used, its duty cycle has to be equal to 50%.

## 6. General Description

### Power supply

The 90121 requires a nominal 3 or 5 volts external power supply. Operation is guaranteed between 2.7 and 5.5 Volts. The current drain depends on the antenna impedance and the output matching network configuration. Care must be taken about the power supply: power supply ripple and noise will severely degrade the overall system performance.

### Transmitter

The output transistor is a low Ron MOSFET. The drain is directly accessible on the TX pin. A recommended application schematic optimized to drive a resistive fifty ohms antenna with a five volts power supply is provided as a part of this specification. A simple resonant circuit or/and a simpler matching network can be connected to the output. In that case, the general performance and harmonic suppression will be reduced.

100 % modulation is achieved by means of gating the square wave drive of the output transistor.

A variable modulation depth is obtained by means of switching a resistor in series with the output transistors' source connection. An external resistor provides the default modulation depth setting. Increasing this external resistor will increase the modulation depth.

### Receiver

The receiver input is typically connected to the antenna through an external resistor. The modulation from the tag is then recovered by means of a diode envelope detector.

### FSK and PSK recovery

The demodulated input signal is amplified and band pass filtered. The signal is then hard limited by a logarithmic amplifier, and fed to the digital section. PSK decoded, FSK decoded or a direct FSK signal can be used for further decoding.

### ASK recovery

For ASK recovery, the high pass sections of the band pass filters are removed, to avoid falling edge degradation by the filter settling time. The signal is DC coupled and fed to the input of the logarithmic amplifier. The logarithmic amplifier works as a high gain amplifier and at the same time it generates the envelope of the ASK signal. The demodulated output from the log amp is then fed to a comparator. To avoid signal degradation, the time constant of the comparator has to be switched from fast response during acquisition to a slow time constant during the tags response. This is done by switching the LTC signal. Switching can be done automatically by the MLX90121 or by an external signal on the LTC input. The recovered data stream is fed to the digital section for further processing.

### Majority Voting

Both FSK/PSK or ASK can use the Majority Voting function that will filter for noise and jitter, that will correct distorted signals and will hence improve performance.

### Reference clock and internal oscillator

The reference clock may be obtained externally by applying a suitable clock signal to the XTAL1 pin. A sine wave centered at VCC/2 or a CMOS logic compatible signal is an acceptable external system clock. The built-in reference oscillator will work either with a quartz crystal or a ceramic resonator. The nominal system clock frequency is 13.56 MHz.

### Reset defaults and power management

After a power on reset has been performed, the device is put in its default configuration. There are three power modes available. In the transmission mode, the device is fully powered. In the idle mode, only the reference oscillator and the receiver chain is running. This allows for a fast start up. In the power down mode, the device internal bias system is completely switched off, offering essentially a zero state.

### Serial communication interface

The communication interface normally uses 6 wires:

- CK: serial clock input
- DIN: data input
- DOUT: data output
- DSYNC: synchronization output for DOUT
- MODE: configuration or communication selection input
- RTB: reception or transmission selection input.

## 7. Applications Information

This schematic has been optimized to drive a fifty ohms resistive antenna, using a five volts power supply.

### Functional description

The transmitter output TX is connected to the supply by means of a choke L3. C3 is added to avoid a high dV/dt at the TX output in case of a sudden interruption of the current in the choke. C3 is chosen high enough to protect the chip, but low enough too keep the resonance of L3-C3 well above 13.56 MHz.

The transmitter signal is coupled with DC blocking capacitor C2 to the antenna matching network, which is a T network made up by L2, CV1 and L1. CV1 allows for a proper matching between the 50Ohm antenna and the output impedance of the transmitter stage.

The receiver part of the chip gets his signal directly from the antenna by means of R1. It limits the voltage swing at the RX pin to a level in between the supplies.

One should take care to properly decouple the power supplies of the chip. Especially the Vdd1 supply which is used for the transmitter output. Any amplitude noise on that supply is AM modulated on the carrier and will hence be perceived as noise by the receiver part. The same holds for any phase noise that gets introduced into the quartz oscillator.

For the signal that go to- and from the microcontroller: one should take care to keep them as far as possible from the analog parts and the quartz oscillator. To do a first evaluation, it is highly recommended to use the MLX90121 evaluation board that can be order from Melexis. The clock for the microcontroller can eventually be derived from the XBUF pin. This pin provides for the 13.56MHz buffered clock or 13.56MHz divided by 2.
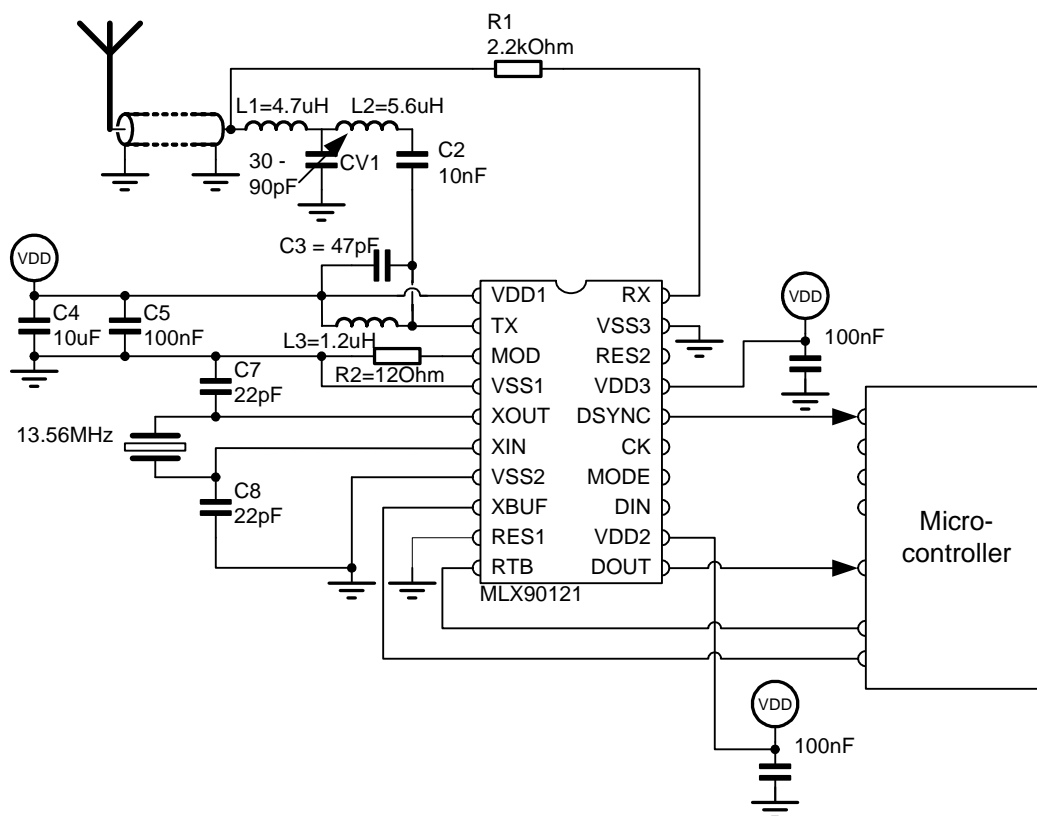
## 8. Block Diagram
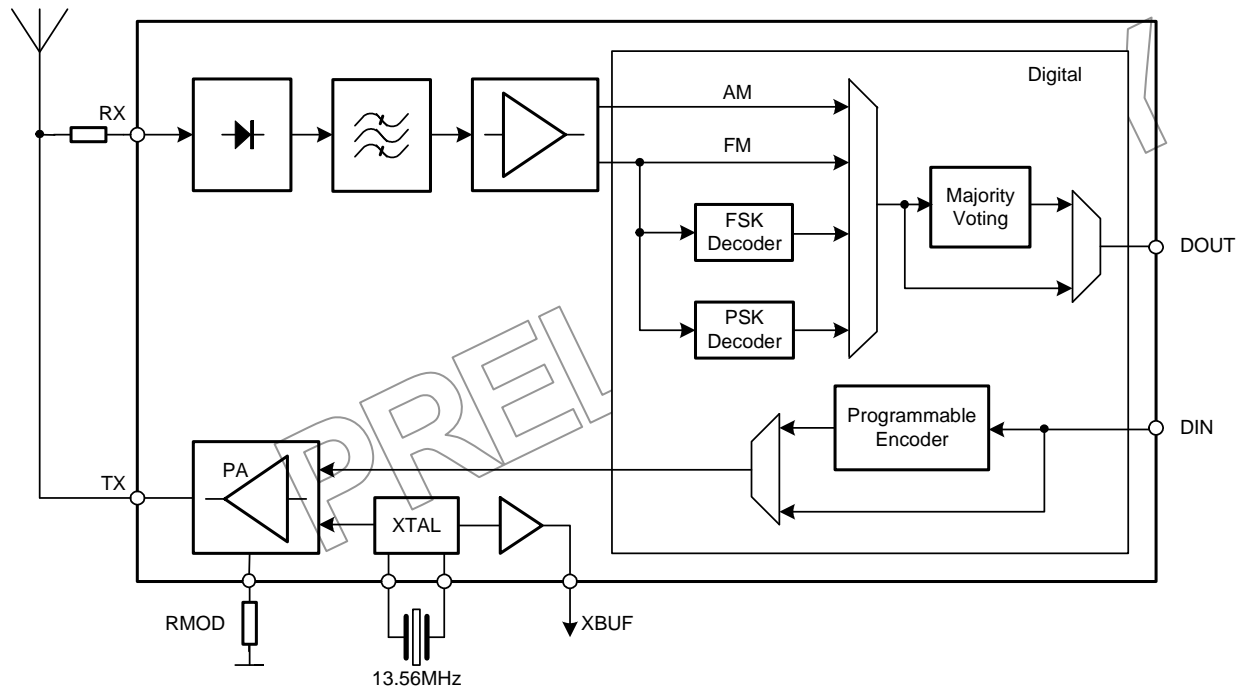


## 9. Digital Interface

The MLX90121 is driven by four signals: MODE and RTB pins are used to select the operating mode and DIN and CK pins are used to configure the chip and to transmit data.

The MLX90121 has two signal outputs. DOUT contains the decoded response of the transponder and DSYNC is used as a synchronization output by the microcontroller.

| Pin Name | I/O | Function |
|---|---|---|
| MODE | I | 0 = Configuration Mode, 1 = Communication Mode |
| RTB | I | 0 = Transmission Mode, 1 = Reception Mode |
| DIN | I | Data Input for Transmission or Configuration |
| CK | I | Clock and Trigger |
| DOUT | O | Data Output from Reception or Configuration |
| DSYNC | O | Data Synchronization Clock for Transmission or Reception |

*Function Summary*

| MODE | RTB | Function |
|---|---|---|
| 0 | 0 | Configuration |
| 1 | 0 | Transmission |
| 0 | 1 | Reserved (*) |
| 1 | 1 | Reception |

(*) the reserved mode is for manufacturing purpose only and should not be applied by the user

# 10.  Operating Modes

## 10.1. Definitions

There are two main operating modes:

- MODE = 0          : Configuration Mode
- MODE = 1          : Communication Mode

The configuration mode allows for writing in the configuration registers. It will configure all parameters in the transceiver.

The communication mode allows communicating with a transponder. Different options are available:

- Direct transmission: The transmission protocol is handled by an external microcontroller.
- Hardware transmission: The low level protocol is handled by an internal programmable encoder. It allows for using a low cost microcontroller.
- Direct Reception: The reception protocol is handled by an external microcontroller.
- Hardware reception: FSK/PSK decoders and Majority Voting can be enabled to allow for using a low cost microcontroller.

## 10.2. Configuration Mode

### Registers Addresses

For configuration purposes, users have access to 13 eight bit registers, which can be addressed using a 4 bit address.

| Address | Register name |
|---------|---------------|
| 0 | AnalogConfig |
| 1 | PowerState |
| 2 | Reserved (*) |
| 3 | DigitalConfig |
| 4 | EncoderSym0 |
| 5 | EncoderSym1 |
| 6 | EncoderSym2 |
| 7 | EncoderSym3 |
| 8 | EncoderSym4 |
| 9 | EncoderSym5 |
| 10 | EncoderTimeRef |
| 11 | DecoderTimeRef |
| 12 | LTC |

(*) the reserved mode is for manufacturing purpose only and should not be used.

### Write Configuration Registers

First the MODE line is asserted low to enable the configuration mode. Then data is fed serially into the chip with the CK and DIN lines. Data on the DIN line is read on the rising edge of CK. The first four first bits on DIN are the register address and the eight following bits are the data. Address and data fields are written MSB (Most Significant Bit) first.
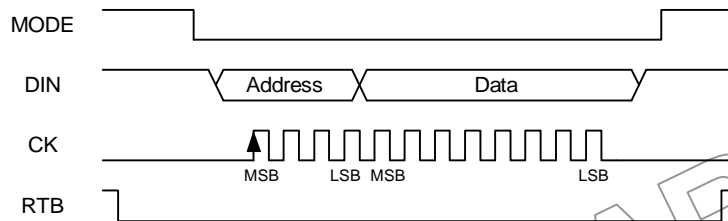
After sending address and data, the MODE line is asserted high and the chip is ready to receive the next register configuration.

| Signal | Assign |
|--------|--------|
| MODE | 0 |
| RTB | 0 |
| DIN | 4-bit Address + 8-bit Data |
| CK | 12 clock pulses |
| DOUT | x |
| DSYNC | x |

### Notes
1. If a register does not contain eight bits, write '0' in the unused bit.
2. When MODE is asserted high, the chip is in communication mode. If the encoder is disabled (by default), DIN has to be kept at '1' to avoid any modulation on the antenna.
3. In case of successive registers writings, it is mandatory to have MODE asserted high for at least 5µs in between each access, as shows in the following diagram.
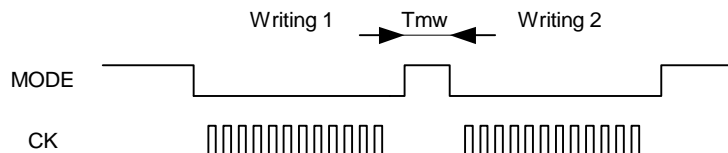


## 10.3. Communication modes

### 10.3.1. Transmission

#### 10.3.1.a. Analog Setup

For the transmission, the modulation depth has to be chosen. This is done by the TModIndex bit of the AnalogConfig register, which selects the modulation index: 10% or 100%.

The modulation index can be further tuned by means of the external RMOD resistor.

### 10.3.1.b. Direct Transmission

Before analog processing, data transmission can be either direct or pre-processed by means of hardware accelerators. Direct transmission can be performed with the following setup:

| Signal | Assign |
|---|---|
| MODE | 1 |
| RTB | 0 |
| DIN | Data to transmit |
| CK | 0 |
| OUT | x |
| DSYNC | x |

Data have to be transmitted in real time by the microcontroller on DIN input. The modulation is done when DIN is asserted low, so by default DIN has to be asserted high. If a configuration register has to be written, keep DIN high when MODE is asserted low. In configuration mode, the field is held without modulation independently of DIN.

### 10.3.1.c. Hardware Encoding Transmission

This programmable encoder allows predefining six different patterns of 8 bits. The encoder is selected by setting the bit EncoderEn in the DigitalConfig register.

#### Symbol Setup

The six symbols are called EncoderSym0 to EncoderSym5. There is a seventh symbol which is hard-coded to 0xFF (11111111).

A symbol is built with 8 bits like shows in the following figure.
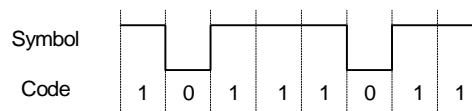


#### ISO Examples

| ISO15693 (1 out of 4) | | |
|---|---|---|
| Symbol | Name | Code |
| Sym0 | Pulse1 | 10111111 |
| Sym1 | Pulse2 | 11101111 |
| Sym2 | Pulse3 | 11111011 |
| Sym3 | Pulse4 | 11111110 |
| Sym4 | SOF | 01111011 |
| Sym5 | EOF | 11011111 |

**ISO14443 A**

| Symbol | Name | Code |
|--------|------|------|
| Sym0 | X | 11110111 |
| Sym1 | Y | 11111111 |
| Sym2 | Z | 01111111 |

**ISO14443 B**

| Symbol | Name | Code |
|--------|------|------|
| Sym0 | L | 00000000 |
| Sym1 | H | 11111111 |

### Time Reference Setup

The time reference is defined in the EncoderTimeRef register. The time reference contains one bit time. Hence $Symbol\_Time = 8 * Bit\_Time$

The bit time is defined by the EncTimeRef parameter. EncTimeRef is an integer value, it is calculated as follows:

$$EncTime\,\mathrm{Re}\,f = \left( \frac{Bit\_Time}{1/3.39Mhz} \right) - 1$$

EncTimeRef is coded on 5 bits. This means that Bit_Time_max = 9.44 us and Symbol_Time_max = 75.52us

### ISO Examples

| Norm | Symbol Time | Bit Time | EncTimeRef |
|------|-------------|----------|------------|
| ISO15693 (1 out of 4) | 75.52 µs | 9.44 µs | 0x31 (11111) |
| ISO14443 | 9.44 µs | 1.18 µs | 0x03 (00011) |

# MLX90121
## 13.56MHz RFID Transceiver

### Symbol Transmission

CK and DIN inputs are used to transmit symbols. As seven symbols are available, they are coded on 3 bits. For fast protocol requiring few symbols, like in ISO14443 type B it is not necessary to transmit every time three bits. For example, if two symbols are required, only one bit is transmitted as shown in the following table.

| Symbol | Short | Start |
|--------|-------|-------|
| Sym0 | 0 | 000 |
| Sym1 | 1 | 001 |
| Sym2 | 10 | 010 |
| Sym3 | 11 | 011 |
| Sym4 | 100 | 100 |
| Sym5 | 101 | 101 |
| Sym6 | 111 | 111 |

To start a transmission, it is necessary to send the first symbol with three bits to initialise the communication. On every rising edge of DSYNC, the following symbol can be send. To stop transmission, do not send any clock after EOF symbol.
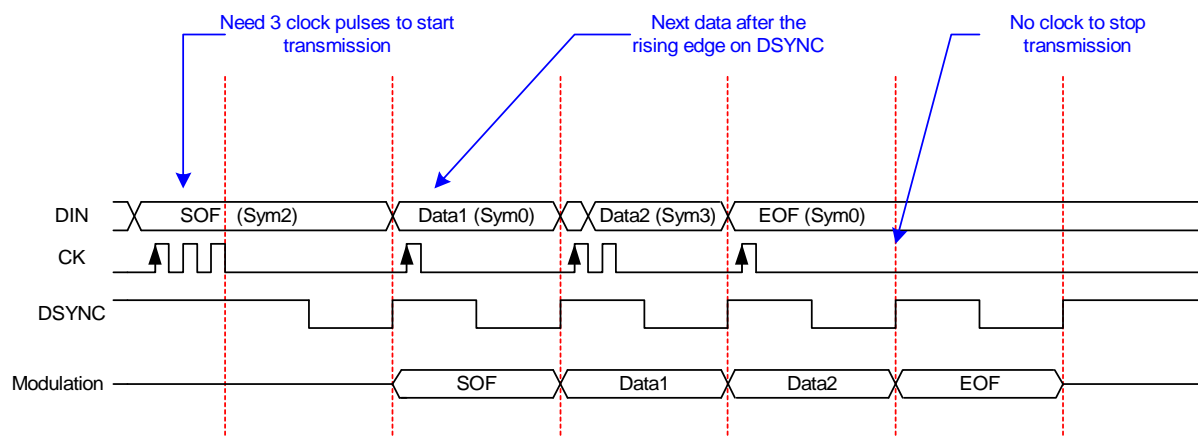


| Signal | Assign |
|--------|--------|
| MODE | 1 |
| RTB | 0 |
| DIN | Symbol to transmit |
| CK | Clock |
| DOUT | x |
| DSYNC | Symbol Synchronization |

### 10.3.2. Reception

#### 10.3.2.a. Analog Setup

For a proper reception, the analog chain has to be configured according to the following parameters in the AnalogConfig register:

- ByPassAll: It bypasses the analog filters in the analog chain. Must be enabled for AM reception.
- RDataRate: It selects the reception data rate – See table.
- RSubCarrier: It selects the reception sub-carrier frequency – See table.

| RDataRate | RSubCarrier | Data Rate | Sub-carrier |
|-----------|-------------|-----------|-------------|
| 0 | 0 | 26 kb/s | 423 / 484 kHz |
| 1 | 0 | 6.6 kb/s | 423 / 484 kHz |
| 0 | 1 | 106 kb/s | 847 kHz |
| *1* | *1* | *Not used* | *Not used* |

#### Note

- If RSubCarrier is set, the data rate is automatically set to 106 kb/s (ISO14443).

#### ISO Examples

| Standard | ByPassAll | RDataRater | RSubCarrier |
|----------|-----------|------------|-------------|
| ISO15693-Single Sub-carrier-Low Data Rate | 1 | 1 | 0 |
| ISO15693-Single Sub-carrier-High Data Rate | 1 | 0 | 0 |
| ISO15693-Dual Sub-carrier-Low Data Rate | 0 | 1 | 0 |
| ISO15693-Dual Sub-carrier-Low Data Rate | 0 | 0 | 0 |
| ISO14443-A | 1 | 0 | 1 |
| ISO14443-B | 0 | 0 | 1 |

#### 10.3.2.b. Direct Reception

After analog processing, data reception can be either direct or pre-processed by hardware accelerators, according to the configuration of the SelDOUT parameter in the DigitalConfig register.

| SelDout | Output | ISO Standard |
|---------|--------|--------------|
| 00 | AM (direct) | ISO15693-Single Sub-carrier and ISO14443-A |
| 01 | FM (direct) | -- |
| 10 | FSK (423/484 kHz) | ISO15693-Double Sub-carrier |
| 11 | PSK (847 kHz) | ISO14443-B |

#### Note

- The output phase of PSK decoder is either normal or inverted.

Direct reception is achieved with the following setup.

| Signal | Assign |
|--------|--------|
| MODE | 1 |
| RTB | 1 |
| DIN | 1 |
| CK | 0 |
| DOUT | Received data |
| DSYNC | x |

### 10.3.2.c. Reception with Majority Voting (MV)

Majority voting allows to:

- Filter noisy signal,
- Compensate jitter,
- Correct distorted signals.

At the beginning of the time slot (MVTime), an up / down counter is reset. When the input signal is asserted high, it is counting up and when the input signal is asserted low, it is counting down. At the end of time slot, the counter value is checked and the output value is set accordingly (low if counter is negative; high if counter is positive).
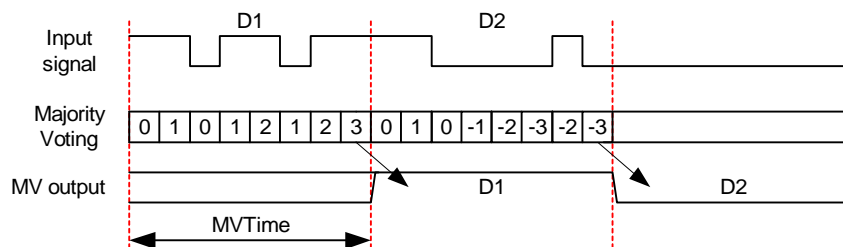


### Majority Voting Setup

The following parameters in the DigitalConfig register have to be set when using majority voting.

- MVEn: it enables the majority voting function.
- DecTimeRef: it defines the duration of the time slot (MVTime)

$$DecTime\operatorname{Re}f = \left( \frac{MVTime}{1/6.78Mhz} \right) - 1$$

$$MVTime\_\max = 37.76us$$

*ISO examples*

| Norm | MVTime | | DecTimeRef |
|------|--------|---|-----------|
| ISO15693 | 18.88 us | (half bit) | 127 |
| ISO14443A | 4.72 us | (half bit) | 31 |
| ISO14443B | 9.44 us | (full bit) | 63 |

*Note*

- For Manchester coding, majority voting is on half bit portions only.

In addition, the MVMode parameter in the DigitalConfig register allows to give more weight to low input levels.

*Note*

- It has to be set when using ISO14443-A standard configuration.

*MV Reception*

To start a reception with majority voting function, assert CK high at the beginning of the response. Then take data on every rising edge of DSYNC. Reception is stopped by asserting CK low on the last rising edge of DSYNC. Data output are delayed by DecTimeRef (see next figure).

This method assumes that the response time is known. If it is not the case, it is possible to do polling on DOUT in direct mode (CK is low).
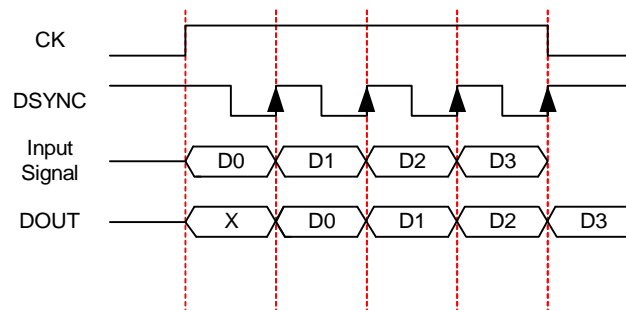
The TrigMode parameter in the DigitalConfig register selects how the majority voting is started.

- Manually: the microcontroller sends a rising edge on CK.
- Trigger: the microcontroller send an authorization to start on the first rising edge of the input signal. The authorization is done by sending a rising edge on CK.

### *Example in ISO15693-Single Sub-carrier*
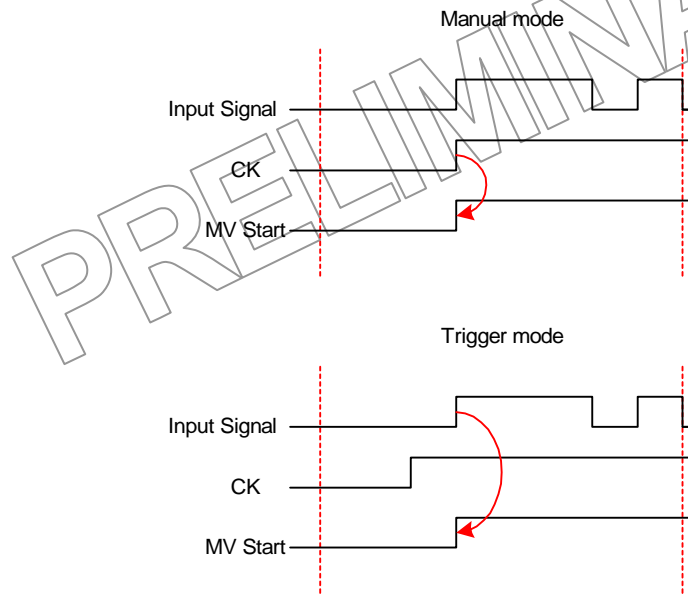


#### Note

Trigger mode is more precise but it can be used only if there is low noise on the input signal, before the first rising edge. In ASK decoding, low level of SOF is lost. In FSK the manual mode has to be used to avoid loosing the low level of SOF.

| Standard | Start mode recommendation | Reference for input signal |
|---|---|---|
| ISO15693-Single Sub-carrier | Manual | Rising edge |
| ISO15693-Double sub-carrier | Trigger | Rising edge |
| ISO14443-A | Trigger | Rising edge |
| ISO14443-B | Trigger | Rising / Falling edge |

#### *LTC*

LTC is the "low time constant" of the comparator. In ASK reception LTC has to be started on the first rising edge of the response.

LTC is controlled according to the following parameters in the LTC register:

- LTCEn: it enables the LTC circuit,
- LTCDelay: delay to activate LTC signal.

$$LTCDelay = \left( \frac{DelayTime}{1/6.78MHz} \right) - 1$$

DelayTime_max = 4.72 us

***Recommended delay for ISO standard***

| Standard | LTCDelay | LTCDelay |
|---|---|---|
| ISO15693-Single Sub-carrier | 4.72 us | 0x1F |
| ISO14443-A | 2.95 us | 0x13 |

## 10.4. Power States

This chip has three power modes. To select one of these modes write the PowerState parameter in the PowerState register.

| PowerState | Power Mode |
|---|---|
| 00 | Power On |
| 01 | Low Power |
| 11 | Power Down |

### Power Down

If the Power Down mode is selected, the crystal oscillator will be turned off. Therefore, it will be impossible to write the PowerState register to wake-up the chip. To wake up the chip, it is necessary to send a falling edge on CK when DIN is low. During Power Down mode, keep DIN high to avoid glitches on CK.
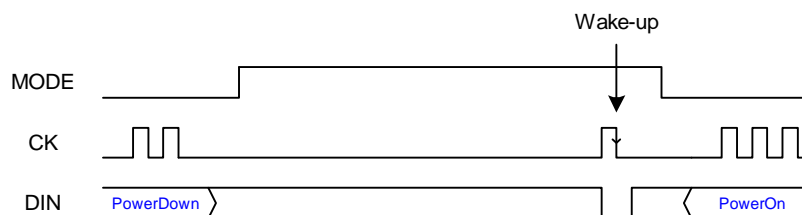
### Notes

After a wake-up, the chip has to be set in Power On (or Low Power) mode again by updating the PowerState register.

### Low Power

The oscillator is still on but all analog circuitry is off.

## 11. Configuration Registers

The following tables explain the meaning of the bit configurations in the 13 registers.

| Register : AnalogConfig | | | |
|---|---|---|---|
| **Address : 0** | | | |
| **Bit** | **Default** | **Name** | **Function** |
| 7 | 0 | XBUFSel | XBUF frequency selection (0 = 6.78MHz, 1 = 13.56MHz ) |
| 6 | 0 | XBUFEn | XBUF Enable (0= Disabled, 1 = Enabled) |
| 5 | 0 | TModIndex | Transmission Modulation Index (0 = 100%, 1= 10%) |
| 4 | 0 | RSubCarrier | Reception SubCarrier (0 = 450K , 1 = 847K) – See notes |
| 3 | 0 | RDataRate | Reception Data Rate (0 = High, 1 = Low) – See notes |
| 2 | 0 | ByPassAll | Bypass analog chain (0= Connected, 1 = Bypassed) – See notes |
| 1:0 | 0 | Reserved | Do not use - Should always be configured 11 |

*Notes*

| ByPassAll | Demodulation |
|---|---|
| 0 | FSK / PSK |
| 1 | ASK |

| RSubCarrier | RDataRate | Baud rate and sub-carrier frequency | |
|---|---|---|---|
| 0 | 0 | 26 kb/s | 423 / 484 kHz |
| 1 | 0 | 106 kb/s | 847 kHz |
| 0 | 1 | 6.6 kb/s | 423 / 484 kHz |

| Register : PowerState | | | |
|---|---|---|---|
| **Address : 1** | | | |
| Bit | Default | Name | Function |
| 7:2 | 0 | Reserved | Do not use |
| 1:0 | 0 | PowerState | Chip Power State – See notes |

*Notes*

| Power State [1:0] | | Mode |
|---|---|---|
| 0 | 0 | Low Power (oscillator on) |
| 0 | 1 | Transmitter On |
| *1* | *0* | *Unused* |
| 1 | 1 | Power Down (oscillator off) |

| Register : Reserved | | | |
|---|---|---|---|
| **Address : 2** | | | |
| **Bit** | **Default** | **Name** | **Function** |
| 7:0 | 0 | Reserved | Do not use |

| Register : DigitalConfig | | | |
|---|---|---|---|
| **Address : 3** | | | |
| **Bit** | **Default** | **Name** | **Function** |
| *7:6* | *0* | *--* | *Unused* |
| 5 | 0 | TrigMode | Trigger Mode (0 = Manual, 1 = Trigger) |
| 4 | 0 | MVMode | Majority Voting Mode (0 = other, 1 = ISO14443A) |
| 3 | 0 | MVEn | Majority Voting Enable (0=Disabled, 1 = Enabled) |
| 2:1 | 0 | SelDout | Reception Output Selection (see table) |
| 0 | 0 | EncoderEn | Hardware Encoder Enable (0=Disabled, 1 = Enabled) |

*Notes*

| SelDout | Output |
|---|---|
| 00 | AM (DATA): '1' = sub carrier ; '0' = no sub carrier |
| 01 | FM (LIMITER): rough digital signal |
| 10 | FSK decoded: '1' when f = 423kHz, '0' when f = 484kHz |
| 11 | PSK decoded |

| Register : EncoderSym | | | |
|---|---|---|---|
| **Address : 4 to 9** | | | |
| **Bit** | **Default** | **Name** | **Function** |
| 7:0 | 0 | EncoderSym0 | Encoder Symbol 0 |
| 7:0 | 0 | EncoderSym1 | Encoder Symbol 1 |
| 7:0 | 0 | EncoderSym2 | Encoder Symbol 2 |
| 7:0 | 0 | EncoderSym3 | Encoder Symbol 3 |
| 7:0 | 0 | EncoderSym4 | Encoder Symbol 4 |
| 7:0 | 0 | EncoderSym5 | Encoder Symbol 5 |

*Notes*

Symbol 6 is hard-coded to 0xFF (11111111).

| Register : EncoderTimeRef | | | |
|---|---|---|---|
| **Address : A** | | | |
| **Bit** | **Default** | **Name** | **Function** |
| *7:5* | *0* | -- | *Unused* |
| 4:0 | 0 | EncTimeRef | Encoder Time Reference |

| Register : DecoderTimeRef | | | |
|---|---|---|---|
| **Address : B** | | | |
| **Bit** | **Default** | **Name** | **Function** |
| 7:0 | 0 | DecTimeRef | Decoder Time Reference |

| Register : LTC | | | |
|---|---|---|---|
| **Address : C** | | | |
| **Bit** | **Default** | **Name** | **Function** |
| *7:6* | *0* | -- | *Unused* |
| 5:1 | 0 | LTCDelay | LTC Delay |
| 0 | 0 | LTCEn | LTC Enable (0=Disabled, 1 = Enabled) |

## 12. Configuration Registers: ISO Configuration Examples

| | Norm | ISO15693 | | ISO14443 | |
|---|---|---|---|---|---|
| | | **ASK** | **FSK** | | |
| **Address** | **Register** | Low Baud Rate 100% modulation | High Baud Rate 10% modulation | **A** | **B** |
| 0 | AnalogConfig | 0F | 23 | 17 | 33 |
| 1 | PowerState* | 01 | 01 | 01 | 01 |
| 2 | AnalogTest | 00 | 00 | 00 | 00 |
| 3 | DigitalConfig | 09 | 2D | 39 | 0F |
| 4 | EncoderSym0 | BF | BF | F3 | 00 |
| 5 | EncoderSym1 | EF | EF | FF | FF |
| 6 | EncoderSym2 | FB | FB | 3F | 00 |
| 7 | EncoderSym3 | FE | FE | 00 | 00 |
| 8 | EncoderSym4 | 7B | 7B | 00 | 00 |
| 9 | EncoderSym5 | DF | DF | 00 | 00 |
| 10 | EncoderTimeRef | 1F | 1F | 03 | 03 |
| 11 | DecoderTimeRef | 7F | 7E | 1F | 3F |
| 12 | LTC | 3F | 00 | 23 | 00 |

**Notes**
- All values are in hexadecimal notation.
- Transmitter is switched on.

## 13. Reliability Information

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)
- CECC00802
  Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- EIA/JEDEC JESD22-B106
  Resistance to soldering temperature for through-hole mounted devices
- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices
- MIL 883 Method 2003 / EIA/JEDEC JESD22-B102
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Based on Melexis commitment to environmental responsibility, European legislation (Directive on the Restriction of the Use of Certain Hazardous substances, RoHS) and customer requests, Melexis has installed a Roadmap to qualify their package families for lead free processes also.
Various lead free generic qualifications are running, current results on request.

For more information on manufacturability/solderability see quality page at our website:
http://www.melexis.com/html/pdf/MLXleadfree-statement.pdf

## 14. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

## 15. Package Information

The device is packaged in a 20 pin SSO-package.

```
  1 VDD1            RX 20
  2 TX            VSS3 19
  3 MOD           RES2 18
  4 VSS1          VDD3 17
  5 XOUT         DSYNC 16
  6 XIN             CK 15
  7 VSS2          MODE 14
  8 XBUF           DIN 13
  9 RES1          VDD2 12
 10 RTB           DOUT 11
```

| Pin # | Symbol | Pin Type | Description |
|-------|--------|----------|-------------|
| 1 | VDD1 | Supply | Transmitter power supply |
| 2 | TX | Ana-Out | Output transistor drain connection |
| 3 | MOD | Ana-In | External resistor to set  modulation depth |
| 4 | VSS1 | Supply | Transmitter section ground |
| 5 | XOUT | Dig-Out | Output of crystal resonator |
| 6 | XIN | Dig-In | Input of crystal resonator and external system clock input |
| 7 | VSS2 | Supply | Digital section ground |
| 8 | XBUF | Dig-Out | Buffered output of crystal oscillator |
| 9 | RES1 | Reserved | Should be grounded  for normal operation |
| 10 | RTB | Dig-In | Receive/Transmit selection |
| 11 | DOUT | Dig-Out | Data output |
| 12 | VDD2 | Supply | Digital section power supply |
| 13 | DIN | Dig-In | Data input for registers or modulation |
| 14 | MODE | Dig-In | Configuration/Communication selection |
| 15 | CK | Dig-In | Serial clock input |
| 16 | DSYNC | Dig-Out | Data synchronization output |
| 17 | VDD3 | Supply | Receiver section power supply |
| 18 | RES2 | Reserved | Should be left unconnected for normal operation |
| 19 | VSS3 | Supply | Receiver section ground |
| 20 | RX | Ana-In | Receiver input |

The mechanical dimensions of this package are depicted on the following page.

PACKAGE OUTLINE, 5.30mm (.209") BODY, SSOP — 32289 — REV. 05 — 1 of 2

**THIS TABLE IN MILLIMETERS**

| | COMMON DIMENSIONS | | | NOTE | VARIATIONS | D | | | N |
|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | | | MIN. | NOM. | MAX. | |
| A | 1.73 | 1.86 | 1.99 | | AA | 6.07 | 6.20 | 6.33 | 14 |
| A₁ | 0.05 | 0.13 | 0.21 | | AB | 6.07 | 6.20 | 6.33 | 16 |
| A₂ | 1.68 | 1.73 | 1.78 | | AC | 7.07 | 7.20 | 7.33 | 20 |
| b | 0.25 | – | 0.38 | 8,10 | AD | 8.07 | 8.20 | 8.33 | 24 |
| b₁ | 0.25 | 0.30 | 0.33 | 10 | AE | 10.07 | 10.20 | 10.33 | 28 |
| c | 0.09 | – | 0.20 | 10 | AF | 10.07 | 10.20 | 10.33 | 30 |
| c₁ | 0.09 | 0.15 | 0.16 | 10 | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | | |
| E | 5.20 | 5.30 | 5.38 | 4 | | | | | |
| e | 0.65 BSC | | | | | | | | |
| H | 7.65 | 7.80 | 7.90 | | | | | | |
| L | 0.63 | 0.75 | 0.95 | 5 | | | | | |
| L₁ | 1.25 REF. | | | | | | | | |
| N | SEE VARIATIONS | | | 6 | | | | | |
| α | 0° | 4° | 8° | | | | | | |
| R | 0.09 | 0.15 | | | | | | | |

VARIATION AF IS DESIGNED BUT NOT TOOLED

**THIS TABLE IN INCHES**

| | COMMON DIMENSIONS | | | NOTE | VARIATIONS | D | | | N |
|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | | | MIN. | NOM. | MAX. | |
| A | .068 | .073 | .078 | | AA | .239 | .244 | .249 | 14 |
| A₁ | .002 | .005 | .008 | | AB | .239 | .244 | .249 | 16 |
| A₂ | .066 | .068 | .070 | | AC | .278 | .284 | .289 | 20 |
| b | .010 | – | .015 | 8,10 | AD | .318 | .323 | .328 | 24 |
| b₁ | .010 | .012 | .013 | 10 | AE | .397 | .402 | .407 | 28 |
| c | .004 | – | .008 | 10 | AF | .397 | .402 | .407 | 30 |
| c₁ | .004 | .006 | .006 | 10 | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | | |
| E | .205 | .209 | .212 | 4 | | | | | |
| e | .0256 BSC | | | | | | | | |
| H | .301 | .307 | .311 | | | | | | |
| L | .025 | .030 | .037 | 5 | | | | | |
| L₁ | .049 REF. | | | | | | | | |
| N | SEE VARIATIONS | | | 6 | | | | | |
| α | 0° | 4° | 8° | | | | | | |
| R | .004 | .006 | | | | | | | |

PACKAGE OUTLINE, 5.30mm (.209") BODY, SSOP — 32289 — REV. 05 — 2 of 2

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