



# ±15kV ESD Protected, +3V to +5.5V, 1μA, 250kbps, RS-232 Transmitters/Receivers

## ICL3221E, ICL3222E, ICL3223E, ICL3232E, ICL3241E, ICL3243E

The Intersil ICL32xxE devices are 3.0V to 5.5V powered RS-232 transmitters/receivers which meet EIA/TIA-232 and V.28/V.24 specifications, even at  $V_{CC} = 3.0V$ . Additionally, they provide ±15kV ESD protection (IEC61000-4-2 Air Gap and Human Body Model) on transmitter outputs and receiver inputs (RS-232 pins). Targeted applications are PDAs, Palmtops, and notebook and laptop computers where the low operational, and even lower standby, power consumption is critical. Efficient on-chip charge pumps, coupled with manual and automatic power-down functions (except for the ICL3232E), reduce the standby supply current to a 1μA trickle. Small footprint packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions. This family is fully compatible with 3.3V-only systems, mixed 3.3V and 5.0V systems, and 5.0V-only systems.

The ICL324xE are 3-driver, 5-receiver devices that provide a complete serial port suitable for laptop or notebook computers. Both devices also include noninverting always-active receivers for “wake-up” capability.

The **ICL3221E, ICL3223E and ICL3243E**, feature an **automatic power-down** function which powers down the on-chip power-supply and driver circuits. This occurs when an attached peripheral device is shut off or the RS-232 cable is removed, conserving system power automatically without changes to the hardware or operating system. These devices power up again when a valid RS-232 voltage is applied to any receiver input.

Table 1 summarizes the features of the devices represented by this data sheet, while Application Note [AN9863](#) summarizes the features of each device comprising the ICL32xxE 3V family.

## Features

- ESD Protection for RS-232 I/O Pins to ±15kV (IEC61000)
- Drop in Replacements for MAX3221E, MAX3222E, MAX3223E, MAX3232E, MAX3241E, MAX3243E, SP3243E
- ICL3221E is a Low Power, Pin Compatible Upgrade for 5V MAX221E
- ICL3222E is a Low Power, Pin Compatible Upgrade for 5V MAX242E, and SP312E
- ICL3232E is a Low Power Upgrade for HIN232E, ICL232 and Pin Compatible Competitor Devices
- RS-232 Compatible with  $V_{CC} = 2.7V$
- Meets EIA/TIA-232 and V.28/V.24 Specifications at 3V
- Latch-Up Free
- On-Chip Voltage Converters Require Only Four External 0.1μF Capacitors
- Manual and Automatic Power-Down Features
- Guaranteed Mouse Driveability (ICL324xE Only)
- Receiver Hysteresis For Improved Noise Immunity
- Guaranteed Minimum Data Rate. . . . . 250kbps
- Wide Power Supply Range . . . Single +3V to +5.5V
- Low Supply Current in Power-Down State . . . . 1μA
- Pb-Free Available (RoHS Compliant)

## Applications

- Any System Requiring RS-232 Communication Ports
  - Battery Powered, Hand-Held, and Portable Equipment
  - Laptop Computers, Notebooks, Palmtops
  - Modems, Printers and other Peripherals
  - Digital Cameras
  - Cellular/Mobile Phones

## Related Literature

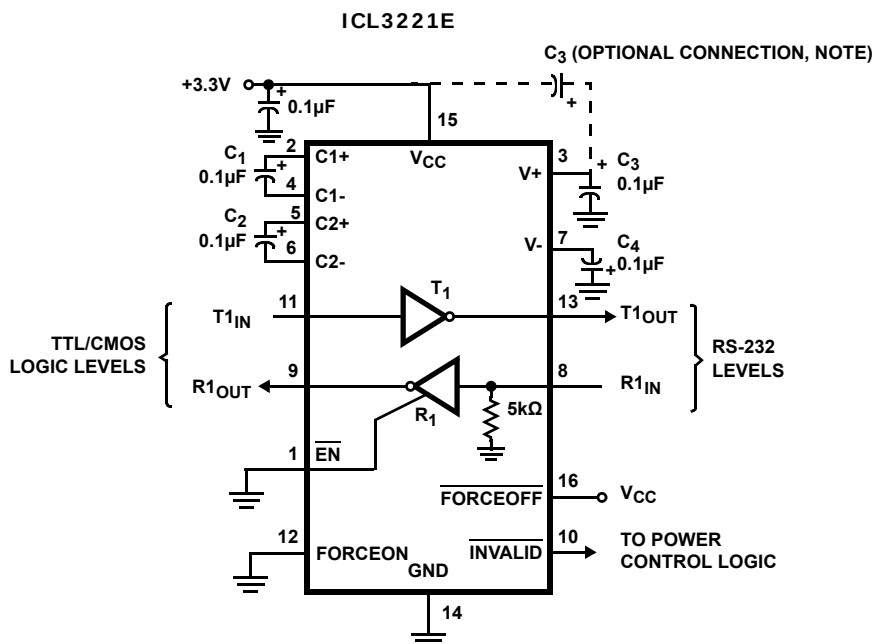
- Technical Brief [TB363](#) “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

ICL3221E, ICL3222E, ICL3223E, ICL3232E, ICL3241E, ICL3243E

TABLE 1. SUMMARY OF FEATURES

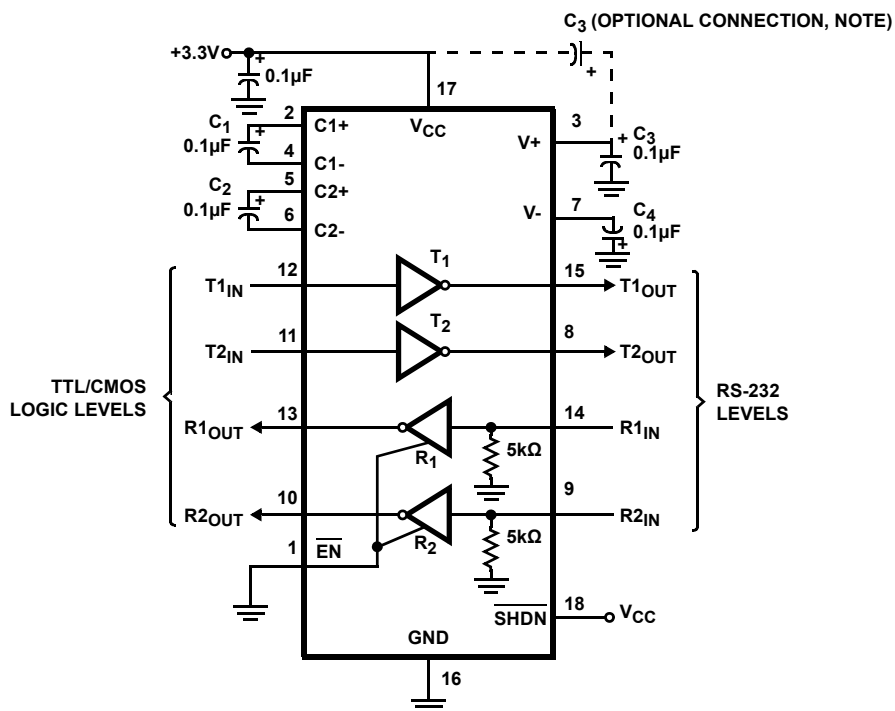
| PART NUMBER | NUMBER OF Tx | NUMBER OF Rx | NUMBER OF MONITOR RECEIVERS (R <sub>OUTB</sub> ) | DATA RATE (kbps) | RECEIVER ENABLE FUNCTION? | READY OUTPUT? | MANUAL POWER-DOWN? | AUTOMATIC POWER-DOWN FUNCTION? |
|-------------|--------------|--------------|--------------------------------------------------|------------------|---------------------------|---------------|--------------------|--------------------------------|
| ICL3221E    | 1            | 1            | 0                                                | 250              | Yes                       | No            | Yes                | Yes                            |
| ICL3222E    | 2            | 2            | 0                                                | 250              | Yes                       | No            | Yes                | No                             |
| ICL3223E    | 2            | 2            | 0                                                | 250              | Yes                       | No            | Yes                | Yes                            |
| ICL3232E    | 2            | 2            | 0                                                | 250              | No                        | No            | No                 | No                             |
| ICL3241E    | 3            | 5            | 2                                                | 250              | Yes                       | No            | Yes                | No                             |
| ICL3243E    | 3            | 5            | 1                                                | 250              | No                        | No            | Yes                | Yes                            |

## Typical Operating Circuits

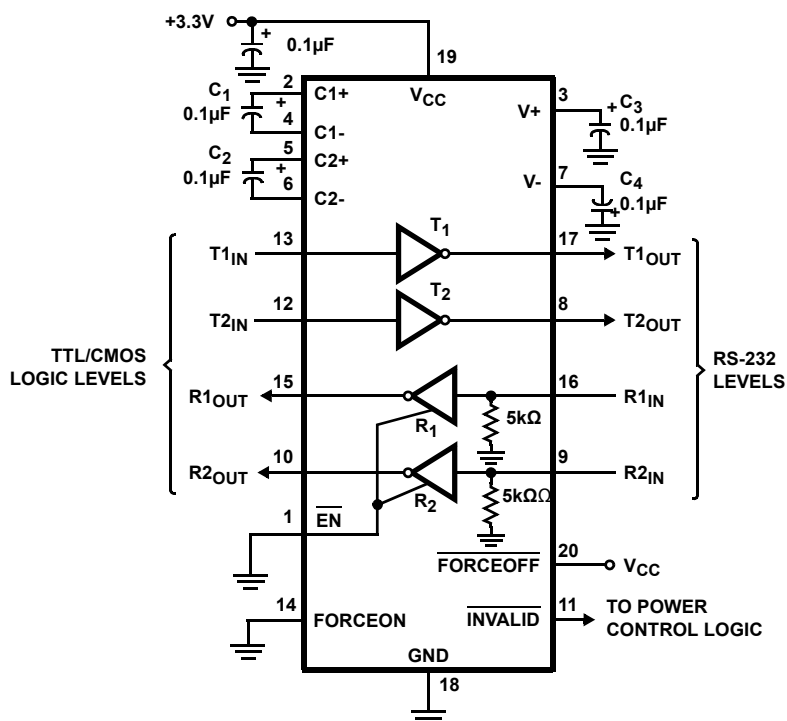


## Typical Operating Circuits (Continued)

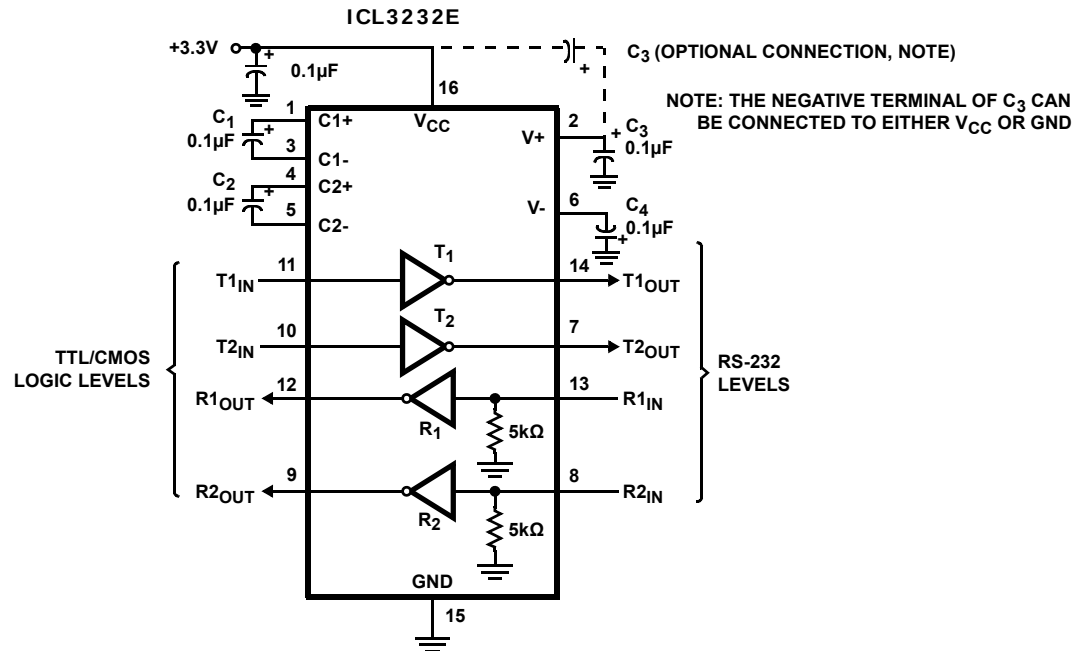
ICL3222E



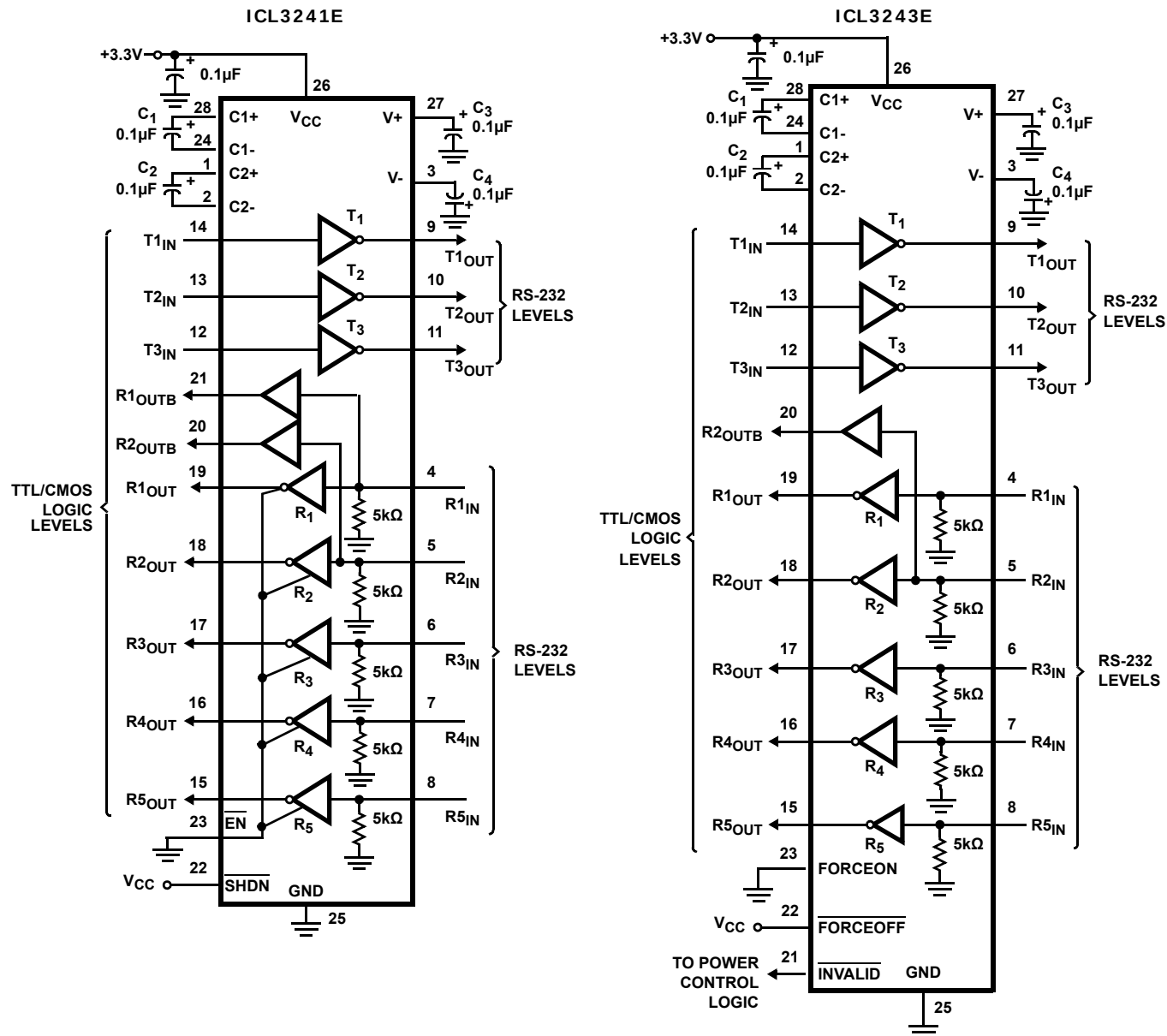
ICL3223E



## Typical Operating Circuits (Continued)

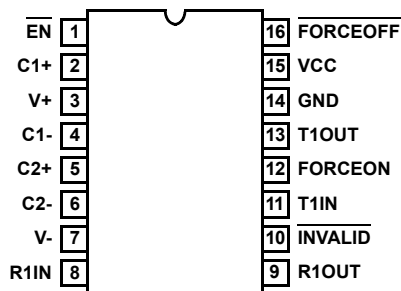


## Typical Operating Circuits (Continued)

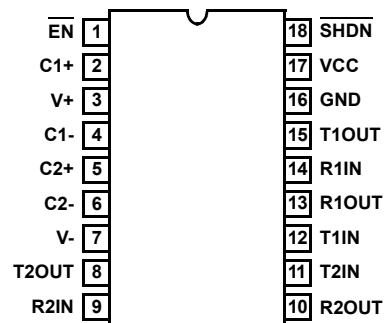


## Pin Configurations

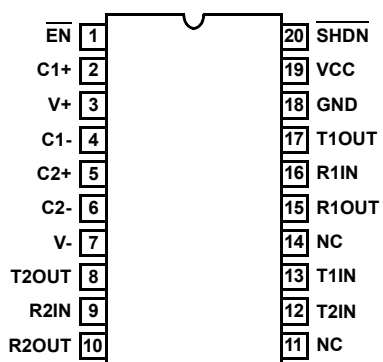
ICL3221E  
(16 LD SSOP, TSSOP)  
TOP VIEW



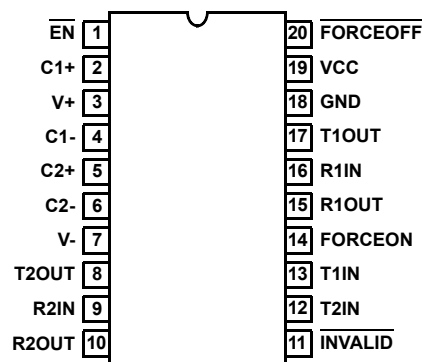
ICL3222E  
(18 LD PDIP, SOIC)  
TOP VIEW



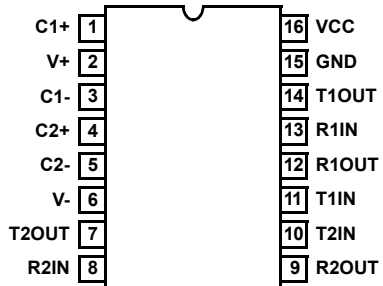
ICL3222E  
(20 LD SSOP, TSSOP)  
TOP VIEW



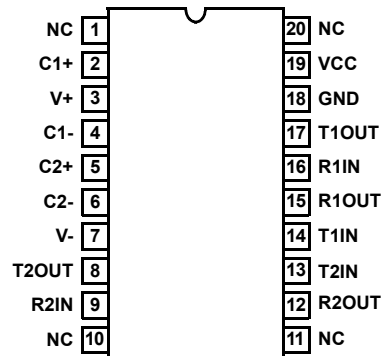
ICL3223E  
(20 LD SSOP, TSSOP)  
TOP VIEW



ICL3232E  
(16 LD SOIC, SSOP, TSSOP-16)  
TOP VIEW

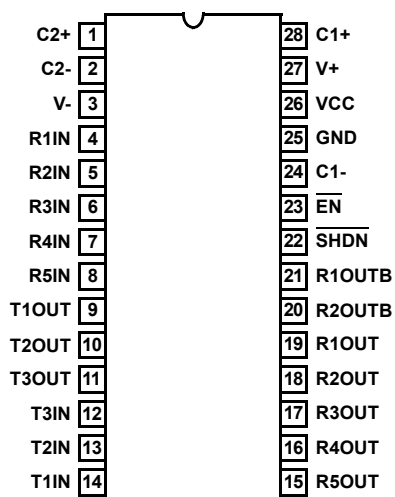


ICL3232E  
(20 LD TSSOP-20)  
TOP VIEW

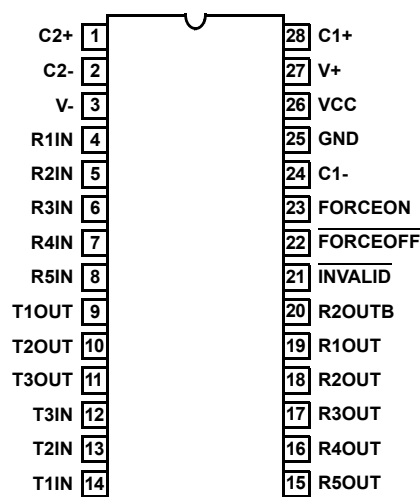


## Pin Configurations (Continued)

ICL3241E  
(28 LD SOIC, SSOP, TSSOP)  
TOP VIEW



ICL3243E  
(28 LD SOIC, SSOP, TSSOP)  
TOP VIEW



## Pin Descriptions

| PIN      | FUNCTION                                                                                                                         |
|----------|----------------------------------------------------------------------------------------------------------------------------------|
| VCC      | System power supply input (3.0V to 5.5V).                                                                                        |
| V+       | Internally generated positive transmitter supply (+5.5V).                                                                        |
| V-       | Internally generated negative transmitter supply (-5.5V).                                                                        |
| GND      | Ground connection.                                                                                                               |
| C1+      | External capacitor (voltage doubler) is connected to this lead.                                                                  |
| C1-      | External capacitor (voltage doubler) is connected to this lead.                                                                  |
| C2+      | External capacitor (voltage inverter) is connected to this lead.                                                                 |
| C2-      | External capacitor (voltage inverter) is connected to this lead.                                                                 |
| TIN      | TTL/CMOS compatible transmitter Inputs.                                                                                          |
| TOUT     | ±15kV ESD Protected, RS-232 level (nominally ±5.5V) transmitter outputs.                                                         |
| RIN      | ±15kV ESD Protected, RS-232 compatible receiver inputs.                                                                          |
| ROUT     | TTL/CMOS level receiver outputs.                                                                                                 |
| ROUTB    | TTL/CMOS level, noninverting, always enabled receiver outputs.                                                                   |
| INVALID  | Active low output that indicates if no valid RS-232 levels are present on any receiver input.                                    |
| EN       | Active low receiver enable control; doesn't disable ROUTB outputs.                                                               |
| SHDN     | Active low input to shut down transmitters and on-board power supply, to place device in low power mode.                         |
| FORCEOFF | Active low to shut down transmitters and on-chip power supply. This overrides any automatic circuitry and FORCEON (see Table 2). |
| FORCEON  | Active high input to override automatic power-down circuitry thereby keeping transmitters active (FORCEOFF must be high).        |

## Ordering Information

| PART NUMBER<br>(Note 3)     | PART<br>MARKING | TEMP RANGE<br>(°C) | PACKAGE               | PKG.<br>DWG. # |
|-----------------------------|-----------------|--------------------|-----------------------|----------------|
| ICL3221ECA                  | ICL 3221ECA     | 0 to +70           | 16 Ld SSOP            | M16.209        |
| ICL3221ECA-T (Note 1)       | ICL 3221ECA     | 0 to +70           | 16 Ld SSOP            | M16.209        |
| ICL3221ECAZ (Note 2)        | ICL32 21ECAZ    | 0 to +70           | 16 Ld SSOP (Pb-free)  | M16.209        |
| ICL3221ECAZ-T (Notes 1, 2)  | ICL32 21ECAZ    | 0 to +70           | 16 Ld SSOP (Pb-free)  | M16.209        |
| ICL3221ECAZA (Note 2)       | ICL32 21ECAZ    | 0 to +70           | 16 Ld SSOP (Pb-free)  | M16.209        |
| ICL3221ECAZA-T (Notes 1, 2) | ICL32 21ECAZ    | 0 to +70           | 16 Ld SSOP (Pb-free)  | M16.209        |
| ICL3221ECV                  | 3221 ECV        | 0 to +70           | 16 Ld TSSOP           | M16.173        |
| ICL3221ECVZ (Note 2)        | 3221 ECVZ       | 0 to +70           | 16 Ld TSSOP (Pb-free) | M16.173        |
| ICL3221ECVZ-T (Notes 1, 2)  | 3221 ECVZ       | 0 to +70           | 16 Ld TSSOP (Pb-free) | M16.173        |
| ICL3221EIA                  | ICL 3221EIA     | -40 to +85         | 16 Ld SSOP            | M16.209        |
| ICL3221EIA-T (Note 1)       | ICL 3221EIA     | -40 to +85         | 16 Ld SSOP            | M16.209        |
| ICL3221EIAZ (Note 2)        | ICL32 21EIAZ    | -40 to +85         | 16 Ld SSOP (Pb-free)  | M16.209        |
| ICL3221EIAZ-T (Notes 1, 2)  | ICL32 21EIAZ    | -40 to +85         | 16 Ld SSOP (Pb-free)  | M16.209        |
| ICL3221EIVZ (Note 2)        | 3221 EIVZ       | -40 to +85         | 16 Ld TSSOP (Pb-free) | M16.173        |
| ICL3221EIVZ-T (Notes 1, 2)  | 3221 EIVZ       | -40 to +85         | 16 Ld TSSOP (Pb-free) | M16.173        |
| ICL3222ECA-T (Note 1)       | ICL 3222ECA     | 0 to +70           | 20 Ld SSOP            | M20.209        |
| ICL3222ECAZ (Note 2)        | ICL32 22ECAZ    | 0 to +70           | 20 Ld SSOP (Pb-free)  | M20.209        |
| ICL3222ECAZ-T (Notes 1, 2)  | ICL32 22ECAZ    | 0 to +70           | 20 Ld SSOP (Pb-free)  | M20.209        |
| ICL3222ECP                  | ICL3222ECP      | 0 to +70           | 18 Ld PDIP            | E18.3          |
| ICL3222ECV-T (Note 1)       | ICL 3222ECV     | 0 to +70           | 20 Ld TSSOP           | M20.173        |
| ICL3222ECVZ (Note 2)        | ICL32 22ECVZ    | 0 to +70           | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3222ECVZ-T (Notes 1, 2)  | ICL32 22ECVZ    | 0 to +70           | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3222EIAZ (Note 2)        | ICL32 22EIAZ    | -40 to +85         | 20 Ld SSOP (Pb-free)  | M20.209        |
| ICL3222EIAZ-T (Notes 1, 2)  | ICL32 22EIAZ    | -40 to +85         | 20 Ld SSOP (Pb-free)  | M20.209        |
| ICL3222EIB                  | ICL3222EIB      | -40 to +85         | 18 Ld SOIC            | M18.3          |
| ICL3222EIB-T (Note 1)       | ICL3222EIB      | -40 to +85         | 18 Ld SOIC            | M18.3          |
| ICL3222EIBZ (Note 2)        | 3222EIBZ        | -40 to +85         | 18 Ld SOIC (Pb-free)  | M18.3          |
| ICL3222EIBZ-T (Notes 1, 2)  | 3222EIBZ        | -40 to +85         | 18 Ld SOIC (Pb-free)  | M18.3          |
| ICL3222EIV                  | ICL 3222EIV     | -40 to +85         | 20 Ld TSSOP           | M20.173        |
| ICL3222EIV-T (Note 1)       | ICL 3222EIV     | -40 to +85         | 20 Ld TSSOP           | M20.173        |
| ICL3222EIVZ (Note 2)        | ICL32 22EIVZ    | -40 to +85         | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3222EIVZ-T (Notes 1, 2)  | ICL32 22EIVZ    | -40 to +85         | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3223ECA                  | ICL 3223ECA     | 0 to +70           | 20 Ld SSOP            | M20.209        |
| ICL3223ECA-T (Note 1)       | ICL 3223ECA     | 0 to +70           | 20 Ld SSOP            | M20.209        |
| ICL3223ECAZ (Note 2)        | ICL32 23ECAZ    | 0 to +70           | 20 Ld SSOP (Pb-free)  | M20.209        |
| ICL3223ECAZ-T (Notes 1, 2)  | ICL32 23ECAZ    | 0 to +70           | 20 Ld SSOP (Pb-free)  | M20.209        |
| ICL3223ECV                  | ICL 3223ECV     | 0 to +70           | 20 Ld TSSOP           | M20.173        |
| ICL3223ECVZ (Note 2)        | ICL32 23ECVZ    | 0 to +70           | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3223ECVZ-T (Notes 1, 2)  | ICL32 23ECVZ    | 0 to +70           | 20 Ld TSSOP (Pb-free) | M20.173        |

## Ordering Information (Continued)

| PART NUMBER<br>(Note 3)       | PART<br>MARKING | TEMP RANGE<br>(°C) | PACKAGE               | PKG.<br>DWG. # |
|-------------------------------|-----------------|--------------------|-----------------------|----------------|
| ICL3223EIA                    | ICL 3223EIA     | -40 to +85         | 20 Ld SSOP            | M20.209        |
| ICL3223EIA-T (Note 1)         | ICL 3223EIA     | -40 to +85         | 20 Ld SSOP            | M20.209        |
| ICL3223EIAZ (Note 2)          | ICL32 23EIAZ    | -40 to +85         | 20 Ld SSOP (Pb-free)  | M20.209        |
| ICL3223EIAZ-T (Notes 1, 2)    | ICL32 23EIAZ    | -40 to +85         | 20 Ld SSOP (Pb-free)  | M20.209        |
| ICL3223EIV                    | ICL 3223EIV     | -40 to +85         | 20 Ld TSSOP           | M20.173        |
| ICL3223EIVZ (Note 2)          | ICL32 23EIVZ    | -40 to +85         | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3223EIVZ-T (Notes 1, 2)    | ICL32 23EIVZ    | -40 to +85         | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3232ECA                    | ICL 3232ECA     | 0 to +70           | 16 Ld SSOP            | M16.209        |
| ICL3232ECA-T (Note 1)         | ICL 3232ECA     | 0 to +70           | 16 Ld SSOP            | M16.209        |
| ICL3232ECAZ (Note 2)          | 3232 ECAZ       | 0 to +70           | 16 Ld SSOP (Pb-free)  | M16.209        |
| ICL3232ECAZ-T (Notes 1, 2)    | 3232 ECAZ       | 0 to +70           | 16 Ld SSOP (Pb-free)  | M16.209        |
| ICL3232ECBZ (Note 2)          | 3232ECBZ        | 0 to +70           | 16 Ld SOIC (Pb-free)  | M16.3          |
| ICL3232ECBZ-T (Notes 1, 2)    | 3232ECBZ        | 0 to +70           | 16 Ld SOIC (Pb-free)  | M16.3          |
| ICL3232ECBN                   | 3232ECBN        | 0 to +70           | 16 Ld SOIC            | M16.15         |
| ICL3232ECBN-T (Note 1)        | 3232ECBN        | 0 to +70           | 16 Ld SOIC            | M16.15         |
| ICL3232ECBNZ (Note 2)         | 3232ECBNZ       | 0 to +70           | 16 Ld SOIC (Pb-free)  | M16.15         |
| ICL3232ECBNZ-T (Notes 1, 2)   | 3232ECBNZ       | 0 to +70           | 16 Ld SOIC (Pb-free)  | M16.15         |
| ICL3232ECV-16T (Note 1)       | 3232E CV-16     | 0 to +70           | 16 Ld TSSOP           | M16.173        |
| ICL3232ECV-16Z (Note 2)       | 3232E CV-16Z    | 0 to +70           | 16 Ld TSSOP (Pb-free) | M16.173        |
| ICL3232ECV-16Z-T (Notes 1, 2) | 3232E CV-16Z    | 0 to +70           | 16 Ld TSSOP (Pb-free) | M16.173        |
| ICL3232ECV-20Z (Note 2)       | ICL3232 ECV-20Z | 0 to +70           | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3232ECV-20Z-T (Notes 1, 2) | ICL3232 ECV-20Z | 0 to +70           | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3232EFV-16Z (Note 2)       | 3232E FV-16Z    | -40 to +125        | 16 Ld TSSOP (Pb-free) | M16.173        |
| ICL3232EFV-16Z-T (Notes 1, 2) | 3232E FV-16Z    | -40 to +125        | 16 Ld TSSOP (Pb-free) | M16.173        |
| ICL3232EIA-T (Note 1)         | ICL3232 EIA     | -40 to +85         | 16 Ld SSOP            | M16.209        |
| ICL3232EIAZ (Note 2)          | 3232 EIAZ       | -40 to +85         | 16 Ld SSOP (Pb-free)  | M16.209        |
| ICL3232EIAZ-T (Notes 1, 2)    | 3232 EIAZ       | -40 to +85         | 16 Ld SSOP (Pb-free)  | M16.209        |
| ICL3232EIB-T (Note 1)         | ICL3232EIB      | -40 to +85         | 16 Ld SOIC            | M16.3          |
| ICL3232EIBZ (Note 2)          | 3232EIBZ        | -40 to +85         | 16 Ld SOIC (Pb-free)  | M16.3          |
| ICL3232EIBZ-T (Notes 1, 2)    | 3232EIBZ        | -40 to +85         | 16 Ld SOIC (Pb-free)  | M16.3          |
| ICL3232EIBNZ (Note 2)         | 3232EIBNZ       | -40 to +85         | 16 Ld SOIC (Pb-free)  | M16.15         |
| ICL3232EIBNZ-T (Notes 1, 2)   | 3232EIBNZ       | -40 to +85         | 16 Ld SOIC (Pb-free)  | M16.15         |
| ICL3232EIV-16                 | 3232E IV-16     | -40 to +85         | 16 Ld TSSOP           | M16.173        |
| ICL3232EIV-16-T (Note 1)      | 3232E IV-16     | -40 to +85         | 16 Ld TSSOP           | M16.173        |
| ICL3232EIV-16Z (Note 2)       | 3232E IV-16Z    | -40 to +85         | 16 Ld TSSOP (Pb-free) | M16.173        |
| ICL3232EIV-16Z-T (Notes 1, 2) | 3232E IV-16Z    | -40 to +85         | 16 Ld TSSOP (Pb-free) | M16.173        |
| ICL3232EIV-20Z (Note 2)       | ICL3232 EIV-20Z | -40 to +85         | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3232EIV-20Z-T (Notes 1, 2) | ICL3232 EIV-20Z | -40 to +85         | 20 Ld TSSOP (Pb-free) | M20.173        |
| ICL3241ECA                    | ICL 3241ECA     | 0 to +70           | 28 Ld SSOP            | M28.209        |

## Ordering Information (Continued)

| PART NUMBER<br>(Note 3)    | PART<br>MARKING | TEMP RANGE<br>(°C) | PACKAGE               | PKG.<br>DWG. # |
|----------------------------|-----------------|--------------------|-----------------------|----------------|
| ICL3241ECA-T (Note 1)      | ICL 3241ECA     | 0 to +70           | 28 Ld SSOP            | M28.209        |
| ICL3241ECAZ (Note 2)       | ICL3241 ECAZ    | 0 to +70           | 28 Ld SSOP (Pb-free)  | M28.209        |
| ICL3241ECAZ-T (Notes 1, 2) | ICL3241 ECAZ    | 0 to +70           | 28 Ld SSOP (Pb-free)  | M28.209        |
| ICL3241ECBZ (Note 2)       | ICL3241ECBZ     | 0 to +70           | 28 Ld SOIC (Pb-free)  | M28.3          |
| ICL3241ECBZ-T (Notes 1, 2) | ICL3241ECBZ     | 0 to +70           | 28 Ld SOIC (Pb-free)  | M28.3          |
| ICL3241ECVZ (Note 2)       | ICL3241 ECVZ    | 0 to +70           | 28 Ld TSSOP (Pb-free) | M28.173        |
| ICL3241EIA-T (Note 1)      | ICL 3241EIA     | -40 to +85         | 28 Ld SSOP            | M28.209        |
| ICL3241EIAZ (Note 2)       | ICL3241 EIAZ    | -40 to +85         | 28 Ld SSOP (Pb-free)  | M28.209        |
| ICL3241EIAZ-T (Notes 1, 2) | ICL3241 EIAZ    | -40 to +85         | 28 Ld SSOP (Pb-free)  | M28.209        |
| ICL3241EIBZ (Note 2)       | ICL3241EIBZ     | -40 to +85         | 28 Ld SOIC (Pb-free)  | M28.3          |
| ICL3241EIBZ-T (Notes 1, 2) | ICL3241EIBZ     | -40 to +85         | 28 Ld SOIC (Pb-free)  | M28.3          |
| ICL3241EIV-T (Note 1)      | ICL3241 EIV     | -40 to +85         | 28 Ld TSSOP           | M28.173        |
| ICL3241EIVZ (Note 2)       | ICL3241 EIVZ    | -40 to +85         | 28 Ld TSSOP (Pb-free) | M28.173        |
| ICL3241EIVZ-T (Notes 1, 2) | ICL3241 EIVZ    | -40 to +85         | 28 Ld TSSOP (Pb-free) | M28.173        |
| ICL3243ECA                 | ICL 3243ECA     | 0 to +70           | 28 Ld SSOP            | M28.209        |
| ICL3243ECA-T (Note 1)      | ICL 3243ECA     | 0 to +70           | 28 Ld SSOP            | M28.209        |
| ICL3243ECAZ (Note 2)       | ICL32 43ECAZ    | 0 to +70           | 28 Ld SSOP (Pb-free)  | M28.209        |
| ICL3243ECAZ-T (Notes 1, 2) | ICL32 43ECAZ    | 0 to +70           | 28 Ld SSOP (Pb-free)  | M28.209        |
| ICL3243ECBZ (Note 2)       | ICL3243ECBZ     | 0 to +70           | 28 Ld SOIC (Pb-free)  | M28.3          |
| ICL3243ECBZ-T (Notes 1, 2) | ICL3243ECBZ     | 0 to +70           | 28 Ld SOIC (Pb-free)  | M28.3          |
| ICL3243ECV-T (Note 1)      | ICL3243 ECV     | 0 to +70           | 28 Ld TSSOP           | M28.173        |
| ICL3243ECVZ (Note 2)       | ICL3243 ECVZ    | 0 to +70           | 28 Ld TSSOP (Pb-free) | M28.173        |
| ICL3243ECVZ-T (Notes 1, 2) | ICL3243 ECVZ    | 0 to +70           | 28 Ld TSSOP (Pb-free) | M28.173        |
| ICL3243EIA-T (Note 1)      | ICL 3243EIA     | -40 to +85         | 28 Ld SSOP            | M28.209        |
| ICL3243EIAZ (Note 2)       | ICL32 43EIAZ    | -40 to +85         | 28 Ld SSOP (Pb-free)  | M28.209        |
| ICL3243EIAZ-T (Notes 1, 2) | ICL32 43EIAZ    | -40 to +85         | 28 Ld SSOP (Pb-free)  | M28.209        |
| ICL3243EIV                 | ICL3243 EIV     | -40 to +85         | 28 Ld TSSOP           | M28.173        |
| ICL3243EIVZ (Note 2)       | ICL3243 EIVZ    | -40 to +85         | 28 Ld TSSOP (Pb-free) | M28.173        |
| ICL3243EIVZ-T (Notes 1, 2) | ICL3243 EIVZ    | -40 to +85         | 28 Ld TSSOP (Pb-free) | M28.173        |

### NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ICL3221E](#), [ICL3222E](#), [ICL3223E](#), [ICL3232E](#), [ICL3241E](#), [ICL3243E](#). For more information on MSL please see techbrief [TB363](#).

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## Absolute Maximum Ratings

|                                               |                                |
|-----------------------------------------------|--------------------------------|
| V <sub>CC</sub> to GND                        | -0.3V to 6V                    |
| V <sub>+</sub> to GND                         | -0.3V to 7V                    |
| V <sub>-</sub> to GND                         | +0.3V to -7V                   |
| V <sub>+</sub> to V <sub>-</sub>              | 14V                            |
| Input Voltages                                |                                |
| T <sub>IN</sub> , FORCEOFF, FORCEON, EN, SHDN | -0.3V to 6V                    |
| R <sub>IN</sub>                               | ±25V                           |
| Output Voltages                               |                                |
| T <sub>OUT</sub>                              | ±13.2V                         |
| R <sub>OUT</sub> , INVALID                    | -0.3V to V <sub>CC</sub> +0.3V |
| Short Circuit Duration                        |                                |
| T <sub>OUT</sub>                              | Continuous                     |
| ESD Rating                                    | See Specification Table        |

## Recommended Operating Conditions

|                                   |                 |
|-----------------------------------|-----------------|
| Temperature Range                 |                 |
| ICL32xxECX                        | 0°C to +70°C    |
| ICL32xxEFX                        | -40°C to +125°C |
| ICL32xxEIX                        | -40°C to +85°C  |
| Supply Voltage (V <sub>CC</sub> ) | 3.3V or 5V      |
| Rx Input Voltage                  | -15V to +15V    |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTE:

4.  $\theta_{JA}$  is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Thermal Information

|                                                                                                                 |                      |
|-----------------------------------------------------------------------------------------------------------------|----------------------|
| Thermal Resistance (Typical, Note 4)                                                                            | $\theta_{JA}$ (°C/W) |
| 18 Ld PDIP Package*                                                                                             | 80                   |
| 16 Ld Wide SOIC Package                                                                                         | 100                  |
| 16 Ld Narrow SOIC Package                                                                                       | 115                  |
| 18 Ld SOIC Package                                                                                              | 75                   |
| 28 Ld SOIC Package                                                                                              | 75                   |
| 16 Ld SSOP Package                                                                                              | 135                  |
| 20 Ld SSOP Package                                                                                              | 122                  |
| 16 Ld TSSOP Package                                                                                             | 145                  |
| 20 Ld TSSOP Package                                                                                             | 140                  |
| 28 Ld SSOP and TSSOP Packages                                                                                   | 100                  |
| Maximum Junction Temperature (Plastic Package)                                                                  | +150°C               |
| Maximum Storage Temperature Range                                                                               | -65°C to +150°C      |
| Pb-Free Reflow Profile                                                                                          | see link below       |
| <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a> |                      |

**Electrical Specifications** Test Conditions: V<sub>CC</sub> = 3V to 5.5V, C<sub>1</sub> - C<sub>4</sub> = 0.1μF; Unless Otherwise Specified.  
Typicals are at T<sub>A</sub> = +25°C. **Boldface limits apply over the operating temperature range.**

| PARAMETER                                         | TEST CONDITIONS                                                                                                           |                                                             | TEMP<br>(°C) | MIN<br>(Note 6)       | TYP                   | MAX<br>(Note 6) | UNITS |
|---------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|--------------|-----------------------|-----------------------|-----------------|-------|
| DC CHARACTERISTICS                                |                                                                                                                           |                                                             |              |                       |                       |                 |       |
| Supply Current, Automatic Power-Down              | All R <sub>IN</sub> Open, FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{\text{CC}}$ (ICL3221E, ICL3223E, ICL3243E Only) |                                                             | 25           | -                     | 1.0                   | 10              | μA    |
| Supply Current, Power-Down                        | $\overline{\text{FORCEOFF}} = \overline{\text{SHDN}} = \text{GND}$ (Except ICL3232E)                                      |                                                             | 25           | -                     | 1.0                   | 10              | μA    |
| Supply Current, Automatic Power-Down Disabled     | All Outputs Unloaded, $\overline{\text{FORCEON}} = \overline{\text{FORCEOFF}} = \overline{\text{SHDN}} = V_{\text{CC}}$   | V <sub>CC</sub> = 3.0V, ICL3241, ICL3243                    | 25           | -                     | 0.3                   | 1.0             | mA    |
|                                                   |                                                                                                                           | V <sub>CC</sub> = 3.0V, ICL3223                             | 25           | -                     | 0.7                   | 3.0             | mA    |
|                                                   |                                                                                                                           | V <sub>CC</sub> = 3.15V, ICL3221, ICL3222, ICL3223, ICL3232 | 25           | -                     | 0.3                   | 1.0             | mA    |
| LOGIC AND TRANSMITTER INPUTS AND RECEIVER OUTPUTS |                                                                                                                           |                                                             |              |                       |                       |                 |       |
| Input Logic Threshold Low                         | T <sub>IN</sub> , FORCEON, $\overline{\text{FORCEOFF}}$ , $\overline{\text{EN}}$ , $\overline{\text{SHDN}}$               |                                                             | Full         | -                     | -                     | 0.8             | V     |
| Input Logic Threshold High                        | T <sub>IN</sub> , FORCEON, $\overline{\text{FORCEOFF}}$ , $\overline{\text{EN}}$ , $\overline{\text{SHDN}}$               | V <sub>CC</sub> = 3.3V                                      | Full         | 2.0                   | -                     | -               | V     |
|                                                   |                                                                                                                           | V <sub>CC</sub> = 5.0V                                      | Full         | 2.4                   | -                     | -               | V     |
| Input Leakage Current                             | T <sub>IN</sub> , FORCEON, $\overline{\text{FORCEOFF}}$ , $\overline{\text{EN}}$ , $\overline{\text{SHDN}}$               | All but ICL3232EF                                           | Full         | -                     | ±0.01                 | ±1.0            | μA    |
|                                                   |                                                                                                                           | ICL3232EF                                                   | Full         | -                     | ±0.01                 | ±10             | μA    |
| Output Leakage Current (Except ICL3232E)          | $\overline{\text{FORCEOFF}} = \text{GND}$ or $\overline{\text{EN}} = V_{\text{CC}}$                                       |                                                             | Full         | -                     | ±0.05                 | ±10             | μA    |
| Output Voltage Low                                | I <sub>OUT</sub> = 1.6mA                                                                                                  |                                                             | Full         | -                     | -                     | 0.4             | V     |
| Output Voltage High                               | I <sub>OUT</sub> = -1.0mA                                                                                                 | All but ICL3232EF                                           | Full         | V <sub>CC</sub> - 0.6 | V <sub>CC</sub> - 0.1 | -               | V     |
|                                                   |                                                                                                                           | ICL3232EF                                                   | Full         | V <sub>CC</sub> - 0.9 | V <sub>CC</sub> - 0.1 | -               | V     |

# ICL3221E, ICL3222E, ICL3223E, ICL3232E, ICL3241E, ICL3243E

**Electrical Specifications** Test Conditions:  $V_{CC} = 3V$  to  $5.5V$ ,  $C_1 - C_4 = 0.1\mu F$ ; Unless Otherwise Specified.  
Typicals are at  $T_A = +25^\circ C$ . **Boldface limits apply over the operating temperature range. (Continued)**

| PARAMETER                                                                                            | TEST CONDITIONS                                                                                                                              | TEMP<br>( $^\circ C$ ) | MIN<br>(Note 6)             | TYP       | MAX<br>(Note 6)            | UNITS      |
|------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|------------------------|-----------------------------|-----------|----------------------------|------------|
| <b>AUTOMATIC POWER-DOWN</b> (ICL3221E, ICL3223E, ICL3243E Only, FORCEON = GND, FORCEOFF = $V_{CC}$ ) |                                                                                                                                              |                        |                             |           |                            |            |
| Receiver Input Thresholds to Enable Transmitters                                                     | ICL32xxE Powers Up (see Figure 6)                                                                                                            | Full                   | <b>-2.7</b>                 | -         | <b>2.7</b>                 | V          |
| Receiver Input Thresholds to Disable Transmitters                                                    | ICL32xxE Powers Down (see Figure 6)                                                                                                          | Full                   | <b>-0.3</b>                 | -         | <b>0.3</b>                 | V          |
| $\overline{INVALID}$ Output Voltage Low                                                              | $I_{OUT} = 1.6mA$                                                                                                                            | Full                   | -                           | -         | <b>0.4</b>                 | V          |
| $\overline{INVALID}$ Output Voltage High                                                             | $I_{OUT} = -1.0mA$                                                                                                                           | Full                   | $V_{CC} - 0.6$              | -         | -                          | V          |
| Receiver Threshold to Transmitters Enabled Delay ( $t_{WU}$ )                                        |                                                                                                                                              | 25                     | -                           | 100       | -                          | $\mu s$    |
| Receiver Positive or Negative Threshold to $\overline{INVALID}$ High Delay ( $t_{INVH}$ )            |                                                                                                                                              | 25                     | -                           | 1         | -                          | $\mu s$    |
| Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low Delay ( $t_{INVL}$ )             |                                                                                                                                              | 25                     | -                           | 30        | -                          | $\mu s$    |
| <b>RECEIVER INPUTS</b>                                                                               |                                                                                                                                              |                        |                             |           |                            |            |
| Input Voltage Range                                                                                  |                                                                                                                                              | 25                     | -25                         | -         | 25                         | V          |
| Input Threshold Low                                                                                  | $V_{CC} = 3.3V$                                                                                                                              | 25                     | 0.6                         | 1.2       | -                          | V          |
|                                                                                                      | $V_{CC} = 5.0V$                                                                                                                              | 25                     | 0.8                         | 1.5       | -                          | V          |
| Input Threshold High                                                                                 | $V_{CC} = 3.3V$                                                                                                                              | 25                     | -                           | 1.5       | 2.4                        | V          |
|                                                                                                      | $V_{CC} = 5.0V$                                                                                                                              | 25                     | -                           | 1.8       | 2.4                        | V          |
| Input Hysteresis                                                                                     |                                                                                                                                              | 25                     | -                           | 0.5       | -                          | V          |
| Input Resistance                                                                                     |                                                                                                                                              | 25                     | 3                           | 5         | 7                          | k $\Omega$ |
| <b>TRANSMITTER OUTPUTS</b>                                                                           |                                                                                                                                              |                        |                             |           |                            |            |
| Output Voltage Swing                                                                                 | All Transmitter Outputs Loaded with 3k $\Omega$ to Ground                                                                                    | Full                   | <b><math>\pm 5.0</math></b> | $\pm 5.4$ | -                          | V          |
| Output Resistance                                                                                    | $V_{CC} = V_+ = V_- = 0V$ , Transmitter Output = $\pm 2V$                                                                                    | Full                   | <b>300</b>                  | 10M       | -                          | $\Omega$   |
| Output Short-Circuit Current                                                                         |                                                                                                                                              | Full                   | -                           | $\pm 35$  | <b><math>\pm 60</math></b> | mA         |
| Output Leakage Current                                                                               | $V_{OUT} = \pm 12V$ , $V_{CC} = 0V$ or $3V$ to $5.5V$ , Automatic Power-Down or FORCEOFF = SHDN = GND                                        | Full                   | -                           | -         | <b><math>\pm 25</math></b> | $\mu A$    |
| <b>MOUSE DRIVEABILITY</b> (ICL324XE Only)                                                            |                                                                                                                                              |                        |                             |           |                            |            |
| Transmitter Output Voltage (see Figure 9)                                                            | $T1_{IN} = T2_{IN} = GND$ , $T3_{IN} = V_{CC}$ , $T3_{OUT}$ Loaded with 3k $\Omega$ to GND, $T1_{OUT}$ and $T2_{OUT}$ Loaded with 2.5mA Each | Full                   | <b><math>\pm 5</math></b>   | -         | -                          | V          |
| <b>TIMING CHARACTERISTICS</b>                                                                        |                                                                                                                                              |                        |                             |           |                            |            |
| Maximum Data Rate                                                                                    | $R_L = 3k\Omega$ , $C_L = 1000pF$ , One Transmitter Switching                                                                                | Full                   | <b>250</b>                  | 500       | -                          | kbps       |
| Receiver Propagation Delay                                                                           | Receiver Input to Receiver Output, $C_L = 150pF$                                                                                             | $t_{PHL}$              | 25                          | -         | 0.15                       | $\mu s$    |
|                                                                                                      |                                                                                                                                              | $t_{PLH}$              | 25                          | -         | 0.15                       | $\mu s$    |
| Receiver Output Enable Time                                                                          | Normal Operation (Except ICL3232E)                                                                                                           | 25                     | -                           | 200       | -                          | ns         |

**Electrical Specifications** Test Conditions:  $V_{CC} = 3V$  to  $5.5V$ ,  $C_1 - C_4 = 0.1\mu F$ ; Unless Otherwise Specified. Typical values are at  $T_A = +25^\circ C$ . **Boldface limits apply over the operating temperature range. (Continued)**

| PARAMETER                    | TEST CONDITIONS                                                                                 |                                  | TEMP<br>(°C) | MIN<br>(Note 6) | TYP | MAX<br>(Note 6) | UNITS |
|------------------------------|-------------------------------------------------------------------------------------------------|----------------------------------|--------------|-----------------|-----|-----------------|-------|
| Receiver Output Disable Time | Normal Operation (Except ICL3232E)                                                              |                                  | 25           | -               | 200 | -               | ns    |
| Transmitter Skew             | t <sub>PHL</sub> to t <sub>PLH</sub> (Note 5)                                                   |                                  | 25           | -               | 100 | -               | ns    |
| Receiver Skew                | t <sub>PHL</sub> to t <sub>PLH</sub>                                                            |                                  | 25           | -               | 50  | -               | ns    |
| Transition Region Slew Rate  | V <sub>CC</sub> = 3.3V,<br>R <sub>L</sub> = 3kΩ to 7kΩ,<br>Measured from 3V to -3V or -3V to 3V | C <sub>L</sub> = 150pF to 2500pF | 25           | 4               | -   | 30              | V/μs  |
|                              |                                                                                                 | C <sub>L</sub> = 150pF to 1000pF | 25           | 6               | -   | 30              | V/μs  |
| ESD PERFORMANCE              |                                                                                                 |                                  |              |                 |     |                 |       |
| RS-232 Pins (TOUT, RIN)      | Human Body Model                                                                                |                                  | 25           | -               | ±15 | -               | kV    |
|                              | IEC61000-4-2 Contact Discharge                                                                  |                                  | 25           | -               | ±8  | -               | kV    |
|                              | IEC61000-4-2 Air Gap Discharge                                                                  |                                  | 25           | -               | ±15 | -               | kV    |
| All Other Pins               | Human Body Model                                                                                |                                  | 25           | -               | ±2  | -               | kV    |

**NOTES:**

- Transmitter skew is measured at the transmitter zero crossing points.
- Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

## Detailed Description

ICL32xxE interface ICs operate from a single  $+3V$  to  $+5.5V$  supply, guarantee a 250kbps minimum data rate, require only four small external  $0.1\mu F$  capacitors, feature low power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: charge pump, transmitters and receivers.

### Charge-Pump

Intersil's new ICL32xxE family utilizes regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate  $\pm 5.5V$  transmitter supplies from a  $V_{CC}$  supply as low as  $3.0V$ . This allows these devices to maintain RS-232 compliant output levels over the  $\pm 10\%$  tolerance range of  $3.3V$  powered systems. The efficient on-chip power supplies require only four small, external  $0.1\mu F$  capacitors for the voltage doubler and inverter functions at  $V_{CC} = 3.3V$ . See "Capacitor Selection" on page 18 and Table 3 on page 18 for capacitor recommendations for other operating conditions. The charge pumps operate discontinuously (i.e., they turn off as soon as the  $V+$  and  $V-$  supplies are pumped up to the nominal values), resulting in significant power savings.

### Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. Coupled with the on-chip  $\pm 5.5V$  supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

Except for the ICL3232E, all transmitter outputs disable and assume a high impedance state when the device enters the power-down mode (see Table 2). These outputs may be driven to  $\pm 12V$  when disabled.

All devices guarantee a 250kbps data rate for full load conditions ( $3k\Omega$  and  $1000pF$ ),  $V_{CC} \geq 3.0V$ , with one transmitter operating at full speed. Under more typical conditions of  $V_{CC} \geq 3.3V$ ,  $R_L = 3k\Omega$ , and  $C_L = 250pF$ , one transmitter easily operates at 900kbps.

Transmitter inputs float if left unconnected, and may cause  $I_{CC}$  increases. Connect unused inputs to GND for the best performance.

### Receivers

All the ICL32xxE devices contain standard inverting receivers that three-state (except for the ICL3232E) via the EN or FORCEOFF control lines. Additionally, the two ICL324XE products include noninverting (monitor) receivers (denoted by the ROUTB label) that are always active, regardless of the state of any control lines. All the receivers convert RS-232 signals to CMOS output levels and accept inputs up to  $\pm 25V$  while presenting the required  $3k\Omega$  to  $7k\Omega$  input impedance (see Figure 1) even if the power is off ( $V_{CC} = 0V$ ). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

The ICL3221E, ICL3222E, ICL3223E, ICL3241E inverting receivers disable only when EN is driven high. ICL3243E receivers disable during forced (manual) power-down, but not during automatic power-down (see Table 2).

ICL3241E and ICL3243E monitor receivers remain active even during manual power-down and forced receiver disable, making them extremely useful for Ring Indicator monitoring. Standard receivers driving powered down peripherals must be disabled to prevent current flow through the peripheral's protection diodes (see Figures 2 and 3). This renders them useless for wake up functions, but the corresponding monitor receiver can be dedicated to this task as shown in Figure 3.

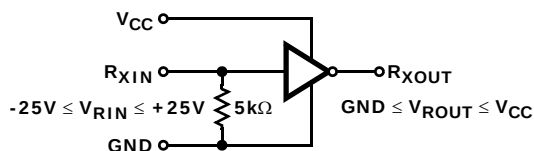


FIGURE 1. INVERTING RECEIVER CONNECTIONS

## Low Power Operation

These 3V devices require a nominal supply current of 0.3mA, even at  $V_{CC} = 5.5V$ , during normal operation (not in power-down mode). This is considerably less than the 5mA to 11mA current required by comparable 5V RS-232 devices, allowing users to reduce system power simply by switching to this new family.

### Pin Compatible Replacements for 5V Devices

The ICL3221E, ICL3222E, ICL3232E are pin compatible with existing 5V RS-232 transceivers - See the "Features" section on page 1 for details.

This pin compatibility coupled with the low  $I_{CC}$  and wide operating supply range, make the ICL32xxE potential lower power, higher performance drop-in replacements for existing 5V applications. As long as the  $\pm 5V$  RS-232 output swings are acceptable, and transmitter input pull-up resistors aren't required, the ICL32xxE should work in most 5V applications.

When replacing a device in an existing 5V application, it is acceptable to terminate  $C_3$  to  $V_{CC}$  as shown on the "Typical Operating Circuits" on page 2. Nevertheless, terminate  $C_3$  to GND if possible, as slightly better performance results from this configuration.

## Power-Down Functionality (Except ICL3232E)

The already low current requirement drops significantly when the device enters power-down mode. In power-down, supply current drops to  $1\mu A$ , because the on-chip charge pump turns off ( $V+$  collapses to  $V_{CC}$ ,  $V-$  collapses to GND), and the transmitter outputs three-state. Inverting receiver outputs may or may not disable in power-down; refer to Table 2 for details. This micro-power mode makes these devices ideal for battery powered and portable applications.

### Software Controlled (Manual) Power-Down

Most devices in the ICL32xxE family provide pins that allow the user to force the IC into the low power, standby state.

On the ICL3222E and ICL3241E, the power-down control is via a simple shutdown ( $\overline{SHDN}$ ) pin. Driving this pin high enables normal operation, while driving it low forces the IC into its power-down state. Connect  $\overline{SHDN}$  to  $V_{CC}$  if the power-down function isn't needed. Note that all the receiver outputs remain enabled during shutdown (see Table 2). For the lowest power consumption during power-down, the receivers should also be disabled by driving the  $\overline{EN}$  input high (see next section, and Figures 2 and 3).

The ICL3221E, ICL3223E, and ICL3243E utilize a two pin approach where the  $\overline{FORCEON}$  and  $\overline{FORCEOFF}$  inputs determine the IC's mode. For always enabled operation,  $\overline{FORCEON}$  and  $\overline{FORCEOFF}$  are both strapped high. To switch between active and power-down modes, under logic or software control, only the  $\overline{FORCEOFF}$  input need be driven. The  $\overline{FORCEON}$  state isn't critical, as  $\overline{FORCEOFF}$  dominates over  $\overline{FORCEON}$ . Nevertheless, if strictly manual control over power-down is desired, the user must strap  $\overline{FORCEON}$  high to disable the automatic power-down circuitry. ICL3243E inverting (standard) receiver outputs also disable when the device is in manual power-down, thereby eliminating the possible current path through a shutdown peripheral's input protection diode (see Figures 2 and 3).

TABLE 2. POWER-DOWN AND ENABLE LOGIC TRUTH TABLE

| RS-232<br>SIGNAL<br>PRESENT<br>AT<br>RECEIVER<br>INPUT? | $\overline{FORCEOFF}$<br>OR $\overline{SHDN}$<br>INPUT | $\overline{FORCEON}$<br>INPUT | $\overline{EN}$<br>INPUT | TRANSMITTER<br>OUTPUTS | RECEIVER<br>OUTPUTS | $R_{OUTB}$<br>OUTPUTS<br>(NOTE 7) | $\overline{INVALID}$<br>OUTPUT | MODE OF<br>OPERATION                     |
|---------------------------------------------------------|--------------------------------------------------------|-------------------------------|--------------------------|------------------------|---------------------|-----------------------------------|--------------------------------|------------------------------------------|
| ICL3222E, ICL3241E                                      |                                                        |                               |                          |                        |                     |                                   |                                |                                          |
| N/A                                                     | L                                                      | N/A                           | L                        | High-Z                 | Active              | Active                            | N/A                            | Manual Power-Down                        |
| N/A                                                     | L                                                      | N/A                           | H                        | High-Z                 | High-Z              | Active                            | N/A                            | Manual Power-Down with Receiver Disabled |
| N/A                                                     | H                                                      | N/A                           | L                        | Active                 | Active              | Active                            | N/A                            | Normal Operation                         |
| N/A                                                     | H                                                      | N/A                           | H                        | Active                 | High-Z              | Active                            | N/A                            | Normal Operation with Receiver Disabled  |

TABLE 2. POWER-DOWN AND ENABLE LOGIC TRUTH TABLE (Continued)

| RS-232<br>SIGNAL<br>PRESENT<br>AT<br>RECEIVER<br>INPUT? | <u>FORCEOFF</u><br>OR SHDN<br>INPUT | FORCEON<br>INPUT | <u>EN</u><br>INPUT | TRANSMITTER<br>OUTPUTS | RECEIVER<br>OUTPUTS | R <sub>OUTB</sub><br>OUTPUTS<br>(NOTE 7) | <u>INVALID</u><br>OUTPUT | MODE OF<br>OPERATION                           |
|---------------------------------------------------------|-------------------------------------|------------------|--------------------|------------------------|---------------------|------------------------------------------|--------------------------|------------------------------------------------|
| <b>ICL3221E, ICL3223E</b>                               |                                     |                  |                    |                        |                     |                                          |                          |                                                |
| No                                                      | H                                   | H                | L                  | Active                 | Active              | N/A                                      | L                        | Normal Operation<br>(Auto Power-Down Disabled) |
| No                                                      | H                                   | H                | H                  | Active                 | High-Z              | N/A                                      | L                        |                                                |
| Yes                                                     | H                                   | L                | L                  | Active                 | Active              | N/A                                      | H                        | Normal Operation<br>(Auto Power-Down Enabled)  |
| Yes                                                     | H                                   | L                | H                  | Active                 | High-Z              | N/A                                      | H                        |                                                |
| No                                                      | H                                   | L                | L                  | High-Z                 | Active              | N/A                                      | L                        | Power-Down Due to Auto<br>Power-Down Logic     |
| No                                                      | H                                   | L                | H                  | High-Z                 | High-Z              | N/A                                      | L                        |                                                |
| Yes                                                     | L                                   | X                | L                  | High-Z                 | Active              | N/A                                      | H                        | Manual Power-Down                              |
| Yes                                                     | L                                   | X                | H                  | High-Z                 | High-Z              | N/A                                      | H                        | Manual Power-Down<br>with Receiver Disabled    |
| No                                                      | L                                   | X                | L                  | High-Z                 | Active              | N/A                                      | L                        | Manual Power-Down                              |
| No                                                      | L                                   | X                | H                  | High-Z                 | High-Z              | N/A                                      | L                        | Manual Power-Down<br>with Receiver Disabled    |
| <b>ICL3243E</b>                                         |                                     |                  |                    |                        |                     |                                          |                          |                                                |
| No                                                      | H                                   | H                | N/A                | Active                 | Active              | Active                                   | L                        | Normal Operation<br>(Auto Power-Down Disabled) |
| Yes                                                     | H                                   | L                | N/A                | Active                 | Active              | Active                                   | H                        | Normal Operation<br>(Auto Power-Down Enabled)  |
| No                                                      | H                                   | L                | N/A                | High-Z                 | Active              | Active                                   | L                        | Power-Down Due to Auto<br>Power-Down Logic     |
| Yes                                                     | L                                   | X                | N/A                | High-Z                 | High-Z              | Active                                   | H                        | Manual Power-Down                              |
| No                                                      | L                                   | X                | N/A                | High-Z                 | High-Z              | Active                                   | L                        | Manual Power-Down                              |

NOTE:

7. Applies only to the ICL3241E and ICL3243E.

The INVALID output always indicates whether or not a valid RS-232 signal is present at any of the receiver inputs (see Table 2), giving the user an easy way to determine when the interface block should power down. In the case of a disconnected interface cable where all the receiver inputs are floating (but pulled to GND by the internal receiver pull down resistors), the INVALID logic detects the invalid levels and drives the output low. The power management logic then uses this indicator to power down the interface block. Reconnecting the cable restores valid levels at the receiver inputs, INVALID switches high, and the power management logic wakes up the interface block. INVALID can also be used to indicate the DTR or RING INDICATOR signal, as long as the other receiver inputs are floating, or driven to GND (as in the case of a powered down driver). Connecting FORCEOFF and FORCEON together disables the automatic power-down feature, enabling them to function as a manual SHUTDOWN input (see Figure 4).

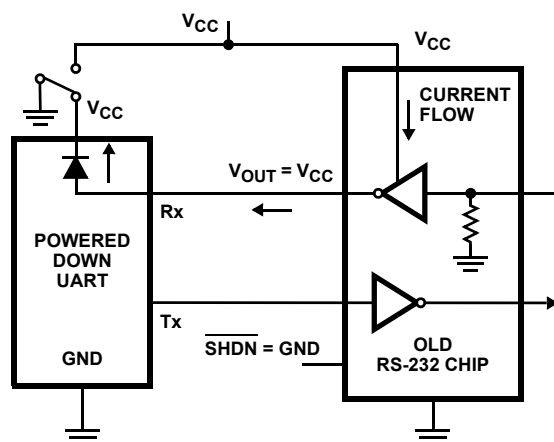


FIGURE 2. POWER DRAIN THROUGH POWERED DOWN PERIPHERAL

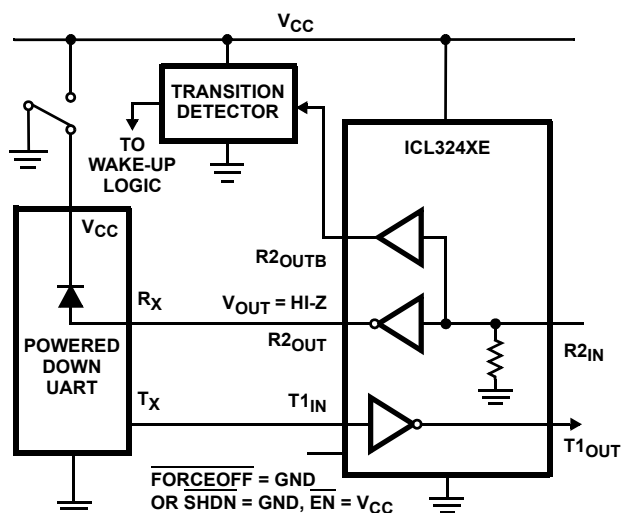


FIGURE 3. DISABLED RECEIVERS PREVENT POWER DRAIN

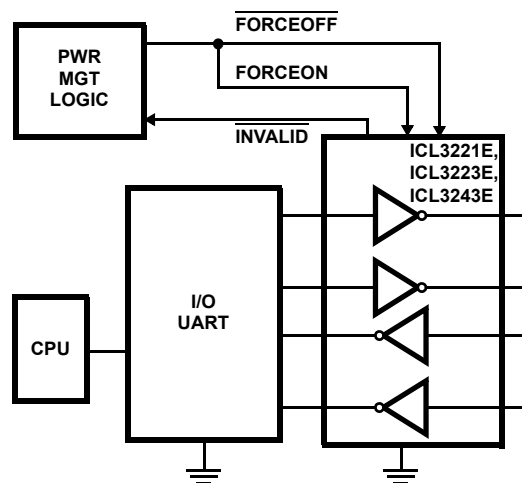


FIGURE 4. CONNECTIONS FOR MANUAL POWER-DOWN WHEN NO VALID RECEIVER SIGNALS ARE PRESENT

With any of the control schemes, the time required to exit power-down, and resume transmission is only 100µs. A mouse, or other application, may need more time to wake up from shutdown. If automatic power-down is being utilized, the RS-232 device will reenter power-down if valid receiver levels aren't reestablished within 30µs of the ICL32xxE powering up. Figure 5 illustrates a circuit that keeps the ICL32xxE from initiating automatic power-down for 100ms after powering up. This gives the slow-to-wake peripheral circuit time to reestablish valid RS-232 output levels.

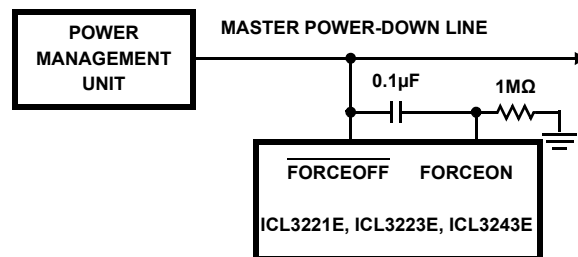


FIGURE 5. CIRCUIT TO PREVENT AUTO POWER-DOWN FOR 100ms AFTER FORCED POWER-UP

### Automatic Power-Down (ICL3221E, ICL3223E, ICL3243E Only)

Even greater power savings is available by using the devices which feature an *automatic* power-down function. When no valid RS-232 voltages (see Figure 6) are sensed on any receiver input for 30µs, the charge pump and transmitters power-down, thereby reducing supply current to 1µA. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. The ICL32xxE powers back up whenever it detects a valid RS-232 voltage level on any receiver input. This automatic power-down feature provides additional system power savings without changes to the existing operating system.

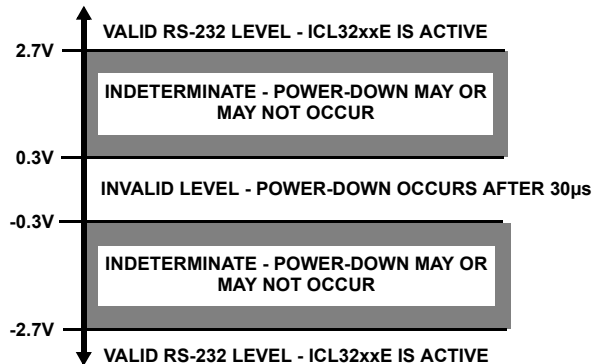


FIGURE 6. DEFINITION OF VALID RS-232 RECEIVER LEVELS

Automatic power-down operates when the FORCEON input is low, and the FORCEOFF input is high. Tying FORCEON high disables automatic power-down, but manual power-down is always available via the overriding FORCEOFF input. Table 2 summarizes the automatic power-down functionality.

Devices with the automatic power-down feature include an  $\overline{\text{INVALID}}$  output signal, which switches low to indicate that invalid levels have persisted on all of the receiver inputs for more than 30 $\mu\text{s}$  (see Figure 7).  $\overline{\text{INVALID}}$  switches high 1 $\mu\text{s}$  after detecting a valid RS-232 level on a receiver input.  $\overline{\text{INVALID}}$  operates in all modes (forced or automatic power-down, or forced on), so it is also useful for systems employing manual power-down circuitry. When automatic power-down is utilized,  $\overline{\text{INVALID}} = 0$  indicates that the ICL32xxE is in power-down mode.

The time to recover from automatic power-down mode is typically 100 $\mu\text{s}$ .

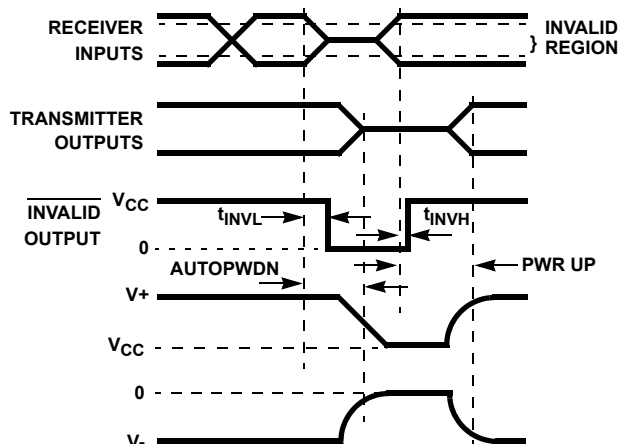


FIGURE 7. AUTOMATIC POWER-DOWN AND INVALID TIMING DIAGRAMS

### Receiver ENABLE Control (ICL3221E, ICL3222E, ICL3223E, ICL3241E Only)

Several devices also feature an  $\overline{\text{EN}}$  input to control the receiver outputs. Driving  $\overline{\text{EN}}$  high disables all the inverting (standard) receiver outputs placing them in a high impedance state. This is useful to eliminate supply current, due to a receiver output forward biasing the protection diode, when driving the input of a powered down ( $V_{CC} = \text{GND}$ ) peripheral (see Figure 2). The enable input has no effect on transmitter nor monitor ( $R_{OUTB}$ ) outputs.

### Capacitor Selection

The charge pumps require 0.1 $\mu\text{F}$  capacitors for 3.3V operation. For other supply voltages refer to Table 3 for capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption.  $C_2$ ,  $C_3$ , and  $C_4$  can be increased without increasing  $C_1$ 's value, however, do not increase  $C_1$  without also increasing  $C_2$ ,  $C_3$ , and  $C_4$  to maintain the proper ratios ( $C_1$  to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a

larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on  $V+$  and  $V-$ .

TABLE 3. REQUIRED CAPACITOR VALUES

| $V_{CC}$<br>(V) | $C_1$<br>( $\mu\text{F}$ ) | $C_2, C_3, C_4$<br>( $\mu\text{F}$ ) |
|-----------------|----------------------------|--------------------------------------|
| 3.0 to 3.6      | 0.1                        | 0.1                                  |
| 4.5 to 5.5      | 0.047                      | 0.33                                 |
| 3.0 to 5.5      | 0.1                        | 0.47                                 |

### Power Supply Decoupling

In most circumstances a 0.1 $\mu\text{F}$  bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple  $V_{CC}$  to ground with a capacitor of the same value as the charge-pump capacitor  $C_1$ . Connect the bypass capacitor as close as possible to the IC.

### Operation Down to 2.7V

ICL32xxE transmitter outputs meet RS-562 levels ( $\pm 3.7\text{V}$ ), at full data rate, with  $V_{CC}$  as low as 2.7V. RS-562 levels typically ensure interoperability with RS-232 devices.

### Transmitter Outputs when Exiting Power-Down

Figure 8 shows the response of two transmitter outputs when exiting power-down mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3k $\Omega$  in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

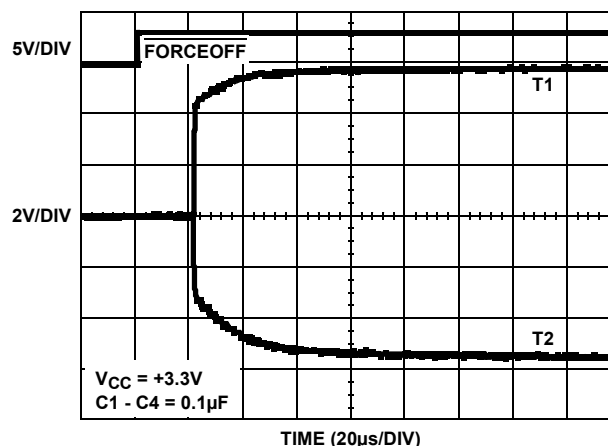


FIGURE 8. TRANSMITTER OUTPUTS WHEN EXITING POWER-DOWN

### Mouse Driveability

The ICL3241E and ICL3243E have been specifically designed to power a serial mouse while operating from low voltage supplies. Figure 9 shows the transmitter

output voltages under increasing load current. The on-chip switching regulator ensures the transmitters will supply at least  $\pm 5V$  during worst case conditions (15mA for paralleled V+ transmitters, 7.3mA for single V- transmitter). The Automatic Power-Down feature does not work with a mouse, so FORCEOFF and FORCEON should be connected to  $V_{CC}$ .

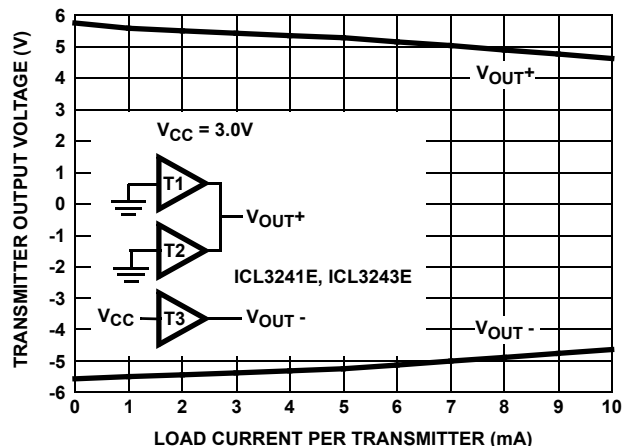


FIGURE 9. TRANSMITTER OUTPUT VOLTAGE vs LOAD CURRENT (PER TRANSMITTER, i.e., DOUBLE CURRENT AXIS FOR TOTAL  $V_{OUT+}$  CURRENT)

## High Data Rates

The ICL32xxE maintain the RS-232  $\pm 5V$  minimum transmitter output voltages even at high data rates. Figure 10 details a transmitter loopback test circuit, and Figure 11 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 12 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

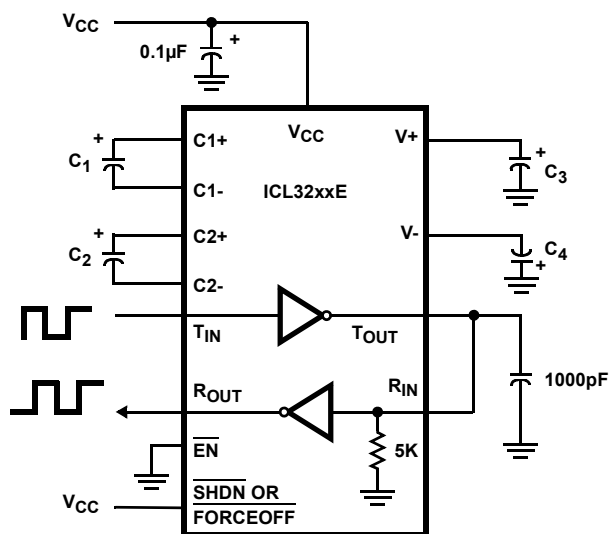


FIGURE 10. TRANSMITTER LOOPBACK TEST CIRCUIT

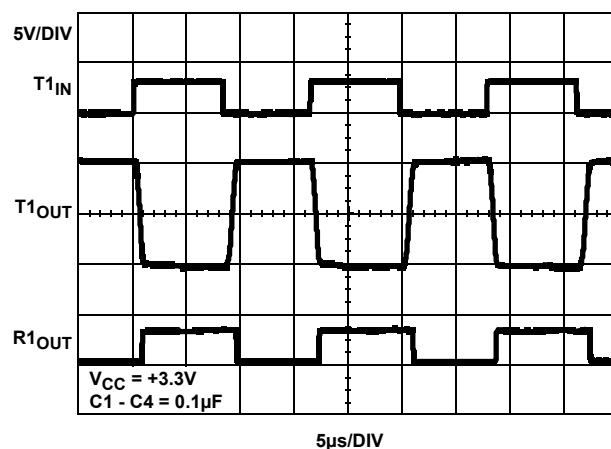


FIGURE 11. LOOPBACK TEST AT 120kbps

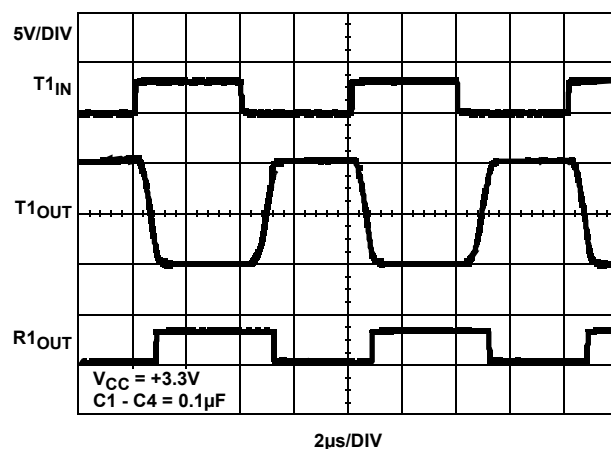


FIGURE 12. LOOPBACK TEST AT 250kbps

## Interconnection with 3V and 5V Logic

The ICL32XX directly interface with 5V CMOS and TTL logic families. Nevertheless, with the ICL32XX at 3.3V, and the logic supply at 5V, AC, HC, and CD4000 outputs can drive ICL32XX inputs, but ICL32XX outputs do not reach the minimum  $V_{IH}$  for these logic families. See Table 4 for more information.

TABLE 4. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES

| SYSTEM POWER-SUPPLY VOLTAGE (V) | $V_{CC}$ SUPPLY VOLTAGE (V) | COMPATIBILITY                                    |
|---------------------------------|-----------------------------|--------------------------------------------------|
| 3.3                             | 3.3                         | Compatible with all CMOS families.               |
| 5                               | 5                           | Compatible with all TTL and CMOS logic families. |

TABLE 4. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES (Continued)

| SYSTEM POWER-SUPPLY VOLTAGE (V) | V <sub>CC</sub> SUPPLY VOLTAGE (V) | COMPATIBILITY                                                                                                         |
|---------------------------------|------------------------------------|-----------------------------------------------------------------------------------------------------------------------|
| 5                               | 3.3                                | Compatible with ACT and HCT CMOS, and with TTL. ICL32XX outputs are incompatible with AC, HC, and CD4000 CMOS inputs. |

## ±15kV ESD Protection

All pins on ICL32XX devices include ESD protection structures, but the ICL32xxE family incorporates advanced structures which allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latch-up mechanism to activate, and don't interfere with RS-232 signals as large as ±25V.

## Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, making the test less severe than the IEC61000 test which utilizes a 330Ω limiting resistor. The HBM method determines an IC's ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

## IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

## AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

## CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

## Typical Performance Curves $V_{CC} = 3.3V$ , $T_A = +25^\circ C$ .

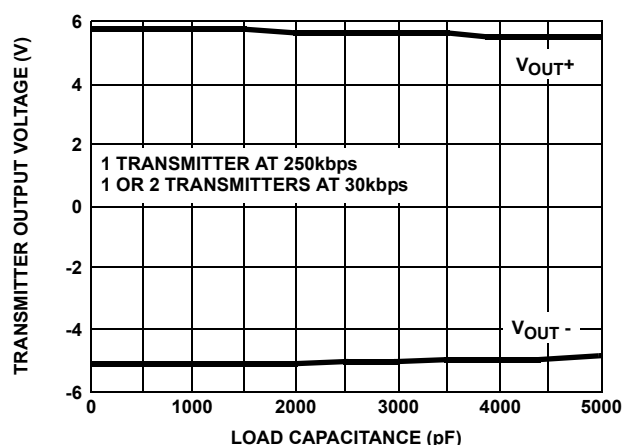


FIGURE 13. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

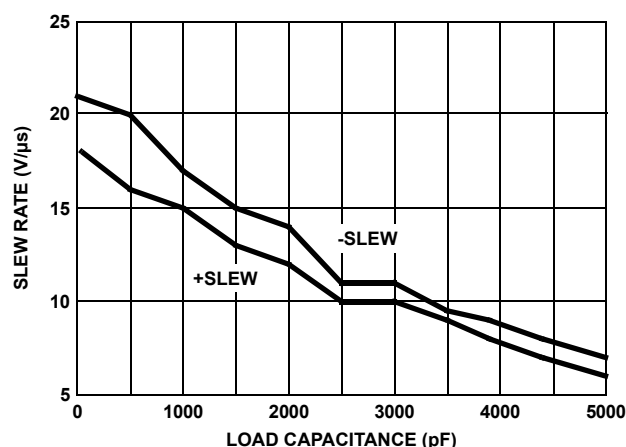


FIGURE 14. SLEW RATE vs LOAD CAPACITANCE

## Typical Performance Curves $V_{CC} = 3.3V$ , $T_A = +25^\circ C$ . (Continued)

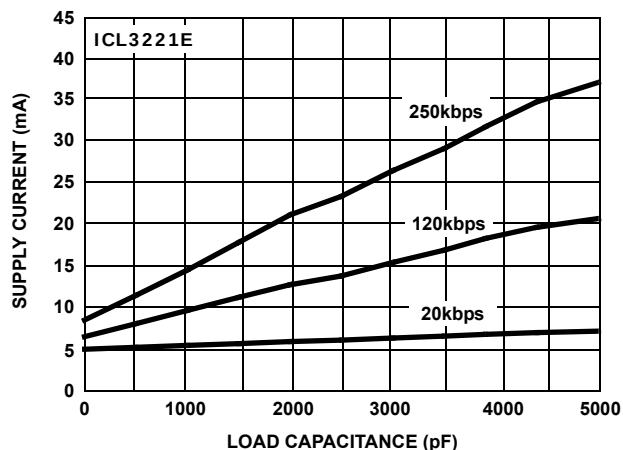


FIGURE 15. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

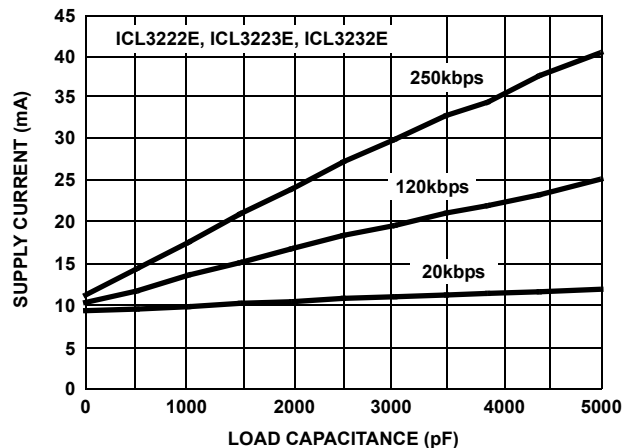


FIGURE 16. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

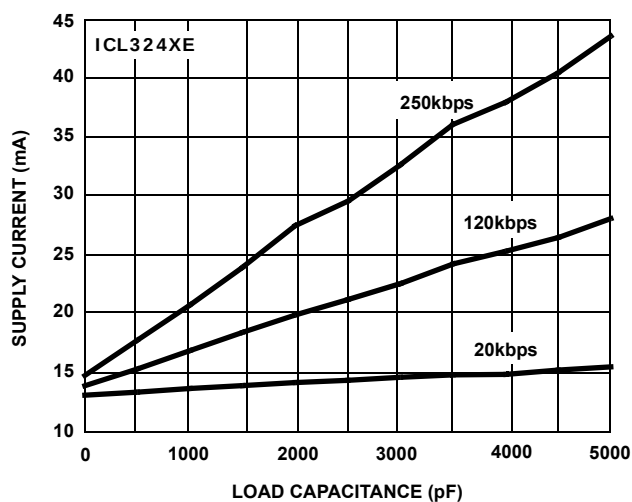


FIGURE 17. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

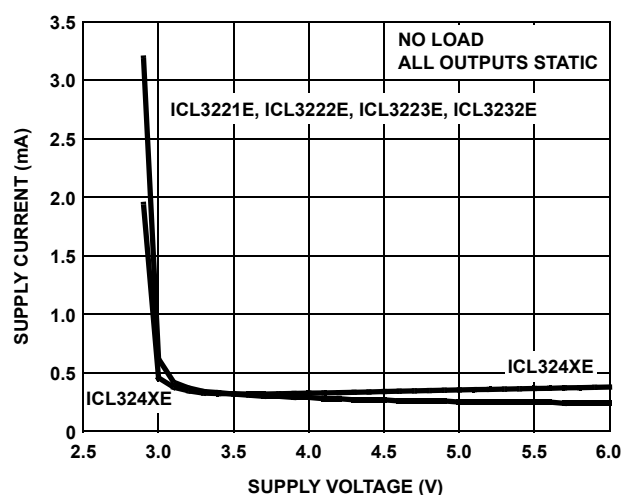


FIGURE 18. SUPPLY CURRENT vs SUPPLY VOLTAGE

## Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

ICL3221E: 286

ICL3222E: 338

ICL3223E: 357

ICL3232E: 296

ICL324XE: 464

PROCESS:

Si Gate CMOS

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE    | REVISION  | CHANGE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2/22/10 | FN4910.21 | <p>Revision history begins with this revision.</p> <p>Converted to new Intersil template.</p> <p>Added new temp grade (F = extended industrial) to ICL3232. Updated ordering info table, Operating Conditions, and added 125°C specs for input I<sub>kg</sub> currents, and rcvr output high voltage.</p> <p>Pages 8-10: Removed all withdrawn devices from Ordering Information table.</p> <p>Pages 12-14: Added "Boldface limits apply over the operating temperature range." to common conditions of Electrical Specs table. Replaced Note 6 "Parts are 100% tested at +25°C. Full temp limits are guaranteed by bench and tester characterization." with "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested."</p> |

## Products

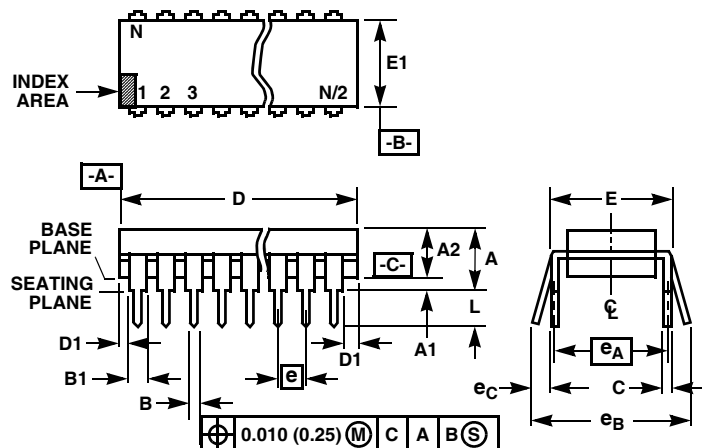
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to [www.intersil.com/products](http://www.intersil.com/products) for a complete list of Intersil product families.

\*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ICL3221E](#), [ICL3222E](#), [ICL3223E](#), [ICL3232E](#), [ICL3241E](#), [ICL3243E](#)

To report errors or suggestions for this datasheet, please go to [www.intersil.com/askourstaff](http://www.intersil.com/askourstaff)

FITs are available from our website at <http://rel.intersil.com/reports/search.php>

## Dual-In-Line Plastic Packages (PDIP)



### NOTES:

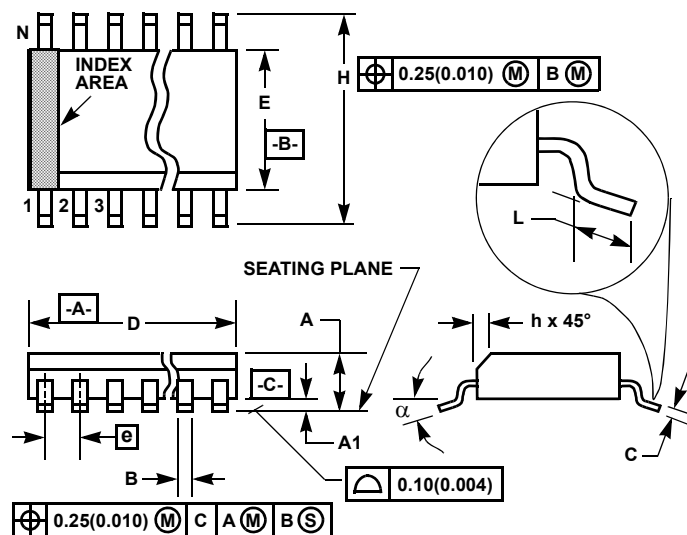
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3 may have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

### E18.3 (JEDEC MS-001-BC ISSUE D) 18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

| SYMBOL | INCHES    |       | MILLIMETERS |       | NOTES |
|--------|-----------|-------|-------------|-------|-------|
|        | MIN       | MAX   | MIN         | MAX   |       |
| A      | -         | 0.210 | -           | 5.33  | 4     |
| A1     | 0.015     | -     | 0.39        | -     | 4     |
| A2     | 0.115     | 0.195 | 2.93        | 4.95  | -     |
| B      | 0.014     | 0.022 | 0.356       | 0.558 | -     |
| B1     | 0.045     | 0.070 | 1.15        | 1.77  | 8, 10 |
| C      | 0.008     | 0.014 | 0.204       | 0.355 | -     |
| D      | 0.845     | 0.880 | 21.47       | 22.35 | 5     |
| D1     | 0.005     | -     | 0.13        | -     | 5     |
| E      | 0.300     | 0.325 | 7.62        | 8.25  | 6     |
| E1     | 0.240     | 0.280 | 6.10        | 7.11  | 5     |
| e      | 0.100 BSC |       | 2.54 BSC    |       | -     |
| $e_A$  | 0.300 BSC |       | 7.62 BSC    |       | 6     |
| $e_B$  | -         | 0.430 | -           | 10.92 | 7     |
| L      | 0.115     | 0.150 | 2.93        | 3.81  | 4     |
| N      | 18        |       | 18          |       | 9     |

Rev. 2 11/03

## Small Outline Plastic Packages (SOIC)



### NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

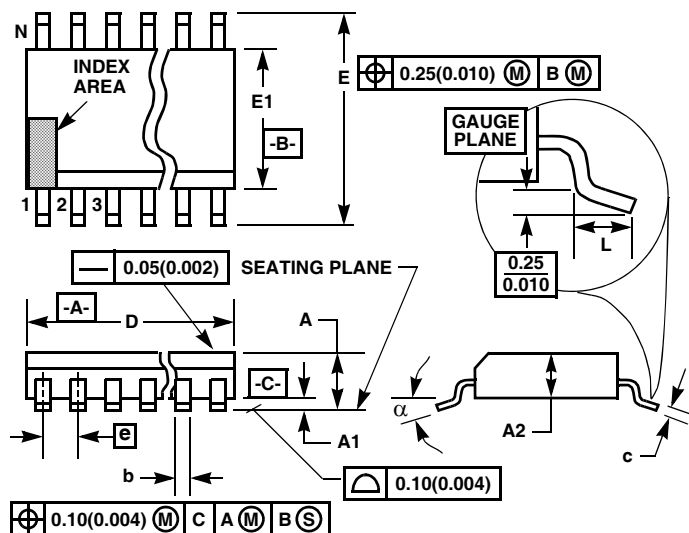
### M16.15 (JEDEC MS-012-AC ISSUE C)

#### 16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES    |        | MILLIMETERS |       | NOTES |
|--------|-----------|--------|-------------|-------|-------|
|        | MIN       | MAX    | MIN         | MAX   |       |
| A      | 0.0532    | 0.0688 | 1.35        | 1.75  | -     |
| A1     | 0.0040    | 0.0098 | 0.10        | 0.25  | -     |
| B      | 0.013     | 0.020  | 0.33        | 0.51  | 9     |
| C      | 0.0075    | 0.0098 | 0.19        | 0.25  | -     |
| D      | 0.3859    | 0.3937 | 9.80        | 10.00 | 3     |
| E      | 0.1497    | 0.1574 | 3.80        | 4.00  | 4     |
| e      | 0.050 BSC |        | 1.27 BSC    |       | -     |
| H      | 0.2284    | 0.2440 | 5.80        | 6.20  | -     |
| h      | 0.0099    | 0.0196 | 0.25        | 0.50  | 5     |
| L      | 0.016     | 0.050  | 0.40        | 1.27  | 6     |
| N      | 16        |        | 16          |       | 7     |
| α      | 0°        | 8°     | 0°          | 8°    | -     |

Rev. 1 6/05

# Thin Shrink Small Outline Plastic Packages (TSSOP)



## NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

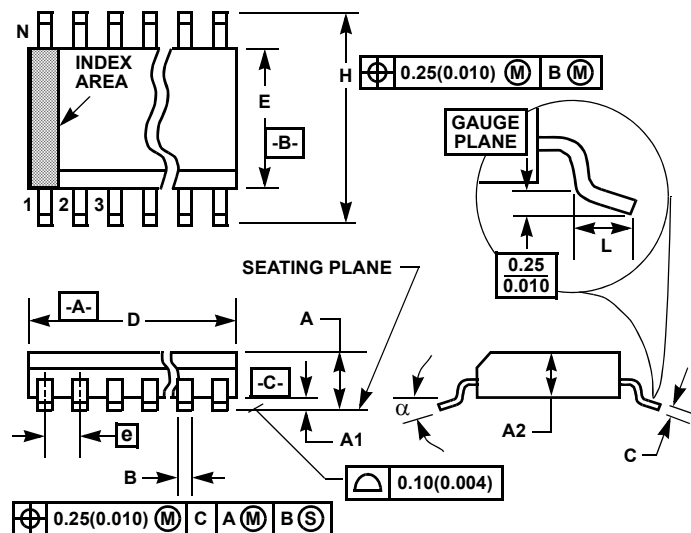
## M16.173

### 16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES    |       | MILLIMETERS |      | NOTES |
|--------|-----------|-------|-------------|------|-------|
|        | MIN       | MAX   | MIN         | MAX  |       |
| A      | -         | 0.043 | -           | 1.10 | -     |
| A1     | 0.002     | 0.006 | 0.05        | 0.15 | -     |
| A2     | 0.033     | 0.037 | 0.85        | 0.95 | -     |
| b      | 0.0075    | 0.012 | 0.19        | 0.30 | 9     |
| c      | 0.0035    | 0.008 | 0.09        | 0.20 | -     |
| D      | 0.193     | 0.201 | 4.90        | 5.10 | 3     |
| E1     | 0.169     | 0.177 | 4.30        | 4.50 | 4     |
| e      | 0.026 BSC |       | 0.65 BSC    |      | -     |
| E      | 0.246     | 0.256 | 6.25        | 6.50 | -     |
| L      | 0.020     | 0.028 | 0.50        | 0.70 | 6     |
| N      | 16        |       | 16          |      | 7     |
| α      | 0°        | 8°    | 0°          | 8°   | -     |

Rev. 1 2/02

## Small Outline Plastic Packages (SSOP)



### NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

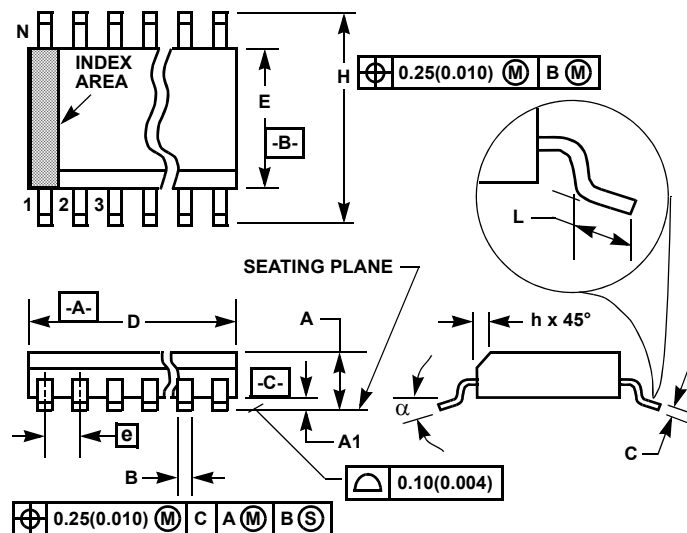
### M16.209 (JEDEC MO-150-AC ISSUE B)

#### 16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES    |       | MILLIMETERS |      | NOTES |
|--------|-----------|-------|-------------|------|-------|
|        | MIN       | MAX   | MIN         | MAX  |       |
| A      | -         | 0.078 | -           | 2.00 | -     |
| A1     | 0.002     | -     | 0.05        | -    | -     |
| A2     | 0.065     | 0.072 | 1.65        | 1.85 | -     |
| B      | 0.009     | 0.014 | 0.22        | 0.38 | 9     |
| C      | 0.004     | 0.009 | 0.09        | 0.25 | -     |
| D      | 0.233     | 0.255 | 5.90        | 6.50 | 3     |
| E      | 0.197     | 0.220 | 5.00        | 5.60 | 4     |
| e      | 0.026 BSC |       | 0.65 BSC    |      | -     |
| H      | 0.292     | 0.322 | 7.40        | 8.20 | -     |
| L      | 0.022     | 0.037 | 0.55        | 0.95 | 6     |
| N      | 16        |       | 16          |      | 7     |
| α      | 0°        | 8°    | 0°          | 8°   | -     |

Rev. 3 6/05

## Small Outline Plastic Packages (SOIC)



### NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

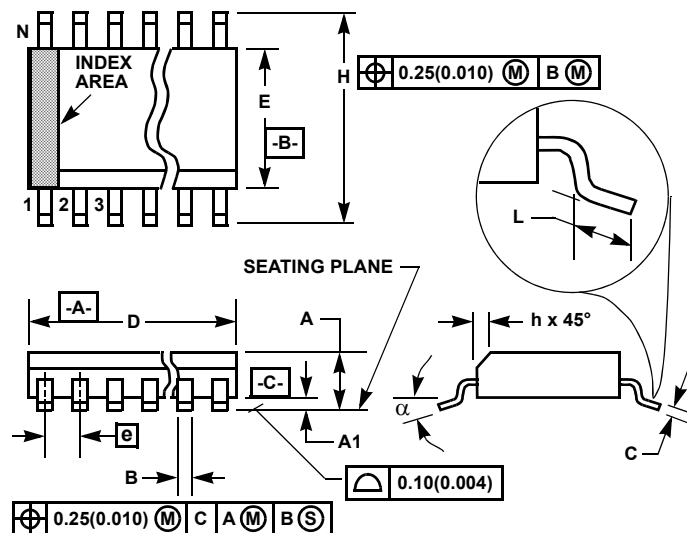
### M16.3 (JEDEC MS-013-AA ISSUE C)

#### 16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES    |        | MILLIMETERS |       | NOTES |
|--------|-----------|--------|-------------|-------|-------|
|        | MIN       | MAX    | MIN         | MAX   |       |
| A      | 0.0926    | 0.1043 | 2.35        | 2.65  | -     |
| A1     | 0.0040    | 0.0118 | 0.10        | 0.30  | -     |
| B      | 0.013     | 0.0200 | 0.33        | 0.51  | 9     |
| C      | 0.0091    | 0.0125 | 0.23        | 0.32  | -     |
| D      | 0.3977    | 0.4133 | 10.10       | 10.50 | 3     |
| E      | 0.2914    | 0.2992 | 7.40        | 7.60  | 4     |
| e      | 0.050 BSC |        | 1.27 BSC    |       | -     |
| H      | 0.394     | 0.419  | 10.00       | 10.65 | -     |
| h      | 0.010     | 0.029  | 0.25        | 0.75  | 5     |
| L      | 0.016     | 0.050  | 0.40        | 1.27  | 6     |
| N      | 16        |        | 16          |       | 7     |
| α      | 0°        | 8°     | 0°          | 8°    | -     |

Rev. 1 6/05

## Small Outline Plastic Packages (SOIC)



### NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

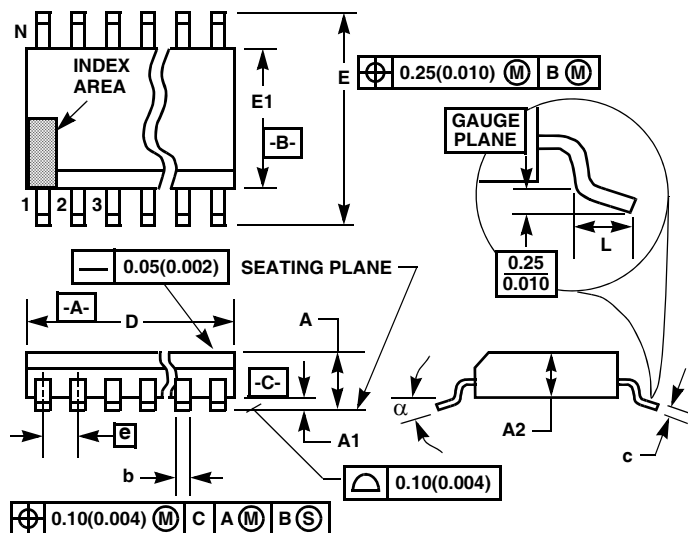
### M18.3 (JEDEC MS-013-AB ISSUE C)

#### 18 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL   | INCHES    |        | MILLIMETERS |       | NOTES |
|----------|-----------|--------|-------------|-------|-------|
|          | MIN       | MAX    | MIN         | MAX   |       |
| A        | 0.0926    | 0.1043 | 2.35        | 2.65  | -     |
| A1       | 0.0040    | 0.0118 | 0.10        | 0.30  | -     |
| B        | 0.013     | 0.0200 | 0.33        | 0.51  | 9     |
| C        | 0.0091    | 0.0125 | 0.23        | 0.32  | -     |
| D        | 0.4469    | 0.4625 | 11.35       | 11.75 | 3     |
| E        | 0.2914    | 0.2992 | 7.40        | 7.60  | 4     |
| e        | 0.050 BSC |        | 1.27 BSC    |       | -     |
| H        | 0.394     | 0.419  | 10.00       | 10.65 | -     |
| h        | 0.010     | 0.029  | 0.25        | 0.75  | 5     |
| L        | 0.016     | 0.050  | 0.40        | 1.27  | 6     |
| N        | 18        |        | 18          |       | 7     |
| $\alpha$ | 0°        | 8°     | 0°          | 8°    | -     |

Rev. 1 6/05

# Thin Shrink Small Outline Plastic Packages (TSSOP)



## M20.173

### 20 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

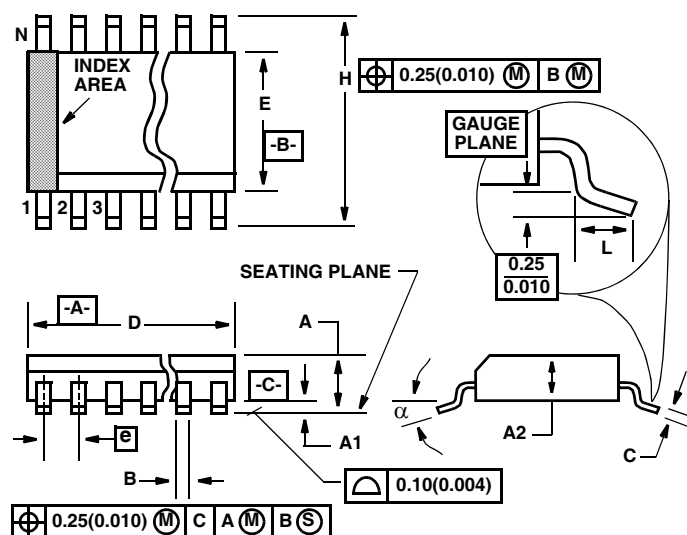
| SYMBOL | INCHES    |        | MILLIMETERS |      | NOTES |
|--------|-----------|--------|-------------|------|-------|
|        | MIN       | MAX    | MIN         | MAX  |       |
| A      | -         | 0.047  | -           | 1.20 | -     |
| A1     | 0.002     | 0.006  | 0.05        | 0.15 | -     |
| A2     | 0.031     | 0.051  | 0.80        | 1.05 | -     |
| b      | 0.0075    | 0.0118 | 0.19        | 0.30 | 9     |
| c      | 0.0035    | 0.0079 | 0.09        | 0.20 | -     |
| D      | 0.252     | 0.260  | 6.40        | 6.60 | 3     |
| E1     | 0.169     | 0.177  | 4.30        | 4.50 | 4     |
| e      | 0.026 BSC |        | 0.65 BSC    |      | -     |
| E      | 0.246     | 0.256  | 6.25        | 6.50 | -     |
| L      | 0.0177    | 0.0295 | 0.45        | 0.75 | 6     |
| N      | 20        |        | 20          |      | 7     |
| α      | 0°        | 8°     | 0°          | 8°   | -     |

Rev. 1 6/98

#### NOTES:

- These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
- The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

## Shrink Small Outline Plastic Packages (SSOP)



### NOTES:

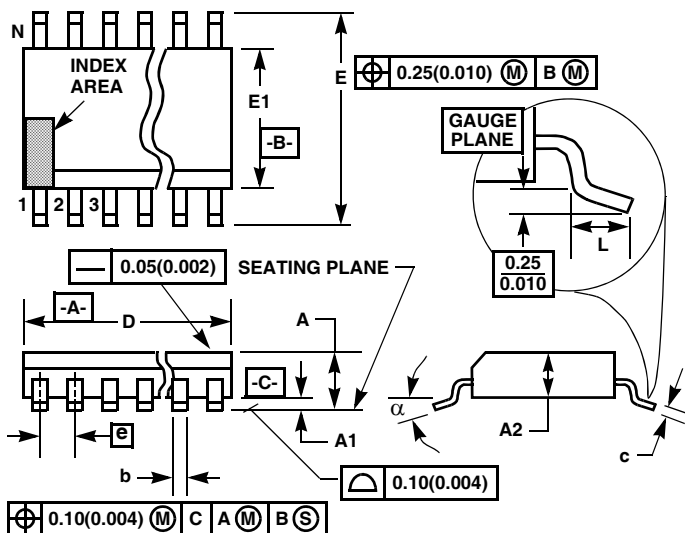
1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

### M20.209 (JEDEC MO-150-AE ISSUE B) 20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL   | INCHES    |        | MILLIMETERS |        | NOTES |
|----------|-----------|--------|-------------|--------|-------|
|          | MIN       | MAX    | MIN         | MAX    |       |
| A        | 0.068     | 0.078  | 1.73        | 1.99   |       |
| A1       | 0.002     | 0.008' | 0.05        | 0.21   |       |
| A2       | 0.066     | 0.070' | 1.68        | 1.78   |       |
| B        | 0.010'    | 0.015  | 0.25        | 0.38   | 9     |
| C        | 0.004     | 0.008  | 0.09        | 0.20'  |       |
| D        | 0.278     | 0.289  | 7.07        | 7.33   | 3     |
| E        | 0.205     | 0.212  | 5.20'       | 5.38   | 4     |
| e        | 0.026 BSC |        | 0.65 BSC    |        |       |
| H        | 0.301     | 0.311  | 7.65        | 7.90'  |       |
| L        | 0.025     | 0.037  | 0.63        | 0.95   | 6     |
| N        | 20        |        | 20          |        | 7     |
| $\alpha$ | 0 deg.    | 8 deg. | 0 deg.      | 8 deg. |       |

Rev. 3 11/02

# Thin Shrink Small Outline Plastic Packages (TSSOP)



## NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AE, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

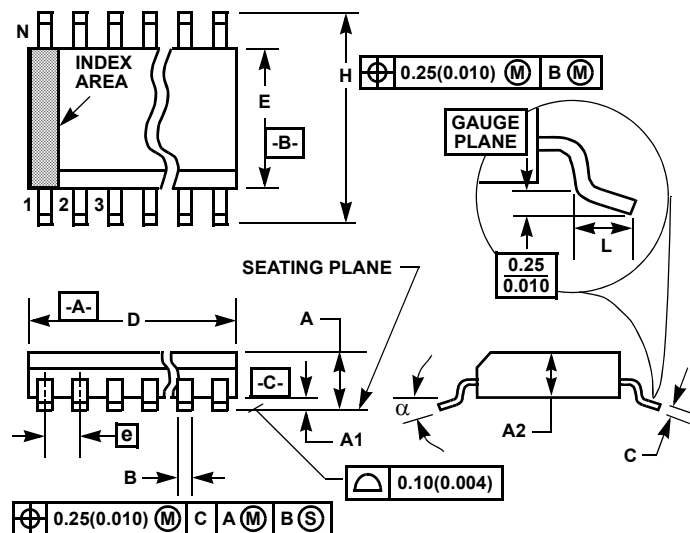
## M28.173

### 28 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES    |        | MILLIMETERS |      | NOTES |
|--------|-----------|--------|-------------|------|-------|
|        | MIN       | MAX    | MIN         | MAX  |       |
| A      | -         | 0.047  | -           | 1.20 | -     |
| A1     | 0.002     | 0.006  | 0.05        | 0.15 | -     |
| A2     | 0.031     | 0.051  | 0.80        | 1.05 | -     |
| b      | 0.0075    | 0.0118 | 0.19        | 0.30 | 9     |
| c      | 0.0035    | 0.0079 | 0.09        | 0.20 | -     |
| D      | 0.378     | 0.386  | 9.60        | 9.80 | 3     |
| E1     | 0.169     | 0.177  | 4.30        | 4.50 | 4     |
| e      | 0.026 BSC |        | 0.65 BSC    |      | -     |
| E      | 0.246     | 0.256  | 6.25        | 6.50 | -     |
| L      | 0.0177    | 0.0295 | 0.45        | 0.75 | 6     |
| N      | 28        |        | 28          |      | 7     |
| α      | 0°        | 8°     | 0°          | 8°   | -     |

Rev. 0 6/98

## Shrink Small Outline Plastic Packages (SSOP)



### NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

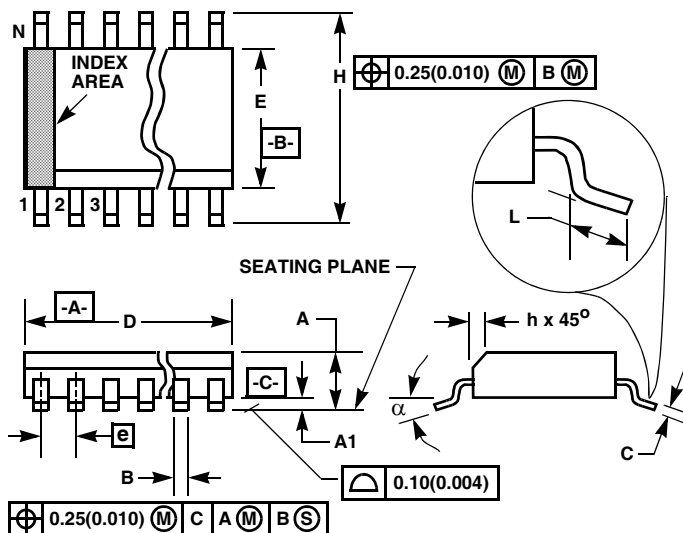
### M28.209 (JEDEC MO-150-AH ISSUE B)

#### 28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES    |       | MILLIMETERS |       | NOTES |
|--------|-----------|-------|-------------|-------|-------|
|        | MIN       | MAX   | MIN         | MAX   |       |
| A      | -         | 0.078 | -           | 2.00  | -     |
| A1     | 0.002     | -     | 0.05        | -     | -     |
| A2     | 0.065     | 0.072 | 1.65        | 1.85  | -     |
| B      | 0.009     | 0.014 | 0.22        | 0.38  | 9     |
| C      | 0.004     | 0.009 | 0.09        | 0.25  | -     |
| D      | 0.390     | 0.413 | 9.90        | 10.50 | 3     |
| E      | 0.197     | 0.220 | 5.00        | 5.60  | 4     |
| e      | 0.026 BSC |       | 0.65 BSC    |       | -     |
| H      | 0.292     | 0.322 | 7.40        | 8.20  | -     |
| L      | 0.022     | 0.037 | 0.55        | 0.95  | 6     |
| N      | 28        |       | 28          |       | 7     |
| α      | 0°        | 8°    | 0°          | 8°    | -     |

Rev. 2 6/05

## Small Outline Plastic Packages (SOIC)



### NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

### M28.3 (JEDEC MS-013-AE ISSUE C)

#### 28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL   | INCHES   |        | MILLIMETERS |       | NOTES |
|----------|----------|--------|-------------|-------|-------|
|          | MIN      | MAX    | MIN         | MAX   |       |
| A        | 0.0926   | 0.1043 | 2.35        | 2.65  | -     |
| A1       | 0.0040   | 0.0118 | 0.10        | 0.30  | -     |
| B        | 0.013    | 0.0200 | 0.33        | 0.51  | 9     |
| C        | 0.0091   | 0.0125 | 0.23        | 0.32  | -     |
| D        | 0.6969   | 0.7125 | 17.70       | 18.10 | 3     |
| E        | 0.2914   | 0.2992 | 7.40        | 7.60  | 4     |
| e        | 0.05 BSC |        | 1.27 BSC    |       | -     |
| H        | 0.394    | 0.419  | 10.00       | 10.65 | -     |
| h        | 0.01     | 0.029  | 0.25        | 0.75  | 5     |
| L        | 0.016    | 0.050  | 0.40        | 1.27  | 6     |
| N        | 28       |        | 28          |       | 7     |
| $\alpha$ | 0°       | 8°     | 0°          | 8°    | -     |

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