

**VFC110**

## High-Frequency VOLTAGE-TO-FREQUENCY CONVERTER

### FEATURES

- HIGH-FREQUENCY OPERATION:  
4MHz FS max
- EXCELLENT LINEARITY:  
 $\pm 0.02\%$  typ at 2MHz
- PRECISION 5V REFERENCE
- DISABLE PIN
- LOW JITTER

### APPLICATIONS

- INTEGRATING A/D CONVERSION
- PROCESS CONTROL
- VOLTAGE ISOLATION
- VOLTAGE-CONTROLLED OSCILLATOR
- FM TELEMETRY

### DESCRIPTION

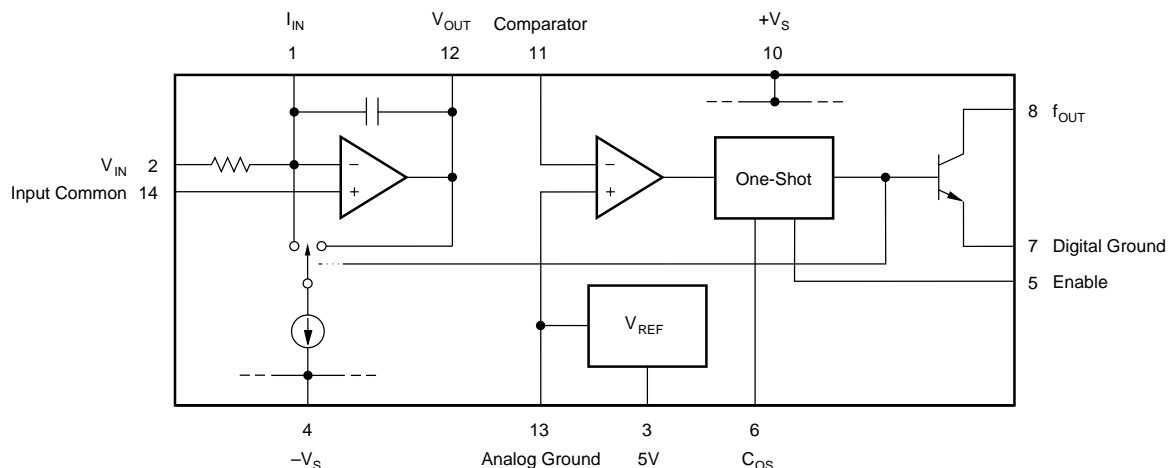
The VFC110 voltage-to-frequency converter is a third-generation VFC offering improved features and performance. These include higher frequency operation, an on-board precision 5V reference and a Disable function.

The precision 5V reference can be used for offsetting the VFC transfer function, as well as exciting transducers or bridges. The Enable pin allows several VFCs' outputs to be paralleled, multiplexed, or simply to shut off the VFC. The open-collector frequency

output is TTL/CMOS-compatible. The output may be isolated by using an opto-coupler or transformer.

Internal input resistor, one-shot and integrator capacitors simplify applications circuits. These components are trimmed for a full-scale output frequency of 4MHz at 10V input. No additional components are required for many applications.

The VFC110 is packaged in plastic and ceramic 14-pin DIPs. Industrial and military temperature range gradeouts are available.



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# SPECIFICATIONS

At  $T_A = +25^{\circ}\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	VFC110BG			VFC110AG/SG/AP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>VOLTAGE-TO-FREQUENCY OPERATION</b> Nonlinearity <sup>(1)</sup> : $f_{\text{FS}} = 100\text{kHz}$ $f_{\text{FS}} = 1\text{MHz}$ $f_{\text{FS}} = 2\text{MHz}$ $f_{\text{FS}} = 4\text{MHz}$ Gain Error, $f = 1\text{MHz}$ Gain Drift, $f = 1\text{MHz}$ Relative to $V_{\text{REF}}$ PSRR	$C_{\text{OS}} = 2.2\text{nF}$ , $R_{\text{IN}} = 44\text{k}\Omega$ $C_{\text{OS}} = 150\text{pF}$ , $R_{\text{IN}} = 40\text{k}\Omega$ $C_{\text{OS}} = 56\text{pF}$ , $R_{\text{IN}} = 34\text{k}\Omega$ $C_{\text{OS}} = (\text{Int})$ , $R_{\text{IN}} = (\text{Int})$ $C_{\text{OS}} = 150\text{pF}$ , $R_{\text{IN}} = 40\text{k}\Omega$ Specified Temp Range Specified Temp Range $V_S = \pm 8\text{V}$ to $\pm 18\text{V}$		0.005 0.01 0.02 1 5 50	0.01 0.05   0.05		0.01  * *  100	0.05 0.1   * 100 0.1	%FS %FS %FS %FS % ppm/ $^{\circ}\text{C}$ ppm/ $^{\circ}\text{C}$ %/V
<b>INPUT</b> Full Scale Input Current $I_{\text{B-}}$ (Inverting Input) $I_{\text{B+}}$ (Non-Inverting Input) $V_{\text{OS}}$ $V_{\text{OS}}$ Drift	Specified Temp Range		250 15 250 35	500 60 3		* 20 * *	* 100 3	$\mu\text{A}$ nA nA mV $\mu\text{V}/^{\circ}\text{C}$
<b>INTEGRATOR AMPLIFIER OUTPUT</b> Output Voltage Range Output Current Drive Capacitive Load	$R_L = 2\text{k}\Omega$ No Oscillations	-0.2 5	20 10	$+V_S - 4$	* *	* 10	*  	V mA nF
<b>COMPARATOR INPUT</b> $I_{\text{B}}$ (Input Bias Current) Trigger Voltage Input Voltage Range		-5	-5 $\pm 50$	$+V_S$	*	* *	*	$\mu\text{A}$ mV V
<b>OPEN COLLECTOR OUTPUT</b> $V_{\text{O}}$ Low $I_{\text{LEAKAGE}}$ Fall Time Delay to Rise Settling Time	To Specified Linearity for a Full-Scale Input Step		0.1 25 25	0.4 1		* * *	* *  	V $\mu\text{A}$ ns ns
<b>REFERENCE VOLTAGE</b> Voltage Voltage Drift Load Regulation PSRR Current Limit	$I_{\text{O}} = 0$ to $10\text{mA}$ $V_S = \pm 8\text{V}$ to $\pm 18\text{V}$ Short Circuit	4.97  15	5 2 5 20	5.03 20 10	*   	*  * * *	* 50 *	V ppm/ $^{\circ}\text{C}$ mV mV/V mA
<b>ENABLE INPUT</b> $V_{\text{HIGH}}$ ( $f_{\text{OUT}}$ Enabled) $V_{\text{LOW}}$ ( $f_{\text{OUT}}$ Disabled) $I_{\text{HIGH}}$ $I_{\text{LOW}}$	Specified Temp Range Specified Temp Range	2	0.1 1	0.4	*  	* * *	*  	V V $\mu\text{A}$ $\mu\text{A}$
<b>POWER SUPPLY</b> Voltage, $\pm V_S$ Current		$\pm 8$	$\pm 15$ 13	$\pm 18$ 16	*  	* * *	* * *	V mA
<b>TEMPERATURE RANGE</b> Specified AG, BG, AP SG Storage AG, BG, SG AP		-25 -55  -65 -40		+85 +125  +150 +125	*  * *		*  * *	$^{\circ}\text{C}$ $^{\circ}\text{C}$  $^{\circ}\text{C}$ $^{\circ}\text{C}$

\* Same specifications as VFC110BG.

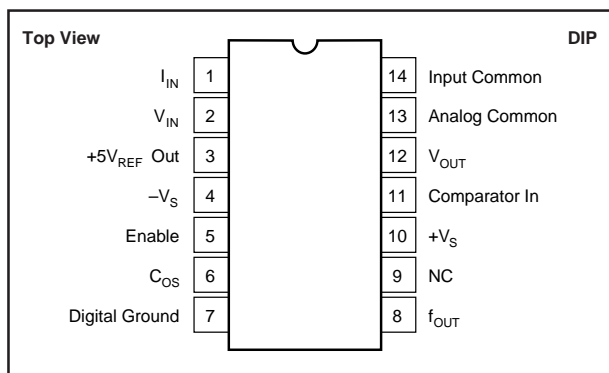
NOTE: (1) Nonlinearity measured from 1V to 10V input.

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VFC110

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages (+V <sub>S</sub> to -V <sub>S</sub> )	40V
f <sub>OUT</sub> Sink Current	50mA
Comparator In Voltage	-5V to +V <sub>S</sub>
Enable Input	+V <sub>S</sub> to -V <sub>S</sub>
Integrator Common-Mode Voltage	-1.5V to +1.5V
Integrator Differential Input Voltage	+0.5V to -0.5V
Integrator Out (short-circuit)	Indefinite
V <sub>REF</sub> Out (short-circuit)	Indefinite
Operating Temperature Range	
G Package	-55°C to +125°C
P Package	-40°C to +85°C
Storage Temperature	
G Package	-60°C to +150°C
P Package	-40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

## PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
VFC110AG	14-Pin Ceramic DIP	169
VFC110BG	14-Pin Ceramic DIP	169
VFC110SG	14-Pin Ceramic DIP	169
VFC110AP	14-Pin Plastic DIP	010

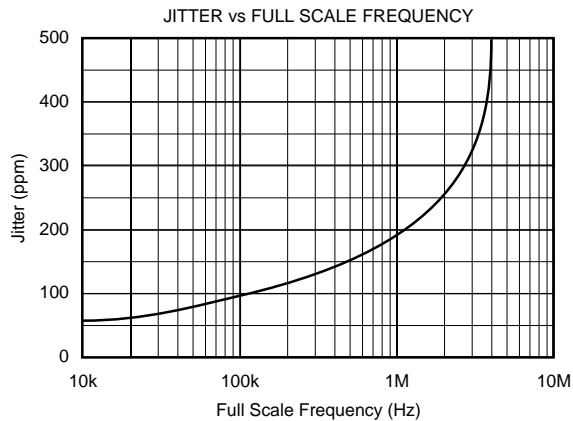
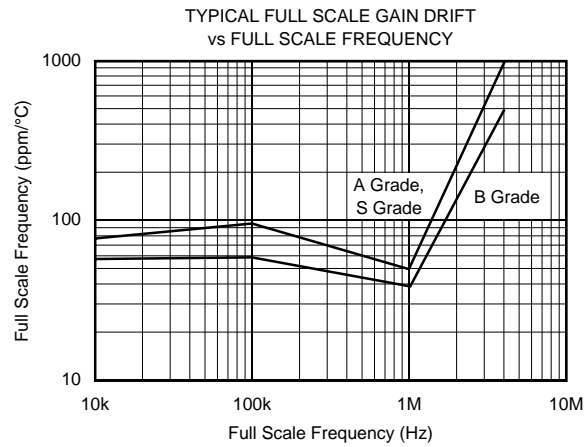
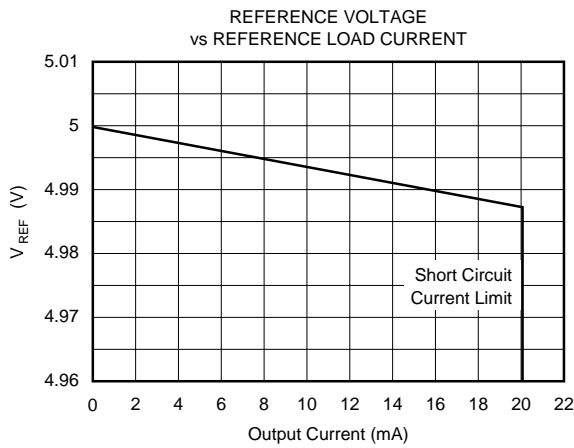
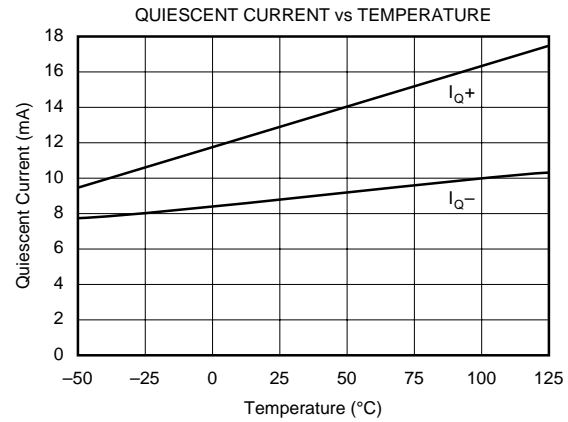
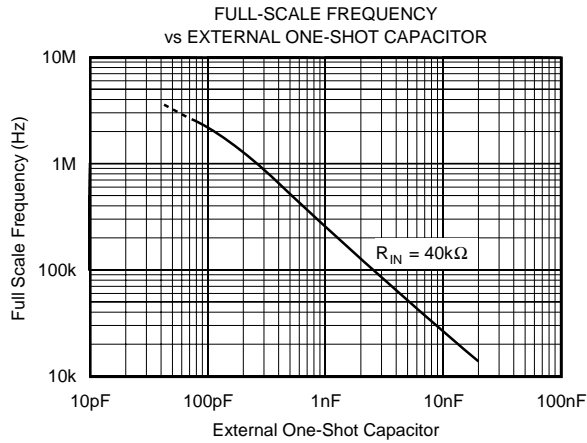
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## ORDERING INFORMATION

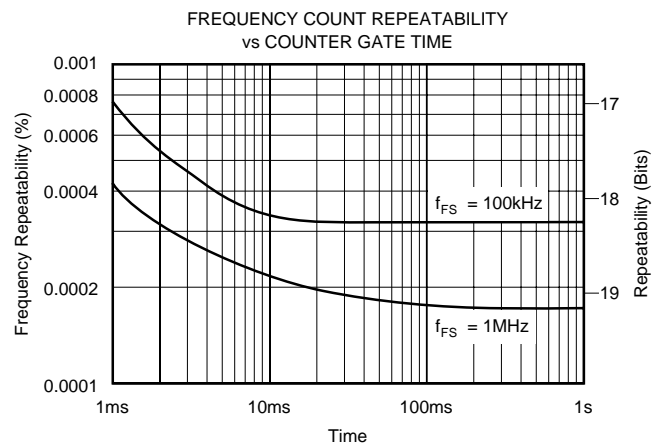
PRODUCT	PACKAGE	TEMPERATURE RANGE
VFC110AG	Ceramic DIP	-25°C to +85°C
VFC110BG	Ceramic DIP	-25°C to +85°C
VFC110SG	Ceramic DIP	-55°C to +125°C
VFC110AP	Plastic DIP	-25°C to +85°C

# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



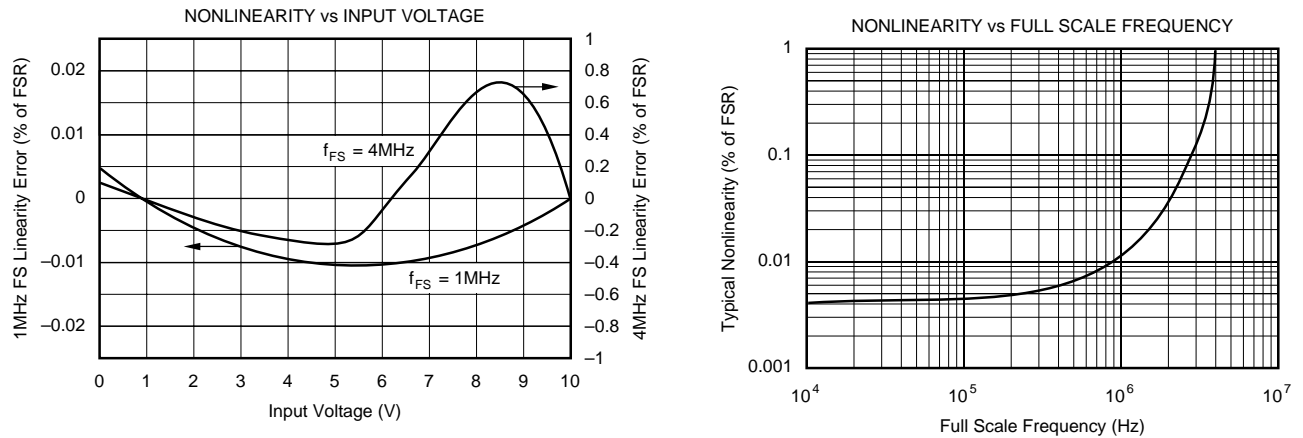
Jitter is the ratio of the  $1\sigma$  value of the distribution of the period ( $1/f_{OUT, \text{max}}$ ) to the mean of the period.



This graph describes the low frequency stability of the VFC110: the ratio of the  $1\sigma$  point of the distribution of 100 runs (where each mean frequency came from 1000 readings for each gate time) to the overall mean frequency.

# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



## OPERATION

Figure 1 shows the connections required for operation at a full-scale output frequency of 4MHz. Only power supply bypass capacitors and an output pull-up resistor,  $R_{PU}$ , are required for this mode of operation. A 0V to 10V input voltage produces a 0Hz to 4MHz output frequency. The internal input resistor, one-shot and integrator capacitors set the full-scale output frequency. The input is applied to the summing junction of the integrator amplifier through the  $25\text{k}\Omega$  internal input resistor. Pin 14 (the non-inverting amplifier input) should be referred directly to the negative side of  $V_{IN}$ . The common-mode range of the integrating amplifier is limited to approximately  $-1\text{V}$  to  $+1\text{V}$  referred to analog ground. This allows the non-inverting input to Kelvin-sense the common connection of  $V_{IN}$ , easily accommodating any

ground-drop errors. The input impedance loading  $V_{IN}$  is equal to the input resistor—approximately  $25\text{k}\Omega$ .

## OPERATION AT LOWER FREQUENCIES

The VFC110 can be operated at lower frequencies simply by limiting the input voltage to less than the nominal 10V full-scale input. To maintain a 10V FS input and highest accuracy, however, external components are required (see Table I). Small adjustments may be required in the nominal values indicated. Integrator and one-shot capacitors are added in parallel to internal capacitors. Figure 2 shows the connections required for 100kHz full scale output. The one-shot capacitor,  $C_{OS}$ , should be connected to logic ground. The one-shot connection (pin 6) is not short-circuit protected. Short-circuits to ground may damage the device.

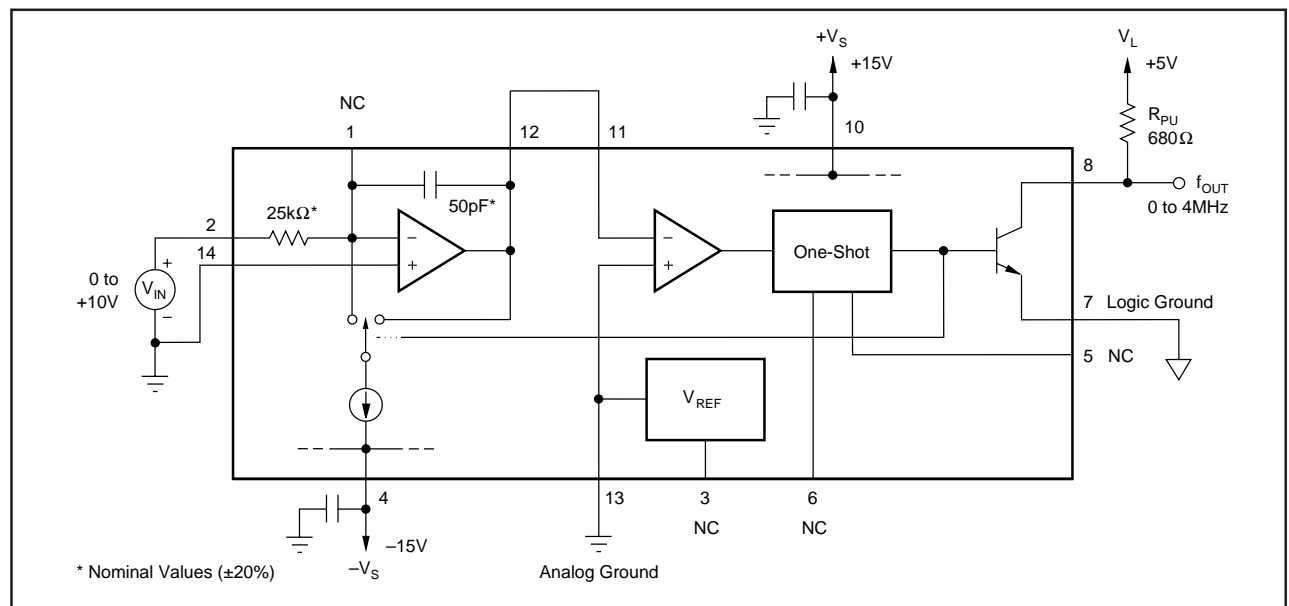


FIGURE 1. 4MHz Full-Scale Operation.

## COMPONENT SELECTION

The integrator capacitor serves as a “charge bucket,” where charge is accumulated from the input,  $V_{IN}$ , and that charge is drained during the one-shot period. While the size of the bucket (capacitor value) is not critical, it must not leak. Capacitor leakage or dielectric absorption can affect the

## PULL-UP RESISTOR

## ENABLE PIN

A logic Low at the Enable input causes output pulses to cease. This is accomplished by interrupting the signal path through the one-shot circuitry. While disabled, all circuitry remains active and quiescent current is unchanged. Since no reset current pulses can occur while disabled, any positive input voltage will cause the integrator op amp to ramp negatively and saturate at its most negative output swing of approximately  $-0.7V$ .

FULL-SCALE FREQUENCY, $f_{FS}$	EXTERNAL COMPONENTS		
	$R_{IN}$	$C_{OS}$	$C_{INT}$
4MHz	*	*	*
2MHz	34k $\Omega$	56pF	*
1MHz	40k $\Omega$	150pF	*
500kHz	58k $\Omega$	330pF	2nF
100kHz	44k $\Omega$	2.2nF	10nF
50kHz	88k $\Omega$	2.2nF	0.1 $\mu$ F
10kHz	44k $\Omega$	22nF	0.1 $\mu$ F

\* Use internal component only.

The values given were determined empirically to give the optimal performance, taking into consideration tradeoffs between linearity and jitter for each given full scale frequency of operation. The capacitors listed were chosen from standard values of NPO ceramic type capacitors while the resistor values were rounded off. Larger  $C_{INT}$  values may improve linearity, but may also increase frequency noise.

TABLE I. Component Selection Table.

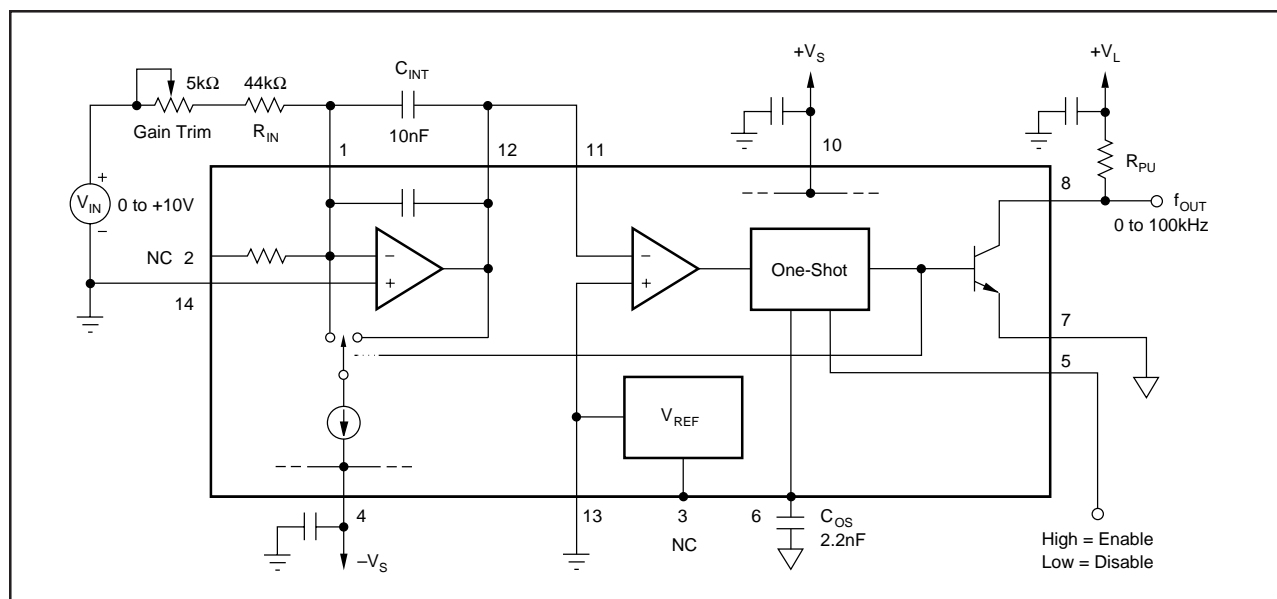


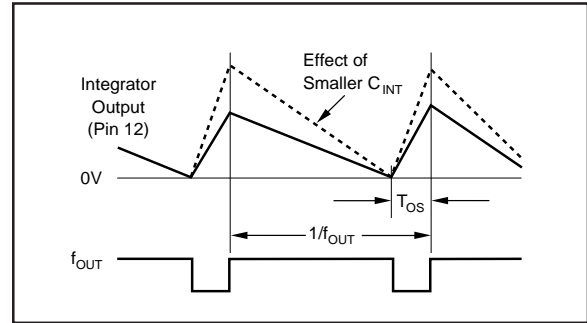
FIGURE 2. 100kHz Full-Scale Operation.

## PRINCIPLE OF OPERATION

The VFC110 uses a charge-balance technique to achieve high accuracy. The heart of this technique is an analog integrator formed by the integrator op amp, feedback capacitor  $C_{INT}$ , and input resistor  $R_{IN}$ . The integrator's output voltage is proportional to the charge stored in  $C_{INT}$ . An input voltage develops an input current of  $V_{IN}/R_{IN}$ , which is forced to flow through  $C_{INT}$ . This current charges  $C_{INT}$ , causing the integrator output voltage to ramp negatively.

When the output of the integrator ramps to 0V, the comparator trips, triggering the one-shot. This connects the reference current,  $I_{REF}$ , to the integrator input during the one-shot period,  $T_{OS}$ . This switched current causes the integrator output to ramp positively until the one-shot period ends. Then the cycle starts again.

The oscillation is regulated by the balance of current (or charge) between the input current and the time-averaged



reset current. The equation of current balance is

$$I_{IN} = I_{REF} \cdot \text{Duty Cycle}$$

$$V_{IN}/R_{IN} = I_{REF} \cdot f_{OUT} \cdot T_{OS}$$

where  $T_{OS}$  is the one-shot period and  $f_{OUT}$  is the oscillation frequency.

When the Enable input receives a logic High (greater than +2V), a reset current cycle is initiated (causing  $f_{OUT}$  to go Low). The integrator ramps positively and normal operation is established. The time required for the output frequency to stabilize is equal to approximately one cycle of the final output frequency plus 1μs.

Using the Enable input, several VFCs' outputs can be connected to a single output line. All disabled VFCs will have a high output impedance; one active VFC can then transmit on the output line. Since the disabled VFCs are not oscillating, they cannot interfere or "lock" with the operating VFC. Locking can occur when one VFC operates at nearly the same frequency as—or a multiple of—a nearby VFC. Coupling between the two may cause them to lock to the same or exact multiple frequency. It then takes a small incremental input voltage change to unlock them. Locking cannot occur when unneeded VFCs are disabled.

## REFERENCE VOLTAGE

The  $V_{REF}$  output is useful for offsetting the transfer function and exciting sensors. Figure 3 shows  $V_{REF}$  used to offset the transfer function of the VFC110 to achieve a bipolar input voltage range. Sub-surface zener reference circuitry is used for low noise and excellent temperature drift. Output current is specified to 10mA and current-limited to approximately 20mA. Excessive or variable loads on  $V_{REF}$  can decrease frequency stability due to internal heating.

## MEASURING THE OUTPUT FREQUENCY

To complete an integrating A/D conversion, the output frequency of the VFC110 must be counted. Simple frequency counting is accomplished by counting output pulses for a reference time (usually derived from a crystal oscillator).

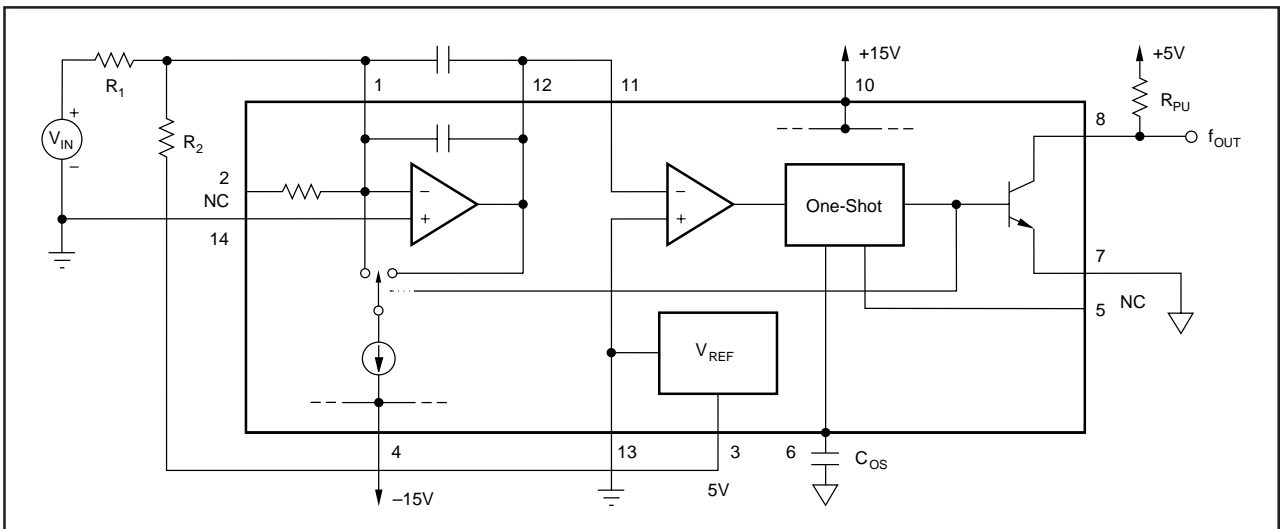


FIGURE 3. Offsetting the Frequency Output.

Since  $f_{OUT}$  is an open-collector device, the negative-going edge provides the fastest logic transition. Clocking the counter on the falling edge will provide the best results in noisy environments.

## FREQUENCY NOISE

Frequency noise (small random variation in the output frequency) limits the useful resolution of fast frequency measurement techniques. Long measurement time averages the effect of frequency noise and achieves the maximum useful resolution. The VFC110 is designed to minimize frequency noise and allows improved useful resolution with short measurement times. The typical curve “Frequency Count Repeatability vs Counter Gate Time” shows the effect of noise as the counter gate time is varied. It shows the one

## FREQUENCY-TO-VOLTAGE CONVERSION

This frequency-to-voltage converter operates by averaging (filtering) the reference current pulses triggered on every falling edge at the frequency input. Voltage ripple with a frequency equal to the input will be present in the output voltage. The magnitude of this ripple voltage is inversely proportional to the integrator capacitor. The ripple can be made arbitrarily small with a large capacitor, but at the sacrifice of settling time. The R-C time constant of  $C_{INT}$  and  $R_{IN}$  determine the settling behavior. A better compromise between output ripple and settling time can be achieved by adding a low-pass filter following the voltage output.

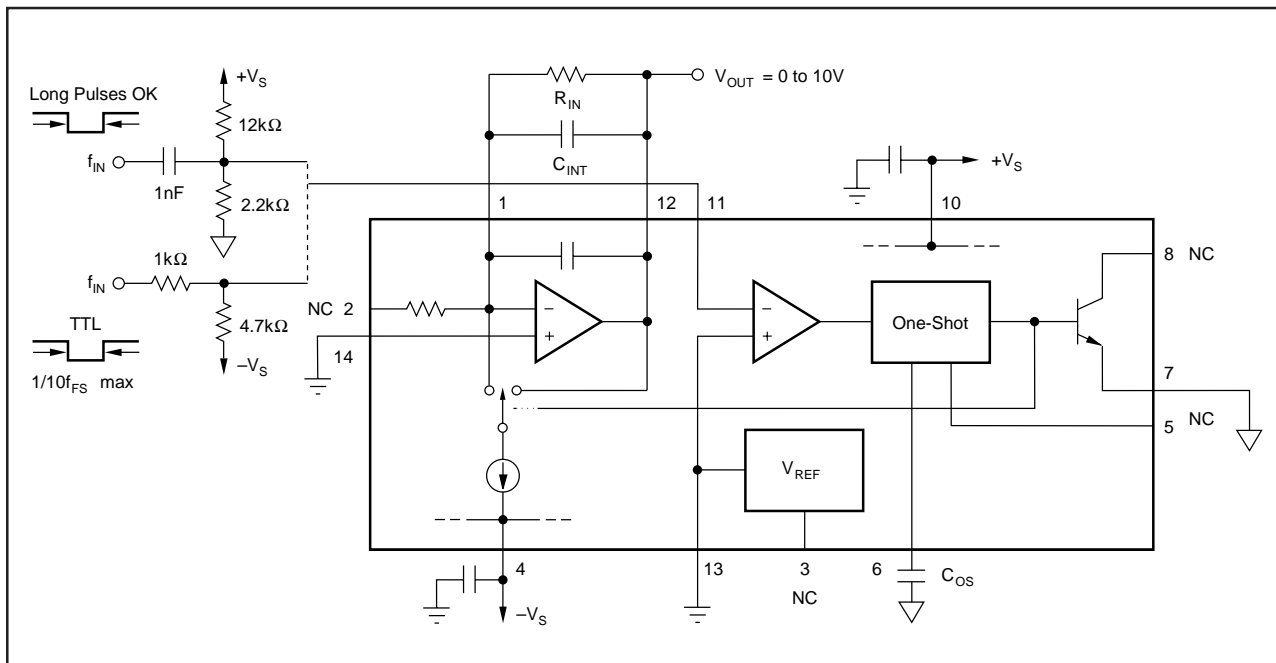


FIGURE 4. Frequency-to-Voltage Conversion.



## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
VFC110AG	OBSOLETE	CDIP SB	JD	14		None	Call TI	Call TI
VFC110AG2	OBSOLETE	CDIP SB	JD	14		None	Call TI	Call TI
VFC110AP	ACTIVE	PDIP	N	14	25	None	Call TI	Level-NA-NA-NA
VFC110BG	OBSOLETE	CDIP SB	JD	14		None	Call TI	Call TI
VFC110BG1	OBSOLETE	CDIP SB	JD	14		None	Call TI	Call TI
VFC110SG	OBSOLETE	CDIP SB	JD	14		None	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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