

80C51 8-bit microcontroller family

4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V), low power, high speed (33 MHz)

80C51/87C51/80C31

DESCRIPTION

The Philips 8XC51/31 is a high-performance static 80C51 design fabricated with Philips high-density CMOS technology with operation from 2.7V to 5.5V.

The 8XC51/31 contains a 4k × 8 ROM, a 128 × 8 RAM, 32 I/O lines, three 16-bit counter/timers, a six-source, four-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device is a low power static design which offers a wide range of operating frequencies down to zero. Two software selectable modes of power reduction—idle mode and power-down mode are available. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative. Since the design is static, the clock can be stopped without loss of user data and then the execution resumed from the point the clock was stopped.

SELECTION TABLE

For applications requiring more ROM and RAM, see the 8XC52/54/58/80C32, 8XC51FA/FB/FC/80C51FA, and 8XC51RA+/RB+/RC+/80C51RA+ data sheet.

ROM/EPROM Memory Size (X by 8)	FLASH Available	RAM Size (X by 8)	Programmable Timer Counter (PCA)
80C31/8XC51			
0K/4K	Yes	128	No
80C32/8XC52/54/58			
0K/8K/16K/32K	Yes	256	No
80C51FA/8XC51FA/FB/FC			
0K/8K/16K/32K		256	Yes
80C51RA+/8XC51RA+/RB+/RC+			
0K/8K/16K/32K	Yes, RC+	512	Yes
8XC51RD+			
64K	Yes	1024	Yes

FEATURES

- 8051 Central Processing Unit
 - 4k × 8 ROM (80C51)
 - 128 × 8 RAM
 - Three 16-bit counter/timers
 - Full duplex serial channel
 - Boolean processor
 - Full static operation
 - Low voltage (2.7V to 5.5V@ 16MHz) operation
- Memory addressing capability
 - 64k ROM and 64k RAM
- Power control modes:
 - Clock can be stopped and resumed
 - Idle mode
 - Power-down mode
- CMOS and TTL compatible
- Three speed ranges at V_{CC} = 5V
 - 0 to 16MHz
 - 0 to 33MHz
- Three package styles
- Extended temperature ranges
- Dual Data Pointers
- Second DPTR register
- Security bits:
 - ROM (2 bits)
 - OTP/EPROM (3 bits)
- Encryption array—64 bytes
- 4 level priority interrupt
- 6 interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
 - Framing error detection
 - Automatic address recognition
- Programmable clock out
- Asynchronous port reset
- Low EMI (inhibit ALE)
- Wake-up from Power Down by an external interrupt (8XC51)

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80C51/87C51 AND 80C31 ORDERING INFORMATION

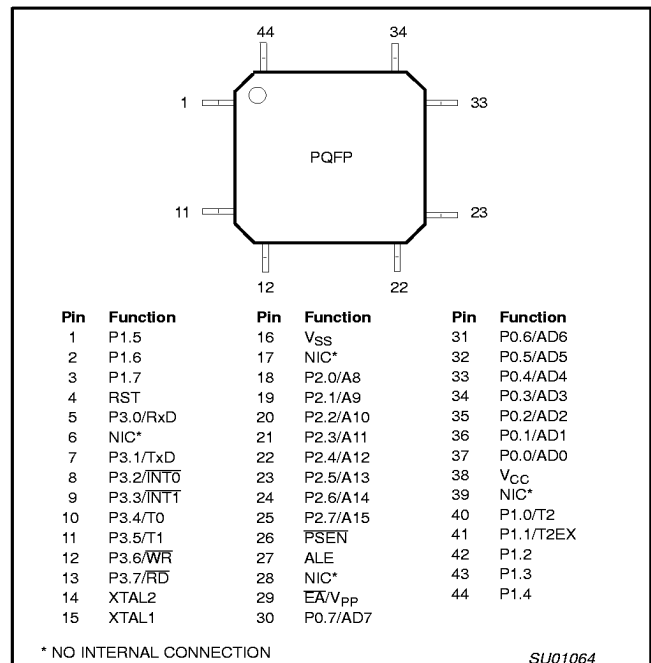
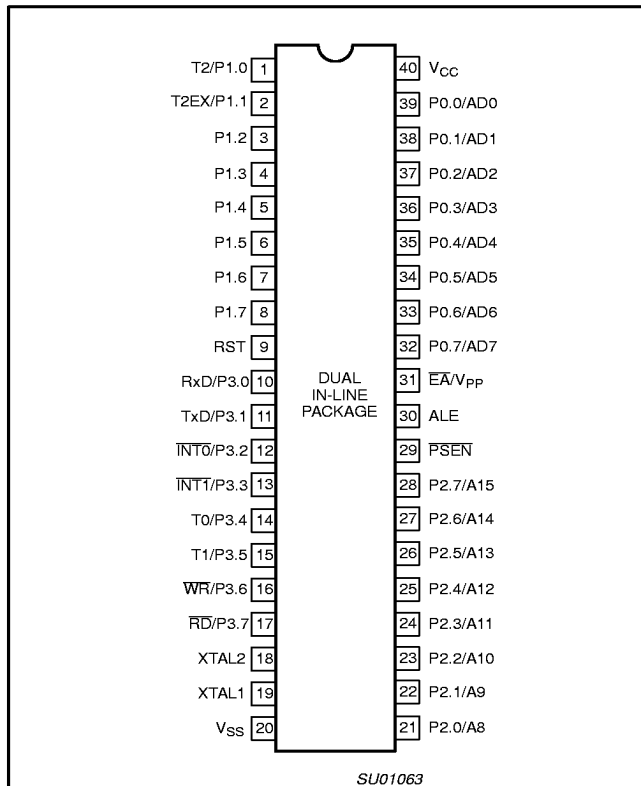
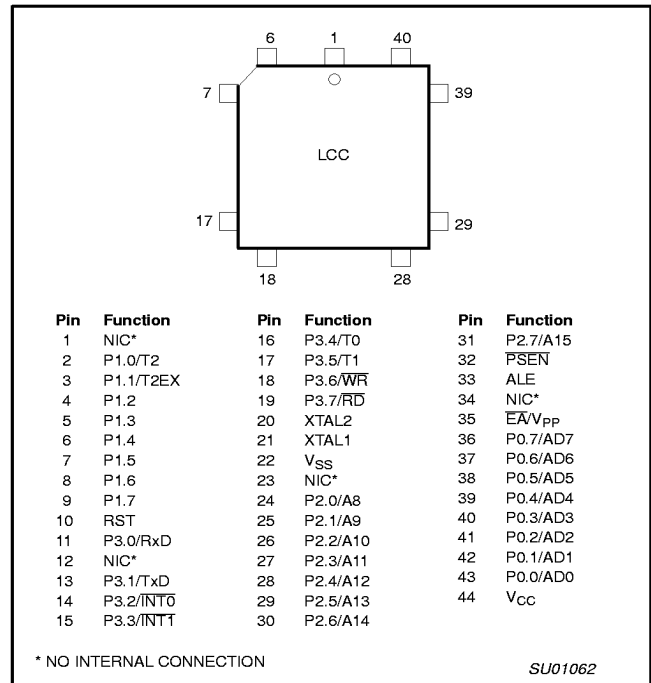
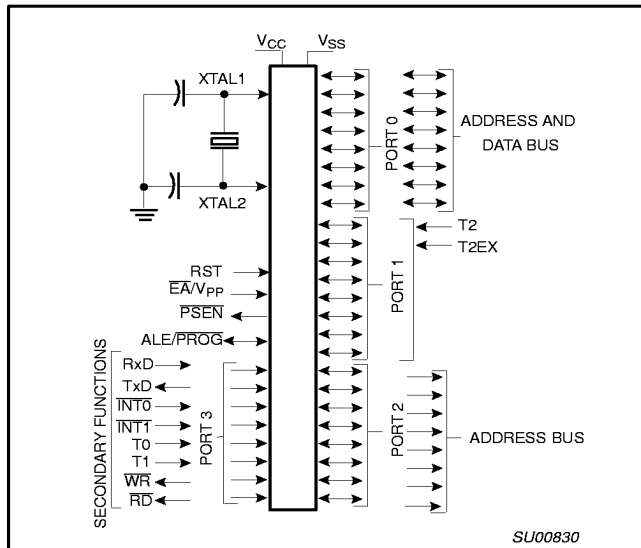
	MEMORY SIZE 4K × 8	ROMless	TEMPERATURE RANGE °C AND PACKAGE	VOLTAGE RANGE	FREQ. (MHz)	DWG. #
ROM	P80C51SBPN	P80C31SBPN	0 to +70, Plastic Dual In-line Package	2.7V to 5.5V	0 to 16	SOT129-1
OTP	P87C51SBPN					
ROM	P80C51SBAA	P80C31SBAA	0 to +70, Plastic Leaded Chip Carrier	2.7V to 5.5V	0 to 16	SOT187-2
OTP	P87C51SBAA					
ROM	P80C51SBBB	P80C31SBBB	0 to +70, Plastic Quad Flat Pack	2.7V to 5.5V	0 to 16	SOT307-2
OTP	P87C51SBBB					
ROM	P80C51SFPN	P80C31SFPN	–40 to +85, Plastic Dual In-line Package	2.7V to 5.5V	0 to 16	SOT129-1
OTP	P87C51SFPN					
ROM	P80C51SFAA	P80C31SFAA	–40 to +85, Plastic Leaded Chip Carrier	2.7V to 5.5V	0 to 16	SOT187-2
OTP	P87C51SFAA					
ROM	P80C51SFBB	P80C31SFBB	–40 to +85, Plastic Quad Flat Pack	2.7V to 5.5V	0 to 16	SOT307-2
OTP	P87C51SFBB					
ROM	P80C51UBAA	P80C31UBAA	0 to +70, Plastic Leaded Chip Carrier	5V	0 to 33	SOT187-2
OTP	P87C51UBAA					
ROM	P80C51UBPN	P80C31UBPN	0 to +70, Plastic Dual In-line Package	5V	0 to 33	SOT129-1
OTP	P87C51UBPN					
ROM	P80C51UBBB	P80C31UBBB	0 to +70, Plastic Quad Flat Pack	5V	0 to 33	SOT307-2
OTP	P87C51UBBB					
ROM	P80C51UFAA	P80C31UFAA	–40 to +85, Plastic Leaded Chip Carrier	5V	0 to 33	SOT187-2
OTP	P87C51UFAA					
ROM	P80C51UFPN	P80C31UFPN	–40 to +85, Plastic Dual In-line Package	5V	0 to 33	SOT129-1
OTP	P87C51UFPN					
ROM	P80C51UFBB	P80C31UFBB	–40 to +85, Plastic Quad Flat Pack	5V	0 to 33	SOT307-2
OTP	P87C51UFBB					

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The block diagram illustrates the internal architecture of the 80C51 microcontroller. It features a central system bus connecting various components. On the left, the Timing and Control block interfaces with external signals (PSEN, ALE/PROG, EAV_{PP}, RST) and the Oscillator (XTAL1, XTAL2). The core includes RAM, ROM/EPROM, and several registers: B, ACC, TMP1, TMP2, PSW, and the Program Address Register. The ALU (Arithmetic Logic Unit) receives data from the registers and performs operations. The SFRs (Special Function Registers) and Timers are also connected to the bus. The I/O ports (0, 1, 2, 3) are shown with their respective drivers and latches. The diagram also indicates the connection to external memory (8-bit and 16-bit buses) and the DPTR's (Data Pointer Register) Multiple register.

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PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
V _{SS}	20	22	16	I	Ground: 0V reference.
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0–P0.7	39–32	43–36	37–30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and received code bytes during EPROM programming. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions for Port 1 include: T2 (P1.0): Timer/Counter 2 external count input/clockout (see Programmable Clock-Out). T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction control.
P2.0–P2.7	1 2 21–28	2 3 24–31	40 41 18–25	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during EPROM programming and verification.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 80C51 family, as listed below: RxD (P3.0): Serial input port TxD (P3.1): Serial output port INT0 (P3.2): External interrupt INT1 (P3.3): External interrupt T0 (P3.4): Timer 0 external input T1 (P3.5): Timer 1 external input WR (P3.6): External data memory write strobe RD (P3.7): External data memory read strobe
RST	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{CC} .
ALE/PROG	30	33	27	O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.
PSEN	29	32	26	O	Program Store Enable: The read strobe to external program memory. When the 8XC51/31 is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
EA/V _{PP}	31	35	29	I	External Access Enable/Programming Supply Voltage: EA must be externally held low to enable the device to fetch code from external program memory locations 0000H and 0FFFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFFH. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming. If security bit 1 is programmed, EA will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier.

NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5V or V_{SS} – 0.5V, respectively.

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Table 1. 8XC51/80C31 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE						
			MSB				LSB										
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H						
AUXR#	Auxiliary	8EH	—	—	—	—	—	—	—	AO	xxxxxxx0B						
AUXR1#	Auxiliary 1	A2H	—	—	—	LPEP ²	WUPD ³	0	—	DPS	xxx000x0B						
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H						
DPTR: DPH DPL	Data Pointer (2 bytes)																
	DPH Data Pointer High	83H									00H						
	DPL Data Pointer Low	82H									00H						
			AF	AE	AD	AC	AB	AA	A9	A8							
IE*	Interrupt Enable	A8H	EA	—	ET2	ES	ET1	EX1	ET0	EX0	0x000000B						
			BF	BE	BD	BC	BB	BA	B9	B8							
IP*	Interrupt Priority	B8H	—	—	PT2	PS	PT1	PX1	PT0	PX0	xx000000B						
			B7	B6	B5	B4	B3	B2	B1	B0							
IPH#	Interrupt Priority High	B7H	—	—	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	xx000000B						
			87	86	85	84	83	82	81	80							
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH						
			97	96	95	94	93	92	91	90							
P1*	Port 1	90H	—	—	—	—	—	—	T2EX	T2	FFH						
			A7	A6	A5	A4	A3	A2	A1	A0							
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH						
			B7	B6	B5	B4	B3	B2	B1	B0							
P3*	Port 3	B0H	RD	WR	T1	T0	INT1	INT0	TxD	RxD	FFH						
PCON# ¹	Power Control	87H	SMOD1	SMOD0	—	POF	GF1	GF0	PD	IDL	00xx0000B						
			D7	D6	D5	D4	D3	D2	D1	D0							
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	—	P	000000x0B						
RACAP2H#	Timer 2 Capture High	CBH									00H						
RACAP2L#	Timer 2 Capture Low	CAH															00H
SADDR#	Slave Address	A9H															00H
SADEN#	Slave Address Mask	B9H															00H
SBUF	Serial Data Buffer	99H									xxxxxxxxxB						
			9F	9E	9D	9C	9B	9A	99	98							
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H						
SP	Stack Pointer	81H									07H						
			8F	8E	8D	8C	8B	8A	89	88							
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H						
			CF	CE	CD	CC	CB	CA	C9	C8							
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T ²	CP/RL ²	00H						
T2MOD#	Timer 2 Mode Control	C9H	—	—	—	—	—	—	T2OE	DCEN	xxxxxx00B						
TH0	Timer High 0	8CH									00H						
TH1	Timer High 1	8DH															00H
TH2#	Timer High 2	CDH															00H
TL0	Timer Low 0	8AH															00H
TL1	Timer Low 1	8BH															00H
TL2#	Timer Low 2	CCH															00H
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H						

* SFRs are bit addressable.

SFRs are modified from or added to the 80C51 SFRs.

— Reserved bits.

1. Reset value depends on reset source.

2. LPEP – Low Power EPROM operation (OTP/EPROM only)

3. Not available on 80C31.

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OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles.

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

Idle Mode

In idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2.0V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

For the 87C51 and 80C51 either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external

interrupt allows both the SFRs and the on-chip RAM to retain their values. WUPD (AUXR1.3—Wakeup from Power Down) enables or disables the wakeup from power down with external interrupt.

Where:

WUPD = 0 Disable

WUPD = 1 Enable

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

For the 80C31, wakeup from power down is always enabled.

LPEP

The eeprom array contains some analog circuits that are not required when V_{CC} is less than 4V, but are required for a V_{CC} greater than 4V. The LPEP bit (AUXR.4), when set, will powerdown these analog circuits resulting in a reduced supply current. This bit should be set ONLY for applications that operate at a V_{CC} less than 4V.

Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

- Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
- Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51/31 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 61Hz to 4MHz at a 16MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

Where:

(RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

TIMER 2 OPERATION

Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2* in the special function register T2CON (see Figure 1). Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 3.

Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/T2* in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2= 1, Timer 2 operates as described above, but with the added feature that a 1- to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and

TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt). The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 2 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/12 pulses.).

Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured (as either a timer or counter (C/T2* in T2CON)) then programmed to count up or down. The counting direction is determined by bit DCEN(Down Counter Enable) which is located in the T2MOD register (see Figure 3). When reset is applied the DCEN=0 which means Timer 2 will default to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 4 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 5 DCEN=1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

Table 3. Timer 2 Operating Modes

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)

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(MSB)				(LSB)			
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T $\overline{2}$	CP/RL $\overline{2}$

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T $\overline{2}$	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).
CP/RL $\overline{2}$	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

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Figure 1. Timer/Counter 2 (T2CON) Control Register

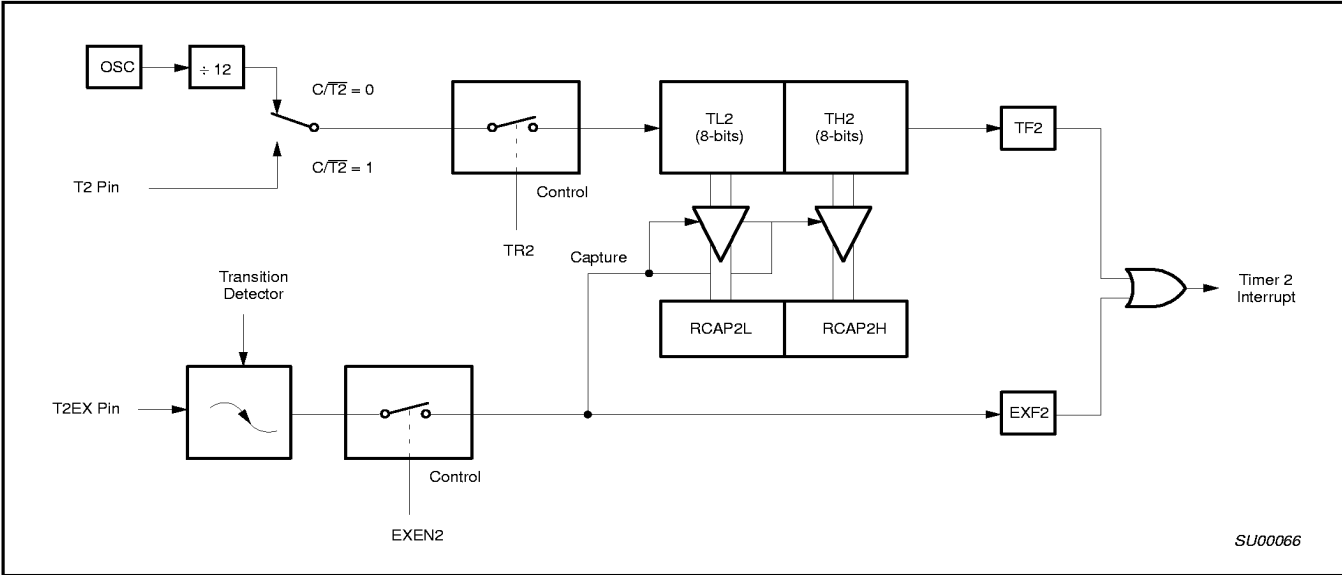


Figure 2. Timer 2 in Capture Mode

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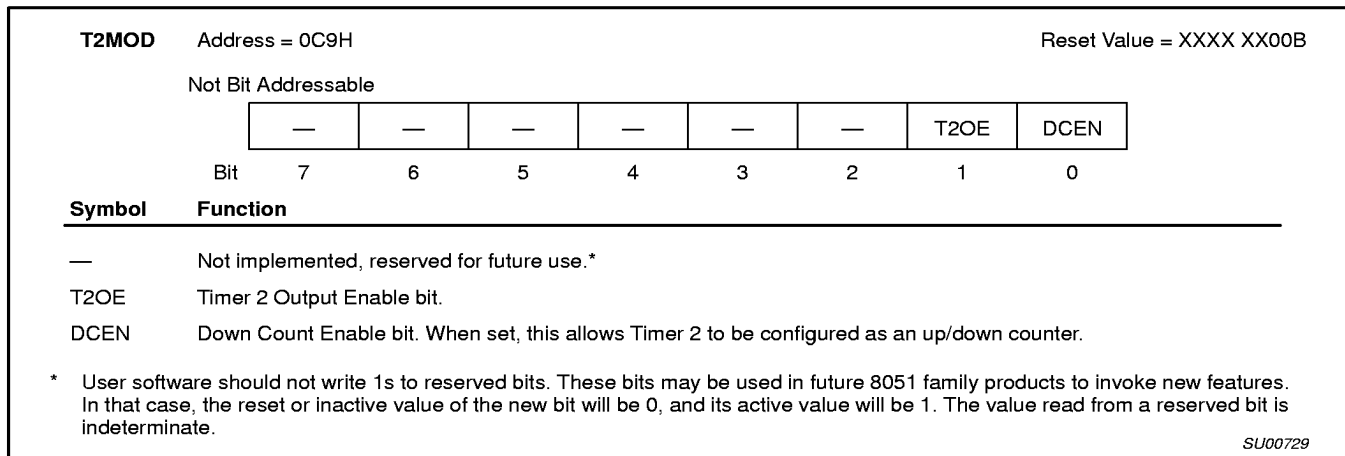


Figure 3. Timer 2 Mode (T2MOD) Control Register

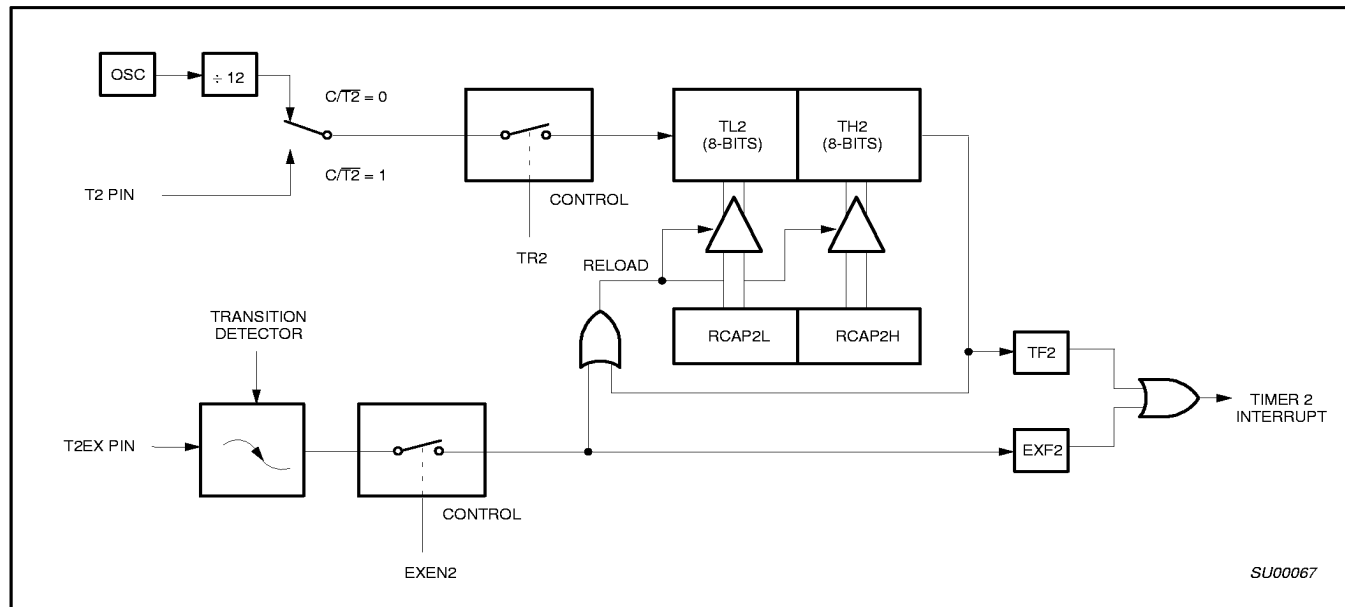


Figure 4. Timer 2 in Auto-Reload Mode (DCEN = 0)

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Baud Rate Generator Mode

Bits TCLK and/or RCLK in T2CON (Table 3) allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer 2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated by Timer 1, the other by Timer 2.

Figure 6 shows the Timer 2 in baud rate generation mode. The baud rate generation mode is like the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In many applications, it is configured for "timer" operation ($C/T2=0$). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., 1/12 the oscillator frequency). As a baud rate generator, it increments every state time (i.e., 1/2 the oscillator frequency). Thus the baud rate formula is as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Oscillator Frequency}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where: (RCAP2H, RCAP2L)= The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode shown in Figure 6, is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time ($\text{osc}/2$) or asynchronously from pin T2;

under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 4 shows commonly used baud rates and how they can be obtained from Timer 2.

Table 4. Timer 2 Generated Commonly Used Baud Rates

Baud Rate	Osc Freq	Timer 2	
		RCAP2H	RCAP2L
375K	12MHz	FF	FF
9.6K	12MHz	FF	D9
2.8K	12MHz	FF	B2
2.4K	12MHz	FF	64
1.2K	12MHz	FE	C8
300	12MHz	FB	1E
110	12MHz	F2	AF
300	6MHz	FD	8F
110	6MHz	F9	57

Summary Of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{\text{OSC}}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where f_{OSC} = Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H, RCAP2L} = 65536 - \frac{f_{\text{OSC}}}{32 \times \text{Baud Rate}}$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. See Table 5 for set-up of Timer 2 as a timer. Also see Table 6 for set-up of Timer 2 as a counter.

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Table 5. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 6. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:

1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

Enhanced UART

The UART operates in all of the usual modes that are described in the first section of *Data Handbook IC20, 80C51-Based 8-Bit Microcontrollers*. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The 8XC51/31 UART also fully supports multiprocessor communication.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 7). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 8.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 9.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the

SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

```
Slave 0    SADDR = 1100 0000
           SADEN = 1111 1101
           Given  = 1100 00X0

Slave 1    SADDR = 1100 0000
           SADEN = 1111 1110
           Given  = 1100 000X
```

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

```
Slave 0    SADDR = 1100 0000
           SADEN = 1111 1001
           Given  = 1100 0XX0

Slave 1    SADDR = 1110 0000
           SADEN = 1111 1010
           Given  = 1110 0X0X

Slave 2    SADDR = 1110 0000
           SADEN = 1111 1100
           Given  = 1110 00XX
```

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0

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and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are leaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

SCON

Address = 98H

Reset Value = 0000 0000B

Bit Addressable

SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
7	6	5	4	3	2	1	0

(SMOD0 = 0/1)*

Symbol	Function																									
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.																									
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)																									
SM1	Serial Port Mode Bit 1																									
	<table> <tr> <th>SM0</th> <th>SM1</th> <th>Mode</th> <th>Description</th> <th>Baud Rate**</th> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>shift register</td> <td>f_{OSC}/12</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>8-bit UART</td> <td>variable</td> </tr> <tr> <td>1</td> <td>0</td> <td>2</td> <td>9-bit UART</td> <td>f_{OSC}/64 or f_{OSC}/32</td> </tr> <tr> <td>1</td> <td>1</td> <td>3</td> <td>9-bit UART</td> <td>variable</td> </tr> </table>	SM0	SM1	Mode	Description	Baud Rate**	0	0	0	shift register	f _{OSC} /12	0	1	1	8-bit UART	variable	1	0	2	9-bit UART	f _{OSC} /64 or f _{OSC} /32	1	1	3	9-bit UART	variable
SM0	SM1	Mode	Description	Baud Rate**																						
0	0	0	shift register	f _{OSC} /12																						
0	1	1	8-bit UART	variable																						
1	0	2	9-bit UART	f _{OSC} /64 or f _{OSC} /32																						
1	1	3	9-bit UART	variable																						
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.																									
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.																									
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.																									
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.																									
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.																									
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.																									

NOTE:

*SMOD0 is located at PCON6.

**f_{OSC} = oscillator frequency

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Figure 7. SCON: Serial Port Control Register

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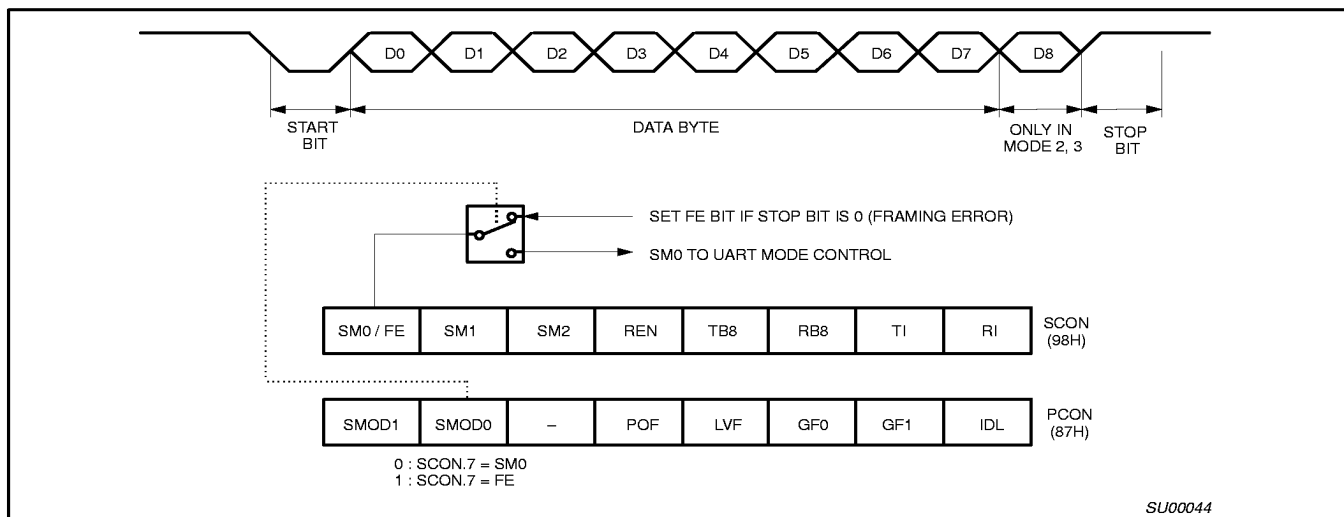


Figure 8. UART Framing Error Detection

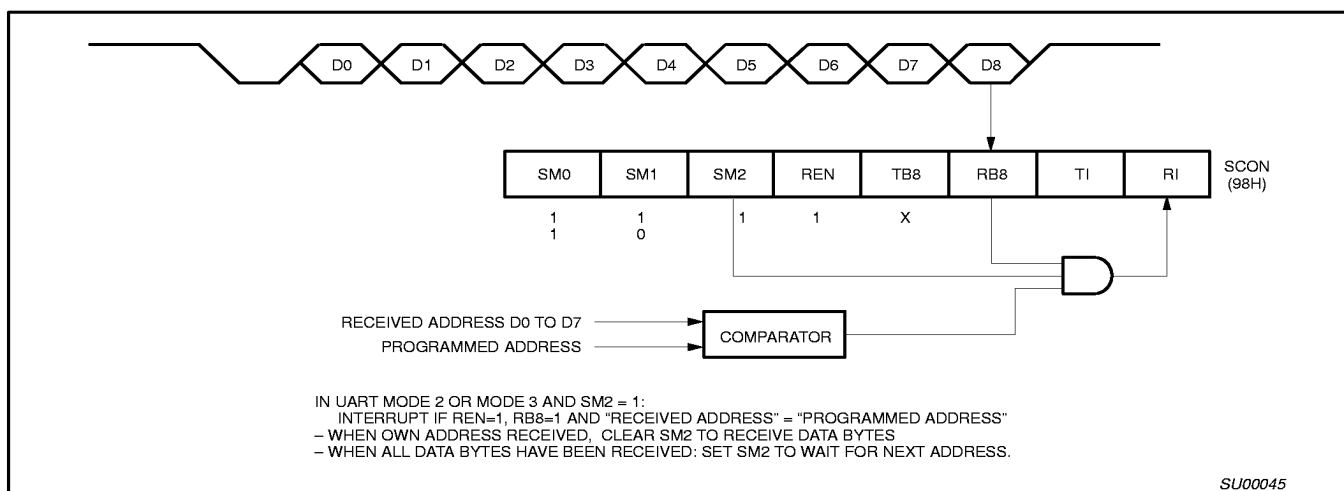


Figure 9. UART Multiprocessor Communication, Automatic Address Recognition

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Interrupt Priority Structure

The 8XC51 and 80C31 only have a 6-source four-level interrupt structure. They are the IE, IP and IPH. (See Figures 10, 11, and 12.) The IPH (Interrupt Priority High) register that makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 12.

The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 7. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L) ¹ Y (T) ²	03H
T0	2	TP0	Y	0BH
X1	3	IE1	N (L) Y (T)	13H
T1	4	TF1	Y	1BH
SP	5	RI, TI	N	23H
T2	6	TF2, EXF2	N	2BH

NOTES:

1. L = Level activated
2. T = Transition activated

		7	6	5	4	3	2	1	0
IE (0A8H)		EA	—	ET2	ES	ET1	EX1	ET0	EX0
		Enable Bit = 1 enables the interrupt. Enable Bit = 0 disables it.							
BIT	SYMBOL	FUNCTION							
IE.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.							
IE.6	—	Not implemented. Reserved for future use.							
IE.5	ET2	Timer 2 interrupt enable bit.							
IE.4	ES	Serial Port interrupt enable bit.							
IE.3	ET1	Timer 1 interrupt enable bit.							
IE.2	EX1	External interrupt 1 enable bit.							
IE.1	ET0	Timer 0 interrupt enable bit.							
IE.0	EX0	External interrupt 0 enable bit.							

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Figure 10. IE Registers

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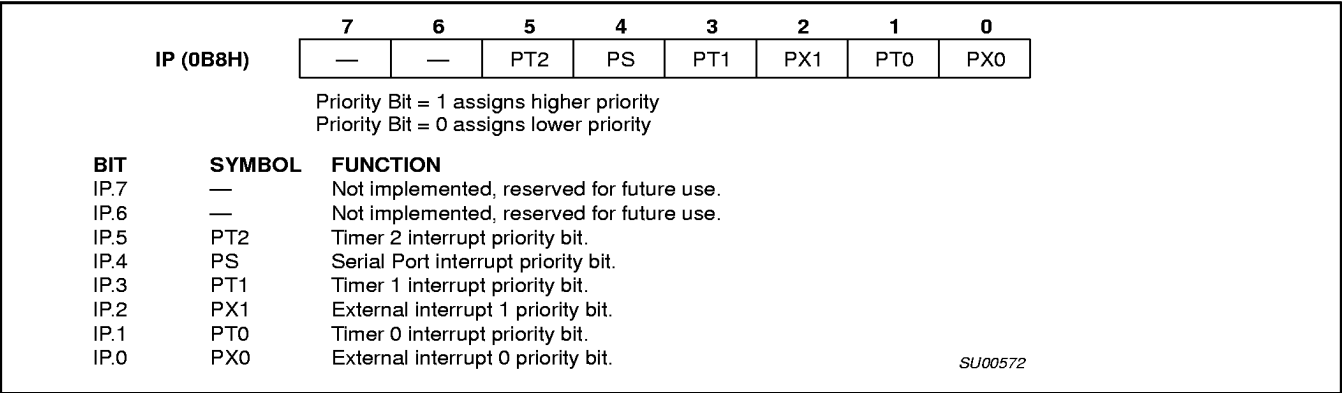


Figure 11. IP Registers

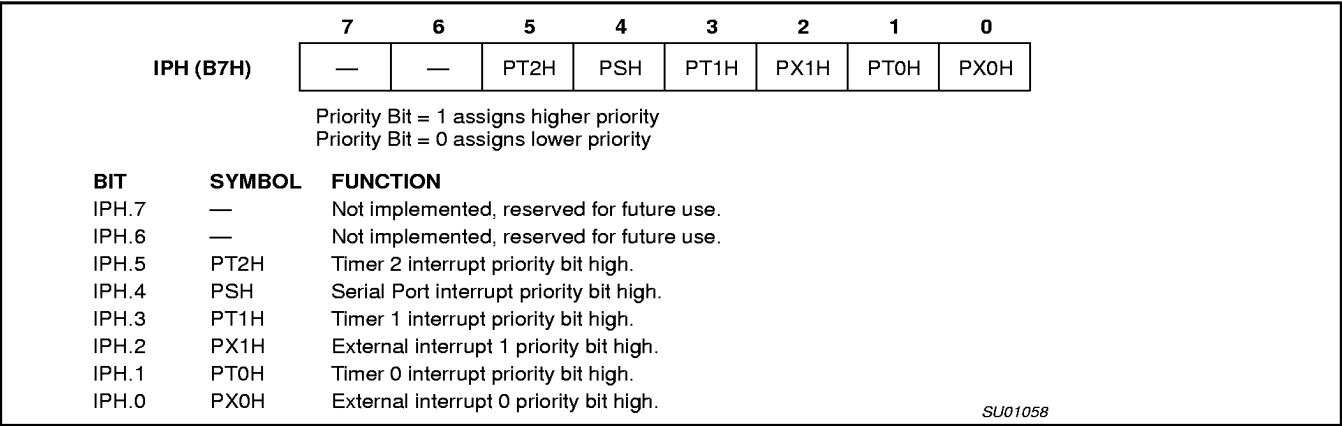


Figure 12. IPH Registers

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Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

Reduced EMI Mode

AUXR (8EH)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	AO

AUXR.0 AO Turns off ALE output.

Dual DPTR

The dual DPTR structure (see Figure 13) enables a way to specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxx000x0B

AUXR1 (A2H)

7	6	5	4	3	2	1	0
–	–	–	LPEP	WUPD	0	–	DPS

Where:

DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC DPTR instruction without affecting the WOPD or LPEP bits.

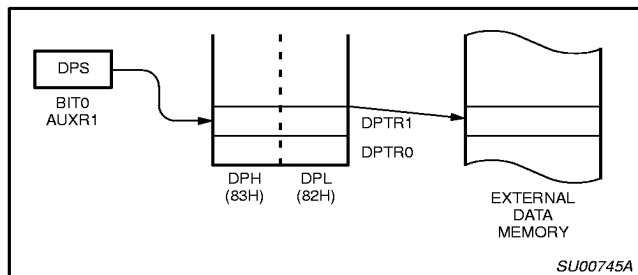


Figure 13.

DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR, A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See application note AN458 for more details.

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ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or –40 to +85	°C
Storage temperature range	–65 to +150	°C
Voltage on EA/V _{PP} pin to V _{SS}	0 to +13.0	V
Voltage on any other pin to V _{SS}	–0.5 to +6.5	V
Maximum I _{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C

SYMBOL	FIGURE	PARAMETER	CLOCK FREQUENCY RANGE –f		UNIT
			MIN	MAX	
1/t _{CLCL}	29	Oscillator frequency Speed versions : S (16MHz) U (33MHz)	0 0	16 33	MHz MHz

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DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 5.5V , $V_{SS} = 0\text{V}$ (16MHz devices)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage	$4.0\text{V} < V_{CC} < 5.5\text{V}$	-0.5		$0.2V_{CC}-0.1$	V
		$2.7\text{V} < V_{CC} < 4.0\text{V}$	-0.5		0.7	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{\text{EA}}$)		$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$		$V_{CC}+0.5$	V
V_{OL}	Output low voltage, ports 1, 2, ⁸	$V_{CC} = 2.7\text{V}$ $I_{OL} = 1.6\text{mA}^2$			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{\text{PSEN}}$ ^{8, 7}	$V_{CC} = 2.7\text{V}$ $I_{OL} = 3.2\text{mA}^2$			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 2.7\text{V}$ $I_{OH} = -20\mu\text{A}$	$V_{CC} - 0.7$			V
		$V_{CC} = 4.5\text{V}$ $I_{OH} = -30\mu\text{A}$	$V_{CC} - 0.7$			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , $\overline{\text{PSEN}}$ ³	$V_{CC} = 2.7\text{V}$ $I_{OH} = -3.2\text{mA}$	$V_{CC} - 0.7$			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{V}$ See note 4			-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$			± 10	μA
I_{CC}	Power supply current (see Figure 21): Active mode @ 16MHz Idle mode @ 16MHz Power-down mode or clock stopped (see Figure 25 for conditions)	See note 5 $T_{amb} = 0^{\circ}\text{C}$ to 70°C $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		3		μA
						μA
					50 75	μA μA
R_{RST}	Internal reset pull-down resistor		40		225	$\text{k}\Omega$
C_{IO}	Pin capacitance ¹⁰ (except $\overline{\text{EA}}$)				15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100\text{pF}$), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{\text{PSEN}}$ to momentarily fall below the $V_{CC}-0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- See Figures 22 through 25 for I_{CC} test conditions.
 Active mode: $I_{CC} = 0.9 \times \text{FREQ.} + 1.1\text{mA}$
 Idle mode: $I_{CC} = 0.18 \times \text{FREQ.} + 1.01\text{mA}$; See Figure 21.
- This value applies to $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$. For $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $I_{TL} = -750\mu\text{A}$.
- Load capacitance for port 0, ALE, and $\overline{\text{PSEN}} = 100\text{pF}$, load capacitance for all other outputs = 80pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
 Maximum I_{OL} per port pin: 15mA (*NOTE: This is 85°C specification.)
 Maximum I_{OL} per 8-bit port: 26mA
 Maximum total I_{OL} for all outputs: 71mA
 If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except $\overline{\text{EA}}$ is 25pF).

80C51 8-bit microcontroller family
 4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
 low power, high speed (33 MHz)

80C51/87C51/80C31

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$, 33MHz devices; 5V $\pm 10\%$; $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage	$4.5\text{V} < V_{CC} < 5.5\text{V}$	-0.5		$0.2V_{CC} - 0.1$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{\text{EA}}$)		$0.2V_{CC} + 0.9$		$V_{CC} + 0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$		$V_{CC} + 0.5$	V
V_{OL}	Output low voltage, ports 1, 2, 3 ⁸	$V_{CC} = 4.5\text{V}$ $I_{OL} = 1.6\text{mA}^2$			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{\text{PSEN}}$ ^{7, 8}	$V_{CC} = 4.5\text{V}$ $I_{OL} = 3.2\text{mA}^2$			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 4.5\text{V}$ $I_{OH} = -30\mu\text{A}$	$V_{CC} - 0.7$			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , $\overline{\text{PSEN}}$ ³	$V_{CC} = 4.5\text{V}$ $I_{OH} = -3.2\text{mA}$	$V_{CC} - 0.7$			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{V}$ See note 4			-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$			± 10	μA
I_{CC}	Power supply current (see Figure 21): Active mode (see Note 5) Idle mode (see Note 5) Power-down mode or clock stopped (see Figure 25 for conditions)	See note 5 $T_{amb} = 0^{\circ}\text{C}$ to 70°C $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		3	50 75	μA μA
R_{RST}	Internal reset pull-down resistor		40		225	k Ω
C_{IO}	Pin capacitance ¹⁰ (except $\overline{\text{EA}}$)				15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100\text{pF}$), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{\text{PSEN}}$ to momentarily fall below the $V_{CC} - 0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- See Figures 22 through 25 for I_{CC} test conditions.
 Active mode: $I_{CC}(\text{MAX}) = 0.9 \times \text{FREQ.} + 1.1\text{mA}$
 Idle mode: $I_{CC}(\text{MAX}) = 0.18 \times \text{FREQ.} + 1.0\text{mA}$; See Figure 21.
- This value applies to $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$. For $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $I_{TL} = -750\mu\text{A}$.
- Load capacitance for port 0, ALE, and $\overline{\text{PSEN}} = 100\text{pF}$, load capacitance for all other outputs = 80pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
 Maximum I_{OL} per port pin: 15mA (*NOTE: This is 85°C specification.)
 Maximum I_{OL} per 8-bit port: 26mA
 Maximum total I_{OL} for all outputs: 71mA
 If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except $\overline{\text{EA}}$ is 25pF).

80C51 8-bit microcontroller family
 4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
 low power, high speed (33 MHz)

80C51/87C51/80C31

AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C or } -40^{\circ}\text{C to } +85^{\circ}\text{C}$, $V_{CC} = +2.7\text{V to } +5.5\text{V}$, $V_{SS} = 0\text{V}^{1, 2, 3}$

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	14	Oscillator frequency ⁵ Speed versions :S			3.5	16	MHz
t_{LHLL}	14	ALE pulse width	85		$2t_{CLCL}-40$		ns
t_{AVLL}	14	Address valid to ALE low	22		$t_{CLCL}-40$		ns
t_{LLAX}	14	Address hold after ALE low	32		$t_{CLCL}-30$		ns
t_{LLIV}	14	ALE low to valid instruction in		150		$4t_{CLCL}-100$	ns
t_{LLPL}	14	ALE low to PSEN low	32		$t_{CLCL}-30$		ns
t_{PLPH}	14	PSEN pulse width	142		$3t_{CLCL}-45$		ns
t_{PLIV}	14	PSEN low to valid instruction in		82		$3t_{CLCL}-105$	ns
t_{PXIX}	14	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	14	Input instruction float after PSEN		37		$t_{CLCL}-25$	ns
t_{AVIV}^{4}	14	Address to valid instruction in		207		$5t_{CLCL}-105$	ns
t_{PLAZ}	14	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	15, 16	RD pulse width	275		$6t_{CLCL}-100$		ns
t_{WLWH}	15, 16	WR pulse width	275		$6t_{CLCL}-100$		ns
t_{RLDV}	15, 16	RD low to valid data in		147		$5t_{CLCL}-165$	ns
t_{RHDX}	15, 16	Data hold after RD	0		0		ns
t_{RHDZ}	15, 16	Data float after RD		65		$2t_{CLCL}-60$	ns
t_{LLDV}	15, 16	ALE low to valid data in		350		$8t_{CLCL}-150$	ns
t_{AVDV}	15, 16	Address to valid data in		397		$9t_{CLCL}-165$	ns
t_{LLWL}	15, 16	ALE low to RD or WR low	137	239	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	15, 16	Address valid to WR low or RD low	122		$4t_{CLCL}-130$		ns
t_{QVWX}	15, 16	Data valid to WR transition	13		$t_{CLCL}-50$		ns
t_{WHQX}	15, 16	Data hold after WR	13		$t_{CLCL}-50$		ns
t_{QVWH}	16	Data valid to WR high	287		$7t_{CLCL}-150$		ns
t_{RLAZ}	15, 16	RD low to address float		0		0	ns
t_{WHLH}	15, 16	RD or WR high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
External Clock							
t_{CHCX}	18	High time	20		20	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	18	Low time	20		20	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	18	Rise time		20		20	ns
t_{CHCL}	18	Fall time		20		20	ns
Shift Register							
t_{XLXL}	17	Serial port clock cycle time	750		$12t_{CLCL}$		ns
t_{QVXH}	17	Output data setup to clock rising edge	492		$10t_{CLCL}-133$		ns
t_{XHQX}	17	Output data hold after clock rising edge	8		$2t_{CLCL}-117$		ns
t_{XHDX}	17	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	17	Clock rising edge to input data valid		492		$10t_{CLCL}-133$	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Interfacing the 8XC51 and 80C31 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
- See application note AN457 for external memory interface.
- Parts are guaranteed to operate down to 0Hz.

80C51 8-bit microcontroller family
 4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
 low power, high speed (33 MHz)

80C51/87C51/80C31

AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C or } -40^{\circ}\text{C to } +85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}^{1, 2, 3}$

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK ⁴ 16MHz to f_{max}		33MHz CLOCK		UNIT
			MIN	MAX	MIN	MAX	
t_{LHLL}	14	ALE pulse width	$2t_{CLCL}-40$		21		ns
t_{AVLL}	14	Address valid to ALE low	$t_{CLCL}-25$		5		ns
t_{LLAX}	14	Address hold after ALE low	$t_{CLCL}-25$				ns
t_{LLIV}	14	ALE low to valid instruction in		$4t_{CLCL}-65$		55	ns
t_{LLPL}	14	ALE low to PSEN low	$t_{CLCL}-25$		5		ns
t_{PLPH}	14	PSEN pulse width	$3t_{CLCL}-45$		45		ns
t_{PLIV}	14	PSEN low to valid instruction in		$3t_{CLCL}-60$		30	ns
t_{PXIX}	14	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	14	Input instruction float after PSEN		$t_{CLCL}-25$		5	ns
t_{AVIV}	14	Address to valid instruction in		$5t_{CLCL}-80$		70	ns
t_{PLAZ}	14	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	15, 16	RD pulse width	$6t_{CLCL}-100$		82		ns
t_{WLWH}	15, 16	WR pulse width	$6t_{CLCL}-100$		82		ns
t_{RLDV}	15, 16	RD low to valid data in		$5t_{CLCL}-90$		60	ns
t_{RHDX}	15, 16	Data hold after RD	0		0		ns
t_{RHDZ}	15, 16	Data float after RD		$2t_{CLCL}-28$		32	ns
t_{LLDV}	15, 16	ALE low to valid data in		$8t_{CLCL}-150$		90	ns
t_{AVDV}	15, 16	Address to valid data in		$9t_{CLCL}-165$		105	ns
t_{LLWL}	15, 16	ALE low to RD or WR low	$3t_{CLCL}-50$	$3t_{CLCL}+50$	40	140	ns
t_{AVWL}	15, 16	Address valid to WR low or RD low	$4t_{CLCL}-75$		45		ns
t_{QVWX}	15, 16	Data valid to WR transition	$t_{CLCL}-30$		0		ns
t_{WHQX}	15, 16	Data hold after WR	$t_{CLCL}-25$		5		ns
t_{QVWH}	16	Data valid to WR high	$7t_{CLCL}-130$		80		ns
t_{RLAZ}	15, 16	RD low to address float		0		0	ns
t_{WHLH}	15, 16	RD or WR high to ALE high	$t_{CLCL}-25$	$t_{CLCL}+25$	5	55	ns
External Clock							
t_{CHCX}	18	High time	$0.38t_{CLCL}$	$t_{CLCL}-t_{CLCX}$			ns
t_{CLCX}	18	Low time	$0.38t_{CLCL}$	$t_{CLCL}-t_{CHCX}$			ns
t_{CLCH}	18	Rise time		5			ns
t_{CHCL}	18	Fall time		5			ns
Shift Register							
t_{XLXL}	17	Serial port clock cycle time	$12t_{CLCL}$		360		ns
t_{QVXH}	17	Output data setup to clock rising edge	$10t_{CLCL}-133$		167		ns
t_{XHGX}	17	Output data hold after clock rising edge	$2t_{CLCL}-80$				ns
t_{XHDX}	17	Input data hold after clock rising edge	0		0		ns
t_{XHDX}	17	Clock rising edge to input data valid		$10t_{CLCL}-133$		167	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Interfacing the 8XC51 and 80C31 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
- Variable clock is specified for oscillator frequencies greater than 16MHz to 33MHz. For frequencies equal or less than 16MHz, see 16MHz "AC Electrical Characteristics", page 23.
- Parts are guaranteed to operate down to 0Hz.

80C51 8-bit microcontroller family

4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address

C – Clock

D – Input data

H – Logic level high

1 – Instruction (program memory contents)

L – Logic level low, or ALE

$$P - \overline{PSEN}$$

Q – Output data

R – $\overline{RD}$ signal

t – Time

V – Valid

W- $\overline{WR}$ signal

X – No longer a valid logic level

Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.

t_{LLPL} = Time for ALE low to $\overline{PSEN}$ low.

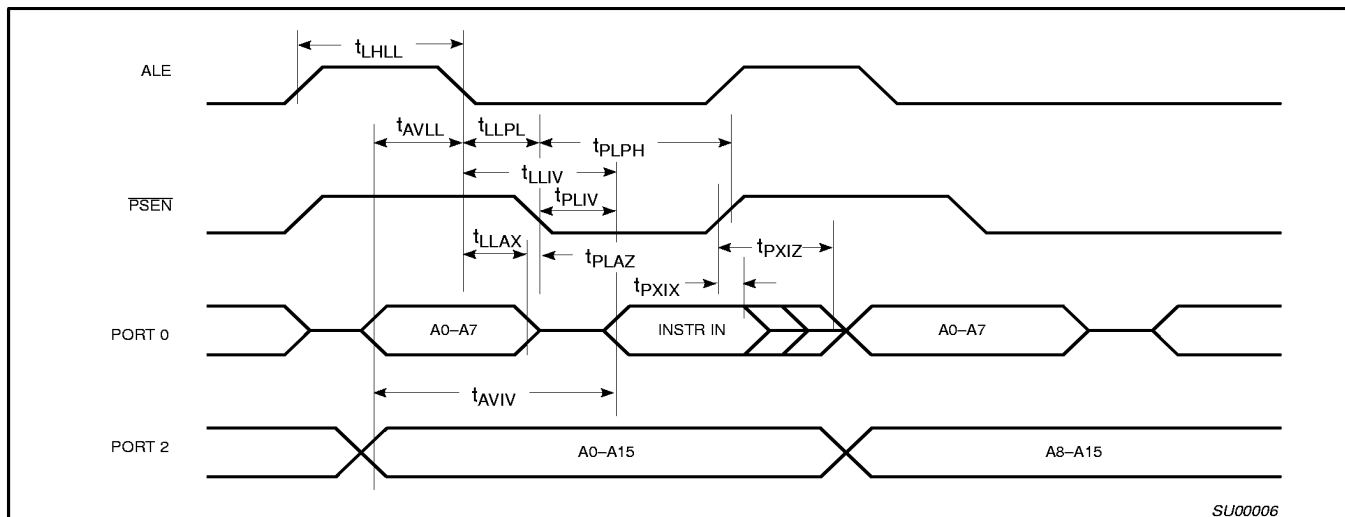


Figure 14. External Program Memory Read Cycle

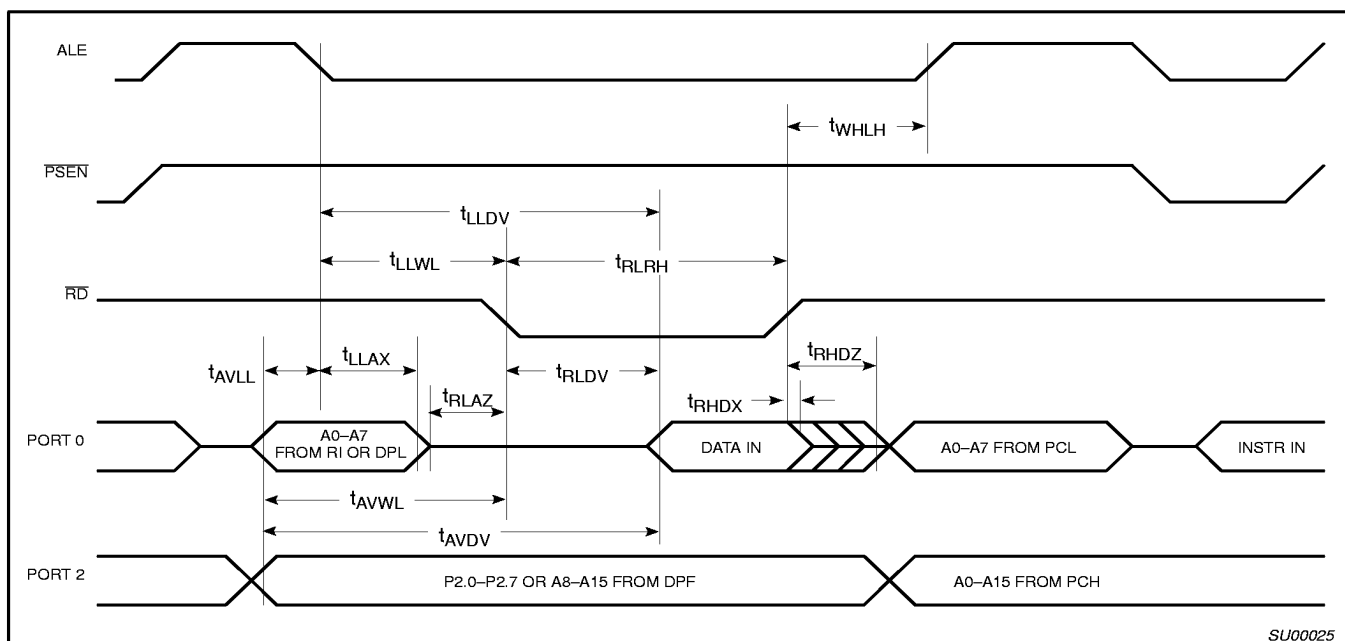


Figure 15. External Data Memory Read Cycle

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4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
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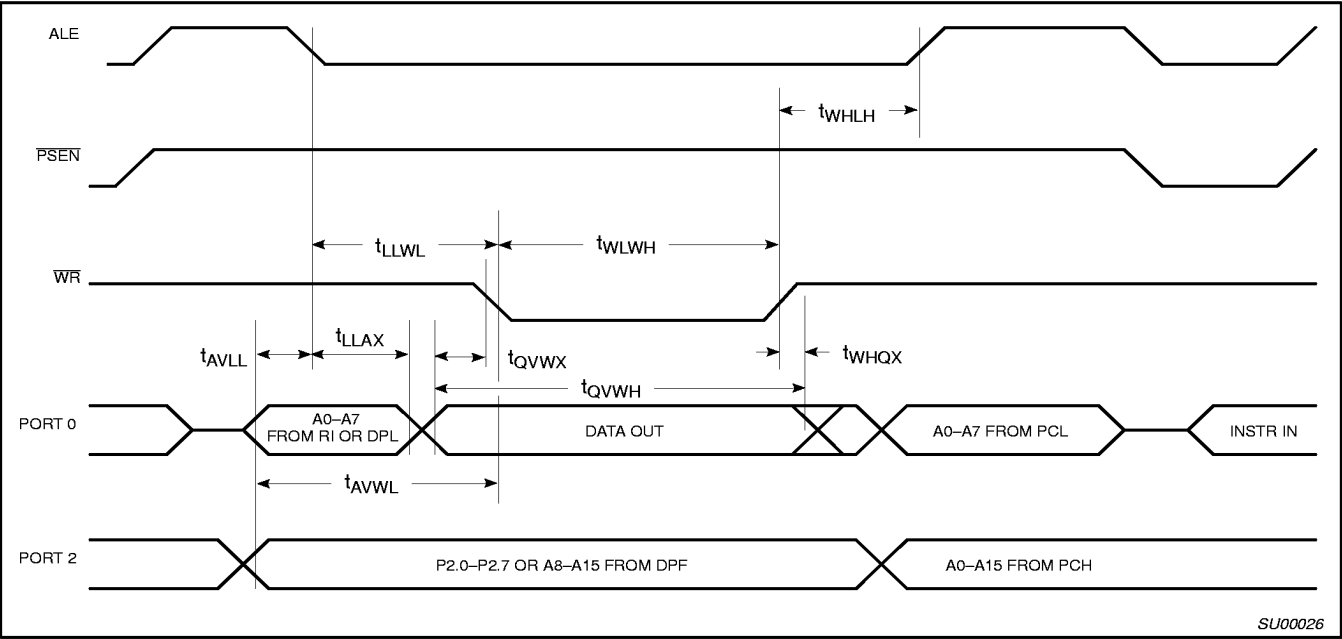


Figure 16. External Data Memory Write Cycle

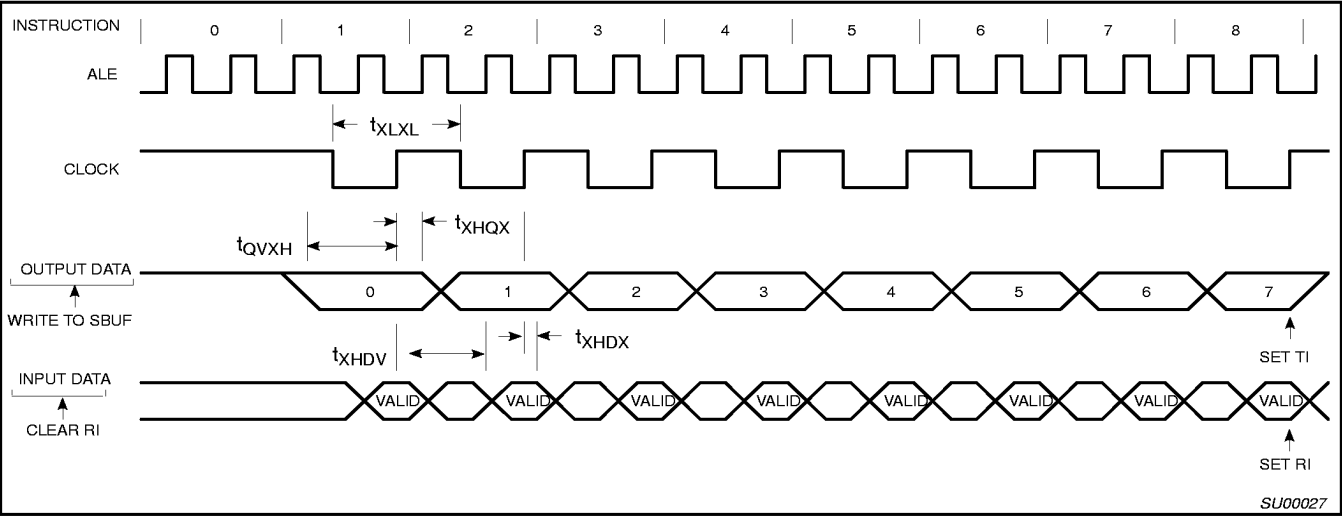


Figure 17. Shift Register Mode Timing

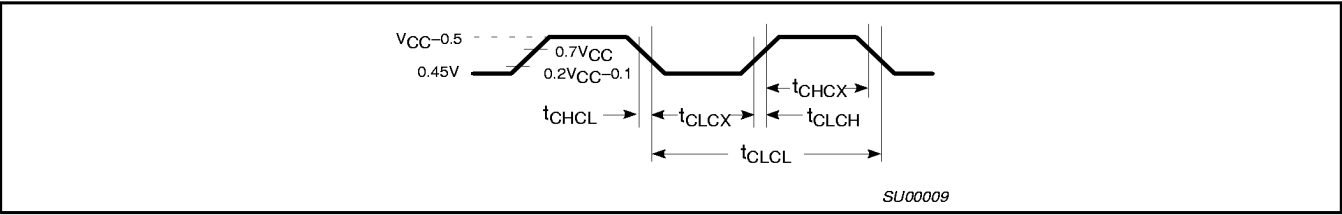


Figure 18. External Clock Drive

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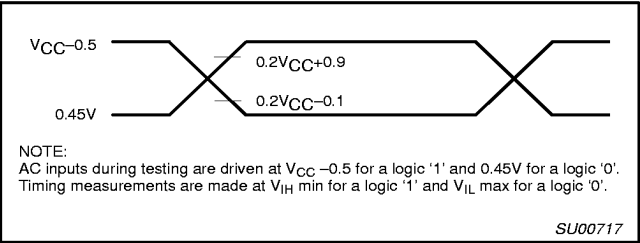


Figure 19. AC Testing Input/Output

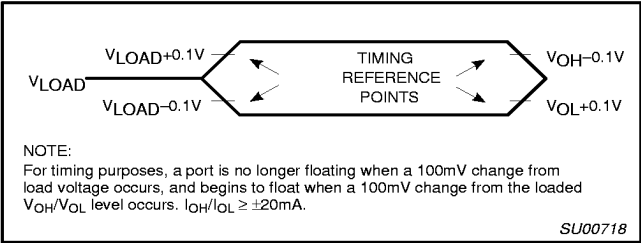


Figure 20. Float Waveform

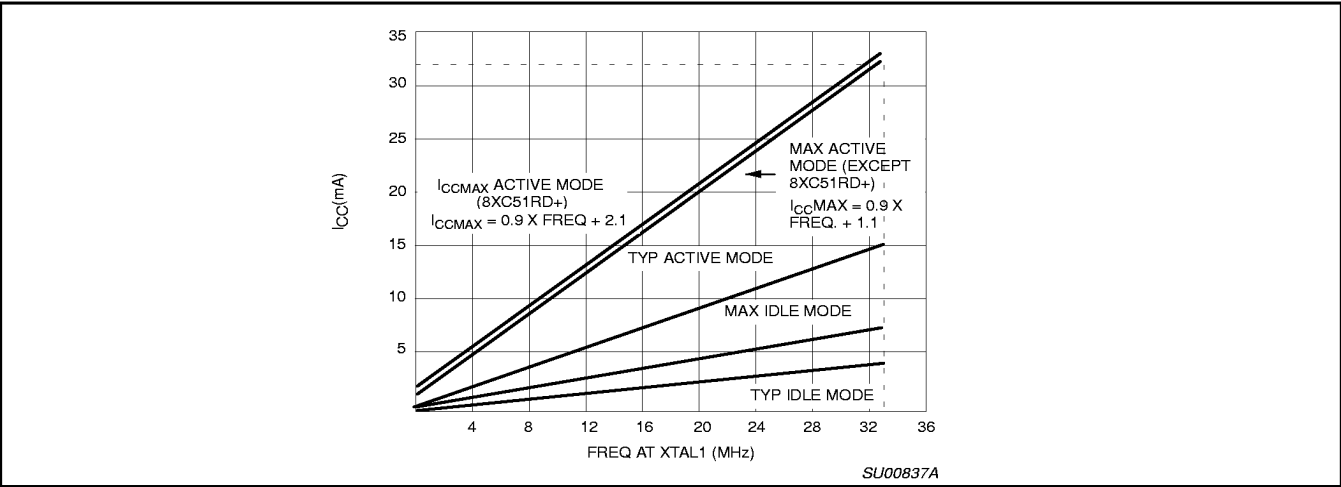


Figure 21. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test

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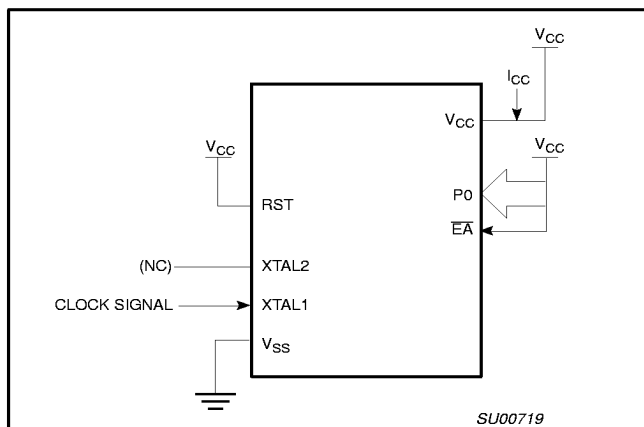


Figure 22. I_{CC} Test Condition, Active Mode
 All other pins are disconnected

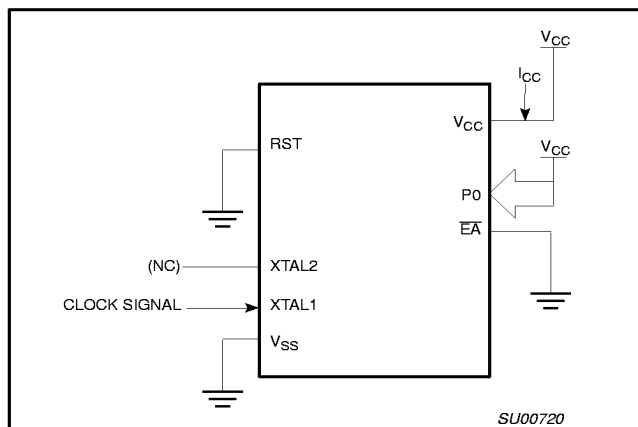


Figure 23. I_{CC} Test Condition, Idle Mode
 All other pins are disconnected

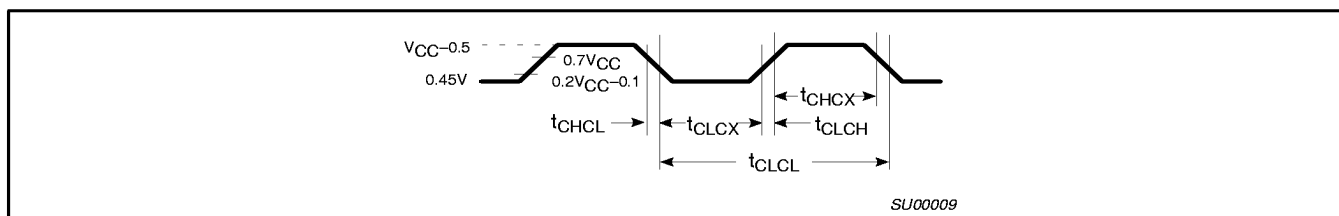


Figure 24. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
 $t_{CLCH} = t_{CHCL} = 5\text{ns}$

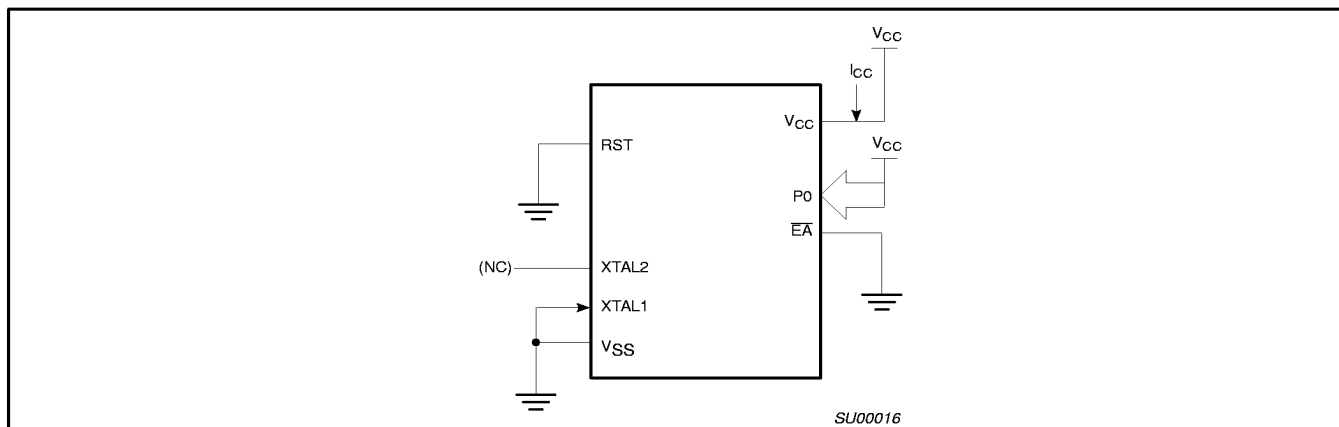


Figure 25. I_{CC} Test Condition, Power Down Mode
 All other pins are disconnected. $V_{CC} = 2\text{V to } 5.5\text{V}$

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EPROM CHARACTERISTICS

All these devices can be programmed by using a modified Improved Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The family contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as being manufactured by Philips.

Table 8 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 26 and 27. Figure 28 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 26. Note that the device is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 26. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 8 are held at the 'Program Code Data' levels indicated in Table 8. The ALE/PROG is pulsed low 5 times as shown in Figure 27.

To program the encryption table, repeat the 5 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 5 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bits can still be programmed.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bits 2 and 3 have not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 28. The other pins are held at the 'Verify Code Data' levels indicated in Table 8. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the 64 byte encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:
 (030H) = 15H indicates manufactured by Philips
 (031H) = 92H indicates 87C51

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 8, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345–5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm². Exposing the EPROM to an ultraviolet lamp of 12,000μW/cm² rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Security Bits

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 (see Table 9) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory, EA is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

Encryption Array

64 bytes of encryption array are initially unprogrammed (all 1s).

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80C51 8-bit microcontroller family
 4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
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Table 8. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	EA/V _{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V _{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V _{PP}	1	0	1	0
Pgm security bit 1	1	0	0*	V _{PP}	1	1	1	1
Pgm security bit 2	1	0	0*	V _{PP}	1	1	0	0
Pgm security bit 3	1	0	0*	V _{PP}	0	1	0	1

NOTES:

1. '0' = Valid low for that pin, '1' = valid high for that pin.

2. V_{PP} = 12.75V ±0.25V.

3. V_{CC} = 5V±10% during programming and verification.

* ALE/PROG receives 5 programming pulses for code data (also for user array; 5 pulses for encryption or security bits) while V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

Table 9. Program Security Bits for EPROM Devices

PROGRAM LOCK BITS ^{1, 2}				PROTECTION DESCRIPTION
	SB1	SB2	SB3	
1	U	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, external execution is disabled. Internal data RAM is not accessible.

NOTES:

1. P – programmed. U – unprogrammed.

2. Any other combination of the security bits is not defined.

80C51 8-bit microcontroller family
 4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
 low power, high speed (33 MHz)

80C51/87C51/80C31

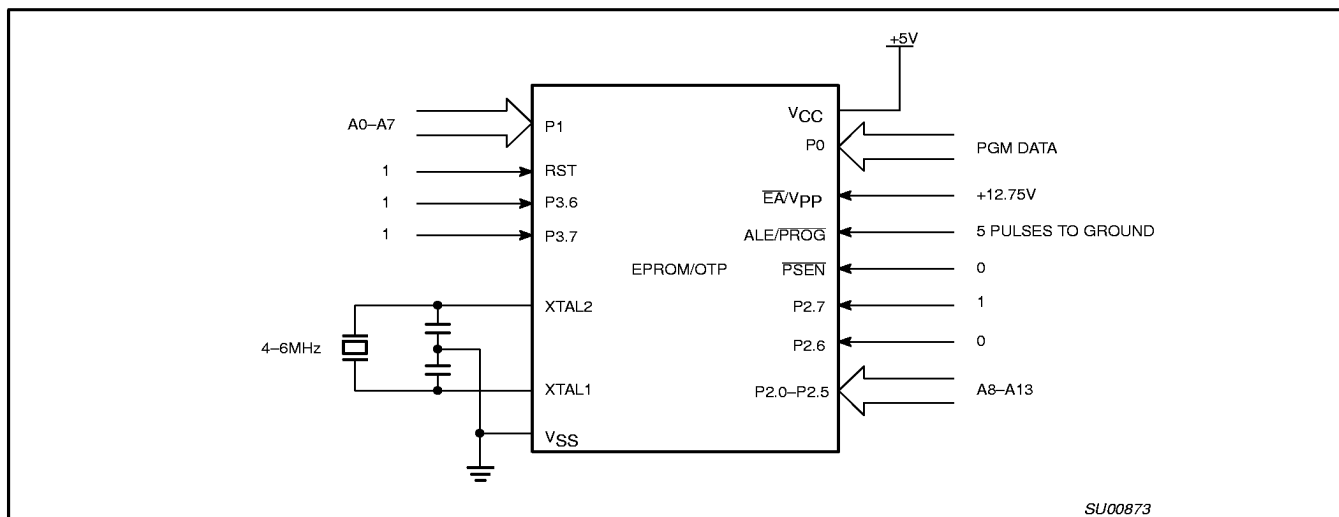


Figure 26. Programming Configuration

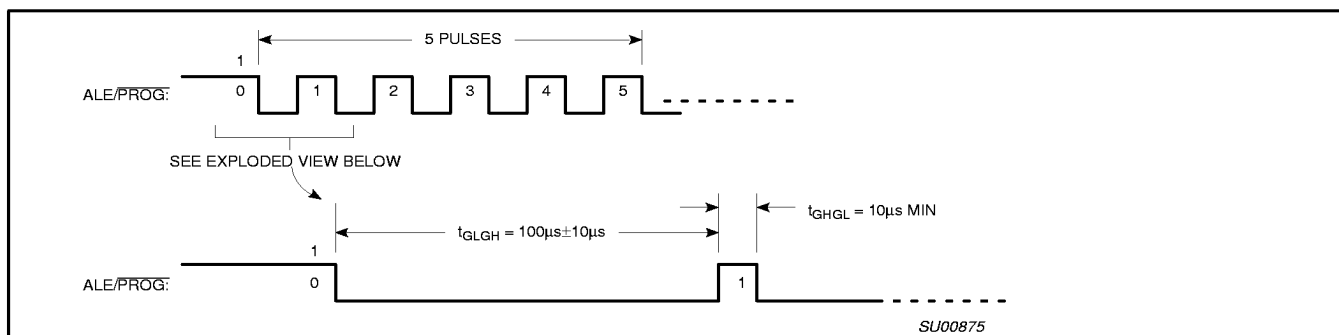


Figure 27. PROG Waveform

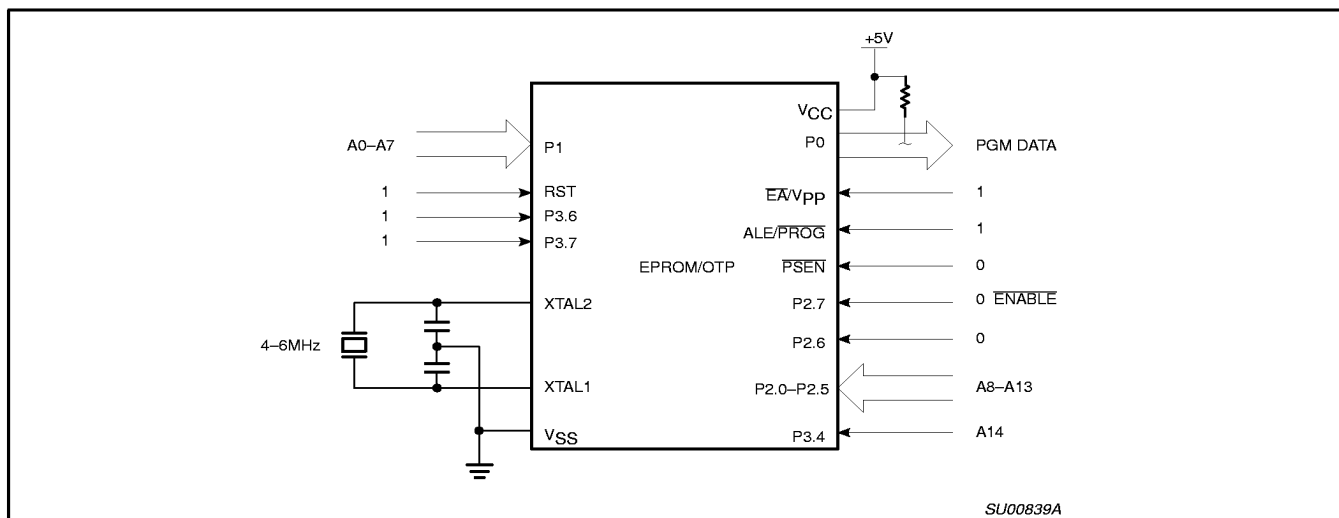


Figure 28. Program Verification

80C51 8-bit microcontroller family
 4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
 low power, high speed (33 MHz)

80C51/87C51/80C31

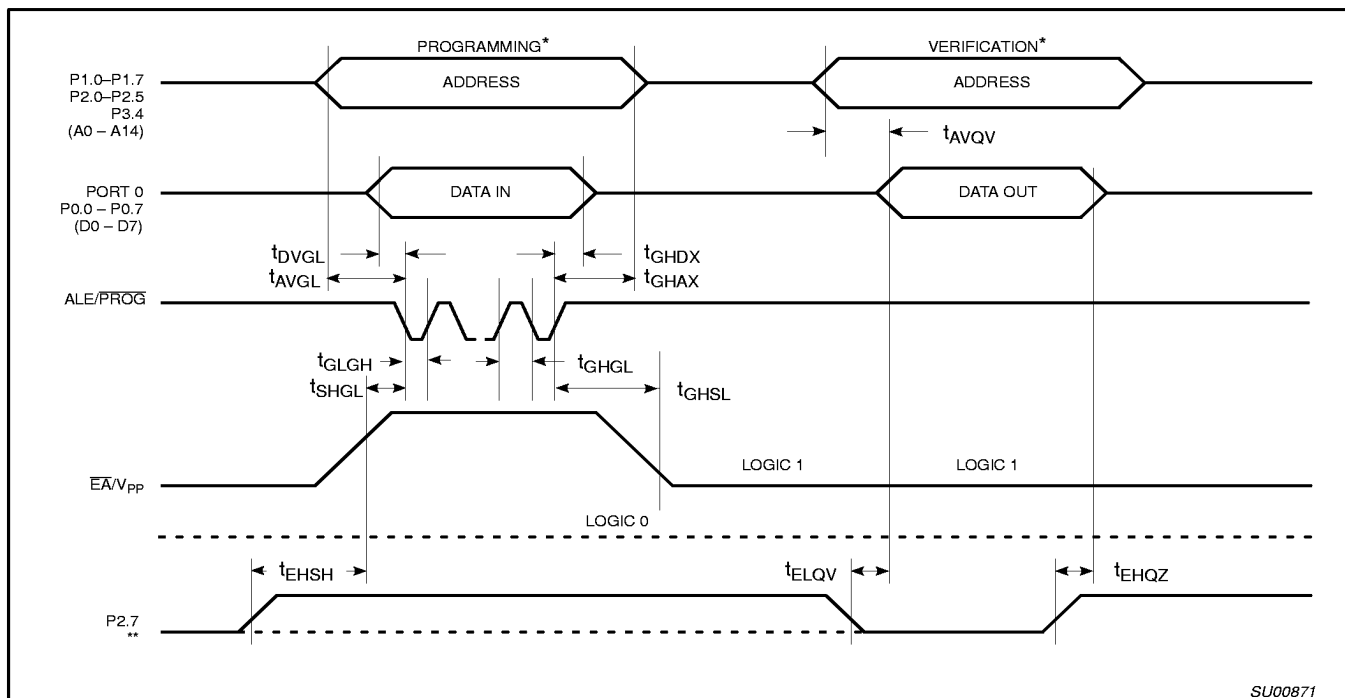
EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_{amb} = 21^{\circ}\text{C}$ to $+27^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$ (See Figure 29)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50 ¹	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{\text{PROG}}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{\text{PROG}}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{EHS}	P2.7 (ENABLE) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{\text{PROG}}$ low	10		μs
t_{GHSL}	V_{PP} hold after $\overline{\text{PROG}}$	10		μs
t_{GLGH}	$\overline{\text{PROG}}$ width	90	110	μs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	ENABLE low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after ENABLE	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{\text{PROG}}$ high to $\overline{\text{PROG}}$ low	10		μs

NOTE:

1. Not tested.



SU00871

NOTES:

* FOR PROGRAMMING CONFIGURATION SEE FIGURE 26.

FOR VERIFICATION CONDITIONS SEE FIGURE 28.

** SEE TABLE 8.

Figure 29. EPROM Programming and Verification

80C51 8-bit microcontroller family
 4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
 low power, high speed (33 MHz)

80C51/87C51/80C31

MASK ROM DEVICES

Security Bits

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 (see Table 10) is programmed, MOV C instructions executed from external program memory are disabled from fetching code bytes

from the internal memory, $\overline{EA}$ is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled.

Encryption Array

64 bytes of encryption array are initially unprogrammed (all 1s).

Table 10. Program Security Bits

PROGRAM LOCK BITS ^{1, 2}			PROTECTION DESCRIPTION
	SB1	SB2	
1	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	MOV C instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on Reset, and further programming of the EPROM is disabled.

NOTES:

1. P – programmed. U – unprogrammed.
2. Any other combination of the security bits is not defined.

ROM CODE SUBMISSION

When submitting ROM code for the 80C51, the following must be specified:

1. 4k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 0FFFFH	DATA	7:0	User ROM Data
1000H to 103FH	KEY	7:0	ROM Encryption Key
1040H	SEC	0	ROM Security Bit 1
1040H	SEC	1	ROM Security Bit 2

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOV C is disabled, and
2. $\overline{EA}$ is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

NOTE: Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

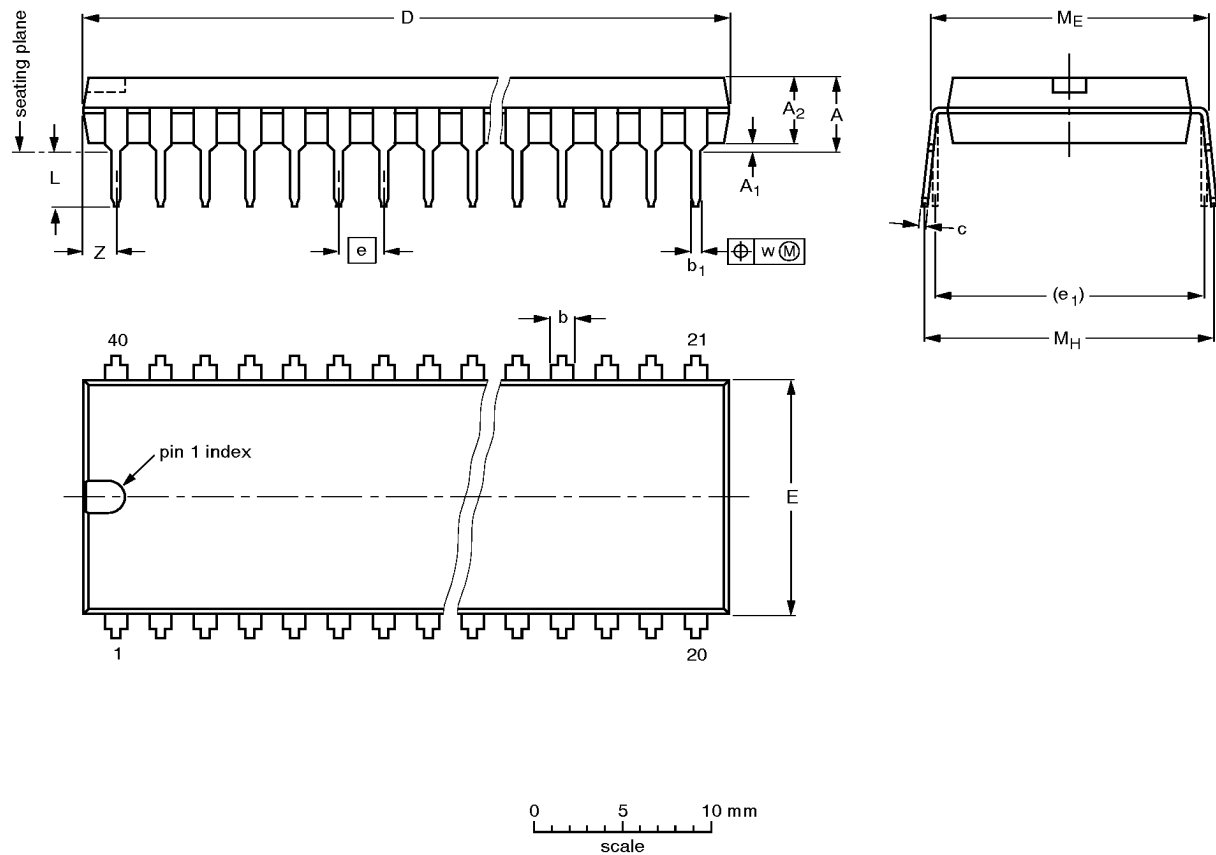
- Security Bit #1: ☐ Enabled ☐ Disabled
- Security Bit #2: ☐ Enabled ☐ Disabled
- Encryption: ☐ No ☐ Yes If Yes, must send key file.

80C51 8-bit microcontroller family
4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
low power, high speed (33 MHz)

80C51/87C51/80C31

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

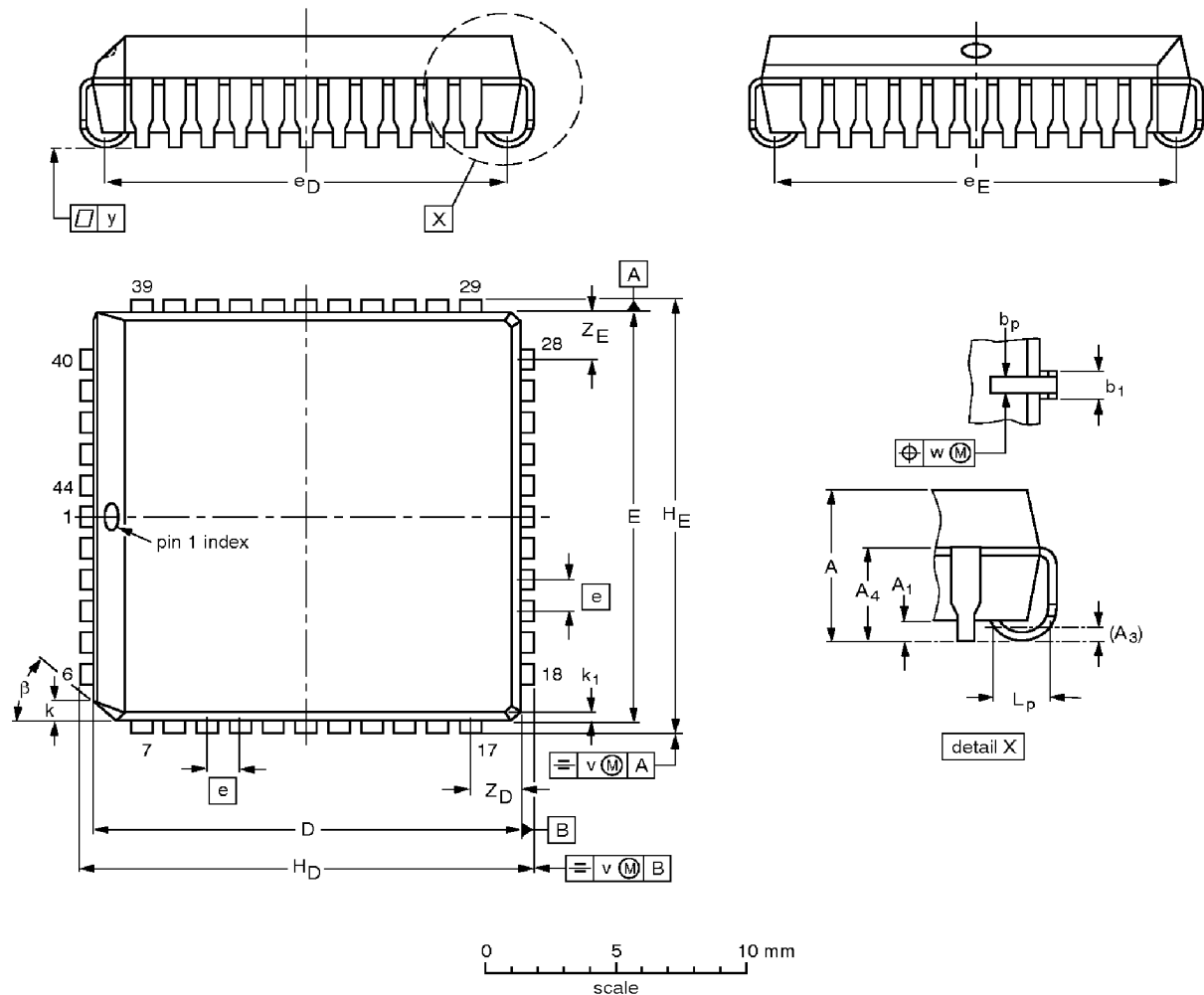
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				92-11-17 95-01-14

80C51 8-bit microcontroller family
4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
low power, high speed (33 MHz)

80C51/87C51/80C31

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	k ₁ max.	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				95-02-25 97-12-16

80C51 8-bit microcontroller family
4K/128 OTP/ROM/ROMless, low voltage (2.7V–5.5V),
low power, high speed (33 MHz)

80C51/87C51/80C31

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2

