

**DAC7800**  
**DAC7801**  
**DAC7802**

## Dual Monolithic CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTERS

### FEATURES

- TWO D/As IN A 0.3" WIDE PACKAGE
- SINGLE +5V SUPPLY
- HIGH SPEED DIGITAL INTERFACE:  
Serial—DAC7800  
8 + 4-Bit Parallel—DAC7801  
12-Bit Parallel—DAC7802
- MONOTONIC OVER TEMPERATURE
- LOW CROSSTALK: -94dB min
- FULLY SPECIFIED OVER -40°C TO +85°C

### APPLICATIONS

- PROCESS CONTROL OUTPUTS
- ATE PIN ELECTRONICS LEVEL SETTING
- PROGRAMMABLE FILTERS
- PROGRAMMABLE GAIN CIRCUITS
- AUTO-CALIBRATION CIRCUITS

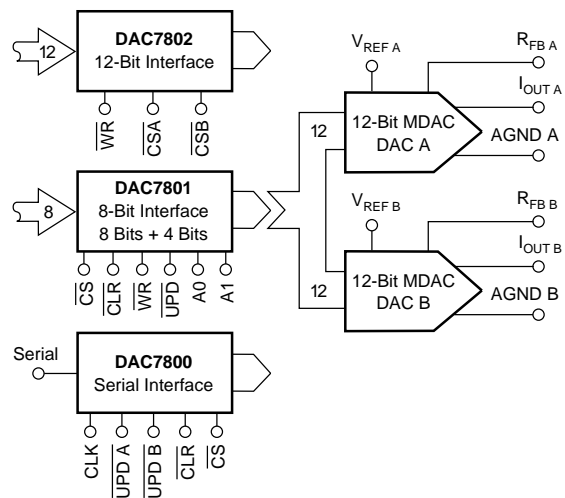
### DESCRIPTION

The DAC7800, DAC7801 and DAC7802 are members of a new family of monolithic dual 12-bit CMOS multiplying digital-to-analog converters. The digital interface speed and the AC multiplying performance are achieved by using an advanced CMOS process optimized for data conversion circuits. High stability on-chip resistors provide true 12-bit integral and differential linearity over the wide industrial temperature range of -40°C to +85°C.

DAC7800 features a serial interface capable of clocking-in data at a rate of at least 10MHz. Serial data is clocked (edge triggered) MSB first into a 24-bit shift register and then latched into each D/A separately or simultaneously as required by the application. An asynchronous CLEAR control is provided for power-on reset or system calibration functions. It is packaged in a 16-pin 0.3" wide plastic DIP.

DAC7801 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each D/A. Then both D/As are updated simultaneously. DAC7801 features an asynchronous CLEAR control. DAC7801 is packaged in a 24-pin 0.3" wide plastic DIP.

DAC7802 has a single-buffered 12-bit data word interface. Parallel data is loaded (edge triggered) into the single D/A register for each D/A. DAC7802 is packaged in a 24-pin 0.3" wide plastic DIP.



# SPECIFICATIONS

## ELECTRICAL

At  $V_{DD} = +5VDC$ ,  $V_{REF A} = V_{REF B} = +10V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.

PARAMETER	CONDITIONS	DAC7800, 7801, 7802K			DAC7800, 7801, 7802L			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>ACCURACY</b> Resolution Relative Accuracy Differential Nonlinearity Gain Error  Gain Temperature Coefficient <sup>(1)</sup> Output Leakage Current	Measured Using $R_{FB A}$ and $R_{FB B}$ All Registers Loaded with All 1s.  $T_A = +25^{\circ}C$ $T_A = -40^{\circ}C$ to $+85^{\circ}C$	12		$\pm 1$ $\pm 1$ $\pm 3$	*		$\pm 1/2$ * $\pm 1$	Bits LSB LSB LSB  ppm/ $^{\circ}C$ nA nA
<b>REFERENCE INPUT</b> Input Resistance Input Resistance Match		6	10 0.5	14 3	*	* *	* 2	k $\Omega$ %
<b>DIGITAL INPUTS</b> $V_{IH}$ (Input High Voltage) $V_{IL}$ (Input Low Voltage) $I_{IN}$ (Input Current)  $C_{IN}$ (Input Capacitance)	$T_A = +25^{\circ}C$ $T_A = -40^{\circ}C$ to $+85^{\circ}C$	2		0.8 $\pm 1$ $\pm 10$ 10	*		* * * *	V V $\mu A$ $\mu A$ pF
<b>POWER SUPPLY</b> $V_{DD}$ $I_{DD}$ Power Supply Rejection	$V_{DD}$ from 4.5V to 5.5V	4.5	0.2	5.5 2 0.002	*	* *	* * *	V mA %/%

\* Same specification as for DAC7800, 7801, 7802K.

## AC PERFORMANCE

### OUTPUT OP AMP IS OPA602.

At  $V_{DD} = +5VDC$ ,  $V_{REF A} = V_{REF B} = +10V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. These specifications are fully characterized but not subject to test.

PARAMETER	CONDITIONS	DAC7800, 7801, 7802K			DAC7800, 7801, 7802L			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OUTPUT CURRENT SETTLING TIME</b>	To 0.01% of Full Scale $R_L = 100\Omega$ , $C_L = 13pF$		0.4	0.8		*	*	$\mu s$
<b>DIGITAL-TO-ANALOG GLITCH IMPULSE</b>	$V_{REF A} = V_{REF B} = 0V$ $R_L = 100\Omega$ , $C_L = 13pF$		0.9			*		nV-s
<b>AC FEEDTHROUGH</b>	$f_{VREF} = 10kHz$		-75	-72		*	*	dB
<b>OUTPUT CAPACITANCE</b>	DAC Loaded with All 0s DAC Loaded with All 1s		30 70	50 100		* *	* *	pF pF
<b>CHANNEL-TO-CHANNEL ISOLATION</b> $V_{REF A}$ to $I_{OUT B}$  $V_{REF B}$ to $I_{OUT A}$	$f_{VREF A} = 10kHz$ $V_{REF B} = 0V$ , Both DACs Loaded with 1s $f_{VREF B} = 10kHz$ $V_{REF A} = 0V$ , Both DACs Loaded with 1s	-90 -90	-94 -101		* *	* *		dB dB
<b>DIGITAL CROSSTALK</b>	Full Scale Transition $R_L = 100\Omega$ , $C_L = 13pF$		0.9			*		nV-s

\* Same specification as for DAC7800, 7801, 7802K.

NOTE: (1) Guaranteed but not tested.

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## PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	RELATIVE ACCURACY	GAIN ERROR
DAC7800KP	16-Pin PDIP	180	$\pm 1\text{LSB}$	$\pm 3\text{LSB}$
DAC7800LP	16-Pin PDIP	180	$\pm 1/2\text{LSB}$	$\pm 1\text{LSB}$
DAC7800KU	16-Lead SOIC	211		
DAC7800LU	16-Lead SOIC	211		
DAC7801KP	24-Pin DIP	243	$\pm 1\text{LSB}$	$\pm 3\text{LSB}$
DAC7801LP	24-Pin DIP	243	$\pm 1/2\text{LSB}$	$\pm 1\text{LSB}$
DAC7801KU	24-Lead SOIC	239		
DAC7801LU	24-Lead SOIC	239		
DAC7802KP	24-Pin DIP	243-3	$\pm 1\text{LSB}$	$\pm 3\text{LSB}$
DAC7802LP	24-Pin DIP	243-3	$\pm 1/2\text{LSB}$	$\pm 1\text{LSB}$
DAC7802KU	24-Lead SOIC	239		
DAC7802LU	24-Lead SOIC	239		

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

$V_{DD}$ to AGND .....	0V, +7V
$V_{DD}$ to DGND .....	0V, +7V
AGND to DGND .....	-0.3, $V_{DD}$
Digital Input to DGND .....	-0.3, $V_{DD} + 0.3$
$V_{REF A}$ , $V_{REF B}$ to AGND .....	$\pm 20\text{V}$
$V_{REF A}$ , $V_{REF B}$ to DGND .....	$\pm 20\text{V}$
$I_{OUT A}$ , $I_{OUT B}$ to AGND .....	-0.3, $V_{DD}$
Storage Temperature Range .....	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Operating Temperature Range .....	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Lead Temperature (soldering, 10s) .....	$+300^\circ\text{C}$
Junction Temperature .....	$+175^\circ\text{C}$



## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure.

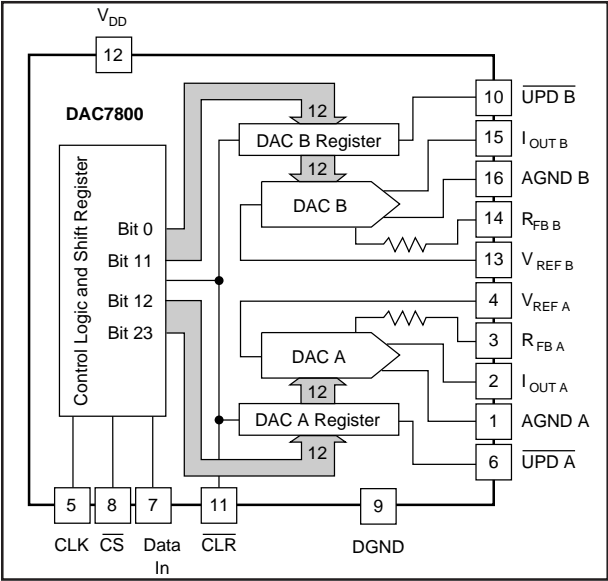
Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

**Digital Inputs:** All digital inputs of the DAC780X family incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500 $\Omega$ ) applied to each digital input.

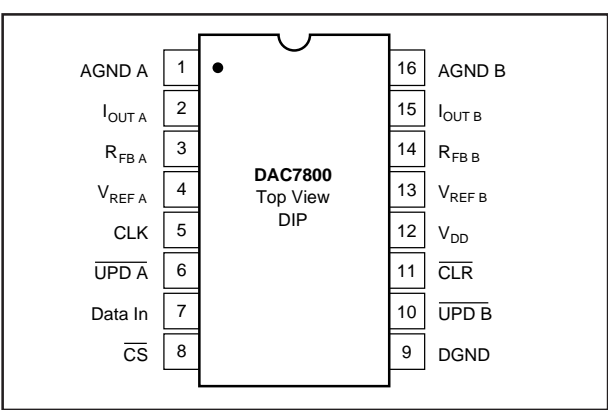
**Analog Pins:** Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500 $\Omega$ ) applied to each pin. AGND,  $I_{OUT}$ , and  $R_{FB}$  show some sensitivity. Failure to observe ESD handling procedures could result in catastrophic device failure.

# DAC7800

## BLOCK DIAGRAM



## PIN CONFIGURATION

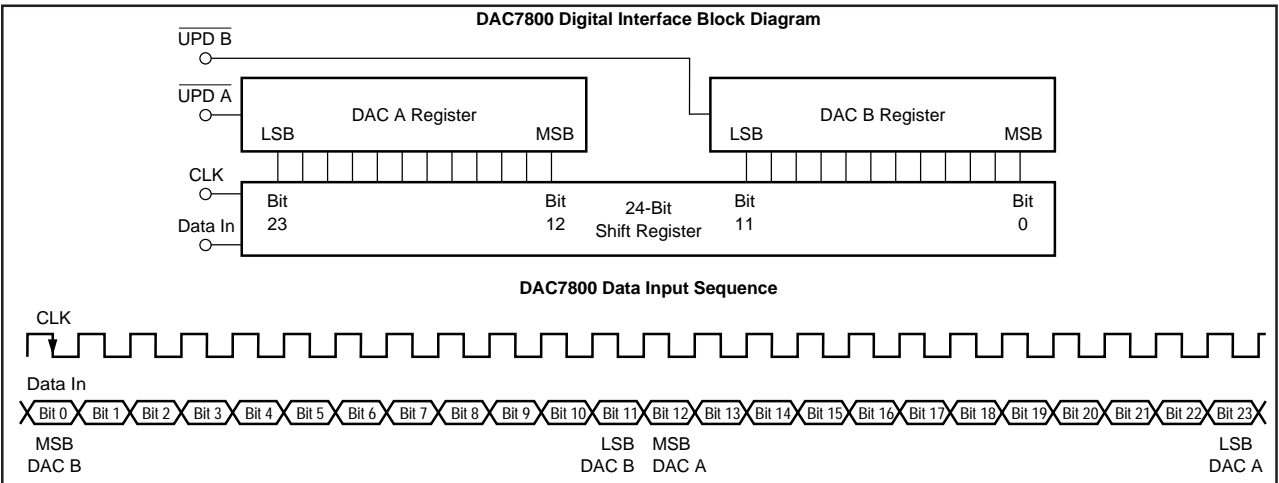


## LOGIC TRUTH TABLE

CLK	UPD A	UPD B	CS	CLR	FUNCTION
X	X	X	X	0	All register contents set to 0's (asynchronous).
X	X	X	1	X	No data transfer.
	X	X	0	1	Input data is clocked into input register (location Bit 23) and previous data shifts.
X	0	1	0	1	Input register bits 23 (LSB)—12 (MSB) are loaded into DAC A.
X	1	0	0	1	Input register bits 11 (LSB)—0 (MSB) are loaded into DAC B.
X	0	0	0	1	Input register bits 23 (LSB)—12 (MSB) are loaded into DAC A, and input register bits 11 (LSB)—0 (MSB) are loaded into DAC B.

X = Don't care. means falling edge triggered.

## DATA INPUT FORMAT



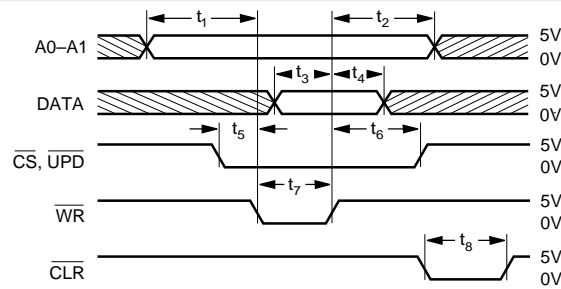


## DAC7801 (CONT)

### TIMING CHARACTERISTICS

$V_{DD} = +5V$ ,  $V_{REF A} = V_{REF B} = +10V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

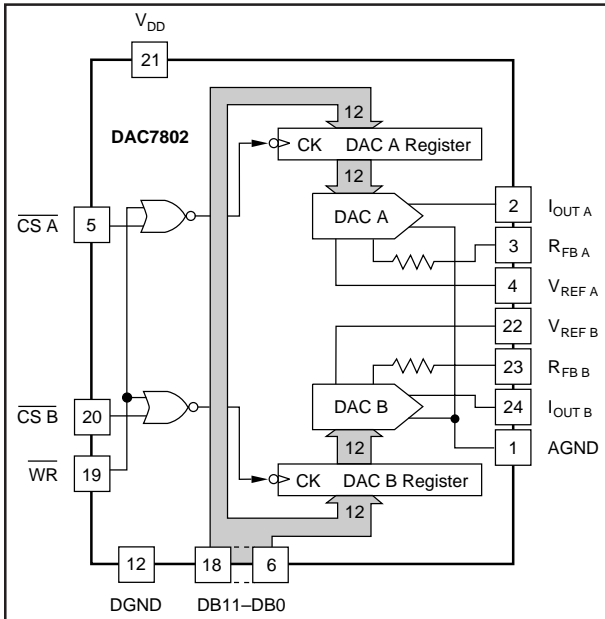
PARAMETER	MINIMUM
$t_1$ — Address Valid to Write Setup Time	10ns
$t_2$ — Address Valid to Write Hold Time	10ns
$t_3$ — Data Setup Time	30ns
$t_4$ — Data Hold Time	10ns
$t_5$ — Chip Select or Update to Write Setup Time	0ns
$t_6$ — Chip Select or Update to Write Hold Time	0ns
$t_7$ — Write Pulse Width	40ns
$t_8$ — Clear Pulse Width	40ns



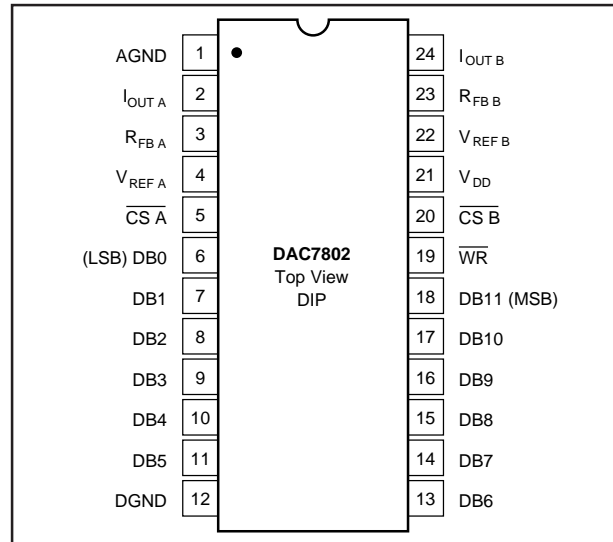
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V.  $t_R = t_F = 5ns$ . (2) Timing measurement reference level is  $\frac{V_{IH} + V_{IL}}{2}$ .

## DAC7802

### BLOCK DIAGRAM



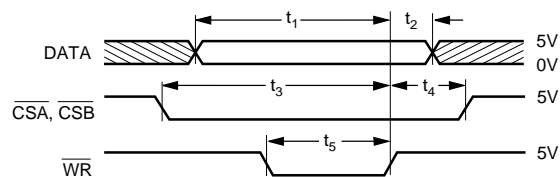
### PIN CONFIGURATION



### TIMING CHARACTERISTICS

At  $V_{DD} = +5V$ , and  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

PARAMETER	MINIMUM
$t_1$ - Data Setup Time	20ns
$t_2$ - Data Hold Time	15ns
$t_3$ - Chip Select to Write Setup Time	30ns
$t_4$ - Chip Select to Write Hold Time	0ns
$t_5$ - Write Pulse Width	30ns



NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V.  $t_R = t_F = 5ns$ . (2) Timing measurement reference level is  $\frac{V_{IH} + V_{IL}}{2}$ .

### LOGIC TRUTH TABLE

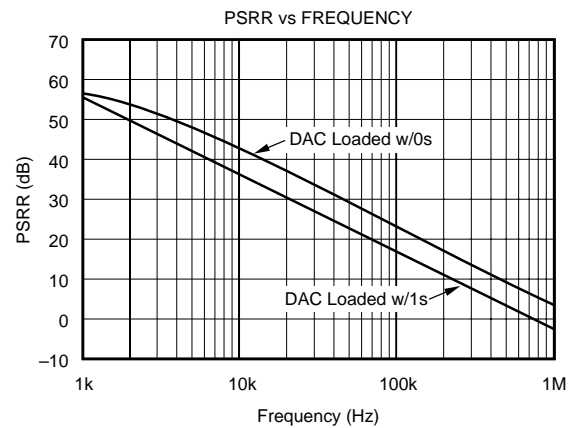
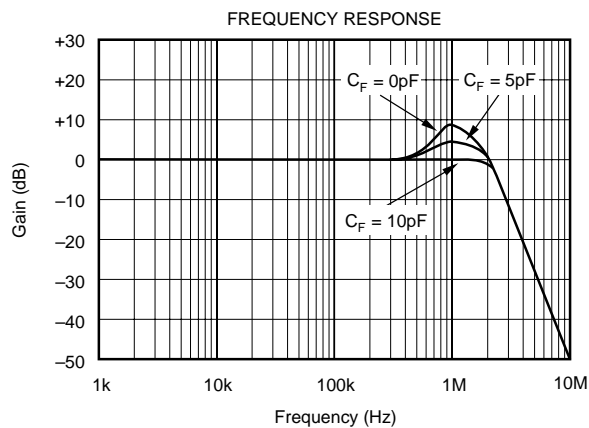
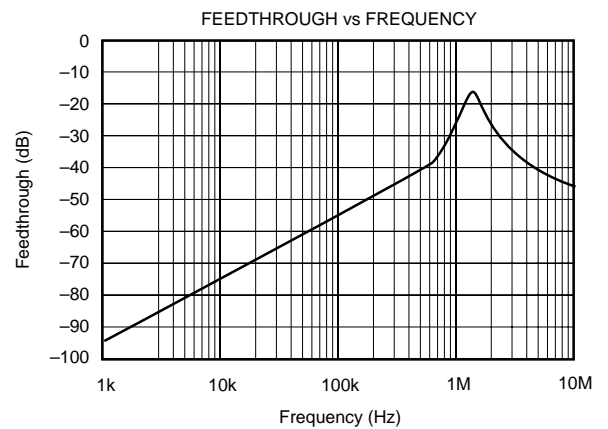
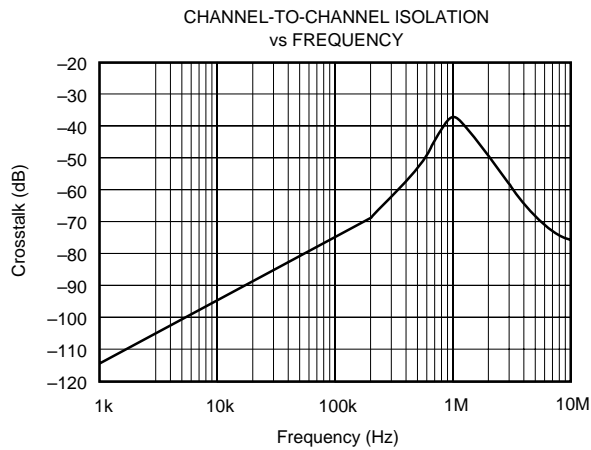
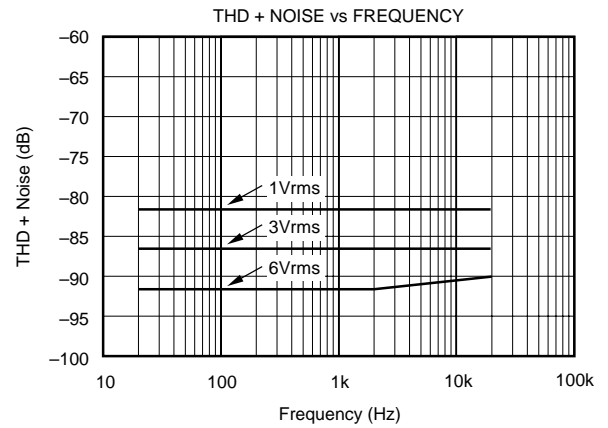
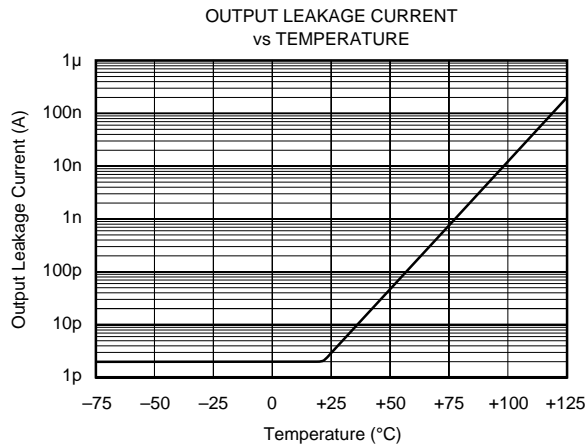
CSA	CSB	WR	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
$\uparrow$	$\uparrow$	0	A Rising Edge on CSA or CSB Loads Data to the Respective DAC
0	1	$\uparrow$	DAC A Register Loaded from Data Bus
1	0	$\uparrow$	DAC B Register Loaded from Data Bus
0	0	$\uparrow$	DAC A and DAC B Registers Loaded from Data Bus

X = Don't care.  $\uparrow$  means rising edge triggered.

# TYPICAL PERFORMANCE CURVES

OUTPUT OP AMP IS OPA602.

$T_A = +25^\circ\text{C}$ ,  $V_{DD} = +5\text{V}$ .



# DISCUSSION OF SPECIFICATIONS

## RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

## DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

## GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC780X is  $-(4095/4096)V_{REF}$ . Gain error may be adjusted to zero using external trims as shown in Figures 5 and 7.

## OUTPUT LEAKAGE CURRENT

The current which appears at  $I_{OUT A}$  and  $I_{OUT B}$  with the DAC loaded with all zeros.

## OUTPUT CAPACITANCE

The parasitic capacitance measured from  $I_{OUT A}$  or  $I_{OUT B}$  to AGND.

## CHANNEL-TO-CHANNEL ISOLATION

The AC output error due to capacitive coupling from DAC A to DAC B or DAC B to DAC A.

## MULTIPLYING FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from  $V_{REF}$  to  $I_{OUT}$  with the DAC loaded with all zeros.

## OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within  $\pm 0.01\%$  of final value for a full scale step.

## DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

## DIGITAL CROSSTALK

Glitch impulse measured at the output of one DAC but caused by a full scale transition on the other DAC. The integrated area of the glitch pulse is measured in nanovolt-seconds.

# CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of one half of a DAC780X. The current from the  $V_{REF A}$  pin is switched between  $I_{OUT A}$  and AGND by 12 single-pole double-throw CMOS switches. This maintains a constant current in each leg

of the ladder regardless of the input code. The input resistance at  $V_{REF}$  is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to  $\pm 20V$ .

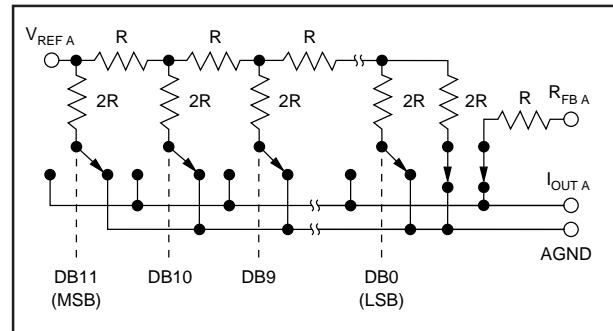


FIGURE 1. Simplified Circuit Diagram for DAC A.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor,  $R_{FB A}$ , compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for DAC A.  $C_{OUT}$  is the output capacitance due to the N-channel switches and varies from about 30pF to 70pF with digital input code. The current source  $I_{LKG}$  is the combination of surface and junction leakages to the substrate.  $I_{LKG}$  approximately doubles every  $10^{\circ}C$ .  $R_O$  is the equivalent output resistance of the D/A and it varies with input code.

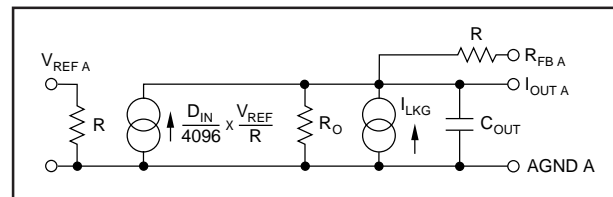


FIGURE 2. Equivalent Circuit for DAC A.

# INSTALLATION

## ESD PROTECTION

All digital inputs of the DAC780X incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

## POWER SUPPLY CONNECTIONS

The DAC780X are designed to operate on  $V_{DD} = +5V \pm 10\%$ . For optimum performance and noise rejection, power supply decoupling capacitors  $C_D$  should be added as shown in the application circuits. These capacitors (1μF tantalum recommended) should be located close to the D/A. AGND and



DGND should be connected together at one point only, preferably at the power supply ground point. Separate returns minimize current flow in low-level signal paths if properly connected. Output op amp analog common (+ input) should be connected as near to the AGND pins of the DAC780X as possible.

## WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the  $V_{REF}$  lines and the  $I_{OUT}$  lines. Similarly, capacitive coupling between DACs may compromise the channel-to-channel isolation. Coupling from any of the digital control or data lines might degrade the glitch and digital crosstalk performance. Solder the DAC780X directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

## AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC780X should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the “noise gain” of the circuit. This “noise gain” is equal to  $(R_F/R_O + 1)$  where  $R_O$  is the output impedance of the D/A  $I_{OUT}$  terminal and  $R_F$  is the feedback network impedance. The nonlinearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where  $R_O = \infty$ ), the  $R_O$  will vary from  $R$  to  $3R$  providing a “noise gain” variation between  $4/3$  and  $2$ . In addition, the variation of  $R_O$  is nonlinear with code, and the largest steps in  $R_O$  occur at major code transitions where the worst differential nonlinearity is also likely to be experienced. The nonlinearity seen at the amplifier output is  $2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3$ . Thus, to maintain good nonlinearity the op amp offset should be much less than  $1/2LSB$ .

## UNIPOLAR CONFIGURATION

Figure 3 shows DAC780X in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

## BIPOLAR CONFIGURATION

Figure 5 shows the DAC780X in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table III.

DATA INPUT	ANALOG OUTPUT
MSB ↓                      ↓ LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096) = $-1/2V_{REF}$
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

TABLE II. Unipolar Output Code.

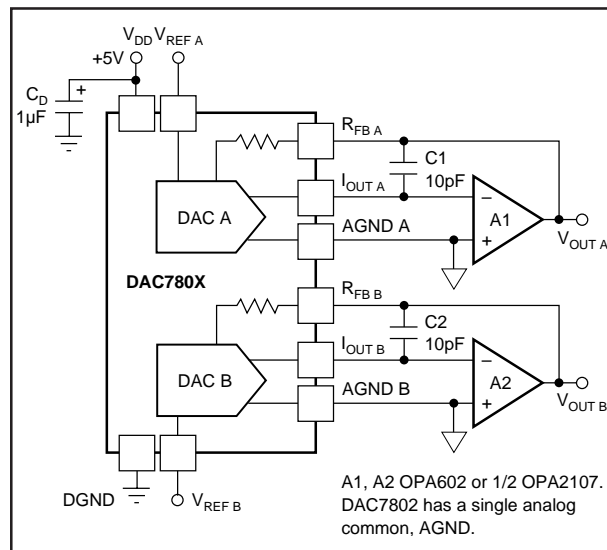


FIGURE 3. Unipolar Configuration.

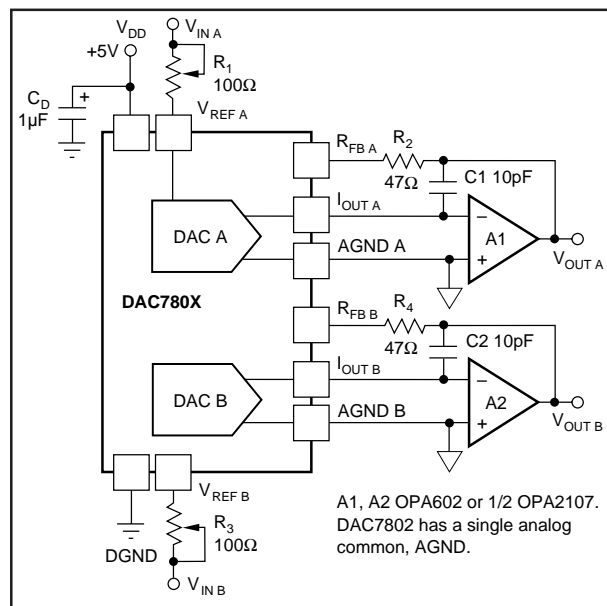
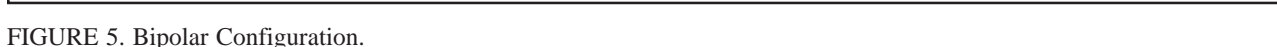


FIGURE 4. Unipolar Configuration with Gain Trim.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, a dual amplifier such as the OPA2107, or a quad amplifier like the OPA404. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R5–R7 and R8–R10 should be ratio-matched to 0.01% to ensure the specified gain error performance.

TABLE III. Bipolar Output Code.

For a bipolar DAC with 12 bi

Another option, shown in Figure 8, also produces a 12-bit

## DIGITALLY PROGRAMMABLE ACTIVE FILTER

DAC780Y are shown in Figure 9 in a digitally programmed

The center frequency is determined by  $f_C = 1/2\pi RC$  where R

Note that the ladder resistance of the D/A may vary from

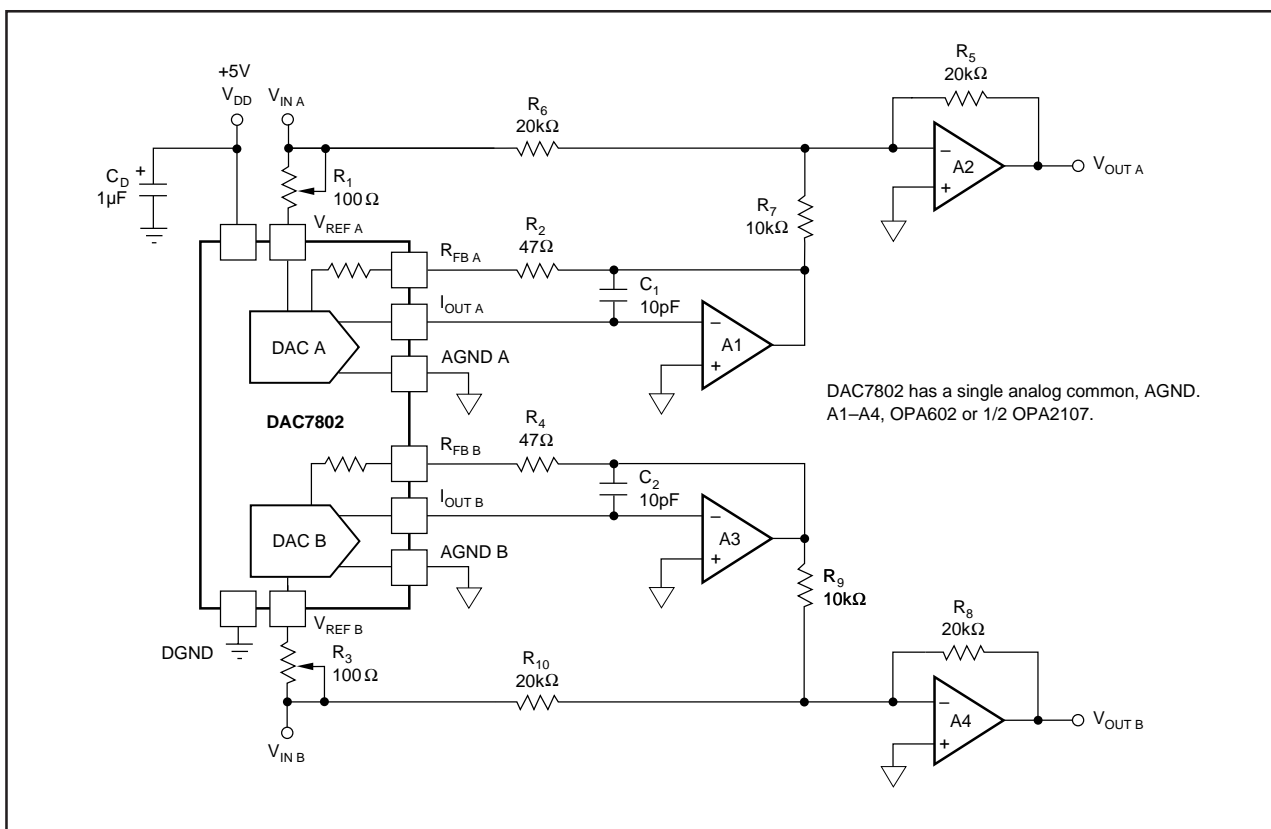


FIGURE 6. Bipolar Configuration with Gain Trim.

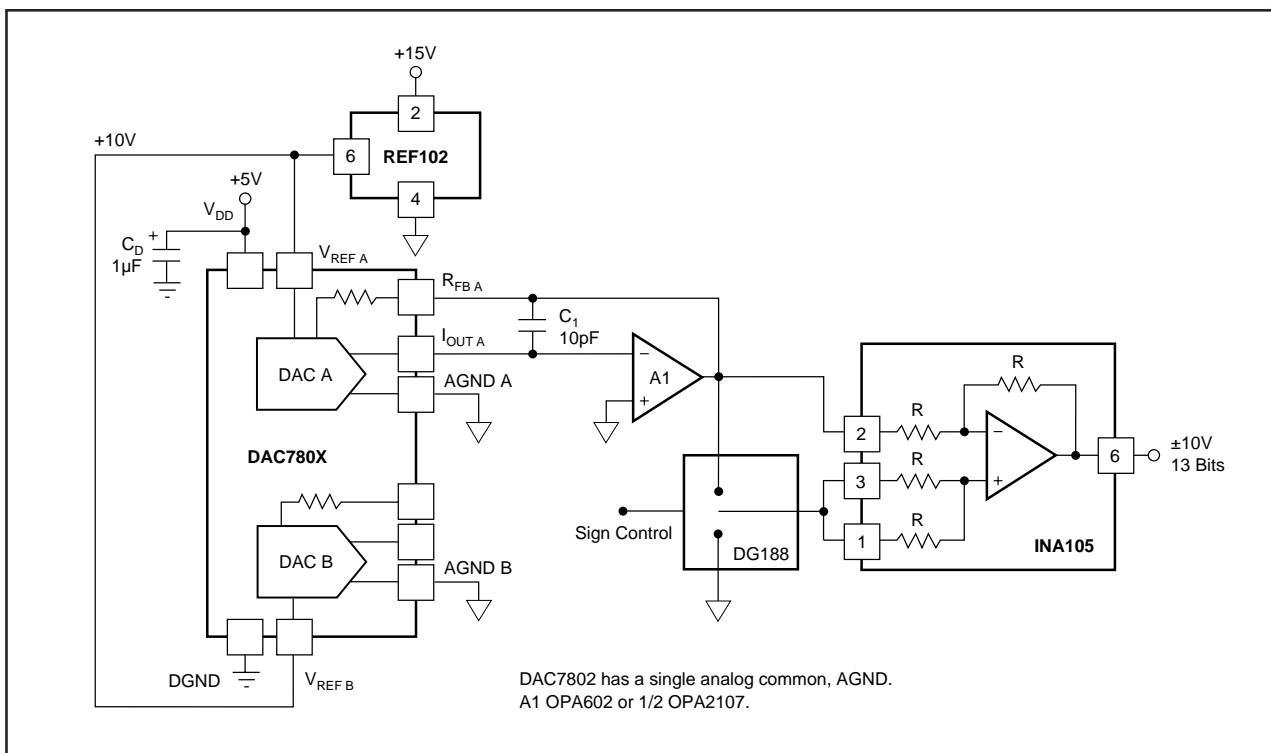


FIGURE 7. 12-Bit Plus Sign DAC.

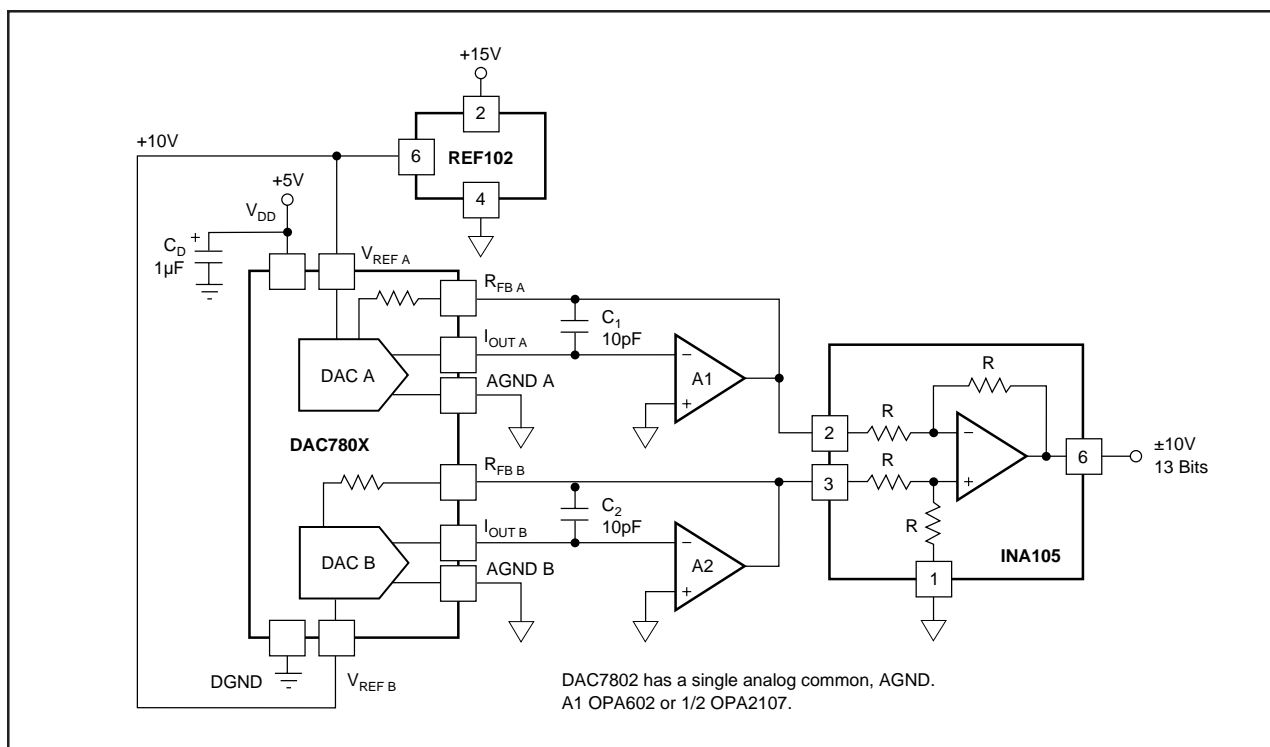


FIGURE 8. 13-Bit Bipolar DAC.

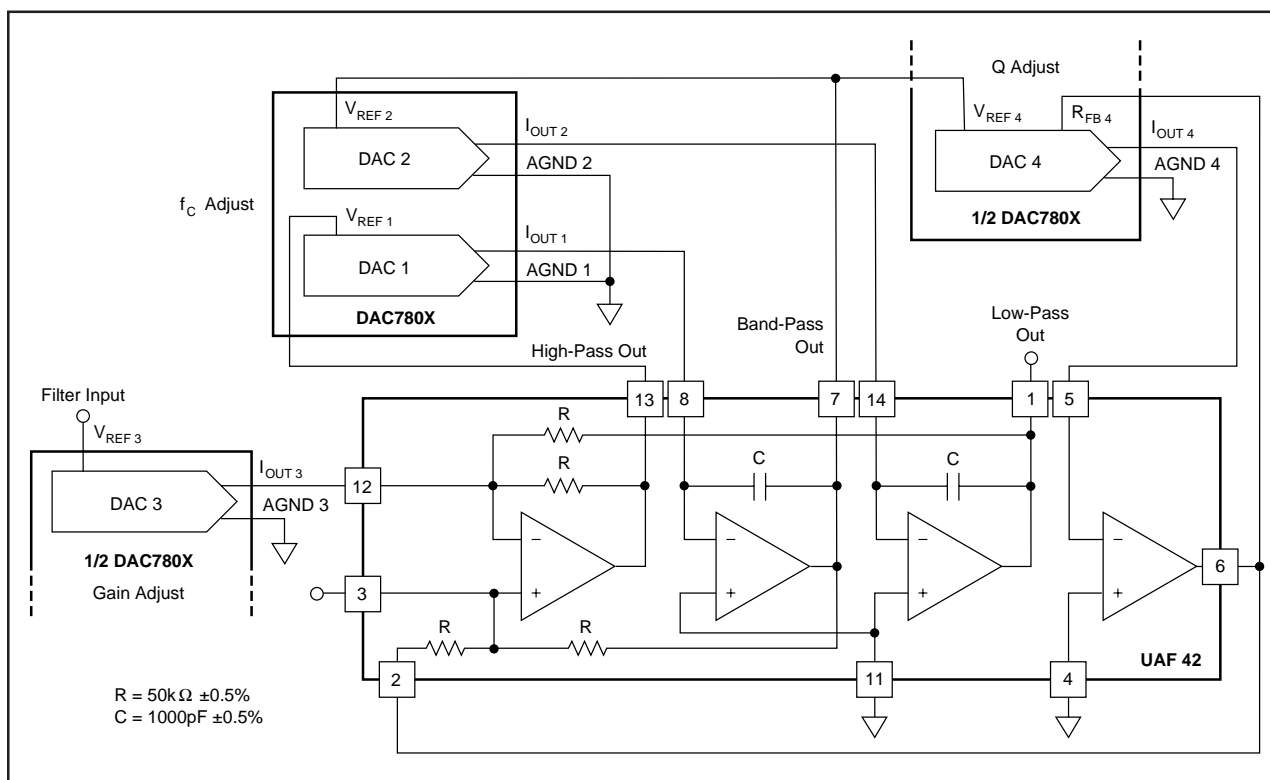


FIGURE 9. Digitally Programmable Universal Active Filter.