Preliminary

162-common x 128 RGB, 4096-Color STN LCD DRIVER

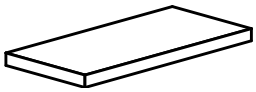
■ GENERAL DESCRIPTION

The **NJU6825** is a STN LCD driver with 162-common x 128 RGB in 4096-color. It consists of 384(128xRGB)-segment, 162-common drivers, serial and parallel MPU interface circuits, internal power supply circuits, gradation palettes and 248,832-bit for graphic display data RAM.

Each segment driver outputs 16-gradation level out of 32-gradation level of gradation palette.

Since the **NJU6825** provides a low operating voltage of 1.7V and low operating current, it is ideally suited for battery-powered handheld applications.

■ PACKAGE OUTLINE

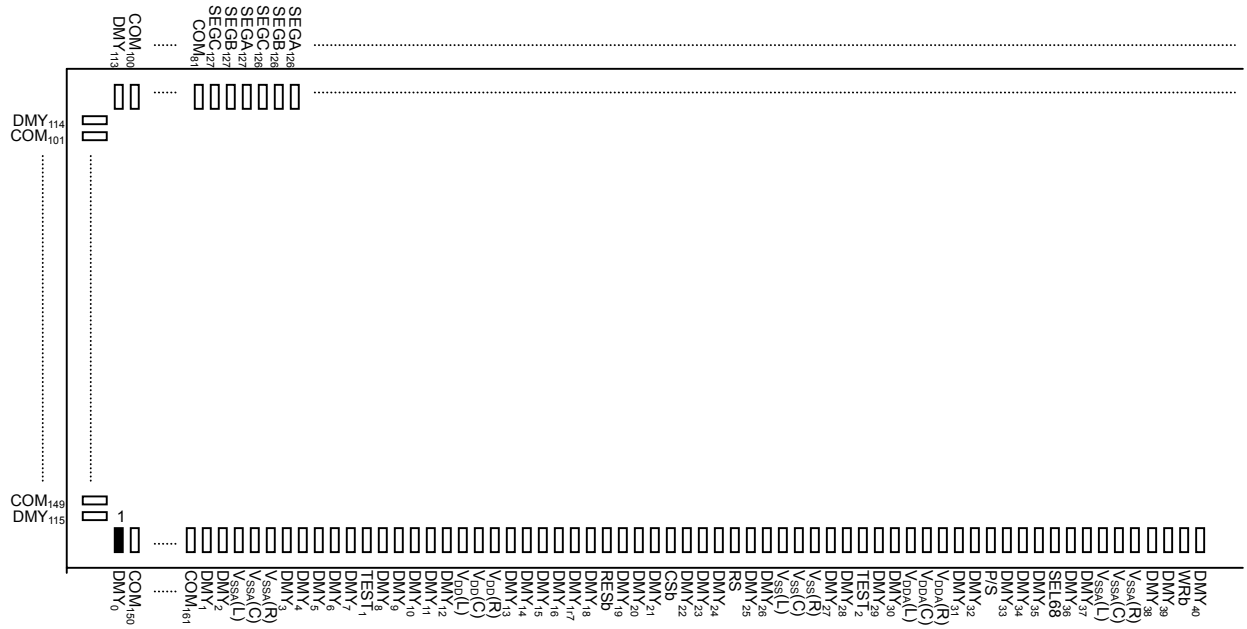


NJU6825CJ

■ FEATURES

- 4096-color STN LCD driver
- LCD drivers 162 commons, 128 RGB
- Display data RAM (DDRAM) 248,832-bit for graphic display
- Color display mode 16 gradation level out of 32-gradation level of gradation palette
- Black & white display mode 162 x 384 pixels in 16 gradation level or 162 x 384 pixels in B&W
- 256-color driving mode
- 8/16bit Parallel interface directly-connective to 68/80 series MPU
- Programmable 8- or 16-bit data bus length for display data
- 3-/4-line serial interface
- Programmable duty and bias ratios
- Programmable internal voltage booster (Maximum 7-times)
- Programmable contrast control using128-step EVR
- Various instructions
  Display data read/write, Display ON/OFF, Reverse display ON/OFF, All pixels ON/OFF, column address, row address, N-line inversion, Initial display line, Initial COM line, Read-modify-write, Gradation mode control, Increment control, Data bus length, Discharge ON/OFF, Duty cycle ratio, LCD bias ratio, Boost level, EVR control, Power save ON/OFF, etc
- Low operating current
- Low logic supply voltage 1.7V to 3.3V
- LCD driving supply voltage 5.0V to 18.0V
- C-MOS technology
- Package Bumped chip / TCP

■ PAD LOCATION

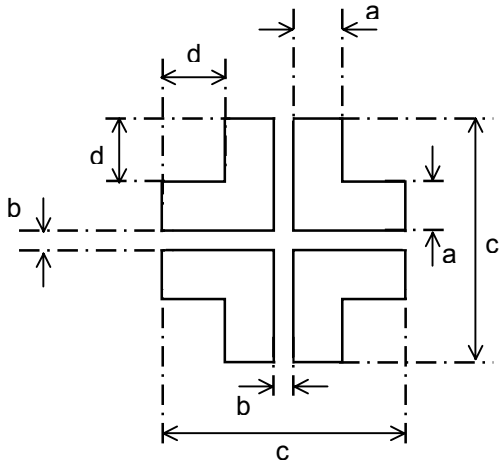


Note1) The PADs of (L), (R) and (C) are shorted mutually in the LSI.
Note2) The DMY PADs are electrically open.

Chip Center	:X= 0μm, Y= 0μm
Chip Size	:19.93mm x 3.06mm
Chip Thickness	:625μm ± 25μm
Bump Size	:32μm x 68μm(COM/SEG Output), 47μm x 68μm(Interface), 68μm x 68μm($DMY_{0,109,110,111,112,113,114,115}$)
Bump Pitch	:45μm(Min)
Bump Height	:14.0~22.5μm (Typical 18μm) <tolerance : ±3μm >
Bump Material	:Au

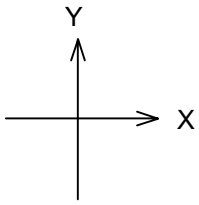
Alignment marks

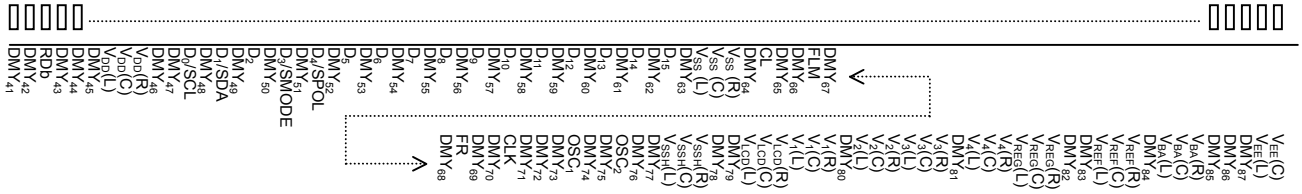
a: 30μm
b: 6μm
c: 120μm
d: 27μm

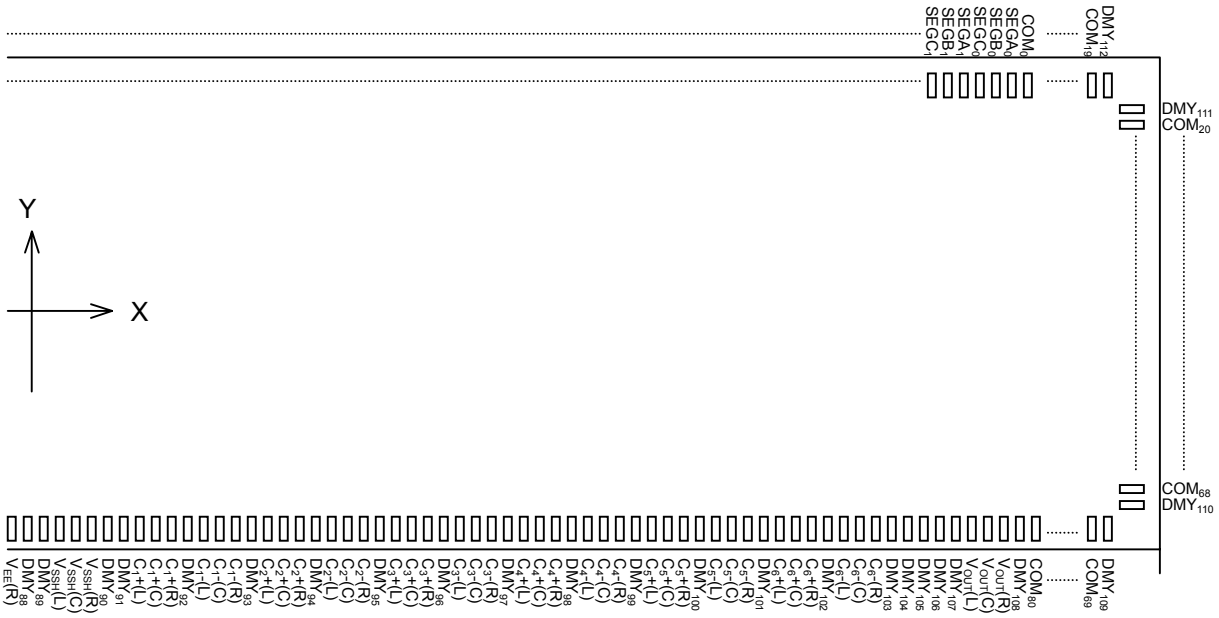


Alignment mark coordinates

X=-9831μm, Y=-1396μm
X= 9831μm, Y=-1396μm


Y
X


DMY41
DMY42
RDb
DMY43
DMY44
DMY45
VDD(L)
VDD(C)
VDD(R)
DMY46
DMY47
D8/SCL
DMY48
D1/SDA
DMY49
D2
DMY50
D3/SMODE
DMY51
D4/SPOL
DMY52
D5
DMY53
D6
DMY54
D7
DMY55
D8
DMY56
D9
DMY57
D10
DMY58
D11
DMY59
D12
DMY60
D13
DMY61
D14
DMY62
D15
DMY63
VSS(L)
VSS(C)
VSS(R)
DMY64
CL
DMY65
DMY66
FLM
DMY67
DMY68
FR
DMY69
CLK
DMY70
OSC1
DMY71
DMY72
DMY73
OSC2
DMY74
DMY75
DMY76
VSSH(L)
DMY77
VSSH(C)
VSSH(R)
DMY78
VLCD(L)
VLCD(C)
VLCD(R)
DMY79
V1(L)
V1(C)
V1(R)
DMY80
V2(L)
V2(C)
V2(R)
V3(L)
V3(C)
V3(R)
DMY81
V4(L)
V4(C)
V4(R)
VREG(L)
VREG(C)
VREG(R)
DMY82
DMY83
VREF(L)
VREF(C)
VREF(R)
DMY84
VBA(L)
VBA(C)
VBA(R)
DMY85
DMY86
DMY87
VEE(L)
VEE(C)


Y
X
COM0
SEGA0
SEGB0
SEGC0
SEGA1
SEGB1
SEGC1
DMY112
COM19
DMY111
COM20
COM68
DMY110
COM80
DMY108
VOUT1(R)
VOUT1(C)
VOUT1(L)
DMY107
DMY106
DMY105
DMY104
DMY103
C6-(R)
C6-(C)
C6-(L)
DMY102
C6+(R)
C6+(C)
C6+(L)
DMY101
C5-(R)
C5-(C)
C5-(L)
DMY100
C5+(R)
C5+(C)
C5+(L)
DMY99
C4-(R)
C4-(C)
C4-(L)
DMY98
C4+(R)
C4+(C)
C4+(L)
DMY97
C3-(R)
C3-(C)
C3-(L)
DMY96
C3+(R)
C3+(C)
C3+(L)
DMY95
C2-(R)
C2-(C)
C2-(L)
DMY94
C2+(R)
C2+(C)
C2+(L)
DMY93
C1-(R)
C1-(C)
C1-(L)
DMY92
C1+(R)
C1+(C)
C1+(L)
DMY91
VSSH(R)
VSSH(C)
VSSH(L)
DMY89
VEE(R)
DMY109
COM69

■ PAD COORDINATES 1

Chip Size 19930μm x 3060μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X (μm)	Y (μm)	PAD No.	Terminal	X (μm)	Y (μm)
1	DMY_0	-9581	-1396	52	V_{SS}(R)	-6510	-1396	103	DMY_{55}	-2250	-1396
2	COM_{150}	-9518	-1396	53	DMY_{27}	-6330	-1396	104	D_8	-2130	-1396
3	COM_{151}	-9473	-1396	54	DMY_{28}	-6270	-1396	105	DMY_{56}	-2010	-1396
4	COM_{152}	-9428	-1396	55	$TEST_2$	-6210	-1396	106	D_9	-1890	-1396
5	COM_{153}	-9383	-1396	56	DMY_{29}	-6150	-1396	107	DMY_{57}	-1770	-1396
6	COM_{154}	-9338	-1396	57	DMY_{30}	-6090	-1396	108	D_{10}	-1650	-1396
7	COM_{155}	-9293	-1396	58	V_{DDA}(L)	-6030	-1396	109	DMY_{58}	-1530	-1396
8	COM_{156}	-9248	-1396	59	V_{DDA}(C)	-5970	-1396	110	D_{11}	-1410	-1396
9	COM_{157}	-9203	-1396	60	V_{DDA}(R)	-5910	-1396	111	DMY_{59}	-1290	-1396
10	COM_{158}	-9158	-1396	61	DMY_{31}	-5850	-1396	112	D_{12}	-1170	-1396
11	COM_{159}	-9113	-1396	62	DMY_{32}	-5790	-1396	113	DMY_{60}	-1050	-1396
12	COM_{160}	-9068	-1396	63	P/S	-5730	-1396	114	D_{13}	-930	-1396
13	COM_{161}	-9023	-1396	64	DMY_{33}	-5670	-1396	115	DMY_{61}	-810	-1396
14	DMY_1	-8910	-1396	65	DMY_{34}	-5610	-1396	116	D_{14}	-690	-1396
15	DMY_2	-8850	-1396	66	DMY_{35}	-5550	-1396	117	DMY_{62}	-570	-1396
16	V_{SSA}(L)	-8790	-1396	67	SEL68	-5490	-1396	118	D_{15}	-450	-1396
17	V_{SSA}(C)	-8730	-1396	68	DMY_{36}	-5430	-1396	119	DMY_{63}	-330	-1396
18	V_{SSA}(R)	-8670	-1396	69	DMY_{37}	-5370	-1396	120	V_{SS}(L)	-270	-1396
19	DMY_3	-8610	-1396	70	V_{SSA}(L)	-5310	-1396	121	V_{SS}(C)	-210	-1396
20	DMY_4	-8550	-1396	71	V_{SSA}(C)	-5250	-1396	122	V_{SS}(R)	-150	-1396
21	DMY_5	-8490	-1396	72	V_{SSA}(R)	-5190	-1396	123	DMY_{64}	30	-1396
22	DMY_6	-8430	-1396	73	DMY_{38}	-5130	-1396	124	CL	150	-1396
23	DMY_7	-8370	-1396	74	DMY_{39}	-5070	-1396	125	DMY_{65}	270	-1396
24	$TEST_1$	-8310	-1396	75	WRb	-5010	-1396	126	DMY_{66}	330	-1396
25	DMY_8	-8250	-1396	76	DMY_{40}	-4950	-1396	127	FLM	450	-1396
26	DMY_9	-8190	-1396	77	DMY_{41}	-4890	-1396	128	DMY_{67}	570	-1396
27	DMY_{10}	-8130	-1396	78	DMY_{42}	-4830	-1396	129	DMY_{68}	630	-1396
28	DMY_{11}	-8070	-1396	79	RDb	-4770	-1396	130	FR	750	-1396
29	DMY_{12}	-8010	-1396	80	DMY_{43}	-4710	-1396	131	DMY_{69}	870	-1396
30	V_{DD}(L)	-7950	-1396	81	DMY_{44}	-4650	-1396	132	DMY_{70}	930	-1396
31	V_{DD}(C)	-7890	-1396	82	DMY_{45}	-4590	-1396	133	CLK	1050	-1396
32	V_{DD}(R)	-7830	-1396	83	V_{DD}(L)	-4530	-1396	134	DMY_{71}	1170	-1396
33	DMY_{13}	-7650	-1396	84	V_{DD}(C)	-4470	-1396	135	DMY_{72}	1230	-1396
34	DMY_{14}	-7590	-1396	85	V_{DD}(R)	-4410	-1396	136	DMY_{73}	1290	-1396
35	DMY_{15}	-7530	-1396	86	DMY_{46}	-4230	-1396	137	OSC_1	1350	-1396
36	DMY_{16}	-7470	-1396	87	DMY_{47}	-4170	-1396	138	DMY_{74}	1410	-1396
37	DMY_{17}	-7410	-1396	88	D_0	-4050	-1396	139	DMY_{75}	1470	-1396
38	DMY_{18}	-7350	-1396	89	DMY_{48}	-3930	-1396	140	OSC_2	1650	-1396
39	RESb	-7290	-1396	90	D_1	-3810	-1396	141	DMY_{76}	1830	-1396
40	DMY_{19}	-7230	-1396	91	DMY_{49}	-3690	-1396	142	DMY_{77}	1890	-1396
41	DMY_{20}	-7170	-1396	92	D_2	-3570	-1396	143	V_{SSH}(L)	1950	-1396
42	DMY_{21}	-7110	-1396	93	DMY_{50}	-3450	-1396	144	V_{SSH}(C)	2010	-1396
43	CSb	-7050	-1396	94	D_3	-3330	-1396	145	V_{SSH}(R)	2070	-1396
44	DMY_{22}	-6990	-1396	95	DMY_{51}	-3210	-1396	146	DMY_{78}	2250	-1396
45	DMY_{23}	-6930	-1396	96	D_4	-3090	-1396	147	DMY_{79}	2310	-1396
46	DMY_{24}	-6870	-1396	97	DMY_{52}	-2970	-1396	148	V_{LCD}(L)	2370	-1396
47	RS	-6810	-1396	98	D_5	-2850	-1396	149	V_{LCD}(C)	2430	-1396
48	DMY_{25}	-6750	-1396	99	DMY_{53}	-2730	-1396	150	V_{LCD}(R)	2490	-1396
49	DMY_{26}	-6690	-1396	100	D_6	-2610	-1396	151	V_1(L)	2670	-1396
50	V_{SS}(L)	-6630	-1396	101	DMY_{54}	-2490	-1396	152	V_1(C)	2730	-1396
51	V_{SS}(C)	-6570	-1396	102	D_7	-2370	-1396	153	V_1(R)	2790	-1396

■ PAD COORDINATES 2

Chip Size 19930μm x 3060μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X (μm)	Y (μm)	PAD No.	Terminal	X (μm)	Y (μm)
154	DMY_{80}	2850	-1396	205	DMY_{95}	6390	-1396	256	COM_{70}	9473	-1396
155	V_2(L)	2910	-1396	206	C_3+(L)	6450	-1396	257	COM_{69}	9518	-1396
156	V_2(C)	2970	-1396	207	C_3+(C)	6510	-1396	258	DMY_{109}	9581	-1396
157	V_2(R)	3030	-1396	208	C_3+(R)	6570	-1396	259	DMY_{110}	9831	-1143
158	V_3(L)	3210	-1396	209	DMY_{96}	6630	-1396	260	COM_{68}	9831	-1080
159	V_3(C)	3270	-1396	210	C_3-(L)	6690	-1396	261	COM_{67}	9831	-1035
160	V_3(R)	3330	-1396	211	C_3-(C)	6750	-1396	262	COM_{66}	9831	-990
161	DMY_{81}	3390	-1396	212	C_3-(R)	6810	-1396	263	COM_{65}	9831	-945
162	V_4(L)	3450	-1396	213	DMY_{97}	6870	-1396	264	COM_{64}	9831	-900
163	V_4(C)	3510	-1396	214	C_4+(L)	6930	-1396	265	COM_{63}	9831	-855
164	V_4(R)	3570	-1396	215	C_4+(C)	6990	-1396	266	COM_{62}	9831	-810
165	V_{REG}(L)	3750	-1396	216	C_4+(R)	7050	-1396	267	COM_{61}	9831	-765
166	V_{REG}(C)	3810	-1396	217	DMY_{98}	7110	-1396	268	COM_{60}	9831	-720
167	V_{REG}(R)	3870	-1396	218	C_4-(L)	7170	-1396	269	COM_{59}	9831	-675
168	DMY_{82}	3930	-1396	219	C_4-(C)	7230	-1396	270	COM_{58}	9831	-630
169	DMY_{83}	3990	-1396	220	C_4-(R)	7290	-1396	271	COM_{57}	9831	-585
170	V_{REF}(L)	4050	-1396	221	DMY_{99}	7350	-1396	272	COM_{56}	9831	-540
171	V_{REF}(C)	4110	-1396	222	C_5+(L)	7410	-1396	273	COM_{55}	9831	-495
172	V_{REF}(R)	4170	-1396	223	C_5+(C)	7470	-1396	274	COM_{54}	9831	-450
173	DMY_{84}	4230	-1396	224	C_5+(R)	7530	-1396	275	COM_{53}	9831	-405
174	V_{BA}(L)	4290	-1396	225	DMY_{100}	7590	-1396	276	COM_{52}	9831	-360
175	V_{BA}(C)	4350	-1396	226	C_5-(L)	7650	-1396	277	COM_{51}	9831	-315
176	V_{BA}(R)	4410	-1396	227	C_5-(C)	7710	-1396	278	COM_{50}	9831	-270
177	DMY_{85}	4470	-1396	228	C_5-(R)	7770	-1396	279	COM_{49}	9831	-225
178	DMY_{86}	4530	-1396	229	DMY_{101}	7830	-1396	280	COM_{48}	9831	-180
179	DMY_{87}	4590	-1396	230	C_6+(L)	7890	-1396	281	COM_{47}	9831	-135
180	V_{EE}(L)	4650	-1396	231	C_6+(C)	7950	-1396	282	COM_{46}	9831	-90
181	V_{EE}(C)	4710	-1396	232	C_6+(R)	8010	-1396	283	COM_{45}	9831	-45
182	V_{EE}(R)	4770	-1396	233	DMY_{102}	8070	-1396	284	COM_{44}	9831	0
183	DMY_{88}	4950	-1396	234	C_6-(L)	8130	-1396	285	COM_{43}	9831	45
184	DMY_{89}	5010	-1396	235	C_6-(C)	8190	-1396	286	COM_{42}	9831	90
185	V_{SSH}(L)	5190	-1396	236	C_6-(R)	8250	-1396	287	COM_{41}	9831	135
186	V_{SSH}(C)	5250	-1396	237	DMY_{103}	8310	-1396	288	COM_{40}	9831	180
187	V_{SSH}(R)	5310	-1396	238	DMY_{104}	8370	-1396	289	COM_{39}	9831	225
188	DMY_{90}	5370	-1396	239	DMY_{105}	8430	-1396	290	COM_{38}	9831	270
189	DMY_{91}	5430	-1396	240	DMY_{106}	8490	-1396	291	COM_{37}	9831	315
190	C_1+(L)	5490	-1396	241	DMY_{107}	8550	-1396	292	COM_{36}	9831	360
191	C_1+(C)	5550	-1396	242	V_{OUT}(L)	8610	-1396	293	COM_{35}	9831	405
192	C_1+(R)	5610	-1396	243	V_{OUT}(C)	8670	-1396	294	COM_{34}	9831	450
193	DMY_{92}	5670	-1396	244	V_{OUT}(R)	8730	-1396	295	COM_{33}	9831	495
194	C_1-(L)	5730	-1396	245	DMY_{108}	8910	-1396	296	COM_{32}	9831	540
195	C_1-(C)	5790	-1396	246	COM_{80}	9023	-1396	297	COM_{31}	9831	585
196	C_1-(R)	5850	-1396	247	COM_{79}	9068	-1396	298	COM_{30}	9831	630
197	DMY_{93}	5910	-1396	248	COM_{78}	9113	-1396	299	COM_{29}	9831	675
198	C_2+(L)	5970	-1396	249	COM_{77}	9158	-1396	300	COM_{28}	9831	720
199	C_2+(C)	6030	-1396	250	COM_{76}	9203	-1396	301	COM_{27}	9831	765
200	C_2+(R)	6090	-1396	251	COM_{75}	9248	-1396	302	COM_{26}	9831	810
201	DMY_{94}	6150	-1396	252	COM_{74}	9293	-1396	303	COM_{25}	9831	855
202	C_2-(L)	6210	-1396	253	COM_{73}	9338	-1396	304	COM_{24}	9831	900
203	C_2-(C)	6270	-1396	254	COM_{72}	9383	-1396	305	COM_{23}	9831	945
204	C_2-(R)	6330	-1396	255	COM_{71}	9428	-1396	306	COM_{22}	9831	990

■ PAD COORDINATES 3

Chip Size 19930μm x 3060μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X (μm)	Y (μm)	PAD No.	Terminal	X (μm)	Y (μm)
307	COM_{21}	9831	1035	358	$SEGA_{9}$	7403	1396	409	$SEGA_{26}$	5108	1396
308	COM_{20}	9831	1080	359	$SEGB_{9}$	7358	1396	410	$SEGB_{26}$	5063	1396
309	DMY_{111}	9831	1144	360	$SEGC_{9}$	7313	1396	411	$SEGC_{26}$	5018	1396
310	DMY_{112}	9581	1396	361	$SEGA_{10}$	7268	1396	412	$SEGA_{27}$	4973	1396
311	COM_{19}	9518	1396	362	$SEGB_{10}$	7223	1396	413	$SEGB_{27}$	4928	1396
312	COM_{18}	9473	1396	363	$SEGC_{10}$	7178	1396	414	$SEGC_{27}$	4883	1396
313	COM_{17}	9428	1396	364	$SEGA_{11}$	7133	1396	415	$SEGA_{28}$	4838	1396
314	COM_{16}	9383	1396	365	$SEGB_{11}$	7088	1396	416	$SEGB_{28}$	4793	1396
315	COM_{15}	9338	1396	366	$SEGC_{11}$	7043	1396	417	$SEGC_{28}$	4748	1396
316	COM_{14}	9293	1396	367	$SEGA_{12}$	6998	1396	418	$SEGA_{29}$	4703	1396
317	COM_{13}	9248	1396	368	$SEGB_{12}$	6953	1396	419	$SEGB_{29}$	4658	1396
318	COM_{12}	9203	1396	369	$SEGC_{12}$	6908	1396	420	$SEGC_{29}$	4613	1396
319	COM_{11}	9158	1396	370	$SEGA_{13}$	6863	1396	421	$SEGA_{30}$	4568	1396
320	COM_{10}	9113	1396	371	$SEGB_{13}$	6818	1396	422	$SEGB_{30}$	4523	1396
321	COM_{9}	9068	1396	372	$SEGC_{13}$	6773	1396	423	$SEGC_{30}$	4478	1396
322	COM_{8}	9023	1396	373	$SEGA_{14}$	6728	1396	424	$SEGA_{31}$	4433	1396
323	COM_{7}	8978	1396	374	$SEGB_{14}$	6683	1396	425	$SEGB_{31}$	4388	1396
324	COM_{6}	8933	1396	375	$SEGC_{14}$	6638	1396	426	$SEGC_{31}$	4343	1396
325	COM_{5}	8888	1396	376	$SEGA_{15}$	6593	1396	427	$SEGA_{32}$	4298	1396
326	COM_{4}	8843	1396	377	$SEGB_{15}$	6548	1396	428	$SEGB_{32}$	4253	1396
327	COM_{3}	8798	1396	378	$SEGC_{15}$	6503	1396	429	$SEGC_{32}$	4208	1396
328	COM_{2}	8753	1396	379	$SEGA_{16}$	6458	1396	430	$SEGA_{33}$	4163	1396
329	COM_{1}	8708	1396	380	$SEGB_{16}$	6413	1396	431	$SEGB_{33}$	4118	1396
330	COM_{0}	8663	1396	381	$SEGC_{16}$	6368	1396	432	$SEGC_{33}$	4073	1396
331	$SEGA_{0}$	8618	1396	382	$SEGA_{17}$	6323	1396	433	$SEGA_{34}$	4028	1396
332	$SEGB_{0}$	8573	1396	383	$SEGB_{17}$	6278	1396	434	$SEGB_{34}$	3983	1396
333	$SEGC_{0}$	8528	1396	384	$SEGC_{17}$	6233	1396	435	$SEGC_{34}$	3938	1396
334	$SEGA_{1}$	8483	1396	385	$SEGA_{18}$	6188	1396	436	$SEGA_{35}$	3893	1396
335	$SEGB_{1}$	8438	1396	386	$SEGB_{18}$	6143	1396	437	$SEGB_{35}$	3848	1396
336	$SEGC_{1}$	8393	1396	387	$SEGC_{18}$	6098	1396	438	$SEGC_{35}$	3803	1396
337	$SEGA_{2}$	8348	1396	388	$SEGA_{19}$	6053	1396	439	$SEGA_{36}$	3758	1396
338	$SEGB_{2}$	8303	1396	389	$SEGB_{19}$	6008	1396	440	$SEGB_{36}$	3713	1396
339	$SEGC_{2}$	8258	1396	390	$SEGC_{19}$	5963	1396	441	$SEGC_{36}$	3668	1396
340	$SEGA_{2}$	8213	1396	391	$SEGA_{20}$	5918	1396	442	$SEGA_{37}$	3623	1396
341	$SEGB_{3}$	8168	1396	392	$SEGB_{20}$	5873	1396	443	$SEGB_{37}$	3578	1396
342	$SEGC_{3}$	8123	1396	393	$SEGC_{20}$	5828	1396	444	$SEGC_{37}$	3533	1396
343	$SEGA_{4}$	8078	1396	394	$SEGA_{21}$	5783	1396	445	$SEGA_{38}$	3488	1396
344	$SEGB_{4}$	8033	1396	395	$SEGB_{21}$	5738	1396	446	$SEGB_{38}$	3443	1396
345	$SEGC_{4}$	7988	1396	396	$SEGC_{21}$	5693	1396	447	$SEGC_{38}$	3398	1396
346	$SEGA_{5}$	7943	1396	397	$SEGA_{22}$	5648	1396	448	$SEGA_{39}$	3353	1396
347	$SEGB_{5}$	7898	1396	398	$SEGB_{22}$	5603	1396	449	$SEGB_{39}$	3308	1396
348	$SEGC_{5}$	7853	1396	399	$SEGC_{22}$	5558	1396	450	$SEGC_{39}$	3263	1396
349	$SEGA_{6}$	7808	1396	400	$SEGA_{23}$	5513	1396	451	$SEGA_{40}$	3218	1396
350	$SEGB_{6}$	7763	1396	401	$SEGB_{23}$	5468	1396	452	$SEGB_{40}$	3173	1396
351	$SEGC_{6}$	7718	1396	402	$SEGC_{23}$	5423	1396	453	$SEGC_{40}$	3128	1396
352	$SEGA_{7}$	7673	1396	403	$SEGA_{24}$	5378	1396	454	$SEGA_{41}$	3083	1396
353	$SEGB_{7}$	7628	1396	404	$SEGB_{24}$	5333	1396	455	$SEGB_{41}$	3038	1396
354	$SEGC_{7}$	7583	1396	405	$SEGC_{24}$	5288	1396	456	$SEGC_{41}$	2993	1396
355	$SEGA_{8}$	7538	1396	406	$SEGA_{25}$	5243	1396	457	$SEGA_{42}$	2948	1396
356	$SEGB_{8}$	7493	1396	407	$SEGB_{25}$	5198	1396	458	$SEGB_{42}$	2903	1396
357	$SEGC_{8}$	7448	1396	408	$SEGC_{25}$	5153	1396	459	$SEGC_{42}$	2858	1396

■ PAD COORDINATES 4

Chip Size 19930μm x 3060μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X (μm)	Y (μm)	PAD No.	Terminal	X (μm)	Y (μm)
460	$SEGA_{43}$	2813	1396	511	$SEGA_{60}$	518	1396	562	$SEGA_{77}$	-1778	1396
461	$SEGB_{43}$	2768	1396	512	$SEGB_{60}$	473	1396	563	$SEGB_{77}$	-1823	1396
462	$SEGC_{43}$	2723	1396	513	$SEGC_{60}$	428	1396	564	$SEGC_{77}$	-1868	1396
463	$SEGA_{44}$	2678	1396	514	$SEGA_{61}$	383	1396	565	$SEGA_{78}$	-1913	1396
464	$SEGB_{44}$	2633	1396	515	$SEGB_{61}$	338	1396	566	$SEGB_{78}$	-1958	1396
465	$SEGC_{44}$	2588	1396	516	$SEGC_{61}$	293	1396	567	$SEGC_{78}$	-2003	1396
466	$SEGA_{45}$	2543	1396	517	$SEGA_{62}$	248	1396	568	$SEGA_{79}$	-2048	1396
467	$SEGB_{45}$	2498	1396	518	$SEGB_{62}$	203	1396	569	$SEGB_{79}$	-2093	1396
468	$SEGC_{45}$	2453	1396	519	$SEGC_{62}$	158	1396	570	$SEGC_{79}$	-2138	1396
469	$SEGA_{46}$	2408	1396	520	$SEGA_{63}$	113	1396	571	$SEGA_{80}$	-2183	1396
470	$SEGB_{46}$	2363	1396	521	$SEGB_{63}$	68	1396	572	$SEGB_{80}$	-2228	1396
471	$SEGC_{46}$	2318	1396	522	$SEGC_{63}$	23	1396	573	$SEGC_{80}$	-2273	1396
472	$SEGA_{47}$	2273	1396	523	$SEGA_{64}$	-23	1396	574	$SEGA_{81}$	-2318	1396
473	$SEGB_{47}$	2228	1396	524	$SEGB_{64}$	-68	1396	575	$SEGB_{81}$	-2363	1396
474	$SEGC_{47}$	2183	1396	525	$SEGC_{64}$	-113	1396	576	$SEGC_{81}$	-2408	1396
475	$SEGA_{48}$	2138	1396	526	$SEGA_{65}$	-158	1396	577	$SEGA_{82}$	-2453	1396
476	$SEGB_{48}$	2093	1396	527	$SEGB_{65}$	-203	1396	578	$SEGB_{82}$	-2498	1396
477	$SEGC_{48}$	2048	1396	528	$SEGC_{65}$	-248	1396	579	$SEGC_{82}$	-2543	1396
478	$SEGA_{49}$	2003	1396	529	$SEGA_{66}$	-293	1396	580	$SEGA_{83}$	-2588	1396
479	$SEGB_{49}$	1958	1396	530	$SEGB_{66}$	-338	1396	581	$SEGB_{83}$	-2633	1396
480	$SEGC_{49}$	1913	1396	531	$SEGC_{66}$	-383	1396	582	$SEGC_{83}$	-2678	1396
481	$SEGA_{50}$	1868	1396	532	$SEGA_{67}$	-428	1396	583	$SEGA_{84}$	-2723	1396
482	$SEGB_{50}$	1823	1396	533	$SEGB_{67}$	-473	1396	584	$SEGB_{84}$	-2768	1396
483	$SEGC_{50}$	1778	1396	534	$SEGC_{67}$	-518	1396	585	$SEGC_{84}$	-2813	1396
484	$SEGA_{51}$	1733	1396	535	$SEGA_{68}$	-563	1396	586	$SEGA_{85}$	-2858	1396
485	$SEGB_{51}$	1688	1396	536	$SEGB_{68}$	-608	1396	587	$SEGB_{85}$	-2903	1396
486	$SEGC_{51}$	1643	1396	537	$SEGC_{68}$	-653	1396	588	$SEGC_{85}$	-2948	1396
487	$SEGA_{52}$	1598	1396	538	$SEGA_{69}$	-698	1396	589	$SEGA_{86}$	-2993	1396
488	$SEGB_{52}$	1553	1396	539	$SEGB_{69}$	-743	1396	590	$SEGB_{86}$	-3038	1396
489	$SEGC_{52}$	1508	1396	540	$SEGC_{69}$	-788	1396	591	$SEGC_{86}$	-3083	1396
490	$SEGA_{53}$	1463	1396	541	$SEGA_{70}$	-833	1396	592	$SEGA_{87}$	-3128	1396
491	$SEGB_{53}$	1418	1396	542	$SEGB_{70}$	-878	1396	593	$SEGB_{87}$	-3173	1396
492	$SEGC_{53}$	1373	1396	543	$SEGC_{70}$	-923	1396	594	$SEGC_{87}$	-3218	1396
493	$SEGA_{54}$	1328	1396	544	$SEGA_{71}$	-968	1396	595	$SEGA_{88}$	-3263	1396
494	$SEGB_{54}$	1283	1396	545	$SEGB_{71}$	-1013	1396	596	$SEGB_{88}$	-3308	1396
495	$SEGC_{54}$	1238	1396	546	$SEGC_{71}$	-1058	1396	597	$SEGC_{88}$	-3353	1396
496	$SEGA_{55}$	1193	1396	547	$SEGA_{72}$	-1103	1396	598	$SEGA_{89}$	-3398	1396
497	$SEGB_{55}$	1148	1396	548	$SEGB_{72}$	-1148	1396	599	$SEGB_{89}$	-3443	1396
498	$SEGC_{55}$	1103	1396	549	$SEGC_{72}$	-1193	1396	600	$SEGC_{89}$	-3488	1396
499	$SEGA_{56}$	1058	1396	550	$SEGA_{73}$	-1238	1396	601	$SEGA_{90}$	-3533	1396
500	$SEGB_{56}$	1013	1396	551	$SEGB_{73}$	-1283	1396	602	$SEGB_{90}$	-3578	1396
501	$SEGC_{56}$	968	1396	552	$SEGC_{73}$	-1328	1396	603	$SEGC_{90}$	-3623	1396
502	$SEGA_{57}$	923	1396	553	$SEGA_{74}$	-1373	1396	604	$SEGA_{91}$	-3668	1396
503	$SEGB_{57}$	878	1396	554	$SEGB_{74}$	-1418	1396	605	$SEGB_{91}$	-3713	1396
504	$SEGC_{57}$	833	1396	555	$SEGC_{74}$	-1463	1396	606	$SEGC_{91}$	-3758	1396
505	$SEGA_{58}$	788	1396	556	$SEGA_{75}$	-1508	1396	607	$SEGA_{92}$	-3803	1396
506	$SEGB_{58}$	743	1396	557	$SEGB_{75}$	-1553	1396	608	$SEGB_{92}$	-3848	1396
507	$SEGC_{58}$	698	1396	558	$SEGC_{75}$	-1598	1396	609	$SEGC_{92}$	-3893	1396
508	$SEGA_{59}$	653	1396	559	$SEGA_{76}$	-1643	1396	610	$SEGA_{93}$	-3938	1396
509	$SEGB_{59}$	608	1396	560	$SEGB_{76}$	-1688	1396	611	$SEGB_{93}$	-3983	1396
510	$SEGC_{59}$	563	1396	561	$SEGC_{76}$	-1733	1396	612	$SEGC_{93}$	-4028	1396

■ PAD COORDINATES 5

Chip Size 19930μm x 3060μm (Chip Center 0μm x 0μm)

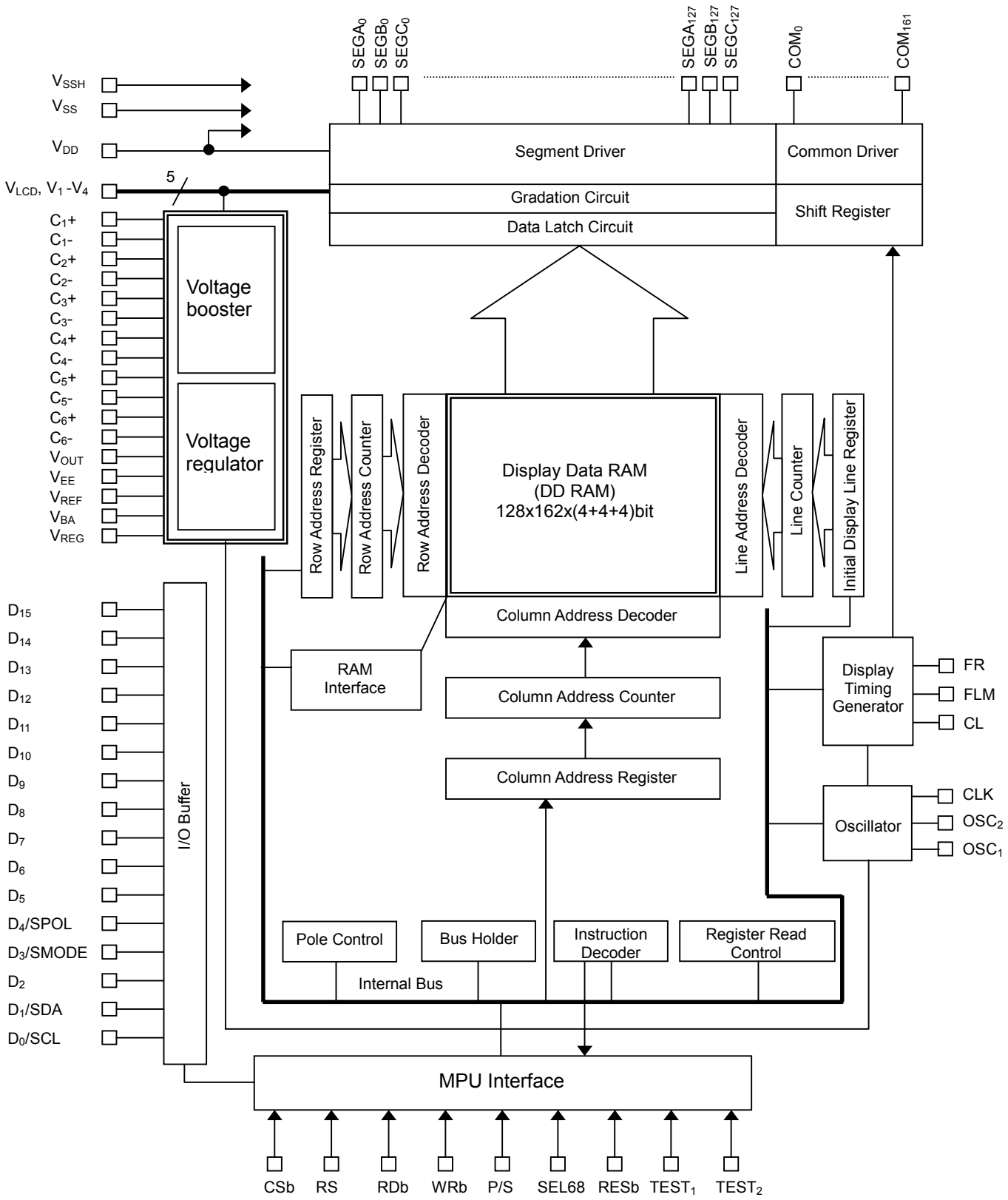
PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X (μm)	Y (μm)	PAD No.	Terminal	X (μm)	Y (μm)
613	$SEGA_{94}$	-4073	1396	664	$SEGA_{111}$	-6368	1396	715	COM_{81}	-8663	1396
614	$SEGB_{94}$	-4118	1396	665	$SEGB_{111}$	-6413	1396	716	COM_{82}	-8708	1396
615	$SEGC_{94}$	-4163	1396	666	$SEGC_{111}$	-6458	1396	717	COM_{83}	-8753	1396
616	$SEGA_{95}$	-4208	1396	667	$SEGA_{112}$	-6503	1396	718	COM_{84}	-8798	1396
617	$SEGB_{95}$	-4253	1396	668	$SEGB_{112}$	-6548	1396	719	COM_{85}	-8843	1396
618	$SEGC_{95}$	-4298	1396	669	$SEGC_{112}$	-6593	1396	720	COM_{86}	-8888	1396
619	$SEGA_{96}$	-4343	1396	670	$SEGA_{113}$	-6638	1396	721	COM_{87}	-8933	1396
620	$SEGB_{96}$	-4388	1396	671	$SEGB_{113}$	-6683	1396	722	COM_{88}	-8978	1396
621	$SEGC_{96}$	-4433	1396	672	$SEGC_{113}$	-6728	1396	723	COM_{89}	-9023	1396
622	$SEGA_{97}$	-4478	1396	673	$SEGA_{114}$	-6773	1396	724	COM_{90}	-9068	1396
623	$SEGB_{97}$	-4523	1396	674	$SEGB_{114}$	-6818	1396	725	COM_{91}	-9113	1396
624	$SEGC_{97}$	-4568	1396	675	$SEGC_{114}$	-6863	1396	726	COM_{92}	-9158	1396
625	$SEGA_{98}$	-4613	1396	676	$SEGA_{115}$	-6908	1396	727	COM_{93}	-9203	1396
626	$SEGB_{98}$	-4658	1396	677	$SEGB_{115}$	-6953	1396	728	COM_{94}	-9248	1396
627	$SEGC_{98}$	-4703	1396	678	$SEGC_{115}$	-6998	1396	729	COM_{95}	-9293	1396
628	$SEGA_{99}$	-4748	1396	679	$SEGA_{116}$	-7043	1396	730	COM_{96}	-9338	1396
629	$SEGB_{99}$	-4793	1396	680	$SEGB_{116}$	-7088	1396	731	COM_{97}	-9383	1396
630	$SEGC_{99}$	-4838	1396	681	$SEGC_{116}$	-7133	1396	732	COM_{98}	-9428	1396
631	$SEGA_{100}$	-4883	1396	682	$SEGA_{117}$	-7178	1396	733	COM_{99}	-9473	1396
632	$SEGB_{100}$	-4928	1396	683	$SEGB_{117}$	-7223	1396	734	COM_{100}	-9518	1396
633	$SEGC_{100}$	-4973	1396	684	$SEGC_{117}$	-7268	1396	735	DMY_{113}	-9581	1396
634	$SEGA_{101}$	-5018	1396	685	$SEGA_{118}$	-7313	1396	736	DMY_{114}	-9831	1143
635	$SEGB_{101}$	-5063	1396	686	$SEGB_{118}$	-7358	1396	737	COM_{101}	-9831	1080
636	$SEGC_{101}$	-5108	1396	687	$SEGC_{118}$	-7403	1396	738	COM_{102}	-9831	1035
637	$SEGA_{102}$	-5153	1396	688	$SEGA_{119}$	-7448	1396	739	COM_{103}	-9831	990
638	$SEGB_{102}$	-5198	1396	689	$SEGB_{119}$	-7493	1396	740	COM_{104}	-9831	945
639	$SEGC_{102}$	-5243	1396	690	$SEGC_{119}$	-7538	1396	741	COM_{105}	-9831	900
640	$SEGA_{103}$	-5288	1396	691	$SEGA_{120}$	-7583	1396	742	COM_{106}	-9831	855
641	$SEGB_{103}$	-5333	1396	692	$SEGB_{120}$	-7628	1396	743	COM_{107}	-9831	810
642	$SEGC_{103}$	-5378	1396	693	$SEGC_{120}$	-7673	1396	744	COM_{108}	-9831	765
643	$SEGA_{104}$	-5423	1396	694	$SEGA_{121}$	-7718	1396	745	COM_{109}	-9831	720
644	$SEGB_{104}$	-5468	1396	695	$SEGB_{121}$	-7763	1396	746	COM_{110}	-9831	675
645	$SEGC_{104}$	-5513	1396	696	$SEGC_{121}$	-7808	1396	747	COM_{111}	-9831	630
646	$SEGA_{105}$	-5558	1396	697	$SEGA_{122}$	-7853	1396	748	COM_{112}	-9831	585
647	$SEGB_{105}$	-5603	1396	698	$SEGB_{122}$	-7898	1396	749	COM_{113}	-9831	540
648	$SEGC_{105}$	-5648	1396	699	$SEGC_{122}$	-7943	1396	750	COM_{114}	-9831	495
649	$SEGA_{106}$	-5693	1396	700	$SEGA_{123}$	-7988	1396	751	COM_{115}	-9831	450
650	$SEGB_{106}$	-5738	1396	701	$SEGB_{123}$	-8033	1396	752	COM_{116}	-9831	405
651	$SEGC_{106}$	-5783	1396	702	$SEGC_{123}$	-8078	1396	753	COM_{117}	-9831	360
652	$SEGA_{107}$	-5828	1396	703	$SEGA_{124}$	-8123	1396	754	COM_{118}	-9831	315
653	$SEGB_{107}$	-5873	1396	704	$SEGB_{124}$	-8168	1396	755	COM_{119}	-9831	270
654	$SEGC_{107}$	-5918	1396	705	$SEGC_{124}$	-8213	1396	756	COM_{120}	-9831	225
655	$SEGA_{108}$	-5963	1396	706	$SEGA_{125}$	-8258	1396	757	COM_{121}	-9831	180
656	$SEGB_{108}$	-6008	1396	707	$SEGB_{125}$	-8303	1396	758	COM_{122}	-9831	135
657	$SEGC_{108}$	-6053	1396	708	$SEGC_{125}$	-8348	1396	759	COM_{123}	-9831	90
658	$SEGA_{109}$	-6098	1396	709	$SEGA_{126}$	-8393	1396	760	COM_{124}	-9831	45
659	$SEGB_{109}$	-6143	1396	710	$SEGB_{126}$	-8438	1396	761	COM_{125}	-9831	0
660	$SEGC_{109}$	-6188	1396	711	$SEGC_{126}$	-8483	1396	762	COM_{126}	-9831	-45
661	$SEGA_{110}$	-6233	1396	712	$SEGA_{127}$	-8528	1396	763	COM_{127}	-9831	-90
662	$SEGB_{110}$	-6278	1396	713	$SEGB_{127}$	-8573	1396	764	COM_{128}	-9831	-135
663	$SEGC_{110}$	-6323	1396	714	$SEGC_{127}$	-8618	1396	765	COM_{129}	-9831	-180

■ PAD COORDINATES 6

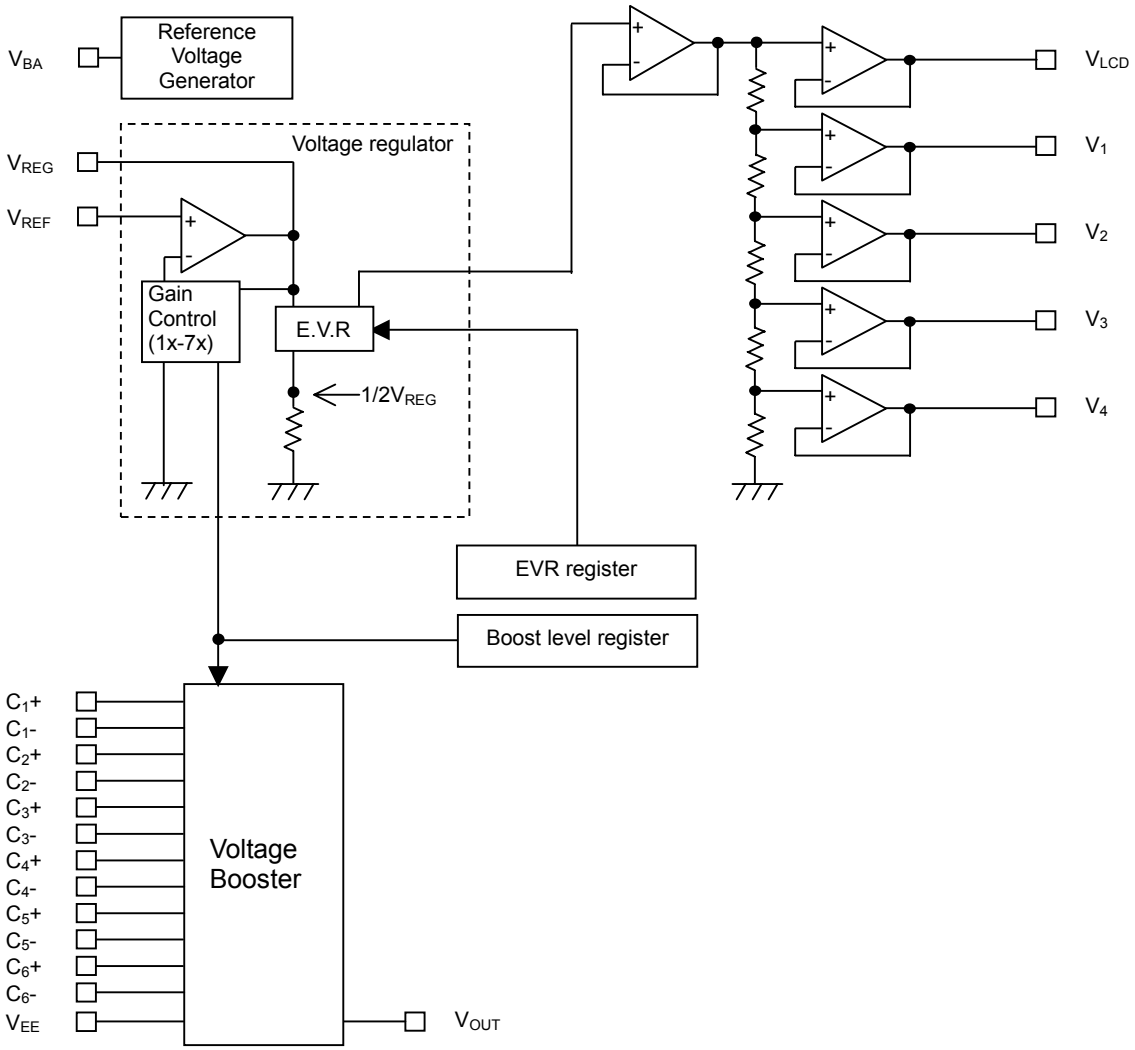
Chip Size 19930μm x 3060μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)
766	COM_{130}	-9831	-225
767	COM_{131}	-9831	-270
768	COM_{132}	-9831	-315
769	COM_{133}	-9831	-360
770	COM_{134}	-9831	-405
771	COM_{135}	-9831	-450
772	COM_{136}	-9831	-495
773	COM_{137}	-9831	-540
774	COM_{138}	-9831	-585
775	COM_{139}	-9831	-630
776	COM_{140}	-9831	-675
777	COM_{141}	-9831	-720
778	COM_{142}	-9831	-765
779	COM_{143}	-9831	-810
780	COM_{144}	-9831	-855
781	COM_{145}	-9831	-900
782	COM_{146}	-9831	-945
783	COM_{147}	-9831	-990
784	COM_{148}	-9831	-1035
785	COM_{149}	-9831	-1080
786	DMY_{115}	-9831	-1144

■ BLOCK DIAGRAM



■ POWER SUPPLY CIRCUITS BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Symbol	I/O	Function
30-32, 83-85	V_{DD}	Power	Power supply for logic circuits
50-52, 120-122	V_{SS}	Power	GND for logic circuits
143-145, 185-187	V_{SSH}	Power	GND for high voltage circuits
58-60	V_{DDA}	Power	This terminal is internally connected to the V_{DD} level. •This terminal is used to fix the selection terminals to the V_{DD} level. Note) Do not use this terminal for a main power supply.
16-18, 70-72	V_{SSA}	Power	This terminal is internally connected to the V_{SS} level. •This terminal is used to fix the selection terminals of the V_{SS} level. Note) Do not use this terminal for a main GND.
148-150, 151-153, 155-157, 158-160, 162-164	V_{LCD} V_1 V_2 V_3 V_4	Power/O	LCD driving voltages •When the internal voltage booster is not used, external LCD driving voltages (V_1 to V_4 and V_{LCD}) must be supplied on these terminals. The external voltages must be maintained with the following relation. $V_{SS}<V_4<V_3<V_2<V_1<V_{LCD}$ • When the internal voltage booster is used, the LCD driving voltages (V_1 to V_4 and V_{LCD}) are enabled by the "Power control" instruction. The capacitors between the V_{SS} and these terminals are necessary.
190-192, 194-196	C_1+ C_1-	O	Capacitor connection terminals for the voltage booster
198-200, 202-204	C_2+ C_2-	O	Capacitor connection terminals for the voltage booster
206-208, 210-212	C_3+ C_3-	O	Capacitor connection terminals or the voltage booster
214-216, 218-220	C_4+ C_4-	O	Capacitor connection terminals for the voltage booster
222-224, 226-228	C_5+ C_5-	O	Capacitor connection terminals for the voltage booster
230-232, 234-236	C_6+ C_6-	O	Capacitor connection terminals for the voltage booster
174-176	V_{BA}	O	Output of the reference-voltage generator
170-172	V_{REF}	I	Input of the Voltage regulator
180-182	V_{EE}	Power	Input of the Voltage booster input •This terminal is normally connected to the V_{DD} level.
242-244	V_{OUT}	Power/O	Output of the Voltage booster Input for high voltage circuits in using external power supply
165-167	V_{REG}	O	Output of the Voltage regulator
39	RESb	I	Reset Active "0"

■ TERMINAL DESCRIPTION 2

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>88</td><td>D_0/SCL</td><td>I/O</td><td rowspan="5">Parallel interface:
D_7 to D_0 : 8-bit bi-directional bus
•In the parallel interface mode (P/S="1"), these terminals connect to 8-bit bi-directional MPU bus.

Serial interface:
SDA : serial data
SCL : serial clock
SMODE : 3-/4-line serial interface mode selection
SPOL : RS polarity selection (in the 3-line serial interface mode)
•In the 3-/4-line serial interface mode (P/S="0"), the D0 terminal is assigned to the SCL and the D_1 terminal to the SDA.
•In the 3-line serial interface mode, the D_4 terminal is assigned to the SPOL.
•Serial data on the SDA is fetched at the rising edge of the SCL signal in the order of the D_7, D_6…D_0, and the fetched data is converted into 8-bit parallel data at the falling edge of the 8th SCL signal.
•The SCL signal must be set to "0" after data transmissions or during non-access.</td></tr>
<tr><td>90</td><td>D_1/SDA</td><td>I/O</td></tr>
<tr><td>94</td><td>D_3/SMODE</td><td>I/O</td></tr>
<tr><td>96</td><td>D_4/SPOL</td><td>I/O</td></tr>
<tr><td>92, 98,
100,102</td><td>D_2, D_5,
D_6, D_7</td><td>I/O</td></tr>
<tr><td>104,106,108,
110,112,114,
116,118</td><td>D_8, D_9, D_{10},
D_{11}, D_{12}, D_{13},
D_{14}, D_{15}</td><td>I/O</td><td>8-bit bi-directional bus
•In the 16-bit data bus mode, these terminals are assigned to the upper 8-bit data bus.
•In the serial interface mode or 8-bit data bus mode of the parallel interface, these terminals must be fixed to "1" or "0".</td></tr>
<tr><td>43</td><td>CSb</td><td>I</td><td>Chip select
Active "0"</td></tr>
<tr><td>47</td><td>RS</td><td>I</td><td>Resister select
•This signal distinguishes transferred data as an instruction or display data as follows.
<table>
<tr><td>RS</td><td>H</td><td>L</td></tr>
<tr><td>Distinct.</td><td>Instruction</td><td>Display data</td></tr>
</table></td></tr>
<tr><td>79</td><td>RDb (E)</td><td>I</td><td>80 series MPU interface (P/S="1", SEL68="0")
RDb signal. Active "0".

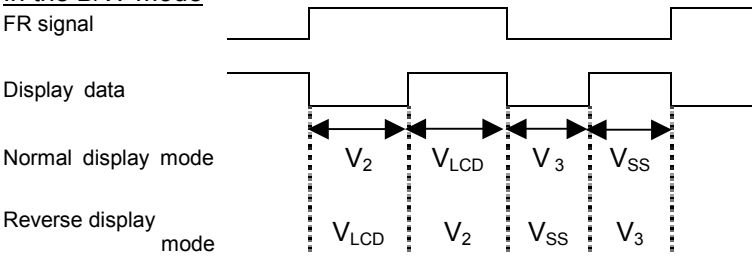
68 series MPU interface (P/S="1", SEL68="1")
Enable signal. Active "1".</td></tr>
<tr><td>75</td><td>WRb (R/W)</td><td>I</td><td>80 series MPU interface (P/S="1", SEL68="0")
WRb signal. Active "0".

68 series MPU interface (P/S="1", SEL68="1")
R/W signal.
<table>
<tr><td>R/W</td><td>H</td><td>L</td></tr>
<tr><td>Status</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
</table>

■ TERMINAL DESCRIPTION 3

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>67</td><td>SEL68</td><td>I</td><td>MPU interface type select
<table>
<tr><td>SEL68</td><td>H</td><td>L</td></tr>
<tr><td>Status</td><td>68 series</td><td>80 series</td></tr>
</table></td></tr>
<tr><td>63</td><td>P/S</td><td>I</td><td>Parallel / serial interface mode selection
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Instruction</td><td>Data</td><td>Read/Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>CSb</td><td>RS</td><td>D0 to D7</td><td>RDb, WRb</td><td>-</td></tr>
<tr><td>L</td><td>CSb</td><td>RS</td><td>SDA (D1)</td><td>Write only</td><td>SCL (D0)</td></tr>
</table>
•Since the D_{15} to D_5 and D_2 terminals are in the high impedance in the serial inter face mode (P/S=”0”), they must be fixed to “1” or “0”. The RDb and WRb terminals also must be “1” or “0”.</td></tr>
<tr><td>124</td><td>CL</td><td>I/O</td><td>This terminal must be opened.</td></tr>
<tr><td>127</td><td>FLM</td><td>I/O</td><td>This terminal must be opened.</td></tr>
<tr><td>130</td><td>FR</td><td>I/O</td><td>This terminal must be opened.</td></tr>
<tr><td>24</td><td>$TEST_1$</td><td>I</td><td>Maker test terminal
This terminal should be fixed to “0”.</td></tr>
<tr><td>55</td><td>$TEST_2$</td><td>I</td><td>Maker test terminal
This terminal must be fixed to “1”.</td></tr>
</table>

■ TERMINAL DESCRIPTION 4

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>331-714</td><td>$SEGA_0$ to $SEGA_{127}$,
$SEGB_0$ to $SEGB_{127}$,
$SEGC_0$ to $SEGC_{127}$</td><td>O</td><td>Segment output
<table><tr><th>REV Mode</th><th>Turn-off</th><th>Turn-on</th></tr><tr><td>Normal</td><td>0</td><td>1</td></tr><tr><td>Reverse</td><td>1</td><td>0</td></tr></table>•These terminals output LCD driving waveforms in accordance with the combination of the FR signal and display data.
<u>In the B/W mode</u>
  </td></tr>
<tr><td>311-330,
260-308,
246-257,
715-734,
737-785,
2-13</td><td>COM_0 to COM_{161}</td><td>O</td><td>Common output
•These terminals output LCD driving waveforms in accordance with the combination of the FR signal and scanning data.
<table><tr><th>Data</th><th>FR</th><th>Output level</th></tr><tr><td>H</td><td>H</td><td>V_{SS}</td></tr><tr><td>L</td><td>H</td><td>V_1</td></tr><tr><td>H</td><td>L</td><td>V_{LCD}</td></tr><tr><td>L</td><td>L</td><td>V_4</td></tr></table></td></tr>
<tr><td>137,
140</td><td>OSC_1
OSC_2</td><td>I
O</td><td>OSC
•When the internal oscillator clock is used, OSC_1 terminal must be fixed to “1” or “0”, and the OSC_2 terminal must be opened. When the oscillation frequency from the internal oscillator is adjusted by an external resistor between OSC_1 terminal and OSC_2
•When an external oscillator is used, external clock is input to the OSC_1 terminal or an external resistor is connected between the OSC_1 and OSC_2 terminals.</td></tr>
<tr><td>133</td><td>CLK</td><td>I/O</td><td>This terminal must be opened.</td></tr>
</table>

(Terminal No.14,15,20-23,25-29,33-38,40-42,44-46,48,49,53,54,56,57,61,62,64-66,68,69,73,74,76-78,80-82, 86,87,89,91,93,95,97,99,101,103,105,107,109,111,113,115,117,119,123,125,126,128,129,131,132,134-136, 138,139,141,142,146,147,154,161,168,169,173,177-179,183,184,188,189,193,197,201,205,209,213,217,221, 225,229,233,237-241,245,258,259,309,310,735,736, and 786 are dummy.)

■ Functional Description

(1) MPU Interface

(1-1) Selection of parallel / serial interface mode

The P/S terminal is used to select parallel or serial interface mode as shown in the following table. In the serial interface mode, it is not possible to read out display data from the DDRAM and status from the internal registers.

Table1

P/S	P/S mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D_7-D_0 (D_{15}-D_0)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

Note 1) " -" mark: Fix to "1" or "0".

(1-2) Selection of MPU interface type

In the parallel interface mode, the SEL68 terminal is used to select 68- or 80-series MPU interface type as shown in the following table.

Table2

SEL68	MPU type	CSb	RS	RDb	WRb	Data
H	68 series MPU	CSb	RS	E	R/W	D_7-D_0 (D_{15}-D_0)
L	80 series MPU	CSb	RS	RDb	WRb	D_7-D_0 (D_{15}-D_0)

(1-3) Data distinction

In the parallel interface mode, the combination of RS, RDb, and WRb (R/W) signals distinguishes transferred data between the LSI and MPU as instruction or display data, as shown in the following table.

Table3

RS	68 series	80 series		Function
	R/W	RDb	WRb	
H	H	L	H	Read out instruction data
H	L	H	L	Write instruction data
L	H	L	H	Read out display data
L	L	H	L	Write display data

(1-4) Selection of serial interface mode

In the serial interface mode, the SMODE terminal is used to select the 3- or 4-line serial interface mode as shown in the following table.

Table4

SMODE	Serial interface mode
H	3-line
L	4-line

(1-5) 4-line serial interface mode

In the 4-line serial interface mode, when the chip select is active (CSb="0"), the SDA and the SCL are enabled. When the chip select is not active (CSb="1"), the SDA and the SCL are disabled and the internal shift register and the counter are being initialized. The 8-bit serial data on the SDA is fetched at the rising edge of the SCL signal (serial clock) in order of the D_7, D_6…D_0, and the fetched data is converted into the 8-bit parallel data at the rising edge of the 8th SCL signal.

In the 4-line serial interface mode, the transferred data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS signal.

Table5

RS	Data distinction
H	Instruction data
L	Display data

Since the serial interface operation is sensitive to external noises, the SCL should be set to "0" after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb="1") after each of the 8-bit data transmissions. The following figure illustrates the interface timing for the 4-line serial interface operation.

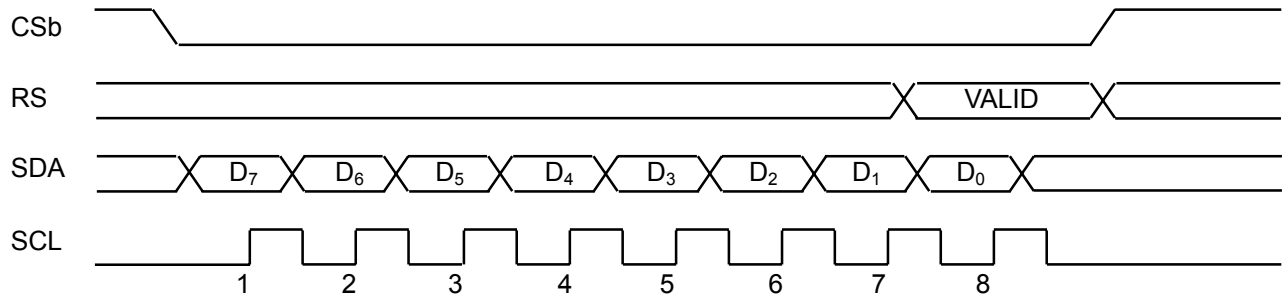


Fig1 4-line serial interface timing

(1-6) 3-line serial interface mode

In the 3-line serial interface mode, when the chip select is active (CSb="0"), the SDA and SCL are enabled. When the chip select is not active (CSb="1"), the SDA and SCL are disabled and the internal shift register and counter are being initialized. 9-bit serial data on the SDA is fetched at the rising edge of the SCL signal in order of the RS, D_7, D_6…D_0, and the fetched data is converted into the 9-bit parallel data at the rising edge of the 9th SCL signal.

In the 3-line serial interface mode, data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS bit of SDA data and the status of the SPOL, as follows.

Table6

SPOL=L		SPOL=H	
RS	Data distinction	RS	Data distinction
L	Display data	L	Instruction data
H	Instruction data	H	Display data

Since the serial interface operation is sensitive to external noises, the SCL must be set to “0” after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb=“1”) after each of 9-bit data transmissions. The following figure illustrates the interface timing of the 3-line serial interface operation.

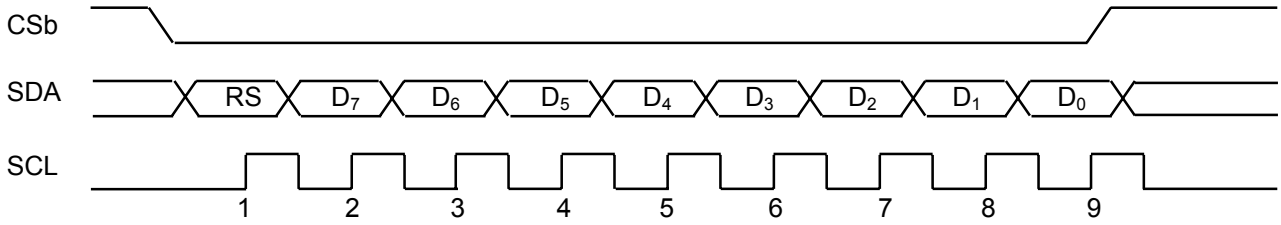


Fig2 3-line serial interface timing

(2) Access to the DDRAM

When the CSb signal is ”0”, the transferred data from MPU is written into the DDRAM or instruction register in accordance with the condition of the RS signal.

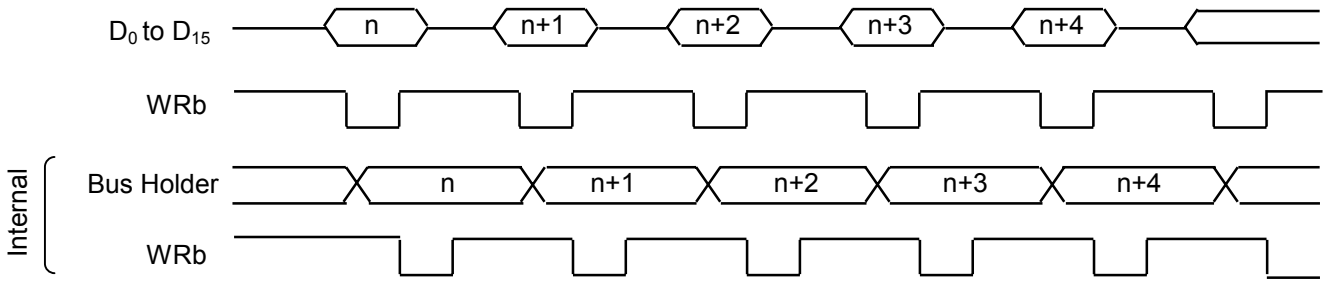
When the RS signal is “1”, the transferred data is distinguished as display data. After the “column address” and “row address” instructions are executed, the display data can be written into the DDRAM by the “display data write” instruction. The display data is written at the rising edge of the WRb signal in the 80 series MPU mode, or at the falling edge of the E signal in the 68 series MPU mode.

Table6

RS	Data
L	Display RAM Data
H	Internal Command Register

In the sequence of the “display data read” operation, the transferred data from MPU is temporarily held in the internal bus-holder, and then transferred to the internal data-bus. When the “display data read” operation is executed just after the “column address” and “row address” instructions or “display data write” instruction, unexpected data on the bus-holder is read out at the 1st execution, then the data of designated DDRAM address is read out from the 2nd execution. For this reason, a dummy read cycle must be executed to avoid the unexpected 1st data read.

Display data write operation



Display data read operation

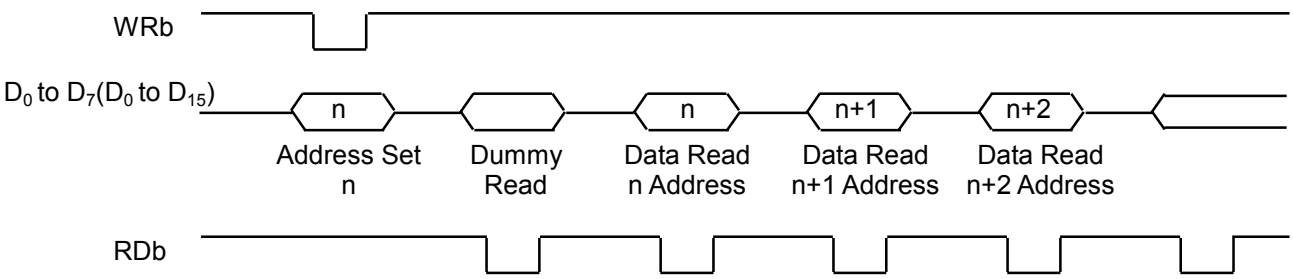


Fig3

Note) In the16-bit data bus mode, instruction data must be 16-bit as well as the display data.

(3) Access to the instruction register

Each instruction resisters is assigned to each address between 0_H and F_H, and the content of the instruction register can be read out by the combination of the “Instruction resister address” and ”Instruction resister read”.

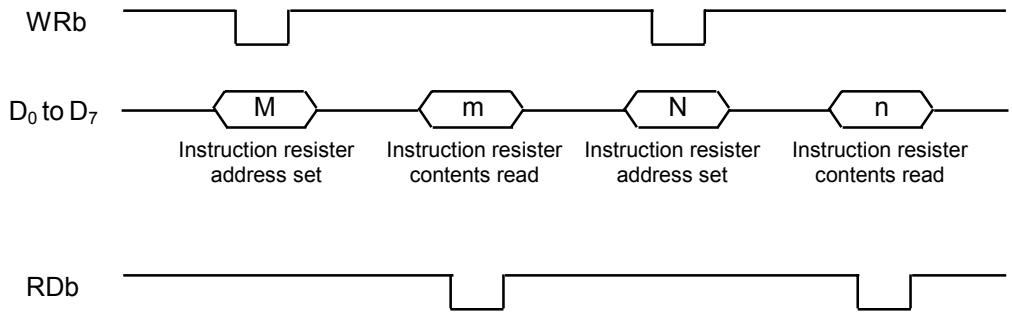


Fig4

(4) 8-/16-bit data bus length for display data (in the parallel interface mode)

The 8- or 16-bit data bus length for display data is determined by the “WLS” of the “Data bus length” instruction.

In the 16-bit data bus mode, instruction data must be 16-bit data (D_{15} to D_0) as well as display data. However, for the access to the instruction register, the only lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

Table8

WLS	Data bus length mode
L	8-bit
H	16-bit

(5) Initial display line register

The initial display line resister specifies the line address, corresponding to the initial COM line, by the “Initial display line” instruction. The initial COM line signifies the common driver, starting scanning the display data in the DDRAM, and specified by the “Initial COM line” instruction.

The line address, established in the initial display line resister, is preset into the line counter whenever the FLM signal becomes “1”. At the rising edge of the CL signal, the line counter is counted-up and addressed 384-bit display data corresponding to the counted-up line address, is latched into the data latch circuit. At the falling edge of the CL signal, the latched data outputs to the segment drivers.

(6) DDRAM mapping

The DDRAM is capable of 1,536-bit (12-bit x 128-segment) for the column address and 162-bit for the row address.

In the gradation mode, each pixel for RGB corresponds to successive 3-segment drivers, and each segment driver has 16-gradation. Therefore, the LSI can drive up to 128x162 pixels in 4096-color display (16-gradation x 16-gradation x 16-gradation).

- In the 8-bit data bus length mode

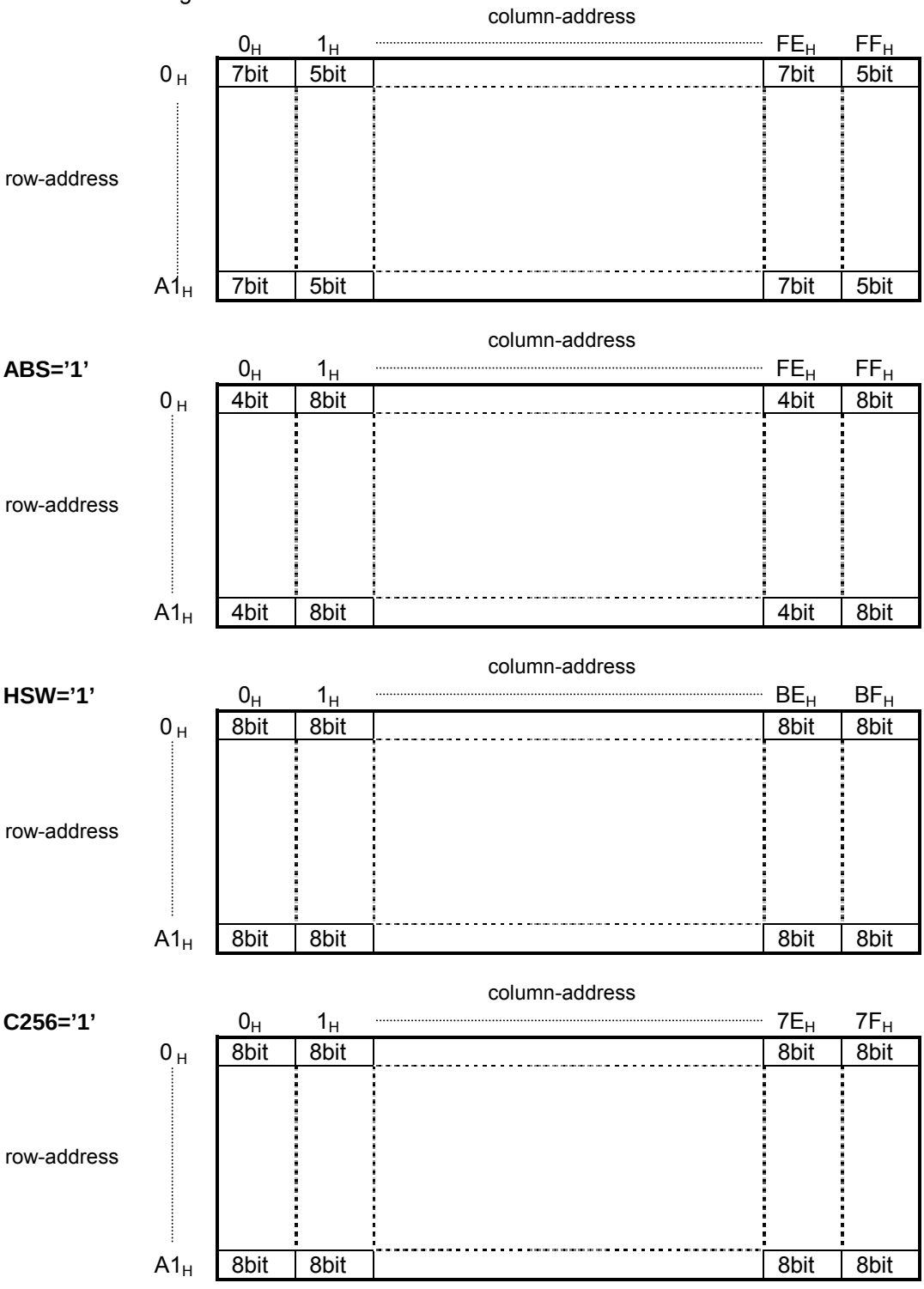


Fig5

- In the 16-bit data bus length mode

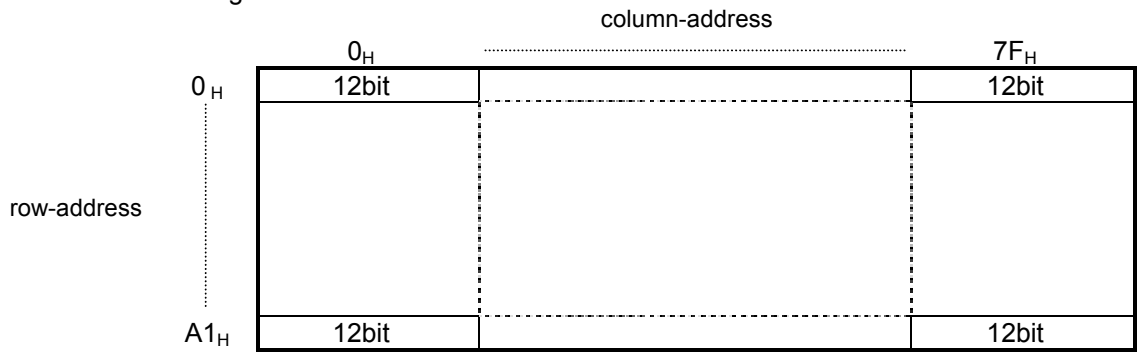


Fig6

In the B&W mode, only MSB data from each 4-bit display data group in the DDRAM is used. Therefore, 384 x 162 pixels in the B&W and 128 x 162 pixels in the 8-gradation are available.

The range of the column address varies depending on data bus length. The range between 00_H and FF_H is used in the 8-bit data bus length and the range between 00_H and $7F_H$ is in the 16-bit data bus length.

The increments for the column address and row address are set to the auto-increment mode by programming the “AXI” and “AYI” registers of the “Increment control” instruction. In this mode, the contents of the column address and row address counters automatically increment whenever the DDRAM is accessed.

The column address and row address counters, independent of the line counter. They are used to designate the column and row addresses for the display data transferred from MPU. On the other hand, the line counter is used to generate the line address, and output display data to the segment drivers, being synchronized with the display control timing of the FLM and CL signals.

RAM Map 1

Mode	WLS	ABS	HSW	REF	256	SEG0				SEG1					SEG126				SEG127			
						Palette A	Palette B	Palette C		Palette A	Palette B	Palette C			Palette A	Palette B	Palette C		Palette A	Palette B	Palette C	
						A3 A2 A1 A0	B3 B2 B1 B0	C3 C2 C1 C0		A3 A2 A1 A0	B3 B2 B1 B0	C3 C2 C1 C0			A3 A2 A1 A0	B3 B2 B1 B0	C3 C2 C1 C0		A3 A2 A1 A0	B3 B2 B1 B0	C3 C2 C1 C0	
16bit	1	0	X	0	0	X=00H				X=01H					X=7EH				X=7FH			
						D15 D14 D13 D12	D10 D9 D8 D7	D4 D3 D2 D1		D15 D14 D13 D12	D10 D9 D8 D7	D4 D3 D2 D1			D15 D14 D13 D12	D10 D9 D8 D7	D4 D3 D2 D1		D15 D14 D13 D12	D10 D9 D8 D7	D4 D3 D2 D1	
	1	0	X	1	0	X=7FH				X=7EH					X=01H				X=00H			
						D15 D14 D13 D12	D10 D9 D8 D7	D4 D3 D2 D1		D15 D14 D13 D12	D10 D9 D8 D7	D4 D3 D2 D1			D15 D14 D13 D12	D10 D9 D8 D7	D4 D3 D2 D1		D15 D14 D13 D12	D10 D9 D8 D7	D4 D3 D2 D1	
	1	1	X	0	0	X=00H				X=01H					X=7EH				X=7FH			
						D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0		D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0			D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0		D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0	
	1	1	X	1	0	X=7FH				X=7EH					X=01H				X=00H			
						D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0		D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0			D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0		D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0	
8bit	0	0	0	0	0	X=00H		X=01H		X=02H		X=03H			X=FCH		X=FDH		X=FEH		X=FFH	
						D7 D6 D5 D4	D2 D1 D0	D7 D4 D3 D2 D1		D7 D6 D5 D4	D2 D1 D0	D7 D4 D3 D2 D1			D7 D6 D5 D4	D2 D1 D0	D7 D4 D3 D2 D1		D7 D6 D5 D4	D2 D1 D0	D7 D4 D3 D2 D1	
	0	0	0	1	0	X=FEH		X=FFH		X=FCH		X=FDH			X=02H		X=03H		X=00H		X=01H	
						D7 D6 D5 D4	D2 D1 D0	D7 D4 D3 D2 D1		D7 D6 D5 D4	D2 D1 D0	D7 D4 D3 D2 D1			D7 D6 D5 D4	D2 D1 D0	D7 D4 D3 D2 D1		D7 D6 D5 D4	D2 D1 D0	D7 D4 D3 D2 D1	
	0	1	0	0	0	X=00H		X=01H		X=02H		X=03H			X=FCH		X=FDH		X=FEH		X=FFH	
						D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0		D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0			D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0		D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	
	0	1	0	1	0	X=FEH		X=FFH		X=FCH		X=FDH			X=02H		X=03H		X=00H		X=01H	
						D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0		D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0			D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0		D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	
	0	X	1	0	0	X=00H		X=01H		X=02H					X=BDH		X=BEH		X=BFH			
						D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4		D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0			D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4		D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	
	0	X	1	1	0	X=BEH(L)		X=BFH		X=BDH		X=BEH(H)			X=01H(L)		X=02H		X=00H		X=01H(H)	
						D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0		D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4			D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0		D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	

RAM Map 2 (256 Color Mode)

Mode	WLS	ABS	HSW	REF	256	SEG0				SEG1					SEG126				SEG127			
						Palette A	Palette B	Palette C		Palette A	Palette B	Palette C			Palette A	Palette B	Palette C		Palette A	Palette B	Palette C	
						A3 A2 A1 A0	B3 B2 B1 B0	C3 C2 C1 C0		A3 A2 A1 A0	B3 B2 B1 B0	C3 C2 C1 C0			A3 A2 A1 A0	B3 B2 B1 B0	C3 C2 C1 C0		A3 A2 A1 A0	B3 B2 B1 B0	C3 C2 C1 C0	
						↗	↗	↗		↗	↗	↗			↗	↗	↗		↗	↗	↗	
8bit	0	X	X	0	1	X=00H				X=01H					X=7EH				X=7FH			
						- - - -	D7 D6 D5 D4	D3 D2 D1 D0		- - - -	D7 D6 D5 D4	D3 D2 D1 D0			- - - -	D7 D6 D5 D4	D3 D2 D1 D0		- - - -	D7 D6 D5 D4	D3 D2 D1 D0	
	0	X	X	1	1	X=7FH				X=7EH					X=01H				X=00H			
						- - - -	D7 D6 D5 D4	D3 D2 D1 D0		- - - -	D7 D6 D5 D4	D3 D2 D1 D0			- - - -	D7 D6 D5 D4	D3 D2 D1 D0		- - - -	D7 D6 D5 D4	D3 D2 D1 D0	

SWAP

REF	SWAP	Palette A				Palette B				Palette C			
		A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
0	0	SEGAx				SEGBx				SEGCx			
1	1												
0	1	SEGCx				SEGBx				SEGAx			
1	0												

Note1) In the 256-color mode, the vacant LSB bit is filled with "1".
Note2) The function of 256-color mode is different from that of fixed 8-gradation mode (fixed 256-color mode).
Note3) The written data in the DD RAM in "C256"=0 is not compatible with the data in "C256"=1.
Note4) In the 256-color mode, only 8-bit length mode is available, but 16-bit is not.

(7) Window addressing mode

In addition to the above usual DDRAM addressing, it is possible to access some part of DDRAM in using the window addressing mode, in which the start and end points are designated. The start point is determined by the "column address" and "row address" instructions, and the end point is determined by the "Window end column address" and "Window end row address" instructions, The setting example of the window addressing is listed, as follows.

.

1. Set WIN=1, AXI=1 and AYI=1 by the "Increment control" instruction
2. Set the start point by the "column address" and "row address" instructions
3. Set the end point by the "Window end column address" and "Window end row address" instructions
4. Enable to access to the DDRAM in the window addressing mode

In the window addressing mode (WIN=1, AXI=1, AYI=1), the read-modify-write operation is available by setting "0" to the "AIM" register of the "Increment control" instruction.

And in the window addressing mode, the following start and end point must be maintained to abide a malfunction.

AX (column address of start point) $\leq$ EX (column address of end point) $\leq$ Maximum of column address
AY (row address of start point) $\leq$ EY (row address of end point) $\leq$ Maximum of row address

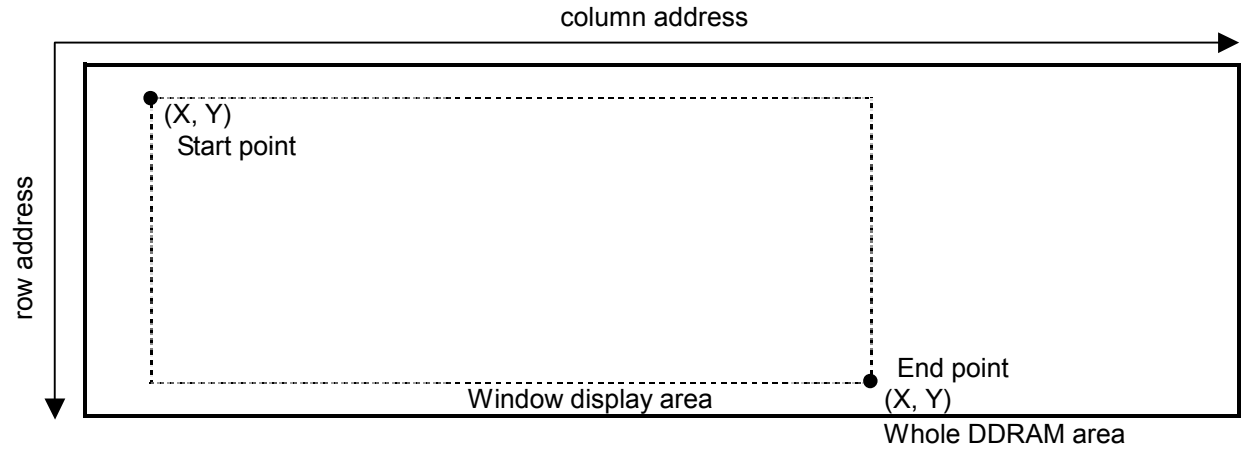


Fig7

(8) Reverse display ON/OFF

The "Reverse display ON/OFF" function is used to reverse the display data without changing the contents of the DDRAM.

Table9

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(9) Segment direction

The "Segment direction" function is used to reverse the assignment for the segment drivers and column address, and it is possible to reduce the restrictions for the placement of the LSI on the LCD modules.

(10) The relationship among the DDRAM column address, display data and segment drivers

In the Color mode, and 16-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign		
*	0	0	0	$X=00_H$	←→	$X=7F_H$
*	0	1	1	$X=7F_H$	←→	$X=00_H$

D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
palette A				palette B				palette C				←→	palette A				palette B				palette C			
$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column address / bit / segment assign		
*	0	0	1	$X=00_H$	←→	$X=7F_H$
*	0	1	0	$X=7F_H$	←→	$X=00_H$

D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
palette A				palette B				palette C				←→	palette A				palette B				palette C			
$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP	Column address / bit / segment assign		
*	1	0	0	$X=00_H$	←→	$X=7F_H$
*	1	1	1	$X=7F_H$	←→	$X=00_H$

D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
palette A				palette B				palette C				←→	palette A				palette B				palette C			
$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column address / bit / segment assign		
*	1	0	1	$X=00_H$	←→	$X=7F_H$
*	1	1	0	$X=7F_H$	←→	$X=00_H$

D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
palette A				palette B				palette C				←→	palette A				palette B				palette C			
$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

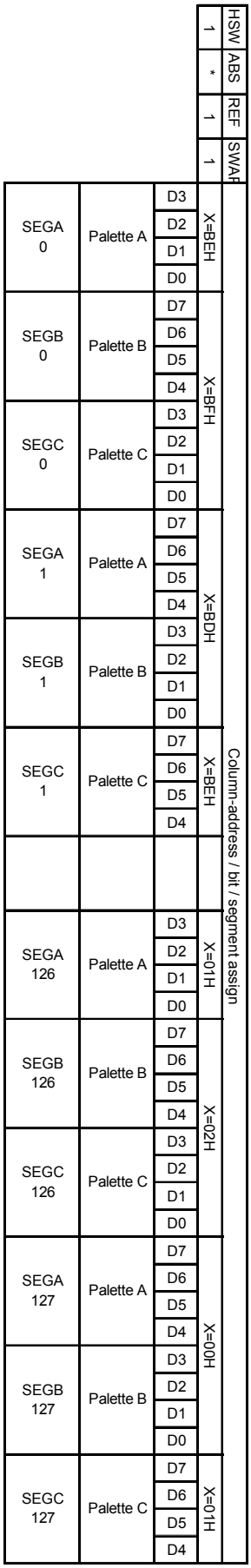
In the Color mode, and 8-bit data bus mode

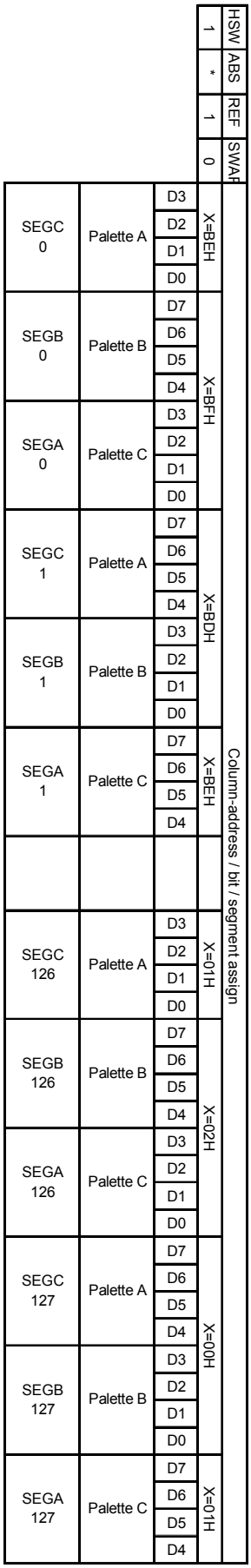
HSW	ABS	REF	SWAP	Column address / bit / segment assign																											
0	0	0	0	X=00_H							X=01_H					↔	X=FE_H							X=FF_H							
0	0	1	1	X=FE_H							X=FF_H					↔	X=00_H							X=01_H							
				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	↔	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1					
				palette A				palette B			palette C					↔	palette A				palette B			palette C								
				$SEGA_0$				$SEGB_0$			$SEGC_0$					↔	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$								

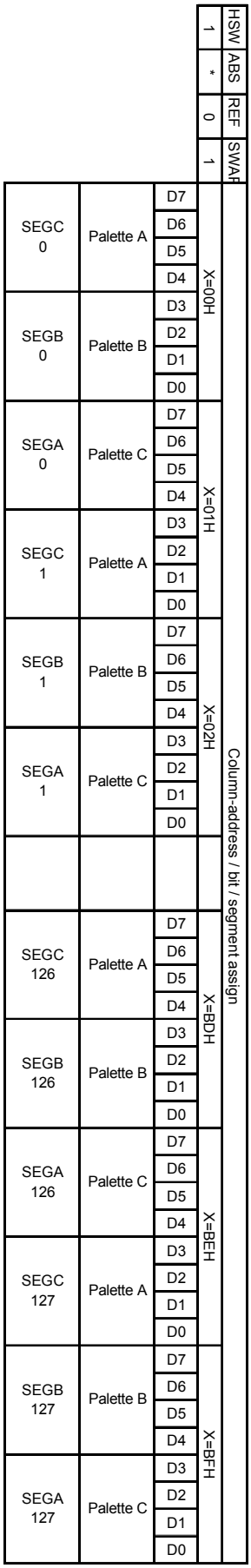
HSW	ABS	REF	SWAP	Column address / bit / segment assign																											
0	0	0	1	X=00_H							X=01_H					↔	X=FE_H							X=FF_H							
0	0	1	0	X=FE_H							X=FF_H					↔	X=00_H							X=01_H							
				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	↔	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1					
				palette A				palette B			palette C					↔	palette A				palette B			palette C								
				$SEGC_0$				$SEGB_0$			$SEGA_0$					↔	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$								

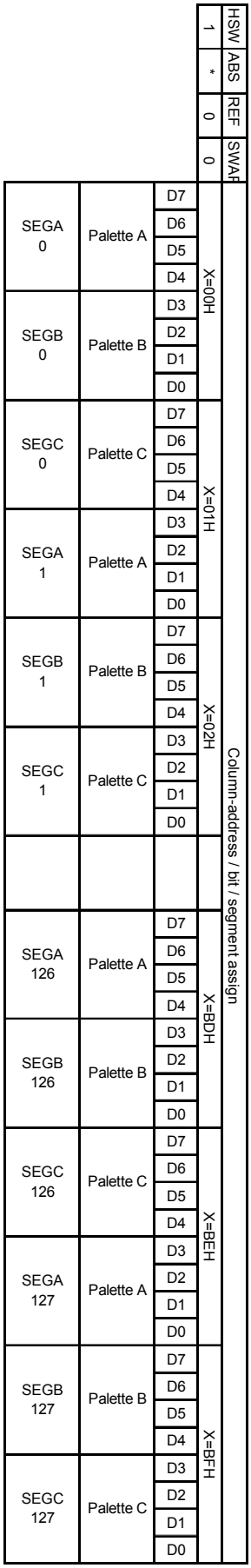
HSW	ABS	REF	SWAP	Column address / bit / segment assign																											
0	1	0	0	X=00_H							X=01_H					↔	X=FE_H							X=FF_H							
0	1	1	1	X=FE_H							X=FF_H					↔	X=00_H							X=01_H							
				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	↔	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0					
				palette A				palette B			palette C					↔	palette A				palette B			palette C								
				$SEGA_0$				$SEGB_0$			$SEGC_0$					↔	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$								

HSW	ABS	REF	SWAP	Column address / bit / segment assign																											
0	1	0	1	X=00_H							X=01_H					↔	X=FE_H							X=FF_H							
0	1	1	0	X=FE_H							X=FF_H					↔	X=00_H							X=01_H							
				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	↔	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0					
				palette A				palette B			palette C					↔	palette A				palette B			palette C								
				$SEGC_0$				$SEGB_0$			$SEGA_0$					↔	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$								


HSW 1
ABS *
REF 1
SWAP 1
SEGA 0 Palette A D3 D2 D1 D0 X=BEH
SEGB 0 Palette B D7 D6 D5 D4
SEGC 0 Palette C D3 D2 D1 D0 X=BFH
SEGA 1 Palette A D7 D6 D5 D4 X=BDH
SEGB 1 Palette B D3 D2 D1 D0
SEGC 1 Palette C D7 D6 D5 D4 X=BEH
SEGA 126 Palette A D3 D2 D1 D0 X=01H
SEGB 126 Palette B D7 D6 D5 D4 X=02H
SEGC 126 Palette C D3 D2 D1 D0
SEGA 127 Palette A D7 D6 D5 D4 X=00H
SEGB 127 Palette B D3 D2 D1 D0
SEGC 127 Palette C D7 D6 D5 D4 X=01H
Column-address / bit / segment assign


HSW 1
ABS *
REF 1
SWAP 0
SEGC 0 Palette A D3 D2 D1 D0 X=BEH
SEGB 0 Palette B D7 D6 D5 D4
SEGA 0 Palette C D3 D2 D1 D0 X=BFH
SEGC 1 Palette A D7 D6 D5 D4 X=BDH
SEGB 1 Palette B D3 D2 D1 D0
SEGA 1 Palette C D7 D6 D5 D4 X=BEH
SEGC 126 Palette A D3 D2 D1 D0 X=01H
SEGB 126 Palette B D7 D6 D5 D4 X=02H
SEGA 126 Palette C D3 D2 D1 D0
SEGC 127 Palette A D7 D6 D5 D4 X=00H
SEGB 127 Palette B D3 D2 D1 D0
SEGA 127 Palette C D7 D6 D5 D4 X=01H
Column-address / bit / segment assign


HSW 1
ABS *
REF 0
SWAP 1
SEGC 0 Palette A D7 D6 D5 D4 X=00H
SEGB 0 Palette B D3 D2 D1 D0
SEGA 0 Palette C D7 D6 D5 D4 X=01H
SEGC 1 Palette A D3 D2 D1 D0
SEGB 1 Palette B D7 D6 D5 D4 X=02H
SEGA 1 Palette C D3 D2 D1 D0
SEGC 126 Palette A D7 D6 D5 D4 X=BDH
SEGB 126 Palette B D3 D2 D1 D0
SEGA 126 Palette C D7 D6 D5 D4 X=BEH
SEGC 127 Palette A D3 D2 D1 D0
SEGB 127 Palette B D7 D6 D5 D4 X=BFH
SEGA 127 Palette C D3 D2 D1 D0
Column-address / bit / segment assign


HSW 1
ABS *
REF 0
SWAP 0
SEGA 0 Palette A D7 D6 D5 D4 X=00H
SEGB 0 Palette B D3 D2 D1 D0
SEGC 0 Palette C D7 D6 D5 D4 X=01H
SEGA 1 Palette A D3 D2 D1 D0
SEGB 1 Palette B D7 D6 D5 D4 X=02H
SEGC 1 Palette C D3 D2 D1 D0
SEGA 126 Palette A D7 D6 D5 D4 X=BDH
SEGB 126 Palette B D3 D2 D1 D0
SEGC 126 Palette C D7 D6 D5 D4 X=BEH
SEGA 127 Palette A D3 D2 D1 D0
SEGB 127 Palette B D7 D6 D5 D4 X=BFH
SEGC 127 Palette C D3 D2 D1 D0
Column-address / bit / segment assign

In the Color mode, 8-bit data bus mode, and C256 mode (C256=1)

HSW	ABS	REF	SWAP	Column address / bit / segment assign															
*	*	0	0	X=00$_H$								←→	X=7F$_H$						
*	*	1	1	X=7F$_H$								←→	X=00$_H$						
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
				palette A			palette B			palette C		←→	palette A			palette B			palette C	
				$SEGA_0$			$SEGB_0$			$SEGC_0$		←→	$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$	

HSW	ABS	REF	SWAP	Column address / bit / segment assign															
*	*	0	1	X=00$_H$								←→	X=7F$_H$						
*	*	1	0	X=7F$_H$								←→	X=00$_H$						
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
				palette A			palette B			palette C		←→	palette A			palette B			palette C	
				$SEGC_0$			$SEGB_0$			$SEGA_0$		←→	$SEGC_{127}$			$SEGB_{127}$			$SEGA_{127}$	

In the B&W mode, and 16-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign
*	0	0	0	$X=00_H$ ←→ $X=7F_H$
*	0	1	1	$X=7F_H$ ←→ $X=00_H$

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$X=00_H$	$SEGA_0$					$SEGB_0$						$SEGC_0$				
←→																
$X=7F_H$	$SEGA_{127}$					$SEGB_{127}$						$SEGC_{127}$				

HSW	ABS	REF	SWAP	Column address / bit / segment assign
*	0	0	1	$X=00_H$ ←→ $X=7F_H$
*	0	1	0	$X=7F_H$ ←→ $X=00_H$

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$X=00_H$	$SEGC_0$					$SEGB_0$						$SEGA_0$				
←→																
$X=7F_H$	$SEGC_{127}$					$SEGB_{127}$						$SEGA_{127}$				

HSW	ABS	REF	SWAP	Column address / bit / segment assign
*	1	0	0	$X=00_H$ ←→ $X=7F_H$
*	1	1	1	$X=7F_H$ ←→ $X=00_H$

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$X=00_H$					$SEGA_0$				$SEGB_0$				$SEGC_0$			
←→																
$X=7F_H$					$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column address / bit / segment assign
*	1	0	1	$X=00_H$ ←→ $X=7F_H$
*	1	1	0	$X=7F_H$ ←→ $X=00_H$

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$X=00_H$					$SEGC_0$				$SEGB_0$				$SEGA_0$			
←→																
$X=7F_H$					$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

In the B&W mode, and 8-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign																							
0	0	0	0	$X=00_H$							$X=01_H$					←→	$X=FE_H$							$X=FF_H$			
0	0	1	1	$X=FE_H$							$X=FF_H$					←→	$X=00_H$							$X=01_H$			
				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	←→	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
				$SEGA_0$				$SEGB_0$			$SEGC_0$					←→	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$				

HSW	ABS	REF	SWAP	Column address / bit / segment assign																							
0	0	0	1	$X=00_H$							$X=01_H$					←→	$X=FE_H$							$X=FF_H$			
0	0	1	0	$X=FE_H$							$X=FF_H$					←→	$X=00_H$							$X=01_H$			
				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	←→	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
				$SEGC_0$				$SEGB_0$			$SEGA_0$					←→	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$				

HSW	ABS	REF	SWAP	Column address / bit / segment assign																							
0	1	0	0	$X=00_H$							$X=01_H$					←→	$X=FE_H$							$X=FF_H$			
0	1	1	1	$X=FE_H$							$X=FF_H$					←→	$X=00_H$							$X=01_H$			
				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
				$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																							
0	1	0	1	$X=00_H$							$X=01_H$					←→	$X=FE_H$							$X=FF_H$			
0	1	1	0	$X=FE_H$							$X=FF_H$					←→	$X=00_H$							$X=01_H$			
				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
				$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP			
1	*	0	0			
SEGA 0	D7	X=00H	Column-address / bit / segment assign			
	D6					
	D5					
	D4					
SEGB 0	D3					
	D2					
	D1					
	D0					
SEGC 0	D7	X=01H				
	D6					
	D5					
	D4					
SEGA 1	D3					
	D2					
	D1					
	D0					
SEGB 1	D7	X=02H				
	D6					
	D5					
	D4					
SEGC 1	D3					
	D2					
	D1					
	D0					
SEGA 126	D7	X=BDH				
	D6					
	D5					
	D4					
SEGB 126	D3					
	D2					
	D1					
	D0					
SEGC 126	D7	X=BEH				
	D6					
	D5					
	D4					
SEGA 127	D3					
	D2					
	D1					
	D0					
SEGB 127	D7	X=BFH				
	D6					
	D5					
	D4					
SEGC 127	D3					
	D2					
	D1					
	D0					

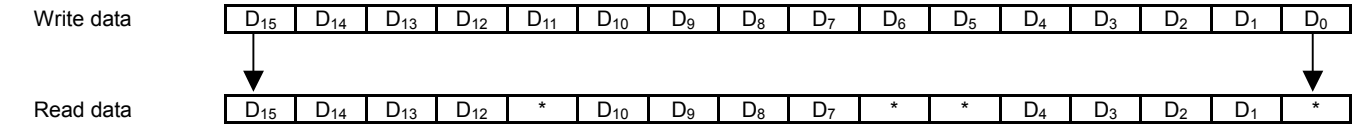
HSW	ABS	REF	SWAP			
1	*	1	1			
SEGC 0	D7	X=00H	Column-address / bit / segment assign			
	D6					
	D5					
	D4					
SEGB 0	D3					
	D2					
	D1					
	D0					
SEGA 0	D7	X=01H				
	D6					
	D5					
	D4					
SEGC 1	D3					
	D2					
	D1					
	D0					
SEGB 1	D7	X=02H				
	D6					
	D5					
	D4					
SEGA 1	D3					
	D2					
	D1					
	D0					
SEGC 126	D7	X=BDH				
	D6					
	D5					
	D4					
SEGB 126	D3					
	D2					
	D1					
	D0					
SEGA 126	D7	X=BEH				
	D6					
	D5					
	D4					
SEGC 127	D3					
	D2					
	D1					
	D0					
SEGB 127	D7	X=BFH				
	D6					
	D5					
	D4					
SEGA 127	D3					
	D2					
	D1					
	D0					

HSW	ABS	REF	SWAP			
1	*	1	0			
SEGC 0	D3	X=BEH	Column-address / bit / segment assign			
	D2					
	D1					
	D0					
SEGB 0	D7	X=BFH				
	D6					
	D5					
	D4					
SEGA 0	D3					
	D2					
	D1					
	D0					
SEGC 1	D7	X=BDH				
	D6					
	D5					
	D4					
SEGB 1	D3					
	D2					
	D1					
	D0					
SEGA 1	D7	X=BEH				
	D6					
	D5					
	D4					
SEGC 126	D3	X=01H				
	D2					
	D1					
	D0					
SEGB 126	D7	X=02H				
	D6					
	D5					
	D4					
SEGA 126	D3					
	D2					
	D1					
	D0					
SEGC 127	D7	X=00H				
	D6					
	D5					
	D4					
SEGB 127	D3					
	D2					
	D1					
	D0					
SEGA 127	D7	X=01H				
	D6					
	D5					
	D4					

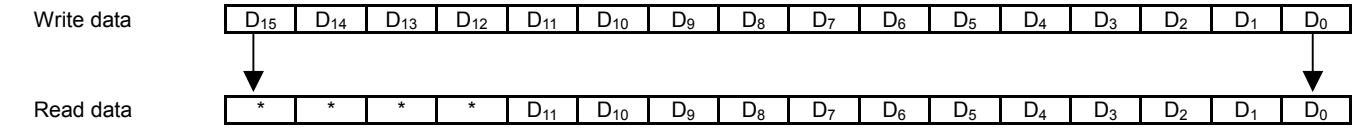
HSW	ABS	REF	SWAP			
1	*	1	1			
SEGA 0	D3	X=BEH	Column-address / bit / segment assign			
	D2					
	D1					
	D0					
SEGB 0	D7	X=BFH				
	D6					
	D5					
	D4					
SEGC 0	D3					
	D2					
	D1					
	D0					
SEGA 1	D7	X=BDH				
	D6					
	D5					
	D4					
SEGB 1	D3					
	D2					
	D1					
	D0					
SEGC 1	D7	X=BEH				
	D6					
	D5					
	D4					
SEGA 126	D3	X=01H				
	D2					
	D1					
	D0					
SEGB 126	D7	X=02H				
	D6					
	D5					
	D4					
SEGC 126	D3					
	D2					
	D1					
	D0					
SEGA 127	D7	X=00H				
	D6					
	D5					
	D4					
SEGB 127	D3					
	D2					
	D1					
	D0					
SEGC 127	D7	X=01H				
	D6					
	D5					
	D4					

Bit assignments between write and read data (in the 16-bit data bus mode)

ABS=0

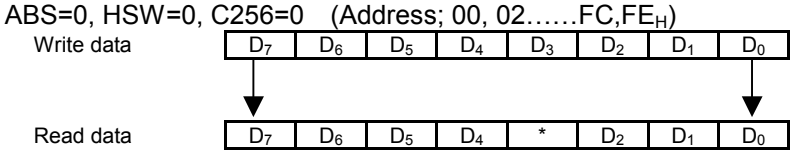


ABS=1

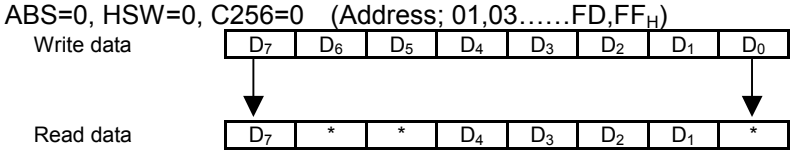


Examples of write and read data (In the 8 bit bus mode)

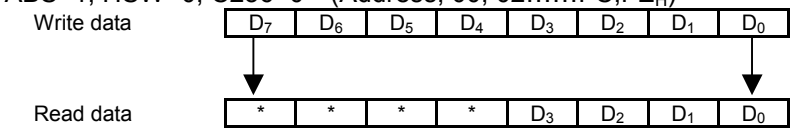
ABS=0, HSW=0, C256=0 (Address; 00, 02……FC,FE_H)



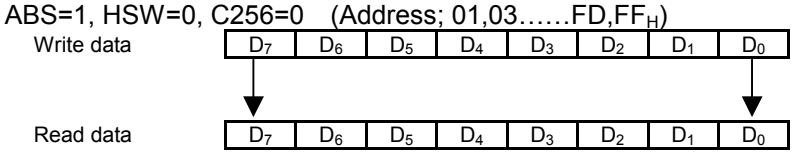
ABS=0, HSW=0, C256=0 (Address; 01,03……FD,FF_H)



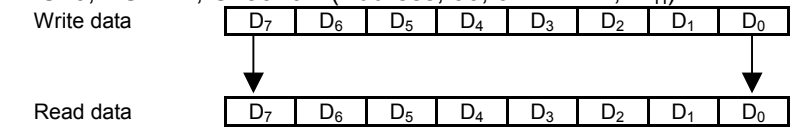
ABS=1, HSW=0, C256=0 (Address; 00, 02……FC,FE_H)



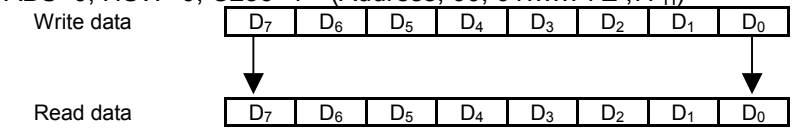
ABS=1, HSW=0, C256=0 (Address; 01,03……FD,FF_H)



ABS=0, HSW=1, C256=0 (Address; 00, 01……BE,BF_H)



ABS=0, HSW=0, C256=1 (Address; 00, 01…… 7E ,$7F_H$)



*: Invalid data

(11) Gradation palette

In the gradation mode, either variable or fixed gradation mode is selected by programming the “PWM” register of the “Gradation control” instruction.

PWM=0: Variable gradation mode
(Select 16 gradation levels out of 32-gradation level of the gradation palette)

PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)

In these mode, each of the gradation palettes Aj, Bj and Cj can select 16-gradation level out of 32-gradation level by setting 5-bit data to the “PA” registers in the “Gradation palette j” instructions (j=0 to Fh).

For instance, the gradation palettes Aj correspond to the SEGAi, the Bj to SEGBi and the Cj to SEGCi (j=0 to 15, i=0 to 127).

Correspondence between display data and gradation palettes

Table 10 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

(MSB) Display data (LSB)				Gradation palette	Default palette value
0	0	0	0	Palette 0	0 0 0 0 0
0	0	0	1	Palette 1	0 0 0 1 1
0	0	1	0	Palette 2	0 0 1 0 1
0	0	1	1	Palette 3	0 0 1 1 1
0	1	0	0	Palette 4	0 1 0 0 1
0	1	0	1	Palette 5	0 1 0 1 1
0	1	1	0	Palette 6	0 1 1 0 1
0	1	1	1	Palette 7	0 1 1 1 1
1	0	0	0	Palette 8	1 0 0 0 1
1	0	0	1	Palette 9	1 0 0 1 1
1	0	1	0	Palette10	1 0 1 0 1
1	0	1	1	Palette11	1 0 1 1 1
1	1	0	0	Palette12	1 1 0 0 1
1	1	0	1	Palette13	1 1 0 1 1
1	1	1	0	Palette14	1 1 1 0 1
1	1	1	1	Palette15	1 1 1 1 1

Gradation palette table (Variable gradation mode, PWM="0", MON="0")

Table 11 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

Palette value	Gradation level	Gradation palette	Palette value	Gradation level	Gradation palette
0 0 0 0 0	0	Palette 0(default)	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette 0(default)8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette 1(default)	1 0 0 1 1	19/31	Palette 9(default)
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette 2(default)	1 0 1 0 1	21/31	Palette 10(default)
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette 3(default)	1 0 1 1 1	23/31	Palette 11(default)
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette 4(default)	1 1 0 0 1	25/31	Palette 12(default)
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette 5(default)	1 1 0 1 1	27/31	Palette 13(default)
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette 6(default)	1 1 1 0 1	29/31	Palette 14(default)
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette 7(default)	1 1 1 1 1	31/31	Palette 15(default)

Gradation palette table (Fixed gradation mode, PWM="1", MON="0")

Table 12 8-gradation segment drivers

(MSB) Display data (LSB)				Gradation level
0	0	0	*	0/7
0	0	1	*	1/7
0	1	0	*	2/7
0	1	1	*	3/7
1	0	0	*	4/7
1	0	1	*	5/7
1	1	0	*	6/7
1	1	1	*	7/7

(MSB) Display data (LSB)				Gradation level
0	0	*	*	0/7
0	0	*	*	
0	1	*	*	3/7
0	1	*	*	
1	0	*	*	5/7
1	0	*	*	
1	1	*	*	7/7
1	1	*	*	

Correspondence between display data and gradation level (B&W mode, MON="1")

Table 13

(MSB) Display data (LSB)				Gradation level
0	*	*	*	0
1	*	*	*	1

*:Don't care

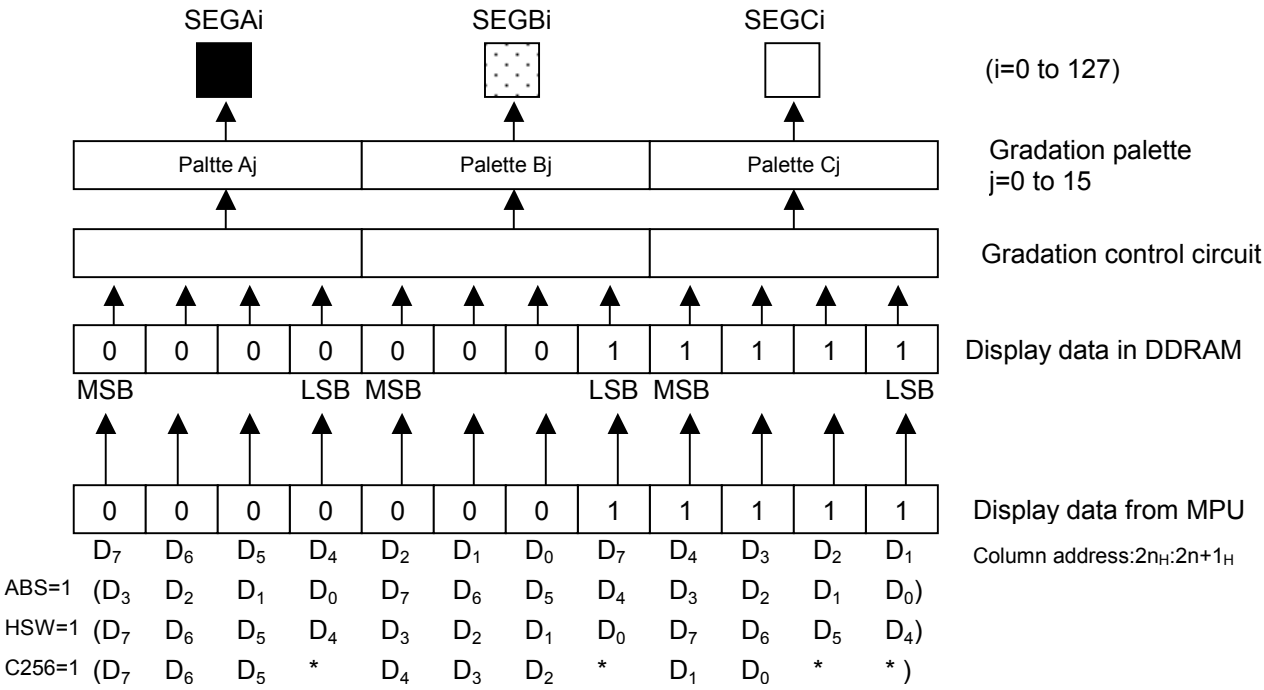
(12) Gradation control and display data

(12-1) Gradation mode

In the graduation mode, each pixel for RGB corresponds to successive 3 segment drivers, and each segment driver provides 16-gradation PWM output by controlling 4 bit display data of the DDRAM. Accordingly, the LSI can drive up to 128x162 pixels in 4096-color (16-gradation x 16-gradation x 16-gradation = 4-bit x 4-bit x 4-bit).

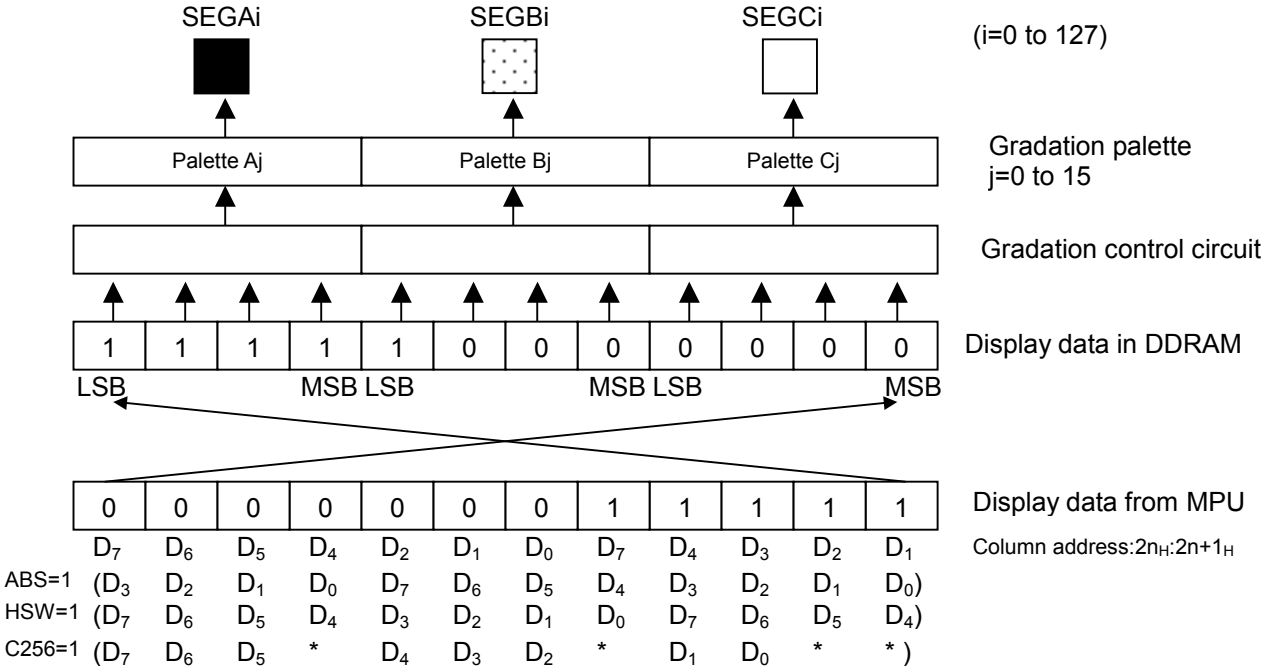
In addition, the LSI can transfer the display data for the RGB by 16-bit at once or 8-bit two-times. The data assignment between gradation palettes and segment drivers varies in accordance with setting for the “SWAP” and “REF” registers of the "Display control (2)" instruction.

(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address :$2n_H$,$2n_H+1_H$ (REF=”0”)
:FE_H -$2n_H$, FF_H-($2n_H+1_H$) (REF=”1”)
HSW=1; 00_H to BF_H, C256=1; 00_H to $7F_H$

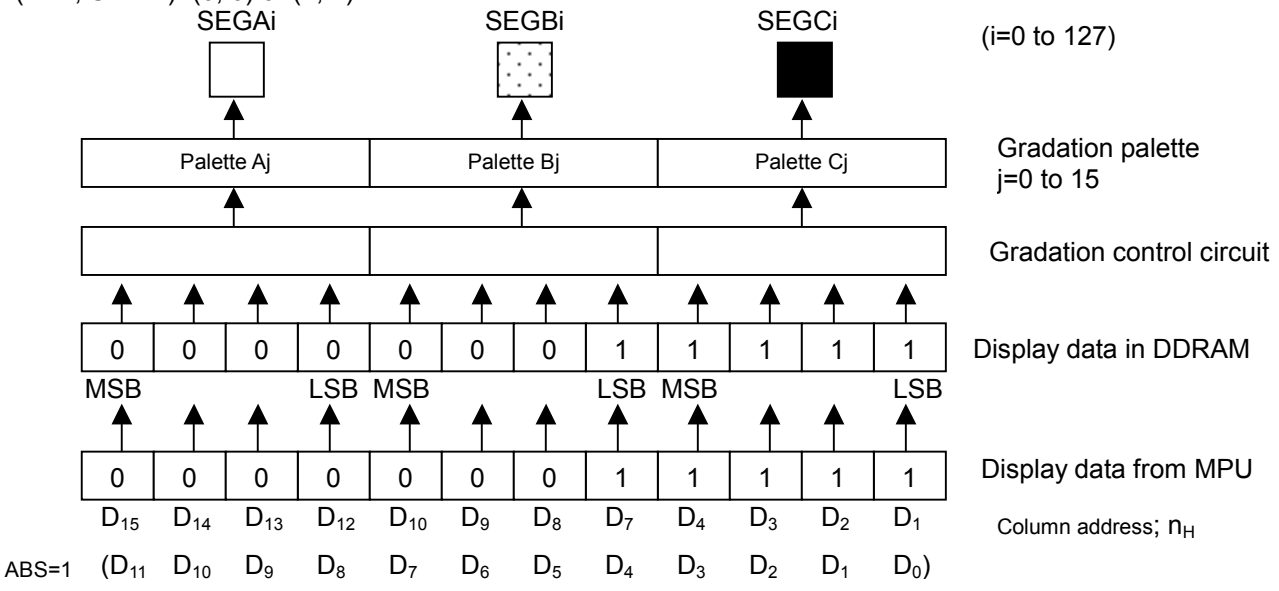
(REF, SWAP)=(0, 1) or (1, 0)



Note) DDRAM column address : $2n_H$,$2n_H+1_H$ (REF="0")
: FE_H -$2n_H$, FF_H-($2n_H+1_H$) (REF="1")
HSW=1; 00_H to BF_H, C256=; 00_H to $7F_H$

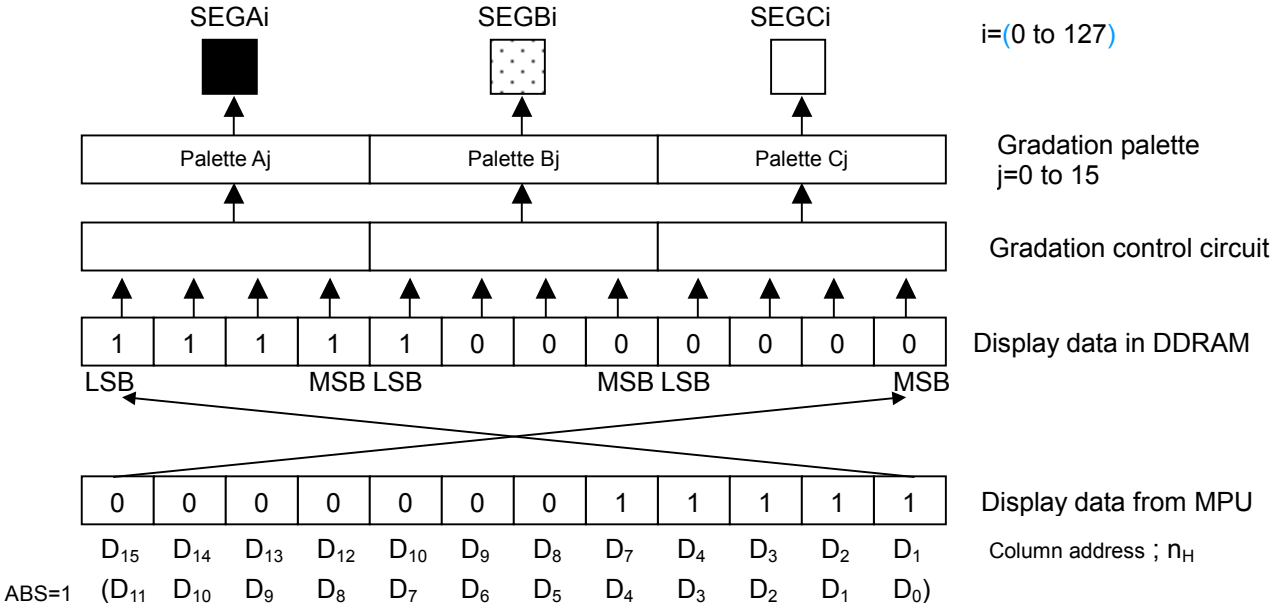
In the 16-bit data bus mode, the data assignments between the gradation palettes and the segment drivers vary in accordance with setting for the "SWAP" and "REF" bit of the "Display control (2)" instruction as well as the assignment in the 8-bit data bus mode.

(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address :n_H (REF="0")
:$7F_H$ - n_H(REF="1")

(REF, SWAP)=(0, 1) or (1, 0)

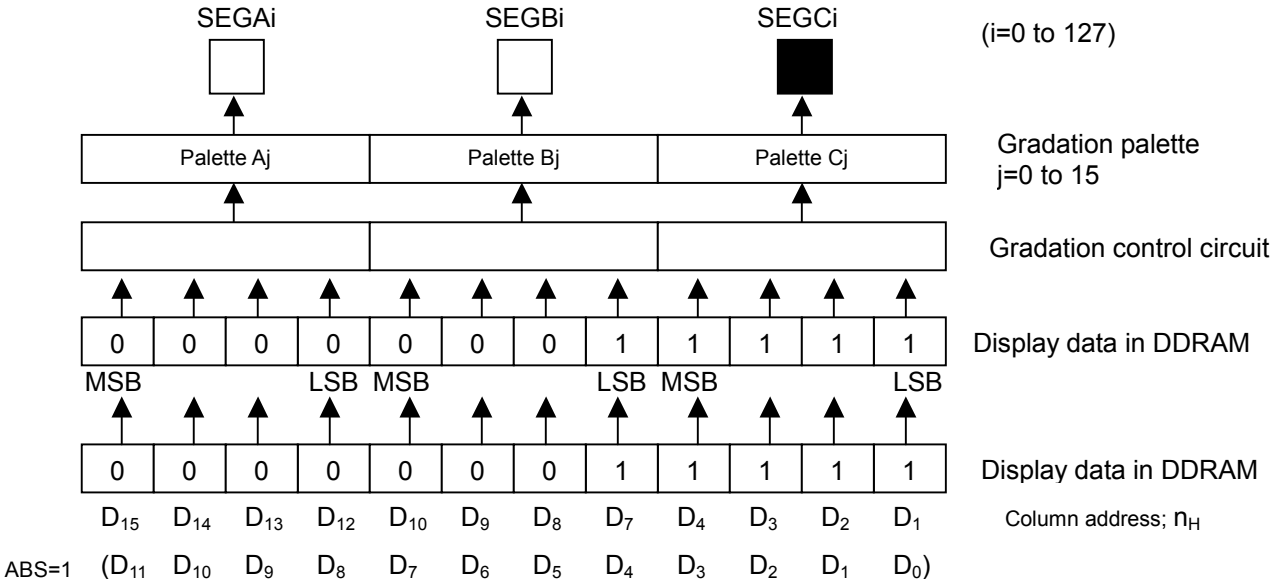


Note) DDRAM column address :n_H (REF="0")
:$7F_H - n_H$ (REF="1")

(12-2) B&W mode (MON="1")

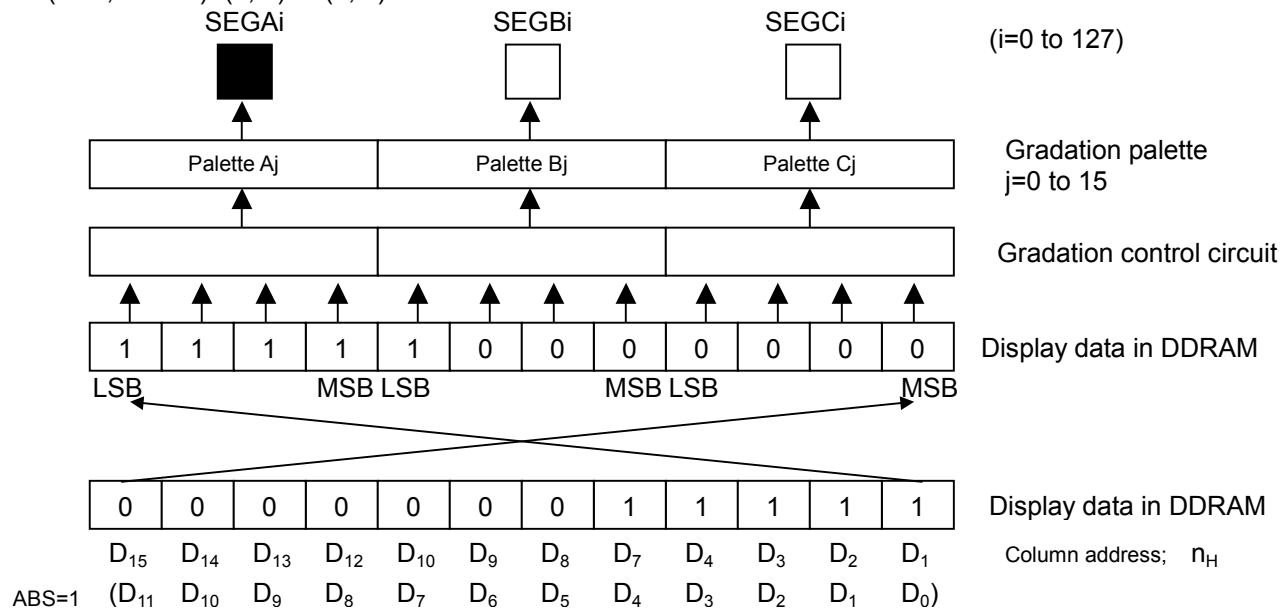
In the B&W mode, 3 bits of the MSB data are used in both of the 16-bit and 8-bit data bus modes.

In the 16-bit data bus mode (Similarly 8-bit data bus access)
(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address : n_H (REF="0")
: $7F_H$-n_H (REF="1")

(REF, SWAP)=(0, 1) or (1, 0)



Note) DDRAM column address : n_H (REF="0")
: $7F_H$-n_H (REF="1")

(13) Display timing generator

The display-timing generator creates the timing pulses such as the CL, the FLM, the FR and the CLK by dividing the oscillation frequency oscillate an external or internal resister mode. The each of timing pulses is outputted through the each output terminals by “SON” = 1.

(14) LCD line clock (CL)

The LCD line clock (CL) is used as a count-up signal for the line counter and a latch signal for the data latch circuit. At the rising edge of the CL signal, the line counter is counted-up and the 384-bit display data, corresponding to this line address, is latched into the data latch circuit. And at the falling edge of the CL signal, this latched data output on the segment drivers. Read out timing of the display data, from DDRAM to the latch circuits is completely independent of the access timing to the MPU. For this reason, the MPU can access to the LSI regardless of an internal operation.

(15) LCD alternate signal (FR) and LCD synchronous signal (FLM)

The FR and FLM signals are created from the CL signal. The FR signal is used to alternate the crystal polarization on a LCD panel. It is programmed that the FR signal is toggle on every frame in the default setting or once every N lines in the N-line inversion mode. The FLM signal is used to indicate a start line of a new display frame. It presets an initial display line address of the line counter when the FLM signal becomes ”1”.

(16) Data latch circuit

The data latch circuit is used temporarily store the display data that will output to the segment drivers. The display data in this circuit is updated in synchronization of the CL signal.

The “All pixels ON/OFF”, “Display ON/OFF” and “Reverse display ON/OFF” instructions change the display data in this circuit but do not change the display data of the DDRAM.

LCD Driving waveforms (In the B&W mode, Reverse display OFF, 1/163 duty)

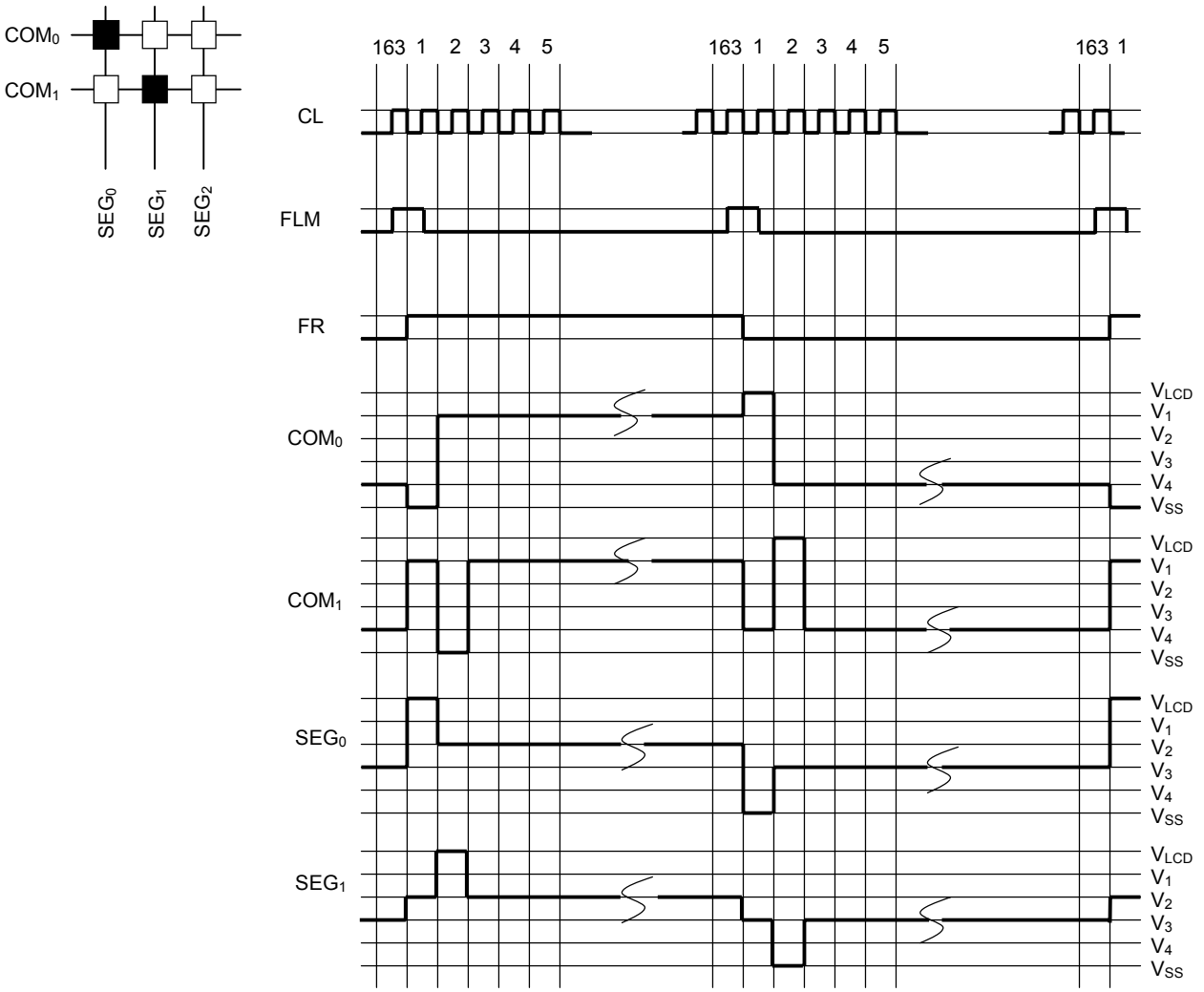


Fig 8

(17) Common and segment drivers

The LSI includes 384-segment drivers and 162-common drivers. The common drivers generate the LCD driving waveforms composed of the V_{LCD}, V_1, V_4 and V_{SS} in accordance with the FR signal and scanning data. The segment drivers generate waveforms composed of the V_{LCD}, V_2, V_3 and V_{SS} in accordance with the FR signal and display data.

(18) Oscillator

The oscillator generates internal clocks for the display timing and the voltage booster. Since the LSI has internal capacitor (C) and resistor (R) for the oscillation, external capacitor and resistor are not usually required. However, in case that an external resistor is used, the resister is connected between the OSC_1 and OSC_2 terminals. The external resistor becomes enabled by setting "1" to the "CKS" register of "Data bus length" instruction. When the internal oscillator is not used, the external clocks with 50% duty cycle ratio must be input to the OSC_1 terminal.

In addition, the feed back resister for the oscillation is varied by programming the "Rf" register of the "Frequency control" instruction, so that it is possible to optimize the frame frequency for a LCD panel. Setting examples of the MON (B&W /Gradation) and the PWM (Variable gradation /Fixed gradation) are described, as follows.

(18-1) Internal oscillation mode (CKS=0)

Symbol	MON	PWM	Display mode
f_1	0	0	Variable gradation mode
f_2	0	1	Fixed gradation mode
f_3	1	*	B&W mode

*: Don't care

(18-2) External resistor oscillation mode(CKS=1)

The internal clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "MON" and "PWM" registers must be set as well.

(18-3) External clock input mode (CKS=1)

The external clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "MON" and "PWM" registers must be set as well.

(19) Power supply circuits

The internal power supply circuits are composed of the voltage booster, the electrical variable resister (EVR), the voltage regulator, reference voltage generator and the voltage followers.

The condition of the power supply circuits is arranged by programming the "DCON" and "AMPON" registers on the "Power control" instruction. For this arrangement, some parts of the internal power supply circuits are activated in using an external power supply, as shown in the following table.

Table 14

DCON	AMPON	Voltage booster	Voltage followers Voltage regulator EVR	External voltage	Note
0	0	Disable	Disable	V_{OUT}, V_{LCD}, V_1, V_2, V_3, V_4	1, 3
0	1	Disable	Enable	V_{OUT}	2, 3
1	1	Enable	Enable	–	–

Note1) The internal power circuits are not used. The external V_{OUT} is required and the C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6-, V_{REF}, V_{REG} and V_{EE} terminals must be open.

Note2) The internal power circuits except the voltage booster are used. The external V_{OUT} is required and the C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6- and V_{EE} terminals must be open. The reference voltage is required to V_{REF} terminal.

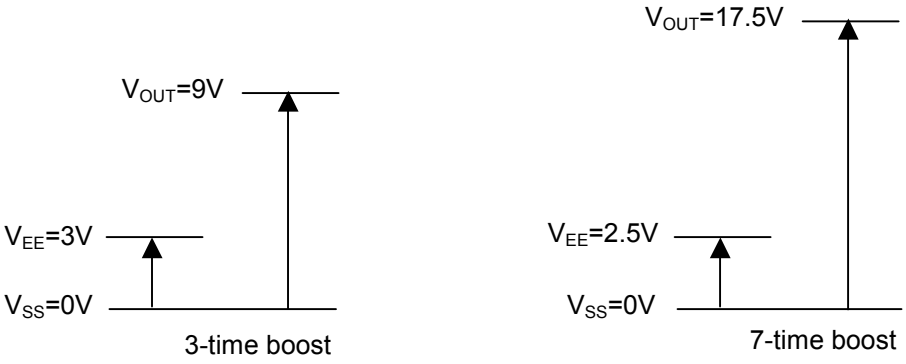
Note3) The relation among the voltages should be maintained as follows.

$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$

(20) Voltage booster

The voltage booster generates maximum 7x voltage of the V_{EE} level. It is programmed so that the boost level is selected out of 1x, 2x, 3x, 4x, 5x, 6x and 7x by the “Boost level select” instruction. The boosted voltage V_{OUT} must not exceed beyond the value of 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

Boosted voltages



Capacitor connections for the voltage Booster

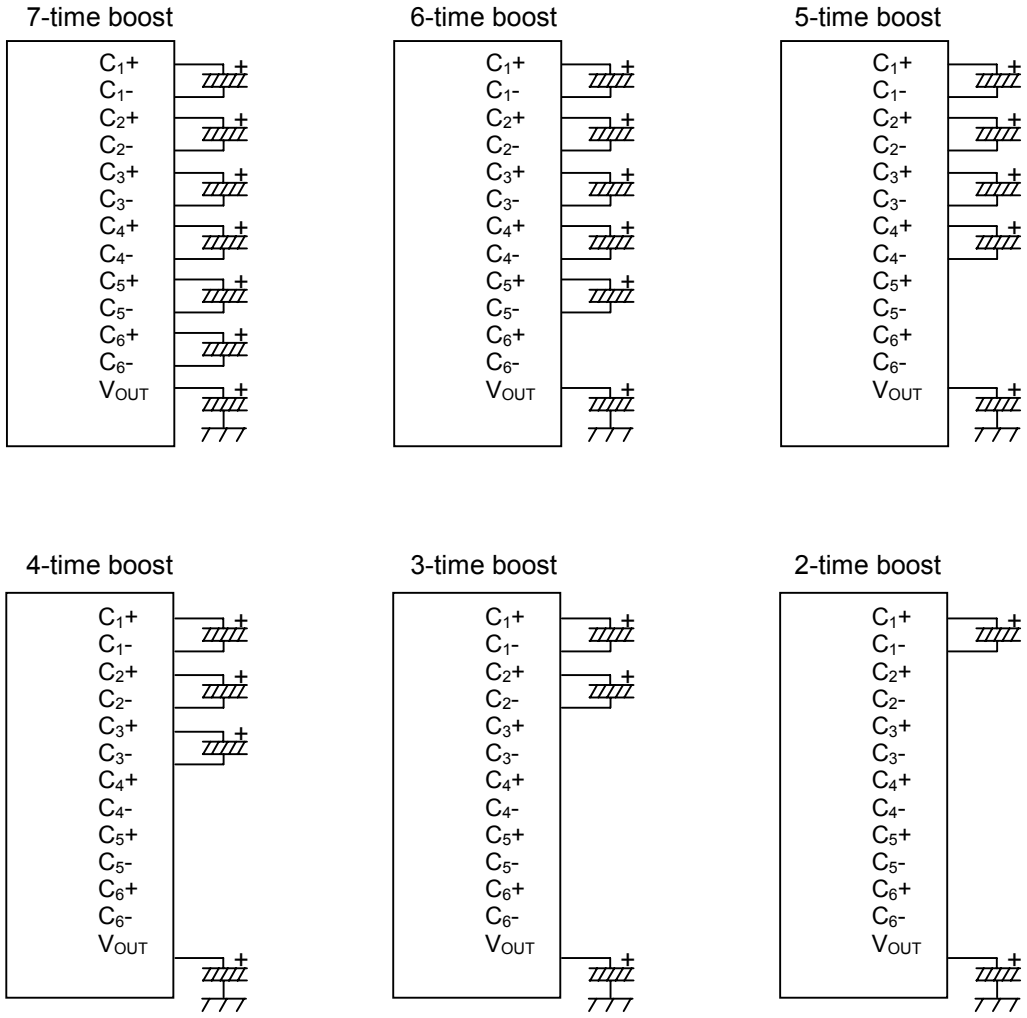


Fig 9

(21) Reference voltage generator

The reference voltage generator is used to produce the reference voltage (V_{BA}), which is output from the V_{BA} terminal and should be input to the V_{REF} terminal.

$V_{BA} = V_{EE} \times 0.9$

(22) Voltage regulator

The voltage regulator, composed of the gain control circuit and an operational amplifier, and is used to gain the reference voltage (V_{REF}) and to create the regulated voltage (V_{REG}). The V_{REG} is used as an input voltage to the EVR circuit, which is programmed by the “VU” register of the “Boost level” instruction.

$V_{REG} = V_{REF} \times N$ (N: register value for the boost level)

(23) Electrical variable resister (EVR)

The EVR is variable within 128-step, and is used to fine-tune the LCD driving voltage (V_{LCD}) by programming the “DV” register in the “EVR control” instruction, so that it is possible to optimize the contrast level for a LCD panels.

$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127$ (M: register value for the EVR)

(24) LCD driving voltage generation circuit

LCD driving voltage generation circuit generates the V_{LCD} voltage levels as V_{LCD}, V_1, V_2, V_3 and V_4 with internal E.V.R and the Bleeder resistors. The bias ratio of the LCD driving voltage is selected out of 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11 and 1/12.

In using the internal power supply, the capacitors CA_2 must be connected to the V_{LCD}, V_1, V_2, V_3 and V_4 terminals, and the CA_2 value must be determined by the evaluation with actual LCD modules.

In using the internal power supply, the external LCD driving voltages such as the V_{LCD}, V_1, V_2, V_3 and V_4 are supplied and the external power supply circuits must be set to “OFF” by DCON = AMPON = "0". In this mode, voltage booster terminals such as C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6-, V_{EE}, V_{REF} and V_{REG} must be opened.

In case that the voltage booster is not used but only some parts of internal power supply circuits (Voltage followers, Voltage regulator and EVR) are used, the C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+ and C_6- terminals must be opened. And, the external power supply is input to the V_{OUT} terminal, and the reference voltage to the V_{REF} terminal. The capacitor CA_3 must connect to the V_{REG} terminal for voltage stabilization.

Connections of the capacitors for the voltage boost

Using All of the internal power supply circuits (7-time boost)

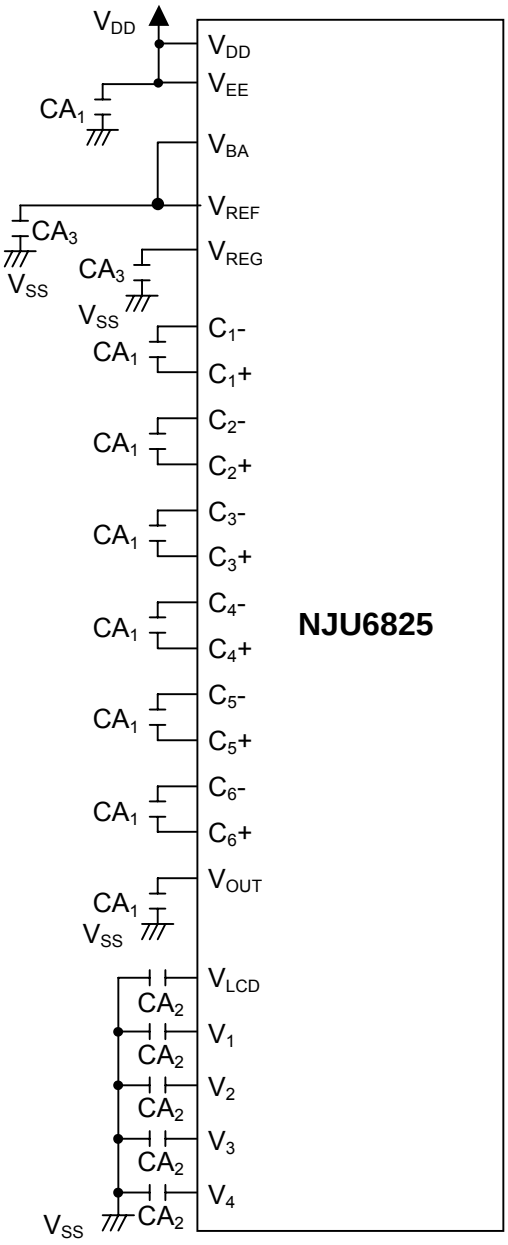


Fig 10

Using only external power supply circuits

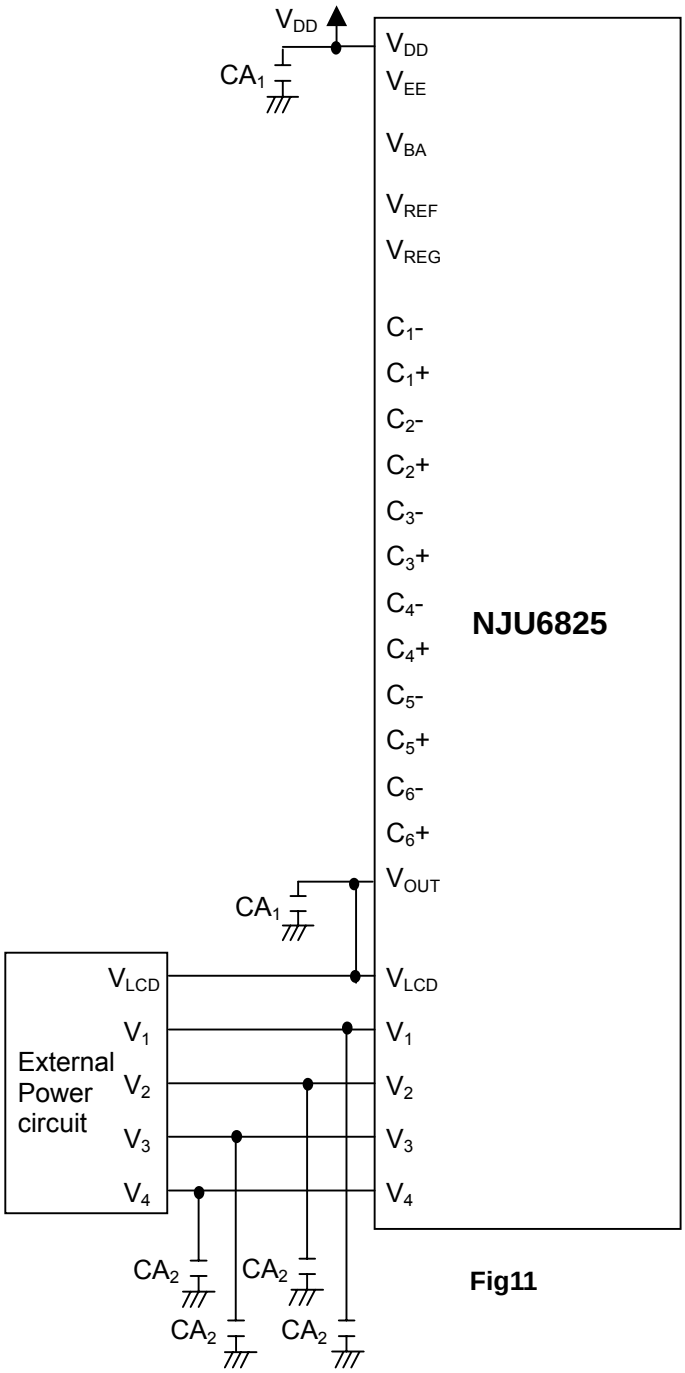


Fig11

Reference values

CA_1	1.0 to 4.7μF
CA_2	1.0 to 2.2μF
CA_3	0.1μF

Note1) B grade capacitor is recommended for CA_1-CA_3. Testing actual samples with an LCD panel is recommended to decide an optimum value of these capacitors.

Note2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces the step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, use the shortest possible wires and place the capacitors to be as close as possible to the LSI.

Using internal power supply circuits
Without the reference voltage generator(1)
(7-time boost)

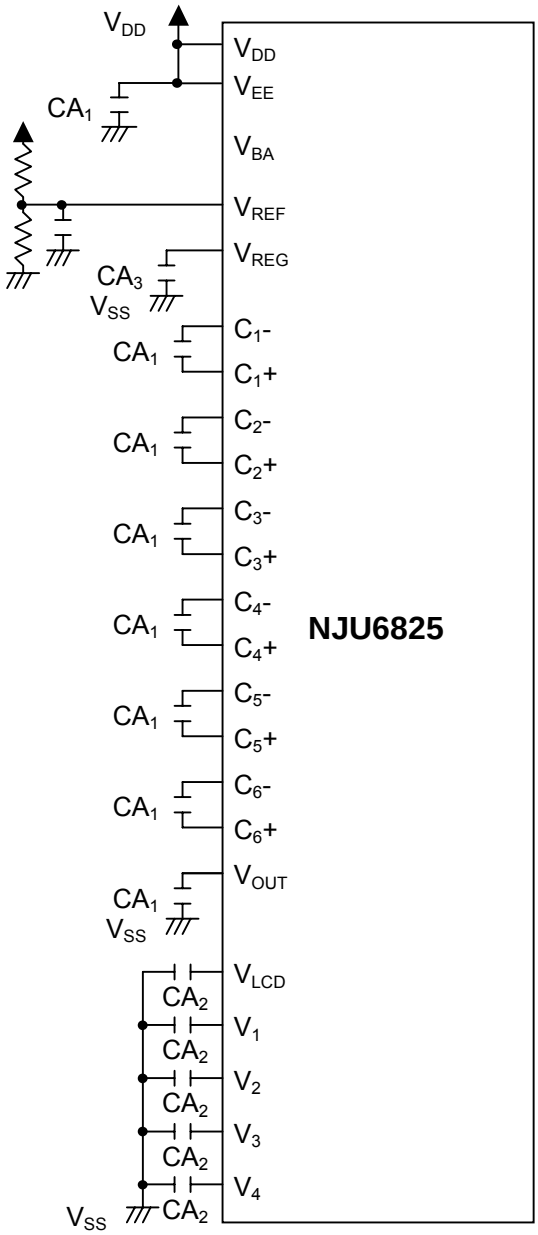


Fig 12

Using internal power supply circuit
Without the reference voltage generator(2)
(7-time boost)

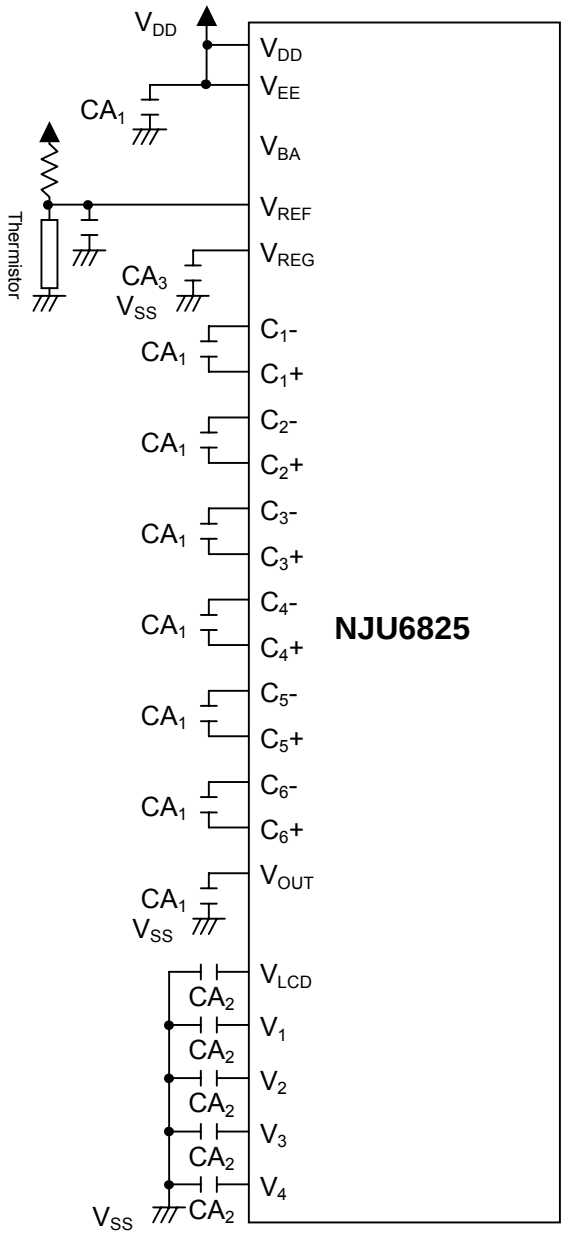


Fig 13

Reference value

CA_1	1.0 to 4.7µF
CA_2	1.0 to 2.2µF
CA_3	0.1µF

Note1) B grade capacitor is recommended for CA_1-CA_3. Testing actual samples with an LCD panel is recommended to decide an optimum value of these capacitors.

Note2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces the step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, use the shortest possible wires and place the capacitors to be as close as possible to the LSI.

Using internal power supply circuits
Without the voltage booster

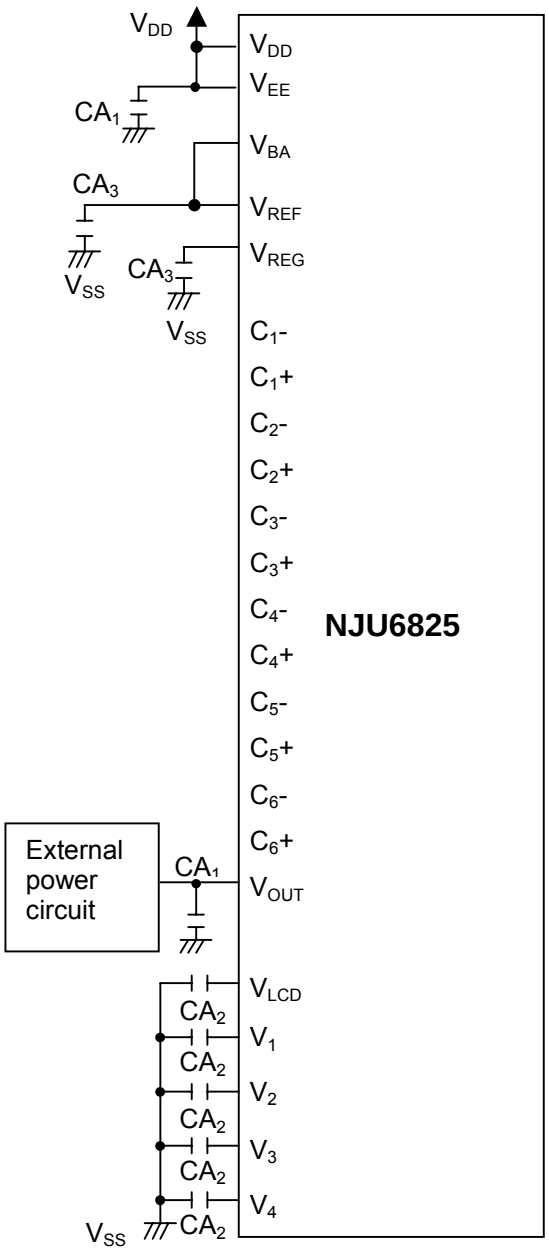


Fig 14

Reference value

CA_1	1.0 to 4.7µF
CA_2	1.0 to 2.2µF
CA_3	0.1µF

Note1) B grade capacitor is recommended for CA_1-CA_3. Testing actual samples with an LCD panel is recommended to decide an optimum value of these capacitors.

Note2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces the step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, use the shortest possible wires and place the capacitors to be as close as possible to the LSI.

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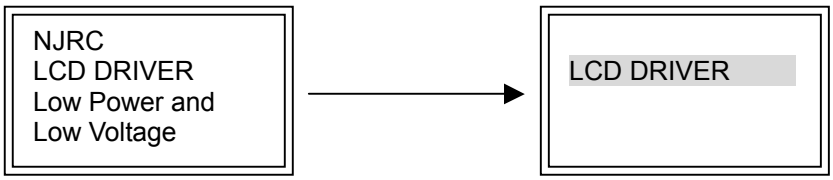
(25) Partial display function

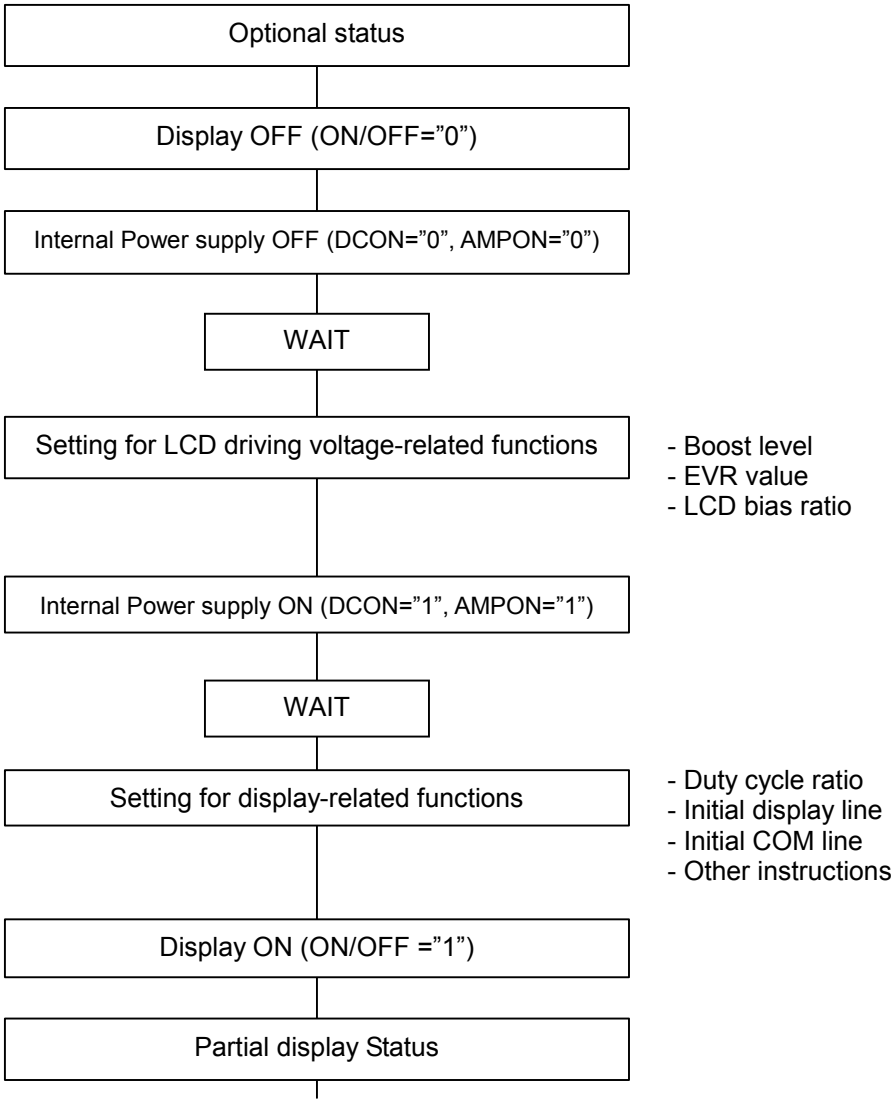
The partial display function is used to partially specify some parts of display area on LCD panels. By using this function, LCD modules can work in lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. It is usually used to display a time and calendar, and is also used to optimize the LSI condition in accordance with the display size. It can be programmed to select the duty cycle ratio (1/16, 1/24, 1/32, 1/40, 1/48, 1/56, 1/64, 1/72, 1/80, 1/96, 1/112, 1/128, 1/133, 1/144, 1/160, 1/163 in case “DSE” is “0”), the LCD bias ratio, the boost level and the EVR value by the instructions.

Partial display image



Normal display　　Partial display

Partial display sequence



(26) Discharge circuit

Discharge circuit is used to discharge the electric charge of the capacitors on the V_1 to V_4 and V_{LCD} terminals. This circuit is activated by setting “1” to the “DIS” register of the “Discharge” instruction or by setting “RESb” terminal to ”0” level. The “Discharge ON/OFF” instruction is usually required just after the internal power supply is turned off by setting “0” into the “DCON” and “AMPON” registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

(27) Reset circuit

The reset circuit initializes the LSI into the following default status. It is activated by setting the RESb terminal to “0” . The RESb terminal is usually required to connect to the MPU reset terminal in order that the LSI can be initialized at the same timing of the MPU.

- Default status

1. DDRAM display data :Undefined
2. column address :$(00)_H$
3. row address :$(00)_H$
4. Initial display line :$(0)_H$ (1st line)
5. Display ON/OFF :OFF
6. Reverse display ON/OFF :OFF (normal)
7. Duty cycle ratio :1/163 duty (DSE=0)
8. N-line Inversion ON/OFF :OFF
9. COM scan direction :$COM_0 \rightarrow COM_{161}$
10. Increment mode :OFF
11. Reverse SEG direction :OFF (normal)
12. SWAP mode :OFF (normal)
13. EVR value :(0, 0, 0, 0, 0, 0, 0)
14. Internal power supply :OFF
15. Display mode :Gradation display mode
16. LCD bias ratio :1/9 bias
17. Gradation Palette 0 :(0, 0, 0, 0, 0)
18. Gradation Palette 1 :(0, 0, 0, 1, 1)
19. Gradation Palette 2 :(0, 0, 1, 0, 1)
20. Gradation Palette 3 :(0, 0, 1, 1, 1)
21. Gradation Palette 4 :(0, 1, 0, 0, 1)
22. Gradation Palette 5 :(0, 1, 0, 1, 1)
23. Gradation Palette 6 :(0, 1, 1, 0, 1)
24. Gradation Palette 7 :(0, 1, 1, 1, 1)
25. Gradation Palette 8 :(1, 0, 0, 0, 1)
26. Gradation Palette 9 :(1, 0, 0, 1, 1)
27. Gradation Palette 10 :(1, 0, 1, 0, 1)
28. Gradation Palette 11 :(1, 0, 1, 1, 1)
29. Gradation Palette 12 :(1, 1, 0, 0, 1)
30. Gradation Palette 13 :(1, 1, 0, 1, 1)
31. Gradation Palette 14 :(1, 1, 1, 0, 1)
32. Gradation Palette 15 :(1, 1, 1, 1, 1)
33. Gradation mode control :Variable gradation mode
34. Data bus length :8-bit data bus length
35. Discharge circuit :OFF

(28) Power supply ON/OFF sequences

The following paragraphs describe power supply ON/OFF sequences, which are to protect the LSI from over current.

(28-1) Using an external power supply

- Power supply ON sequence

  Logic voltage (V_{DD}) must be always input first, and next the LCD driving voltages (V_1 to V_4 and V_{LCD}) are turned on. In using the external V_{OUT}, the V_{DD} must be input first, next the reset operation must be performed, and finally the V_{OUT} can be input.

- Power supply OFF sequence

  Either the reset operation, cutting off the V_1 to V_4 and V_{LCD} from the LSI by the RESb terminal or the "Power control" instruction must be performed first, and next the V_{DD} is turned off. It is recommended that a series-resister between 50 Ω and 100 Ω is added on the V_{LCD} line (or V_{OUT} line in using only the external V_{OUT} voltage) in order to protect the LSI from the over current.

(28-2) Using the internal power supply circuits

- Power supply ON sequence

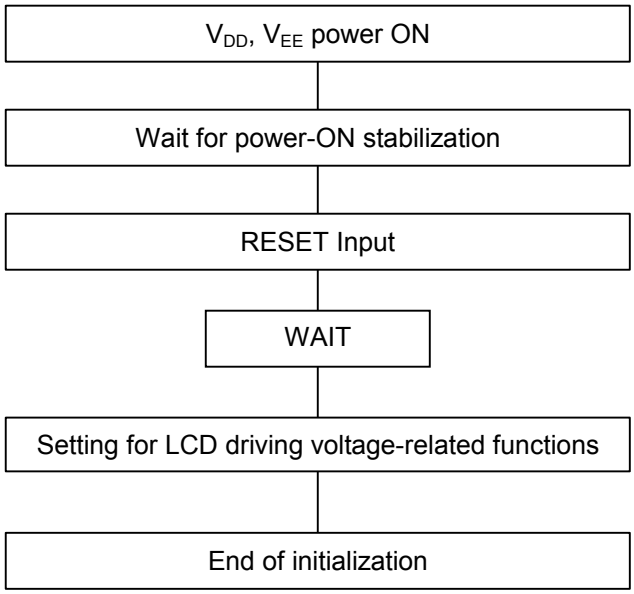
  The V_{DD} must be input first, next the reset operation must be performed, and finally the V_1 to V_4 and V_{LCD} can be turned on by setting "1" to the "DCON" and "AMPON" registers of the "Power control" instruction.

- Power supply OFF sequence

  Either the reset operation by the RESb terminal or the "Power control" instruction must be performed first, and next the input voltage for the voltage booster (V_{EE}) and the V_{DD} can be turned off. If the V_{EE} is supplied from different power sources for V_{DD}, the V_{EE} is turned off first, and next the V_{DD} is turned off.

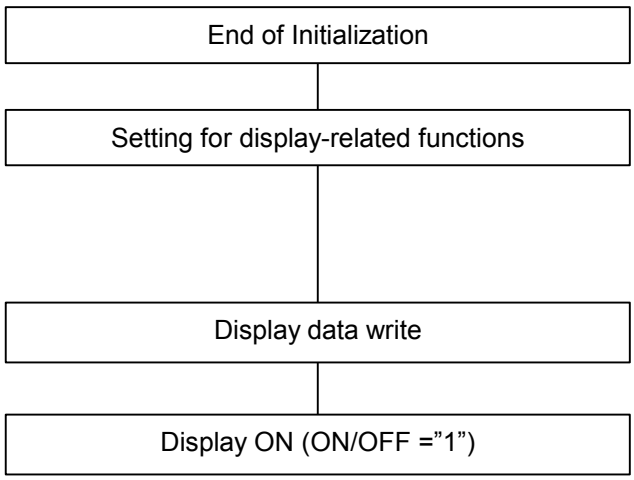
(29) Referential instruction sequences

(29-1) Initialization in using the internal power supply circuits



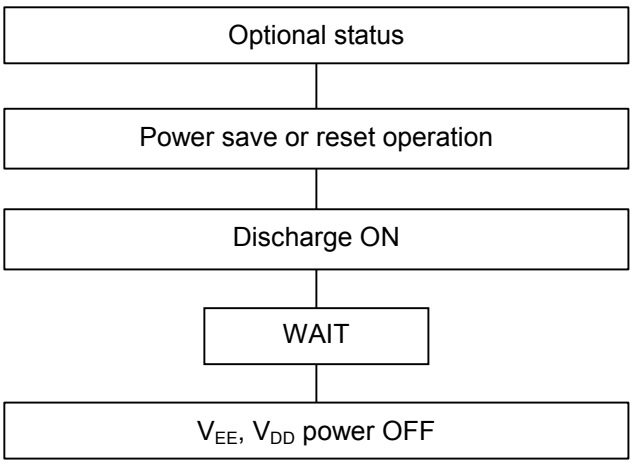
- EVR value
- LCD bias ratio
- Power control (DCON="1", AMPON="1")

(29-2) Display data writing



- Initial display line
- Increment mode
- column address
- row address

(29-3) Power OFF



- All COM/SEG output V_{SS} level.

(30) Instruction table

Instruction Table (1)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display data write	0	0	1	0	0/1	0/1	0/1	Write Data								Write display data to DDRAM
Display data read	0	0	0	1	0/1	0/1	0/1	Read Data								Read display data from DDRAM
column address (Lower) [0_H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	DDRAM column address
column address (Upper) [1_H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	DDRAM column address
row address (Lower) [2_H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	DDRAM row address
row address (Upper) [3_H]	0	1	1	0	0	0	0	0	0	1	1	AY7	AY6	AY5	AY4	DDRAM row address
Initial display line (Lower) [4_H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Row address for an initial COM line (Scan start line)
Initial display line (Upper) [5_H]	0	1	1	0	0	0	0	0	1	0	1	LA7	LA6	LA5	LA4	Row address for an initial COM line (Scan start line)
N-line inversion (Lower) [6_H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	The number of N-line inversion
N-line inversion (Upper) [7_H]	0	1	1	0	0	0	0	0	1	1	1	N7	N6	N5	N4	The number of N-line inversion
Display control (1) [8_H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF	SHIFT: Common direction MON: Gradation or B/W display mode ALLON: All pixels ON/OFF ON/OFF: Display ON/OFF
Display control (2) [9_H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: Reverse display ON/OFF NLIN: N-line inversion ON/OFF, SWAP: SWAP mode ON/OFF REF: Segment direction
Increment control [A_H]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: Window addressing mode ON/OFF AIM: Read-modify-write ON/OFF AYI: Row auto-increment mode ON/OFF AXI: Column auto-increment mode ON/OFF
Power control [B_H]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON: Voltage followers ON/OFF HALT: Power save ON/OFF DCON: Voltage booster ON/OFF ACL: Reset
Duty cycle ratio [C_H]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Sets LCD duty cycle ratio
Boost level [D_H]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	Sets boost level
LCD bias ratio [E_H]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Sets LCD bias ratio
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.
Note 2) [N_H] : Address of instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (2)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette A0/A8 (Lower) [0_H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A0/A8 (Upper) [1_H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A1/A9 (Lower) [2_H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A1/A9 (Upper) [3_H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A2/A10 (Lower) [4_H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A2/A10 (Upper) [5_H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A3/A11 (Lower) [6_H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A3/A11 (Upper) [7_H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A4/A12 (Lower) [8_H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A4/A12 (Upper) [9_H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A5/A13 (Lower) [A_H]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A5/A13 (Upper) [B_H]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A6/A14 (Lower) [C_H]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
Gradation palette A6/A14 (Upper) [D_H]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (3)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette A7/A15 (Lower) [0_H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette A7/A15 (Upper) [1_H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette B0/B8 (Lower) [2_H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B0/B8 (Upper) [3_H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PB84	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B1/B9 (Lower) [4_H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B1/B9 (Upper) [5_H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B2/B10 (Lower) [6_H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B2/B10 (Upper) [7_H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B3/B11 (Lower) [8_H]	0	1	1	0	0	1	0	1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B3/B11 (Upper) [9_H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B4/B12 (Lower) [A_H]	0	1	1	0	0	1	0	1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B4/B12 (Upper) [B_H]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B5/B13 (Lower) [C_H]	0	1	1	0	0	1	0	1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
Gradation palette B5/B13 (Upper) [D_H]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.
Note 2) [N_H] : Address of instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (4)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette B6/B14 (Lower) [0_H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B6/B14 (Upper) [1_H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B7/B15 (Lower) [2_H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette B7/B15 (Upper) [3_H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette C0/C8 (Lower) [4_H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C0/C8 (Upper) [5_H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C1/C9 (Lower) [6_H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C1/C9 (Upper) [7_H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C2/C10 (Lower) [8_H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C2/C10 (Upper) [9_H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C3/C11 (Lower) [A_H]	0	1	1	0	0	1	1	1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C3/C11 (Upper) [B_H]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C4/C12 (Lower) [C_H]	0	1	1	0	0	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
Gradation palette C4/C12 (Upper) [D_H]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44/ PC124	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.
Note 2) [N_H] : Address of instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (5)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette C5/C13 (Lower) [0_H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C5/C13 (Upper) [1_H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C6/C14 (Lower) [2_H]	0	1	1	0	1	0	0	0	0	1	0	PC63/P C143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C6/C14 (Upper) [3_H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC154	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C7/C15 (Lower) [4_H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Gradation palette C7/C15 (Upper) [5_H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Initial COM line [6_H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Sets scan-starting common driver
Display control Signal/ Duty Select [7_H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display clock ON/OFF DSE : Duty-1 ON/OFF
Gradation mode control [8_H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	FDC1	FDC2	PWM : Variable/Fixed gradation mode C256 : 256-Color Mode ON/OFF FDC : Boost Clock
Data bus length [9_H]	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : High speed access ON/OFF ABS : ABS mode ON/OFF CKS : Internal/external oscilation WLS : Display data Length
EVR control (Lower) [A_H]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Sets EVR level (Lower bit)
EVR control (Upper) [B_H]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Sets EVR level (Upper bit)
Frequency control [D_H]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Oscillation frequency
Discharge ON/OFF [E_H]	0	1	1	0	1	0	0	1	1	1	0	*	*	*	DIS	Discharge the electric charge in capacitors on V_1 to V_4 and V_{LCD}
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag
Instruction register address [C_H]	0	1	1	0	1	0	0	1	1	0	0	Reading address				Sets instruction register address
Instruction register read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data				Read out instruction register data

Note 1) * : Don't care.
Note 2) [N_H] : Address of instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.
Note 4) CKS=0: Internal oscillation mode (default)
CKS=1: External oscillation mode

Instruction Table (6)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Window end column address (Lower) [0_H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Sets column address for end point
Window end column address (Upper) [1_H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Sets column address for end point
Window end row address (Lower) [2_H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Sets row address for end point
Window end row address (Upper) [3_H]	0	1	1	0	1	0	1	0	0	1	1	EY7	EY6	EY5	EY4	Sets row address for end point
Initial reverse line (Lower) [4_H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Sets address for reverse line
Initial reverse line (Upper) [5_H]	0	1	1	0	1	0	1	0	1	0	1	LS7	LS6	LS5	LS4	Sets address for reverse line
Last reverse line (Lower) [6_H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Sets address for reverse line
Last reverse line (Upper) [7_H]	0	1	1	0	1	0	1	0	1	1	1	LE7	LE6	LE5	LE4	Sets address for reverse line
Reverse line display ON/OFF [8_H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink type setting LREV : Reverse line display ON/OFF
Gradation palette setting control [9_H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	Upper 8 gradation setting Lower 8 gradation setting
PWM control [A_H]	0	1	1	0	1	0	1	1	0	1	0	PWM S	PWM A	PWM B	PWM C	Sets PWM mode
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag

Note 1) * : Don't care.

Note 2) [N_H] : Address of instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

(31) Instruction descriptions

This chapter provides detail descriptions and instruction registers. Nonexistent instruction codes must not be set into the LSI.

(31-1) Display data write

The “Display data write” instruction is used to write 8-bit display data into the DDRAM.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	0	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display data							

(31-2) Display data read

The “Display data read” instruction is used to read out 8-bit display data from the DDRAM, where the column address and row address must be specified beforehand by the “column address” and “row address” instructions. The dummy read is required just after the “column address” and “row address” instructions.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	0	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display data							

(31-3) Column address

The “column address” instruction is used to specify the column address for the display data’s reading and writing operations. It requires dual bytes for lower 4-bit and upper 4-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for the upper 4-bit.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	AX_3	AX_2	AX_1	AX_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	AX_7	AX_6	AX_5	AX_4

(31-4) Row address

The “row address” instruction is used to specify the row address for the display data read and write operations. It requires dual bytes for lower 4-bit and upper 4-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for upper 4-bit. The row address is specified in between 00_H and $A1_H$. The setting for nonexistent row address between $A2_H$ and FF_H is prohibited.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	AY_3	AY_2	AY_1	AY_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	AY_7	AY_6	AY_5	AY_4

(31-5) Initial display line

The “Initial display line” instruction is used to specify the line address corresponding to the initial COM line. The initial COM line specified by the “Initial COM line” instruction and indicates the common driver that starts scanning the display data.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LA_3	LA_2	LA_1	LA_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	LA_7	LA_6	LA_5	LA_4

LA_7	LA_6	LA_5	LA_4	LA_3	LA_2	LA_1	LA_0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	1	0	0	0	0	1	161

(31-6) N-line inversion

The “N-line inversion” instruction is used to control the alternate rates of the liquid crystal direction. It is programmed to select the N value between 2 and 161, and the FR signal toggles once every N lines by setting “1” into the “NLIN” register of the “Display control (2)” instruction. When the N-line inversion is disabled by setting “0” into the “NLIN” register, the FR signal toggles by the frame.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	N3	N2	N1	N0

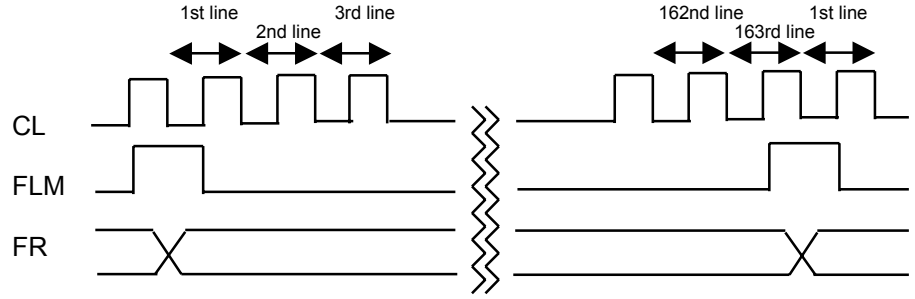
CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	N7	N6	N5	N4

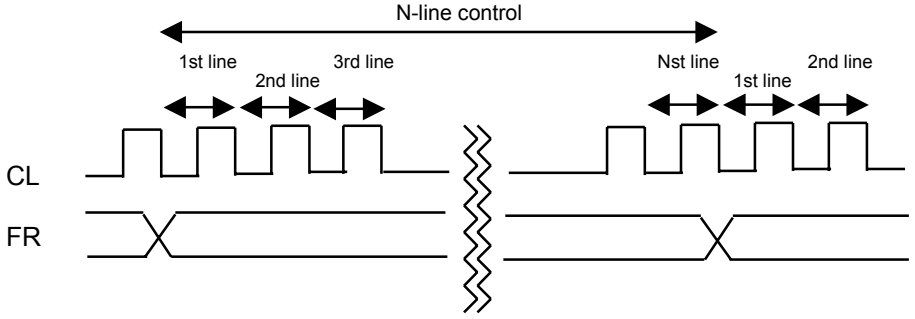
N7	N6	N5	N4	N3	N2	N1	N0	N value
0	0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	0	1	2
				:				:
1	0	1	0	0	0	0	0	161

● N-line Inversion Timing (1/163 duty cycle ratio)

N-line inversion OFF



N-line inversion ON



(31-7) Display control (1)

The “Display control (1)” instruction is used to control display conditions by setting the “Display ON/OFF”, “All pixels ON/OFF”, “Display mode” and “Common direction” registers.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SHIFT	MON	ALLON	ON/OFF

● ON/OFF register

ON/OFF=0 : Display OFF (All COM/SEG output Vss level.)
ON/OFF=1 : Display ON

● All ON register

The “All pixels ON/OFF” register is used to turn on all pixels without changing display data of the DDRAM. The setting for the “All pixels ON/OFF” register has a priority over the “Reverse display ON/OFF” register.

ALLON=0 : Normal
ALLON=1 : All pixels turn on.

● MON register

MON=0 : Gradation mode
MON=1 : B&W mode

● SHIFT register

SHIFT=0 : $COM_0 \rightarrow COM_{161}$
SHIFT=1 : $COM_{161} \rightarrow COM_0$

(31-8) Display control (2)

The “Display control (2)” instruction is used to control the display conditions by setting the “Segment direction”, “SWAP mode ON/OFF”, “N-line inversion ON/OFF” and “Reverse display ON/OFF” registers.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	REV	NLIN	SWAP	REF

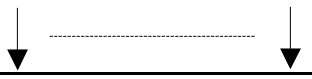
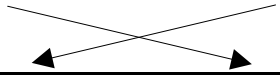
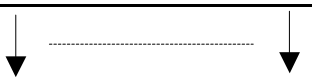
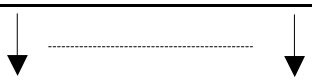
● REF register

The “REF” register is used to reverse the assignment between segment drivers and column address, and it is possible to reduce restrictions for placement of the LSI on the LCD modules. For more information, see (10) “The relation among the DDRAM column address, display data and segment drivers”.

● SWAP register

The “SWAP” register is used to reverse the arrangement of display data in the DDRAM.

SWAP=0 : SWAP mode OFF (Normal)
SWAP=1 : SWAP mode ON

	SWAP=”0”	SWAP=”1”
Write data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
		
RAM data	d7 d6 d5 d4 d3 d2 d1 d0	d0 d1 d2 d3 d4 d5 d6 d7
		
Read data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

● NLIN register

The “NLIN” is used to enable or disable the N-line inversion.

NLIN=0 : N-line inversion OFF (The FR signal toggles by the flame.)
NLIN=1 : N-line inversion ON (The FR signal toggles once every N frames.)

● REV register

The “REV” register is used to enable or disable the reverse display mode that reverses the polarity of display data without changing display data of the DDRAM.

REV=0 : Reverse display mode OFF
REV=1 : Reverse display mode ON

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(31-9) Increment control

The “Increment control” instruction is used for the increment mode. In using the auto-increment mode, DDRAM address automatically increments (+1) whenever the DDRAM is accessed by the “Display data write” or “Display data read” instruction. Therefore, once “Display data write” or “Display data read” instruction is established, it is possible to continuously access to the DDRAM without the “column address” and “row address” instructions. The settings for the “AIM”, “AXI” and “AYI” registers are listed in the following tables.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	WIN	AIM	AYI	AXI

● AIM, AYI and AXI registers

AIM	Increment mode	Note
0	Auto-increment for both of the display data read and write operations	1
1	Auto-increment for the display write operation (Read modify write)	2

Note 1) It is effective for usual operations accessing successive addresses.
Note 2) It is effective for the read-modify-write operation

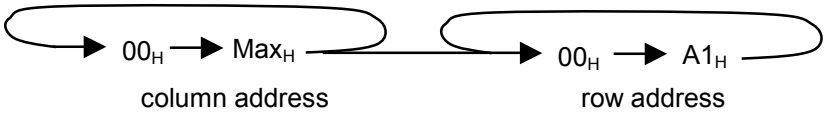
AYI	AXI	Increment mode	Note
0	0	No auto-increment	1
0	1	Auto-increment for the column address	2
1	0	Auto-increment for the row address	3
1	1	Auto-increment for the column address and row address	4

Note 1) Auto-increment is disabled regardless of the “AIM” register.
Note 2) Auto-increment of the column address is enabled in accordance with the “AIM” register.

MAX_H in the 8-bit data bus mode : FF_H
MAX_H in the 16-bit data bus mode : $7F_H$

Note 3) Auto-increment of the row address is enabled in accordance with the “AIM” register.

Note 4) Auto-increment of the column address and the row address are enabled. The row address increments whenever the column address reaches to the MAX_H.



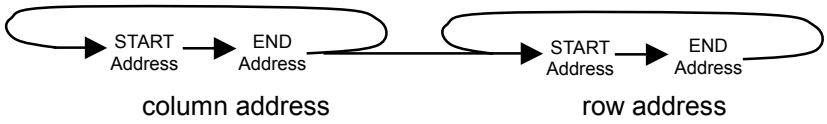
MAX_H in the 8-bit data bus mode : FF_H
MAX_H in the 16-bit data bus mode : $7F_H$

● WIN register

The “WIN” register is used to access to the DDRAM for the window display area, where the start point is determined by the “column address” and “row address” instructions, and the end point by the “Window end column address “and ”Window end row address” instructions. The setting sequence for the window display area is listed as follows. For more detail, see (7) “Window addressing mode”.

WIN=0 :Window addressing mode OFF
WIN=1 :Window addressing mode ON

1. Set WIN=1, AXI=1, and AYI=1 by “Increment control” instruction.
2. Set the start point by the “column address” and “row address” instructions
3. Set the end point by the “Window end column address” and “Window end row address” instructions
4. Enable to access to the DDRAM in the window addressing mode



(31-10) Power control

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	AMPON	HALT	DCON	ACL

● ACL register

The “ACL” register is used to initialize the internal power supply circuits.

ACL=0 : Initialization OFF (Normal)
ACL=1 : Initialization ON

When the data of the “ACL register” is read out by the “Instruction register read” instruction, the read-out data is “1” during the initialization and “0” after the initialization. This initialization is performed by using the signal produced by 2 clocks on the OSC_1. For this reason, the wait time for 2 clocks of the OSC_1 is necessary until next instruction.

● DCON register

The “DCON” register is used to enable or disable the voltage booster.

DCON=0 : Voltage booster OFF
DCON=1 : Voltage booster ON

● HALT register

The “HALT” register is used to enable or disable the power save mode. It is possible to reduce operating current down to stand-by level. The internal status in the power save mode is listed below.

HALT=0 : Power save OFF (Normal)
HALT=1 : Power save ON

Internal status in the power save mode

- The oscillation circuits and internal power supply circuits are halted.
- All segment and common drivers output V_{SS} level.
- The clock input into the OSC_1 is inhibited.
- The display data in the DDRAM is maintained.
- The operational modes before the power save mode are maintained.
- The V_1 to V_4 and V_{LCD} are in the high impedance.

As a power save ON sequence, the “Display OFF” must be executed first, next the “Power save ON” instruction, and then all common and segment drivers output the V_{SS} level. And as power save OFF sequence, the “Power save OFF” instruction is executed first, next the “Display ON” instruction. If the “Power save OFF” instruction is executed in the display ON status, unexpected pixels may instantly turn on.

● AMPON register

The “AMPON” register is used to enable or disable the voltage followers, voltage regulator and EVR.

AMPON=0 : The voltage followers, voltage regulator and the EVR OFF
AMPON=1 : The voltage followers, voltage regulator and the EVR ON

(31-11) Duty cycle ratio

The “Duty cycle ratio” instruction is used to select LCD duty cycle ratio for the partial display function. The partial display function specifies some parts of display area on a LCD panel in the condition of lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. Therefore, it is possible to optimize the LSI’s conditions with extremely low power consumption.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	DS_3	DS_2	DS_1	DS_0

DS_3	DS_2	DS_1	DS_0	Duty cycle ratio		Row way displays
				DSE=0	DSE=1	
0	0	0	0	1/163	1/162	162 commons
0	0	0	1	1/161	1/160	160 commons
0	0	1	0	1/145	1/144	144 commons
0	0	1	1	1/133	1/132	132 commons
0	1	0	0	1/129	1/128	128 commons
0	1	0	1	1/113	1/112	112 commons
0	1	1	0	1/97	1/96	96 commons
0	1	1	1	1/81	1/80	80 commons
1	0	0	0	1/73	1/72	72 commons
1	0	0	1	1/65	1/64	64 commons
1	0	1	0	1/57	1/56	56 commons
1	0	1	1	1/49	1/48	48 commons
1	1	0	0	1/41	1/40	40 commons
1	1	0	1	1/33	1/32	32 commons
1	1	1	0	1/25	1/24	24 commons
1	1	1	1	1/17	1/16	16 commons

The duty cycle ratio is controlled by the “DS_3 to DS_0” registers of the “Duty cycle ratio” instruction and the “DSE” register of the “Display Clock / Duty-1” instruction.

DSE=”0” : The number of commons + 1 (Duty cycle ratio in the default setting)
DSE=”1” : The number of commons (Duty-1)

When the “DSE” is “0”, all common drivers output non-selective levels in period of last common. And the segment drivers output the same data for the last line as the for previous line: For instance they output the same data for the 162^{nd} and 163^{rd} lines when the duty cycle ratio is set to 1/163. For the setting of the “DSE” register, see (31-17) “Display clock / Duty-1”.

(31-12) Boost level

The “Boost level” is used to select the multiple of the voltage booster for the partial display function.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	VU_2	VU_1	VU_0

VU_2	VU_1	VU_0	Boost level
0	0	0	1-time (No boost)
0	0	1	2-time
0	1	0	3-time
0	1	1	4-time
1	0	0	5-time
1	0	1	6-time
1	1	0	7-time
1	1	1	Inhibited

(31-13) LCD bias ratio

The “LCD bias ratio” is used to select the LCD bias ratio for the partial display function.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	B_2	B_1	B_0

B_2	B_1	B_0	LCD bias ratio
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

(31-14) RE flag

The “RE flag” registers are used to determine the contents for the RE registers (RE_2, RE_1 and RE_0) and it is possible to access to the instruction registers.

The data in the “TST_0” register must be “0”, and it is used maker tests only.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	1	TST_0	RE_2	RE_1	RE_0

(31-15) Gradation palette A, B and C

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	0	0	PA_{03}/ PA_{83}	PA_{02}/ PA_{82}	PA_{01}/ PA_{81}	PA_{00}/ PA_{80}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA_{04}/ PA_{84}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	1	0	PA13/ PA_{93}	PA_{12}/ PA_{92}	PA_{11}/ PA_{91}	PA_{10}/ PA_{90}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA_{14}/ PA_{94}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	0	0	PA_{23}/ PA_{103}	PA_{22}/ PA_{102}	PA_{21}/ PA_{101}	PA_{20}/ PA_{100}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA_{24}/ PA_{104}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	1	0	PA_{33}/ PA_{113}	PA_{32}/ PA_{112}	PA_{31}/ PA_{111}	PA_{30}/ PA_{110}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA_{34}/ PA_{114}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	1	0	0	0	PA_{43}/ PA_{123}	PA_{42}/ PA_{122}	PA_{41}/ PA_{121}	PA_{40}/ PA_{120}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PA_{44}/ PA_{124}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PA_{53}/ PA_{133}	PA_{52}/ PA_{132}	PA_{51}/ PA_{131}	PA_{50}/ PA_{130}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PA_{54}/ PA_{134}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PA_{63}/ PA_{143}	PA_{62}/ PA_{142}	PA_{61}/ PA_{141}	PA_{60}/ PA_{140}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PA_{64}/ PA_{144}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PA_{73}/ PA_{153}	PA_{72}/ PA_{152}	PA_{71}/ PA_{151}	PA_{70}/ PA_{150}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PA_{74}/ PA_{154}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB_{03}/ PB_{83}	PB_{02}/ PB_{82}	PB_{01}/ PB_{81}	PB_{00}/ PB_{80}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB_{04}/ PB_{84}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PB_{13}/ PB_{93}	PB_{12}/ PB_{92}	PB_{11}/ PB_{91}	PB_{10}/ PB_{90}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PB_{14}/ PB_{94}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PB_{23}/ PB_{103}	PB_{22}/ PB_{102}	PB_{21}/ PB_{101}	PB_{20}/ PB_{100}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PB_{24}/ PB_{104}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PB_{33}/ PB_{113}	PB_{32}/ PB_{112}	PB_{31}/ PB_{111}	PB_{30}/ PB_{110}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PB_{34}/ PB_{114}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PB_{43}/ PB_{123}	PB_{42}/ PB_{122}	PB_{41}/ PB_{121}	PB_{40}/ PB_{120}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PB_{44}/ PB_{124}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PB53/ PB_{133}	PB_{52}/ PB_{132}	PB_{51}/ PB_{131}	PB_{50}/ PB_{130}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PB_{54}/ PB_{134}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PB_{63}/ PB_{143}	PB_{62}/ PB_{142}	PB61/ PB_{141}	PB_{60}/ PB_{140}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PB_{64}/ PB_{144}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB_{73}/ PB_{153}	PB_{72}/ PB_{152}	PB_{71}/ PB_{151}	PB_{70}/ PB_{150}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB_{74}/ PB_{154}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC_{03}/ PC_{83}	PC_{02}/ PC_{82}	PC_{01}/ PC_{81}	PC_{00}/ PC_{80}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC_{04}/ PC_{84}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PC_{13}/ PC_{93}	PC_{12}/ PC_{92}	PC_{11}/ PC_{91}	PC_{10}/ PC_{90}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PC_{14}/ PC_{94}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PC_{23}/ PC_{103}	PC_{22}/ PC_{102}	PC_{21}/ PC_{101}	PC_{20}/ PC_{100}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PC_{24}/ PC_{104}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PC_{33}/ PC_{113}	PC_{32}/ PC_{112}	PC_{31}/ PC_{111}	PC_{30}/ PC_{110}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PC_{34}/ PC_{114}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PC_{43}/ PC_{123}	PC_{42}/ PC_{122}	PC_{41}/ PC_{121}	PC_{40}/ PC_{120}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PC_{44}/ PC_{124}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PC_{53}/ PC_{133}	PC_{52}/ PC_{132}	PC_{51}/ PC_{131}	PC_{50}/ PC_{130}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PC_{54}/ PC_{134}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PC_{63}/ PC_{143}	PC_{62}/ PC_{142}	PC_{61}/ PC_{141}	PC_{60}/ PC_{140}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PC_{64}/ PC_{144}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC_{73}/ PC_{153}	PC_{72}/ PC_{152}	PC_{71}/ PC_{151}	PC_{70}/ PC_{150}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC_{74}/ PC_{154}

Gradation Palette Table (Variable gradation mode, PWM="0" and MON="0")

(Palette Aj, Palette Bj, Palette Cj, (j=0 to 15))

Palette Value	Gradation Level	Note	Palette Value	Gradation Level	Note
0 0 0 0 0	0/31	Gradation Palette 0 Initial Value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Gradation Palette 8 Initial Value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Gradation Palette 1 Initial Value	1 0 0 1 1	19/31	Gradation Palette 9 Initial Value
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Gradation Palette2 Initial Value	1 0 1 0 1	21/31	Gradation Palette 10 Initial Value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Gradation Palette 3 Initial Value	1 0 1 1 1	23/31	Gradation Palette 11 Initial Value
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Gradation Palette 4 Initial Value	1 1 0 0 1	25/31	Gradation Palette 12 Initial Value
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Gradation Palette 5 Initial Value	1 1 0 1 1	27/31	Gradation Palette 13 Initial Value
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Gradation Palette 6 Initial Value	1 1 1 0 1	29/31	Gradation Palette 14 Initial Value
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Gradation Palette 7 Initial Value	1 1 1 1 1	31/31	Gradation Palette 15 Initial Value

(31-16) Initial COM line

The “Initial COM line” instruction is used to specify the common driver that starts scanning the display data. The line address, corresponding to the initial COM line, is specified by the “Initial display line” instruction.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	SC_3	SC_2	SC_1	SC_0

SC3	SC2	SC1	SC0	Initial COM line (SHIFT=0)	Initial COM line (SHIFT=1)
0	0	0	0	COM_0	COM_{161}
0	0	0	1	COM_1	COM_{160}
0	0	1	0	COM_9	COM_{152}
0	0	1	1	COM_{14}	COM_{146}
0	1	0	0	COM_{17}	COM_{144}
0	1	0	1	COM_{25}	COM_{136}
0	1	1	0	COM_{33}	COM_{128}
0	1	1	1	COM_{41}	COM_{120}
1	0	0	0	COM_{49}	COM_{112}
1	0	0	1	COM_{57}	COM_{104}
1	0	1	0	COM_{65}	COM_{96}
1	0	1	1	COM_{73}	COM_{88}
1	1	0	0	COM_{122}	COM_{39}
1	1	0	1	COM_{130}	COM_{31}
1	1	1	0	COM_{138}	COM_{23}
1	1	1	1	COM_{146}	COM_{15}

SHIFT=0: Positive scan direction ($COM_0 \rightarrow COM_{161}$)
SHIFT=1: Negative scan direction ($COM_{161} \rightarrow COM_0$)

(31-17) Display clock / Duty-1

The “Display clock / Duty-1” instruction is used to enable or disable the display clocks (CL, FLM, FR, and CLK), and to control ON/OFF of the “Duty-1”. For more detail about the “Duty-1”, see (31-11) “Duty cycle ratio”.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	DSE	SON

SON=0: CL, FLM, FR, and CLK outputs level “0”.
SON=1: CL, FLM, FR, and CLK outputs are active.

DSE=0: Duty - 1 OFF
DSE=1: Duty - 1 ON

(31-18) Gradation mode control

The “Gradation mode control” is used to select display mode as follows.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PWM	C256	FDC1	FDC2

● PWM register

PWM=0: Variable gradation mode
(Variable 16-gradation levels out of 32-gradation level of the gradation palette)
PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)

● C256 register

C256=0 256-color mode OFF (4,096-color in the default setting)
C256=1 256-color mode ON

● FDC1 and FDC2 register

FDC1	FDC2	Boost Clock
0	0	×1
0	1	×2
1	0	×4
1	1	×1/2

(31-19) Data bus length

The “Data bus length” instruction is used to select the 8- or 16- bit data bus length and determine the internal or external oscillation. In the 16-bit data bus mode, instruction data must be 16-bit (D_{15} to D_0) as well as display data. However, for the access to the instruction registers, the lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	HSW	ABS	CKS	WLS

- HSW register

HSW =0: High Speed access mode OFF.
HSW=1: High Speed access mode ON (only in the 8-bit data bus length).

- ABS register

ABS=0: ABS mode OFF (normal)
ABS=1: ABS Mode ON

- WLS register

WLS=0: 8-bit data bus length
WLS =1: 16-bit data bus length

- CKS register

CKS =0: Internal oscillation
(The OSC_1 terminal must be fixd “1” or “0”.)
CKS =1: External oscillation
(By the external clock into the OSC_1 or external resister between the OSC_1 and OSC_2. OSC_2 should be open when clock is inputted from OSC_1.)

(31-20) EVR control

The “EVR control” instruction is used to fine-tune the LCD driving voltage (V_{LCD}) so that it is possible to optimize the contrast level for a LCD panel.

This instruction must be programmed by upper 3-bit data first, next lower 4-bit data. And it becomes enabled when the lower 4-bit data is programmed, so that it can prevent unexpected high voltage for the V_{LCD} from being generated.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	DV_3	DV_2	DV_1	DV_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	DV_6	DV_5	DV_4

DV_6	DV_5	DV_4	DV_3	DV_2	DV_1	DV_0	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
1	1	1	1	1	1	1	High

The formula of the V_{LCD} is shown below.

V_{LCD} [V] = 0.5 x V_{REG} + M (V_{REG} − 0.5 x V_{REG}) / 127

$V_{BA} = V_{EE} \times 0.9$
$V_{REG} = V_{REF} \times N$

V_{BA} : Output voltage of the reference voltage generator
V_{REF} : Input voltage of the voltage regulator
V_{REG} : Output voltage of the voltage regulator
N : Register value for the voltage booster
M : Register value for the EVR

(31-21) Frequency control

The “Frequency control” instruction is used to control the frame frequency for a LCD panel.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	Rf_2	Rf_1	Rf_0

● Rfx register (x=0, 1, 2)

The “Rfx” register is used to determine the feed back resister value for the internal oscillator and it is possible to adjust the frame frequency for the LCD modules.

Rf 2	Rf 1	Rf 0	Feedback resistor value
0	0	0	Reference value
0	0	1	0.8 x reference value
0	1	0	0.9 x reference value
0	1	1	1.1 x reference value
1	0	0	1.2 x reference value
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

(31-22) Discharge ON/OFF

Discharge circuit is used to discharge the electric charge of the capacitors on the V_1 to V_4 and the V_{LCD} terminals. The “Discharge ON/OFF” instruction is usually required just after the internal power supply is turned off by setting “0” into the “DCON” and “AMPON” registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	*	*	DIS

DIS=0: Discharge OFF
DIS=1: Discharge ON

(31-23) Instruction register address

The “Instruction register address” is used to specify the instruction register address, so that it is possible to read out the contents of the instruction registers in combination with the “Instruction register read” instruction.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	RA_3	RA_2	RA_1	RA_0

(31-24) Instruction register read

The “Instruction register read” instruction is used to read out the contents of the instruction register in combination with the “Instruction register address” instruction.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	*	*	*	Internal register data read			

(31-25) Window end column address

The “Window end column address” is used to specify the column address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 4-bit data can be programmed.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	EX_3	EX_2	EX_1	EX_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	EX_7	EX_6	EX_5	EX_4

(31-26) Window end row address set

The “Window end row address” is used to specify the row address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 4-bit data can be programmed.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	EY_3	EY_2	EY_1	EY_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	EY_7	EY_6	EY_5	EY_4

(31-27) Initial reverse line

The “Initial reverse line” instruction is used to specify the initial reverse line address for the reverse line display. Lower 4-bit data must be programmed first, next upper 4-bit data. It is programmed in between 00_H and $A1_H$ and the line address beyond $A1_H$ is inhibited. The address relation: LSi < LEi (i=7 to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LS_3	LS_2	LS_1	LS_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	LS_7	LS_6	LS_5	LS_4

(31-28) Last reverse line

The “Last reverse line” instruction is used to specify the last reverse line address for the reverse line display. Lower 4-bit must be programmed first, next upper 4-bit data. It is programmed in between 00_H and $A1_H$ and the line address beyond $A1_H$ is inhibited. The address relation: LSi < LEi (i=7 to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	LE_3	LE_2	LE_1	LE_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	LE_7	LE_6	LE_5	LE_4

(31-29) Reverse line display ON/OFF

The “Reverse line display ON/OFF” is used to enable or disable the reverse line display for the blink operation and determine the reverse line display mode.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	*	*	BT	LREV

- LREV register

  The “LREV” register is used to enable or disable the reverse line display.

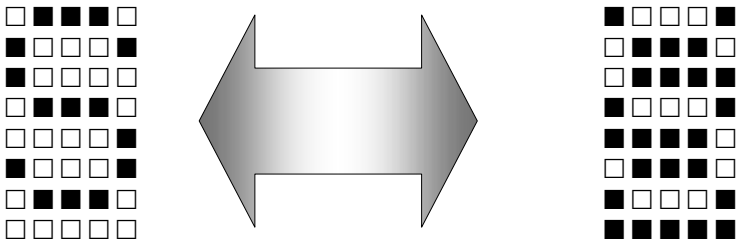
  LREV =0: Reverse line display OFF (Normal)
  LREV =1: Reverse line display ON

● BT register

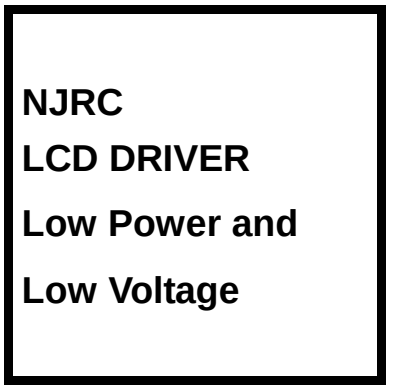
The “BT” register is used to determine the reverse line display mode in the reverse line display ON (LREV=1) status.

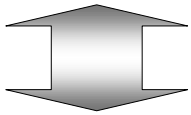
BT =0: Normal reverse line display
BT =1: Blink once every 32 frames

Display examples in the LREV=”1” and BT=”1”

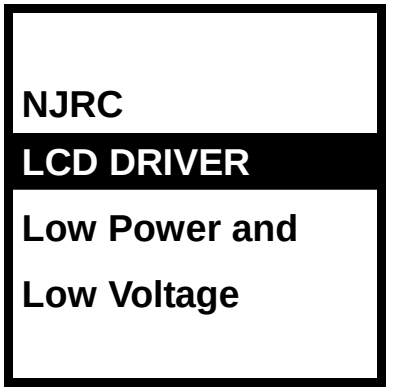


Blink once every 32 frames





Blink once every 32 frames



←Initial reverse line address

←Last reverse line address

(31-30) Gradation Palette setting control

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PS

PS=0: Lower 8 Gradation setting
PS=1: Upper 8 Gradation setting

(31-31) PWM control

The "PWM control" is used to determine the PWM type for the segment waveforms, where the type can be specified for each of the SEGAi, SEGBi and SEGCi (i=0-127) drivers.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PWMS	PWMA	PWMB	PWMC

- PWMS register

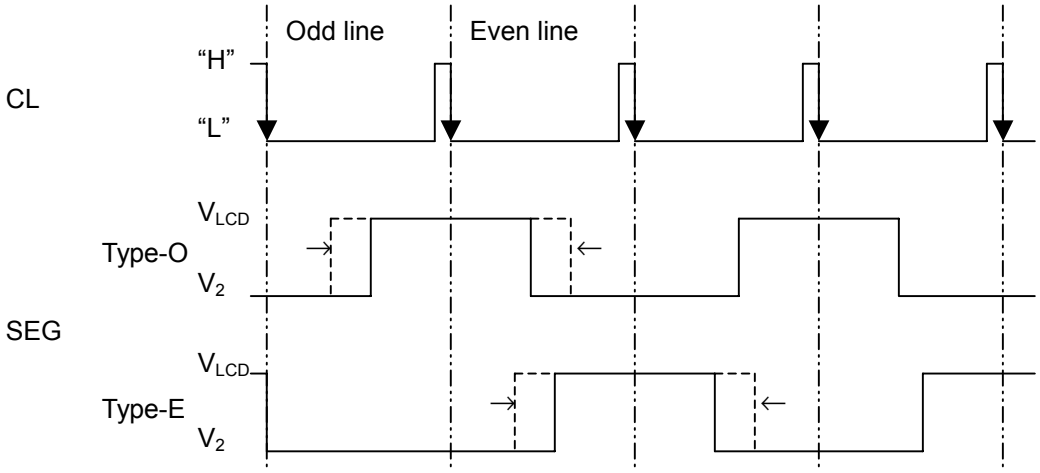
PWMS=0: Type 1
PWMS=1: Type 2

- PWMA, B and C registers

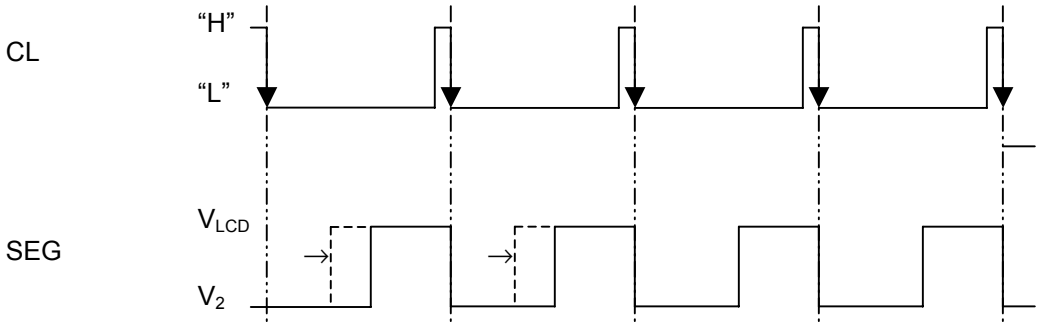
The "PWMA, PWMB and PWMC" registers are used to select the type 1-O or type 1-E.

PWMZ=0 (Z=A, B and C): Type 1-O
PWMZ=1 (Z=A, B and C): Type 1-E

PWM type1 (PWMS="0")



PWM type2 (PWMS="1")



(32) The relationship between Common drivers and row addresses

Row address assignment of common drivers is programmed by the " SHIFT " register of the " Display control (1) " , " Duty cycle ratio ", " Internal display line " and " Initial COM line " instructions

When initial display line is "0"

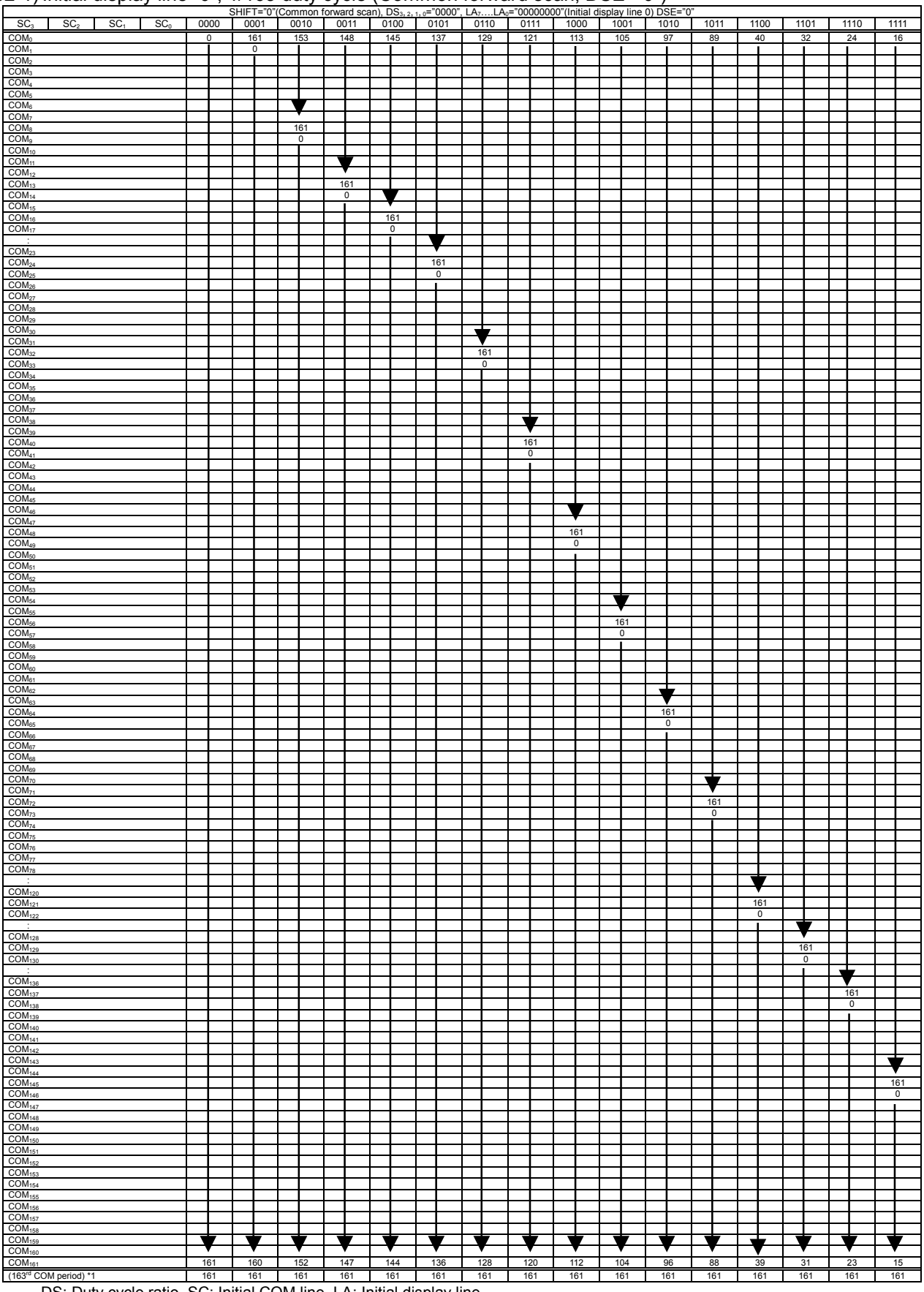
If the " SHIFT " is " 0 ", the scan direction is normal. When the " LA_0 to LA_7 " registers of the " Initial display line "instruction is " 0 ", the " MY " corresponding to the initial COM line is " 0 " and is increasing during display.

When initial display line is not "0"

If the " SHIFT " is " 1 ", the scan direction is inversed. When the " LA_0 to LA_7 " registers of the " Initial display line "instruction is not " 0 ", the " MY " corresponding to the initial COM line is this setting value and is increasing during display.

The following are examples of setting the start-line 0 or 5 at 1/163(DSE=0), 1/80(DSE=1), or 1/16(DSE=1) duty.

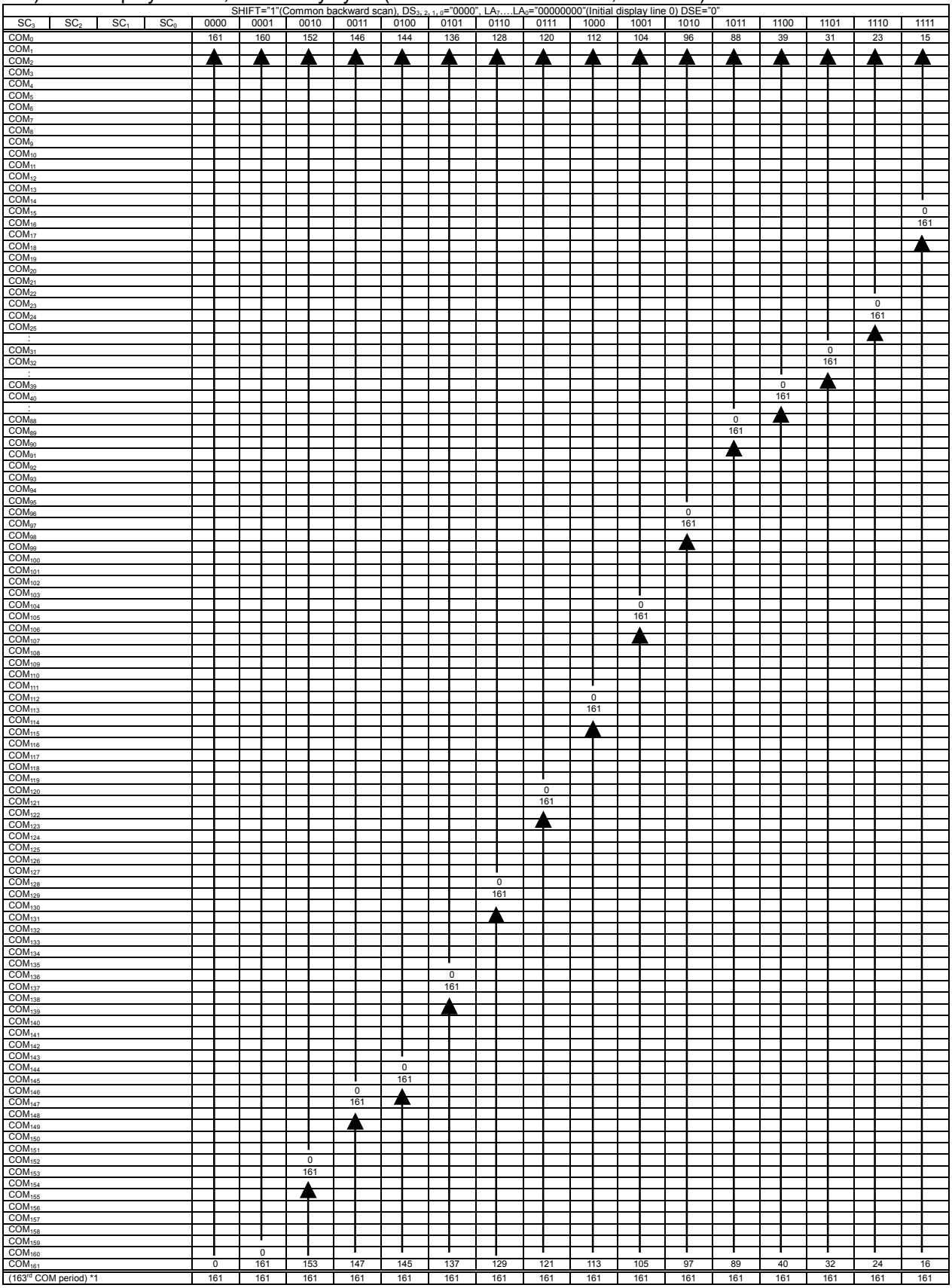
(32-1) Initial display line “0”, 1/163 duty cycle (Common forward scan, DSE=”0”)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 163rd COM period is not selected.

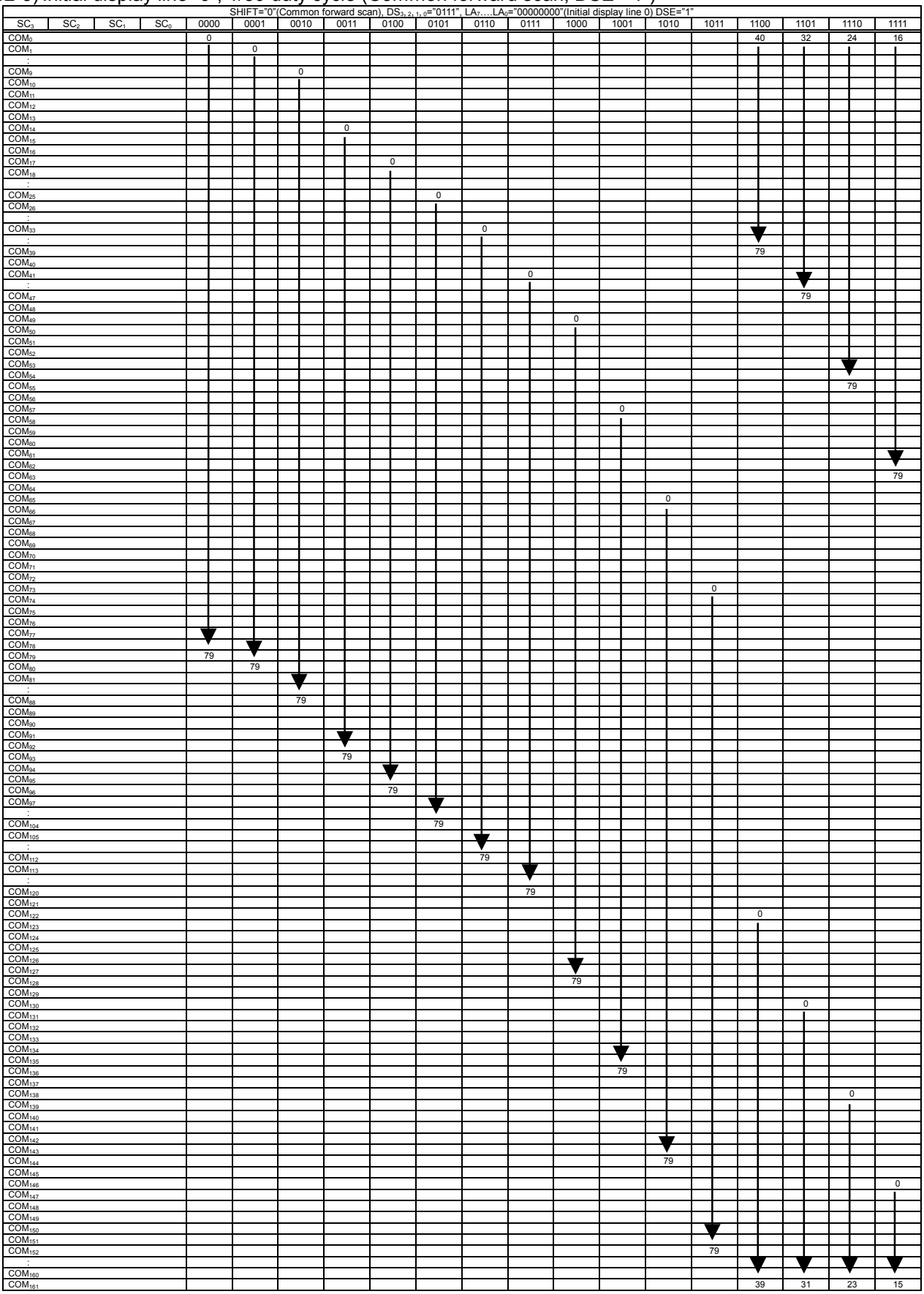
(32-2) Initial display line “0”, 1/163 duty cycle (Common backward scan, DSE=”0”)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

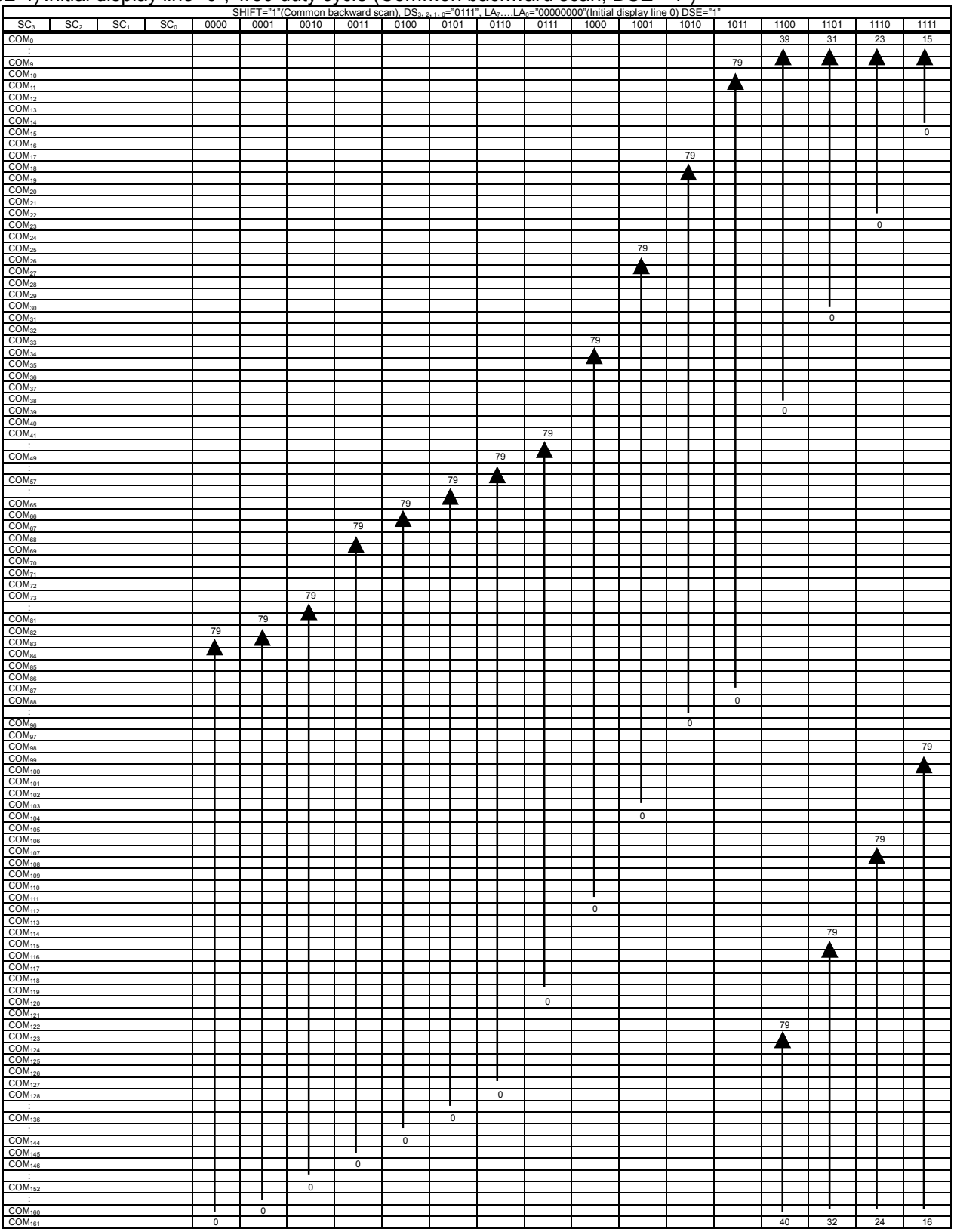
*1 : 163rd COM period is not selected.

(32-3) Initial display line “0”, 1/80 duty cycle (Common forward scan, DSE=”1”)



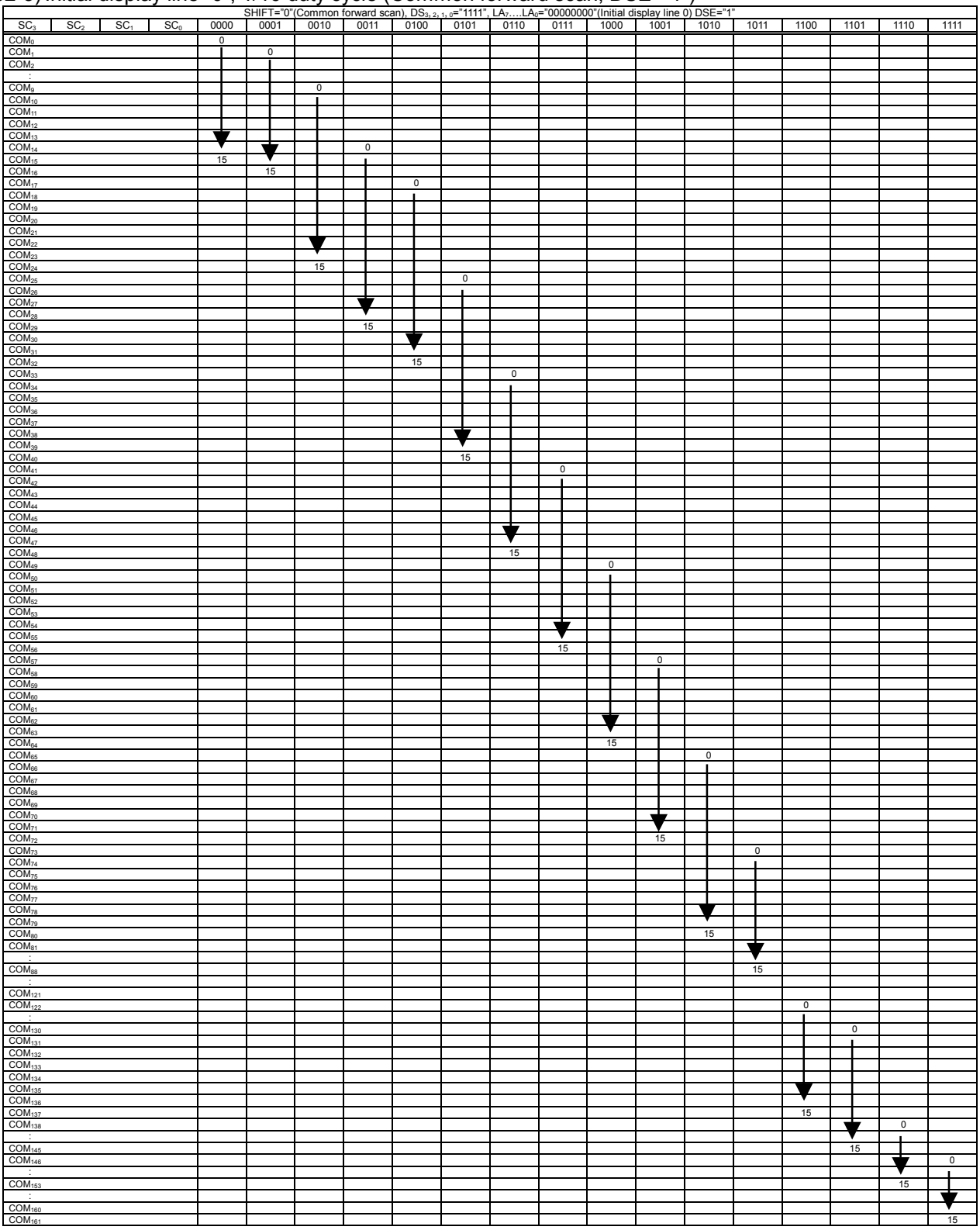
DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(32-4) Initial display line “0”, 1/80 duty cycle (Common backward scan, DSE=”1”)



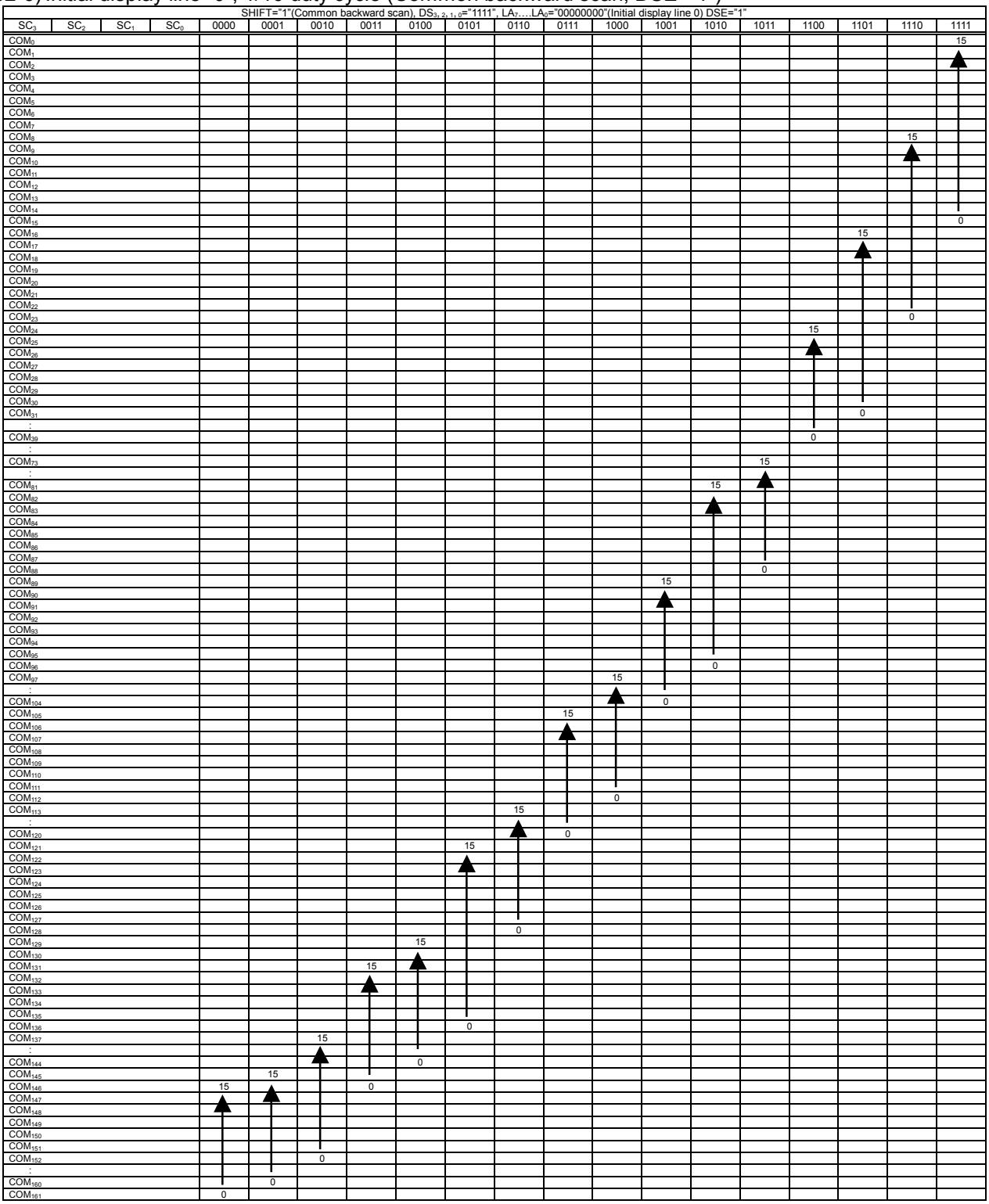
DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(32-5) Initial display line “0”, 1/16 duty cycle (Common forward scan, DSE=”1”)



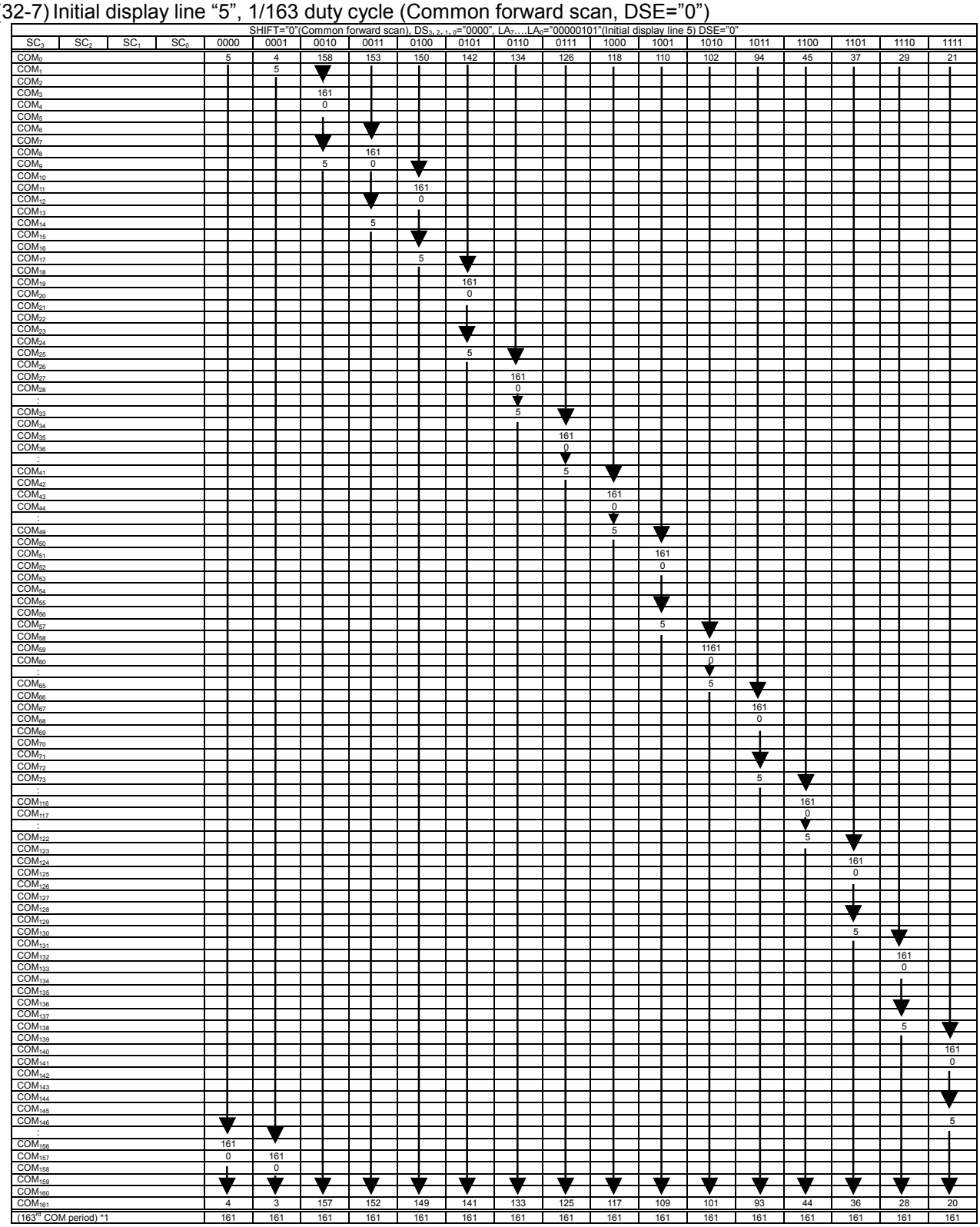
DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(32-6) Initial display line “0”, 1/16 duty cycle (Common backward scan, DSE=”1”)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

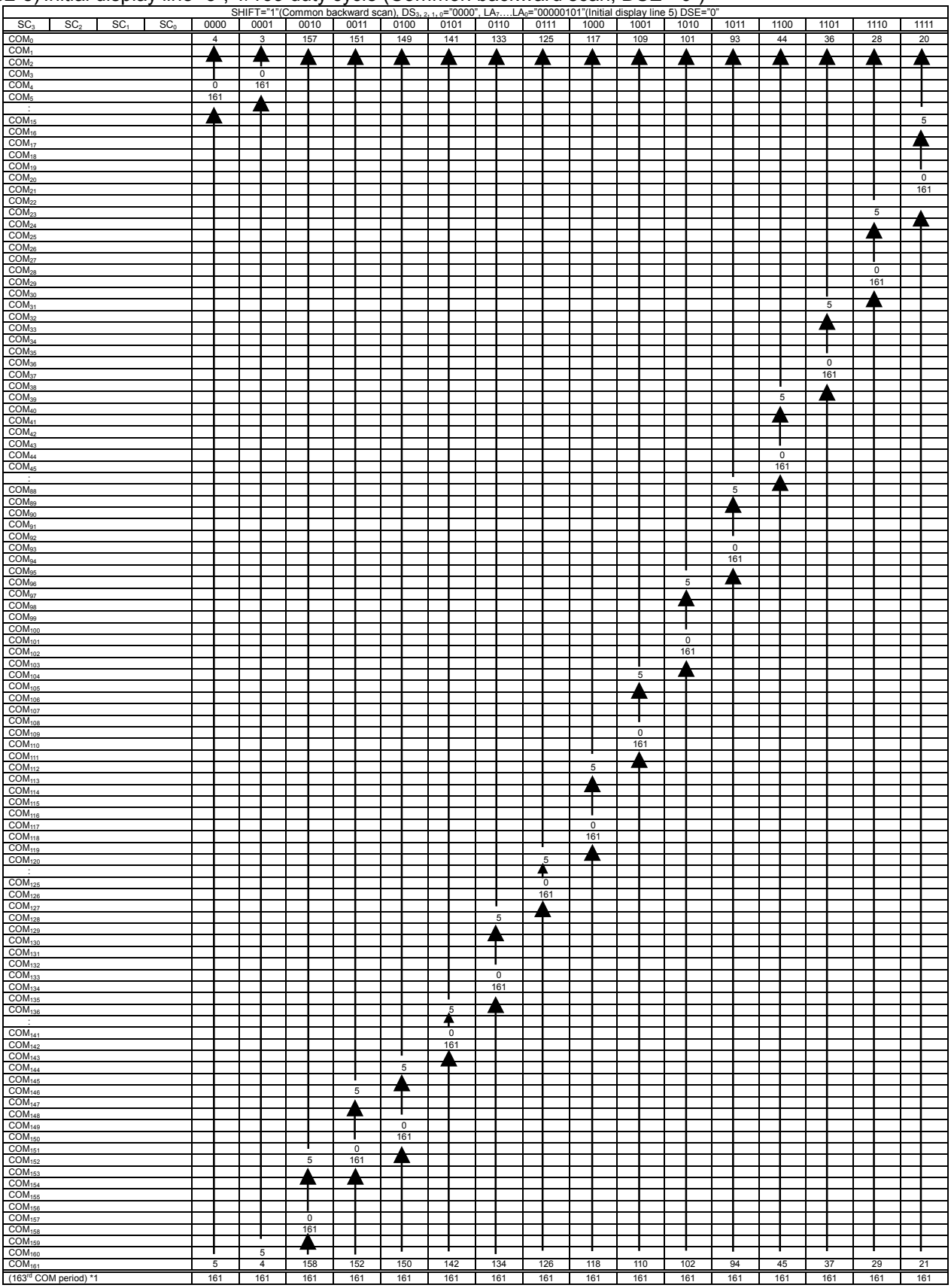
(32-7) Initial display line “5”, 1/163 duty cycle (Common forward scan, DSE=”0”)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 163rd COM period is not selected.

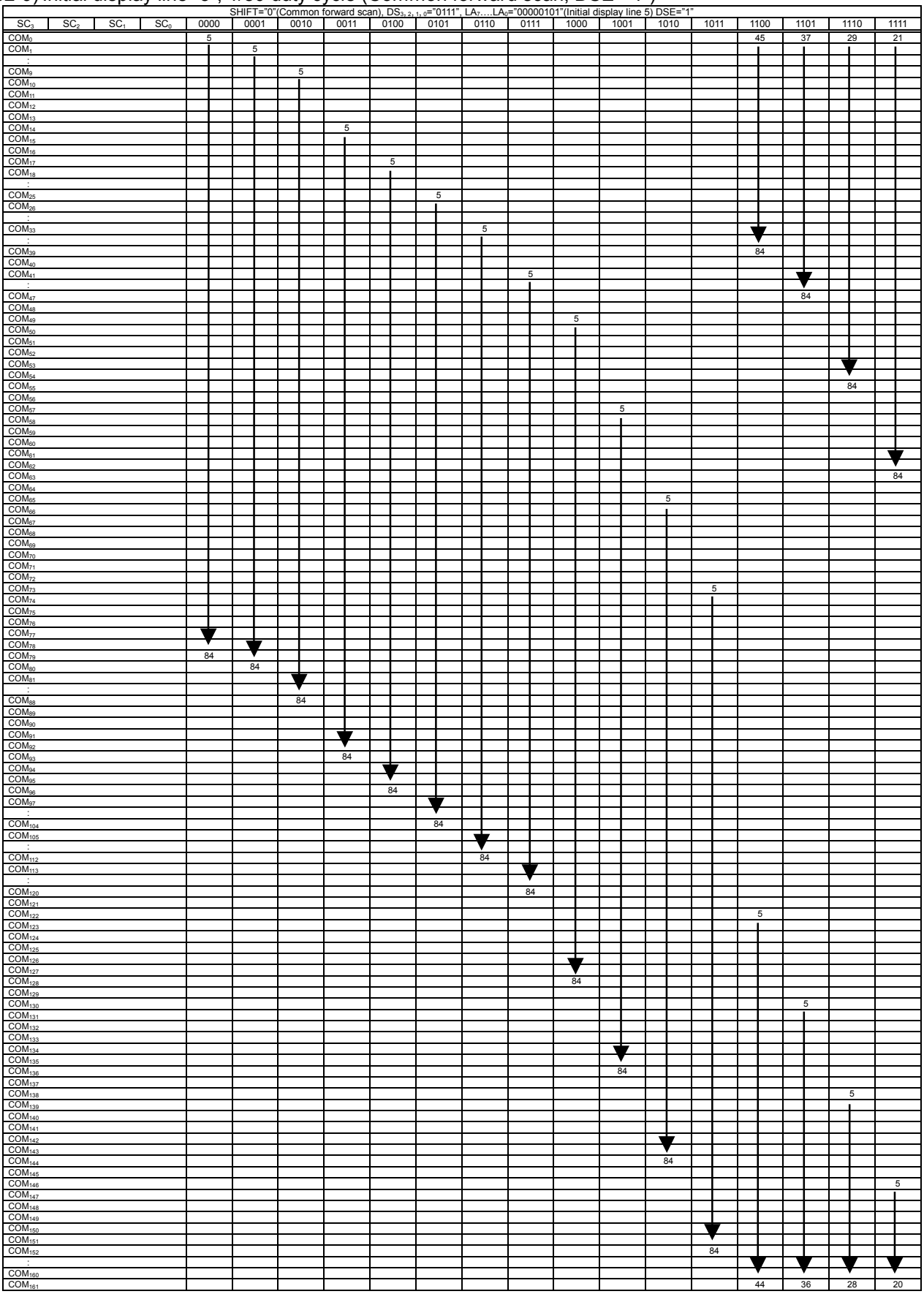
(32-8) Initial display line “5”, 1/163 duty cycle (Common backward scan, DSE=”0”)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

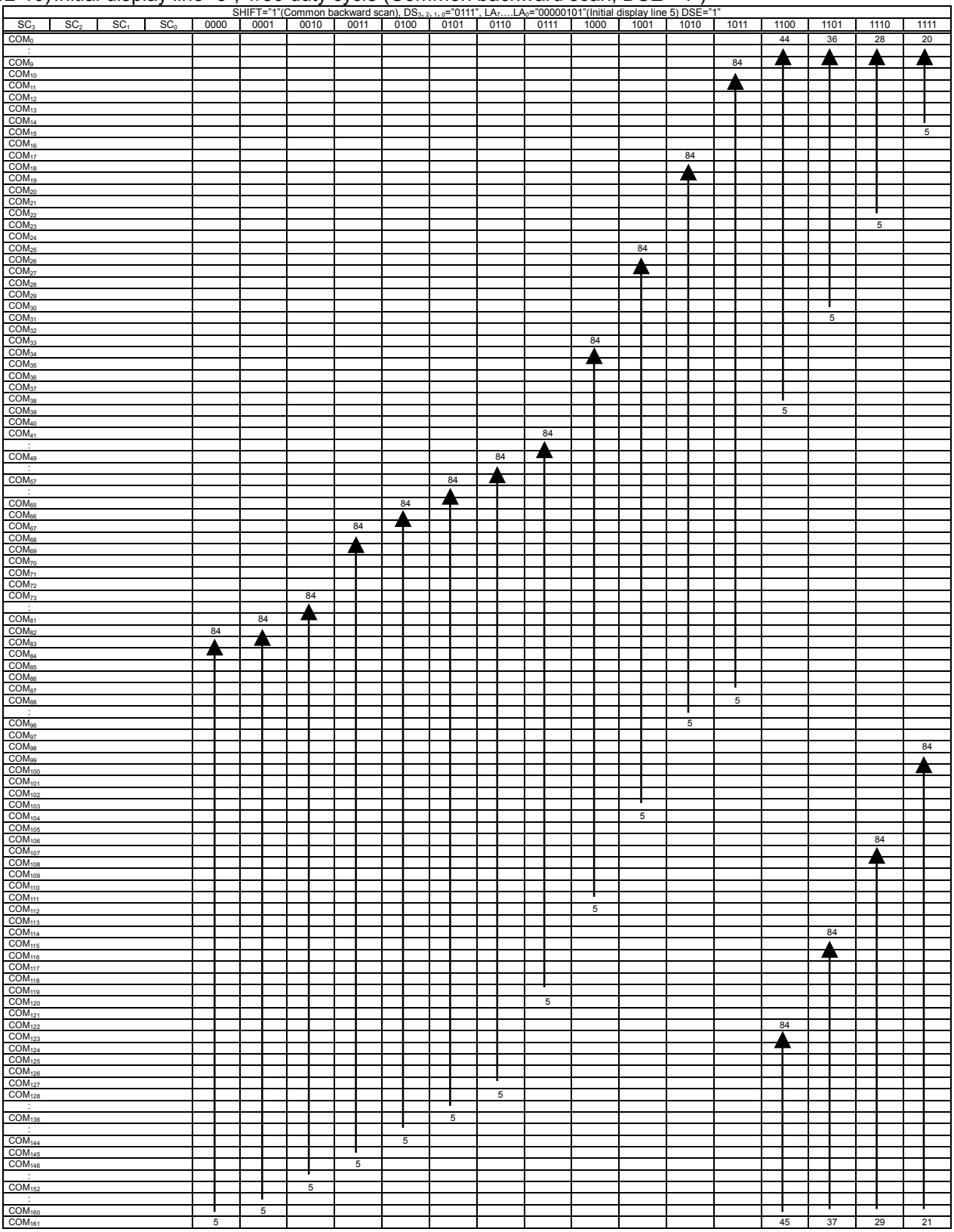
*1 : 163rd COM period is not selected.

(32-9) Initial display line “5”, 1/80 duty cycle (Common forward scan, DSE=”1”)



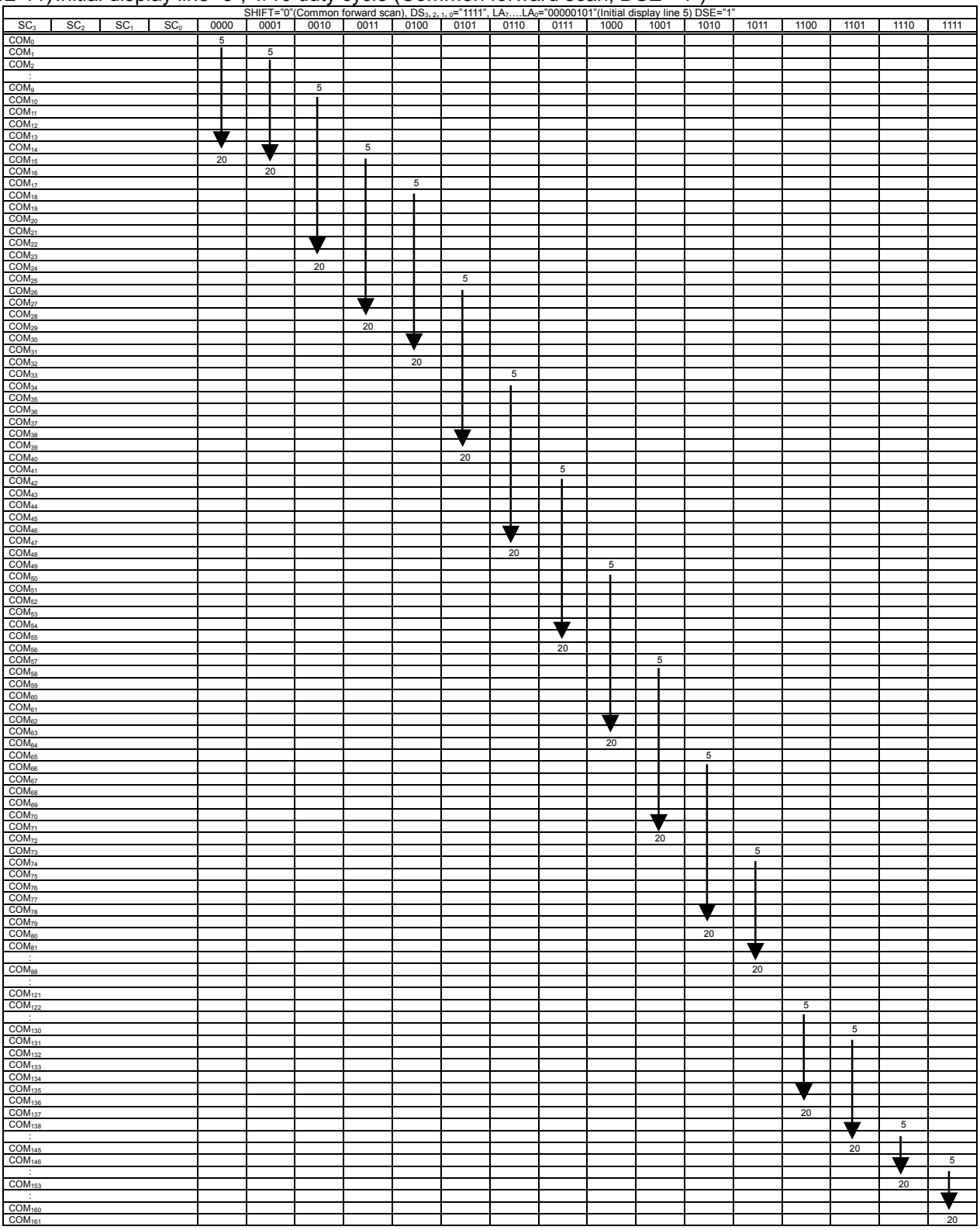
DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(32-10) Initial display line “5”, 1/80 duty cycle (Common backward scan, DSE=”1”)



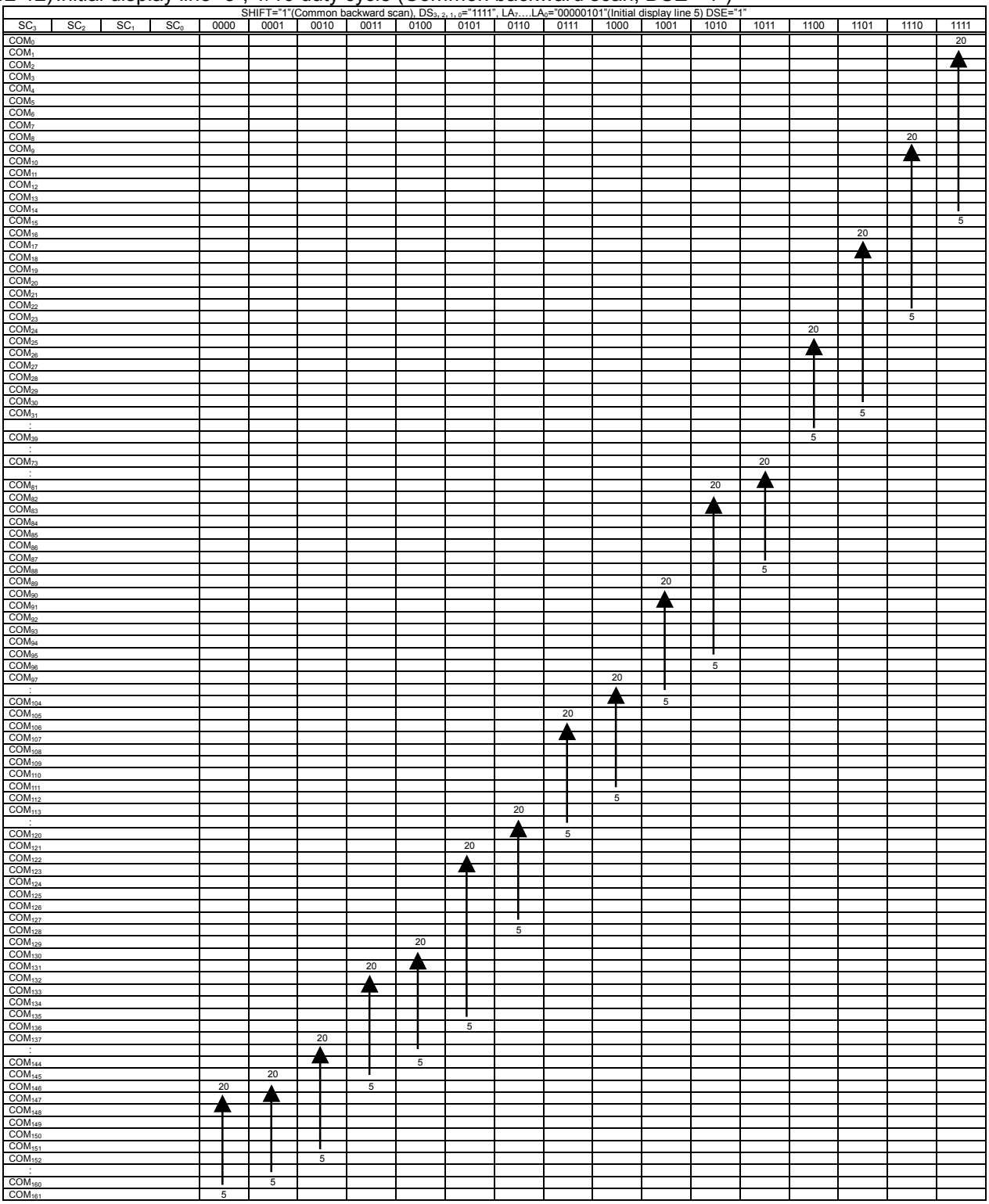
DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(32-11) Initial display line “5”, 1/16 duty cycle (Common forward scan, DSE=”1”)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(32-12) Initial display line “5”, 1/16 duty cycle (Common backward scan, DSE=”1”)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	V_{SS}=0V Ta = +25°C	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +19.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +19.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +19.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to V_{LCD} + 0.3	V
Input Voltage	V_I		*1	-0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{stg}			-45 to +125	°C

Note 1) D_0 to D_{15}, CSb, RS, RDb, WRb, OSC_1, RESb, $TEST_1$, $TEST_2$, terminals.
Note 2) To stabilize the voltage booster operation, decoupling capacitors must be connected between the V_{DD} and V_{SS} pins and between the V_{EE} and V_{SSH} pins.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
	V_{EE}	V_{EE}	2.4		3.3	V	*3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	*5
Operating Temperature	T_{opr}		-30		85	°C	

Note1) Applies to the condition when the reference voltage generator is not used.
Note2) Applies to the condition when the reference voltage generator is used.
Note3) Applies to the condition when the voltage booster is used.
Note4) The following relationship among the supply voltages must be maintained.
$V_{SS}<V_4<V_3<V_2<V_1<V_{LCD}\leq V_{OUT}$
Note5) The relationship: $V_{REF}<V_{EE}$ must be maintained.

■ DC CHARACTERISTICS 1

V_{SS} = 0V, V_{DD} = +1.7 to +3.3V, Ta = -30 to +85°C

PARAMETER	SYM BOL	CONDITION		MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}			0.8 V_{DD}		V_{DD}	V	*1
Low level input voltage	V_{IL}			0		0.2V_{DD}	V	*1
High level output voltage	V_{OH1}	I_{OH} = -0.4mA		V_{DD} - 0.4			V	*2
Low level output voltage	V_{OL1}	I_{OL} = 0.4mA				0.4	V	*2
High level output voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DD} - 0.4			V	*3
Low level output voltage	V_{OL2}	I_{OL} = 0.1mA				0.4	V	*3
Input leakage current	I_{LI}	V_I = V_{SS} or V_{DD}		-10		10	µA	*4
Output leakage current	I_{LO}	V_I = V_{SS} or V_{DD}		-10		10	µA	*5
Driver ON-resistance	R_{ON1}	$\|\Delta V_{ON}\|$ = 0.5V	V_{LCD} = 10V		1	2	kΩ	*6
			V_{LCD} = 6V		2	4		
Stand-by current	I_{STB}	CSb=V_{DD}, Ta=25°C	V_{DD} = 3V			15	µA	*7
Internal oscillation Frequency	f_{OSC1}	V_{DD} = 3V Ta = 25°C		625	763	900	kHz	*8
	f_{OSC2}			141	172	203		*9
	f_{OSC3}			20.5	25	29.5		*10
External oscillation Frequency	f_{r1}	Rf=10kΩ			750		kHz	*11
	f_{r2}	Rf=51kΩ			185			
	f_{r3}	Rf=390kΩ			27.2			
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 7) RL = 500kΩ (V_{OUT} - V_{SS})		(N x V_{EE}) x 0.95			V	*12
Supply current (1)	I_{DD1}	V_{DD} = 2.5V, 7-time booster Whole ON pattern			870	1300	µA	*13
Supply current (2)	I_{DD2}	V_{DD} = 2.5V, 7-time booster Checker pattern			1060	1590		
Supply current (3)	I_{DD3}	V_{DD} = 3V, 6-time booster Whole ON pattern			760	1140		
Supply current (4)	I_{DD4}	V_{DD} = 3V, 6-time booster Checker pattern			930	1400		
Supply current (5)	I_{DD5}	V_{DD} = 3V, 5-time booster Whole ON pattern			520	780		
Supply current (6)	I_{DD6}	V_{DD} = 3V, 5-time booster Checker pattern			650	980		
Supply current (7)	I_{DD7}	V_{DD} = 3V, 4-time booster Whole ON pattern			360	540		
Supply current (8)	I_{DD8}	V_{DD} = 3V, 4-time booster Checker pattern			450	680		
V_{BA} Operating voltage	V_{BA}	V_{EE} = 2.4 to 3.3V		(0.9 V_{EE}) x 0.98	0.9 V_{EE}	(0.9 V_{EE}) x 1.02	V	*14
V_{REG} Operating voltage	V_{REG}	V_{EE} = 2.4 to 3.3V V_{REF} = 0.9 x V_{EE} N-time booster (N=2 to 7)		(V_{REF} x N) x 0.97	(V_{REF} x N)	(V_{REF} x N) x 1.03	V	*15
Output Voltage	V_2			-100	0	+100	mV	*16
	V_3			-100	0	+100		
	V_{D12}			-30	0	+30		
	V_{D34}			-30	0	+30		
	V_{D24}			-30	0	+30		

■ CLOCK and FRAME FREQUENCY

PARAMETER	SYMBOL	Display mode	Display duty cycle ratio (1/D) <DSE=0>				NOTE
			1/163 to 1/97	1/81 to 1/57	1/49 to 1/33	1/25 to 1/17	
Internal clock	f_{OSC}	16 Gradation mode	f_{OSC} / (62xD)	f_{OSC} / (62xDx2)	f_{OSC} / (62xDx4)	f_{OSC} / (62xDx8)	FLM
		Simplified 8 gradation mode	f_{OSC} / (14xD)	f_{OSC} / (14xDx2)	f_{OSC} / (14xDx4)	f_{OSC} / (14xDx8)	
		B&W mode	f_{OSC} / (2xD)	f_{OSC} / (2xDx2)	f_{OSC} / (2xDx4)	f_{OSC} / (2xDx8)	
External clock	f_{CK}	16 Gradation mode	f_{CK} / (62xD)	f_{CK} / (62xDx2)	f_{CK} / (62xDx4)	f_{CK} / (62xDx8)	
		Simplified 8 gradation mode	f_{CK} / (14xD)	f_{CK} / (14xDx2)	f_{CK} / (14xDx4)	f_{CK} / (14xDx8)	
		B&W mode	f_{CK} / (2xD)	f_{CK} / (2xDx2)	f_{CK} / (2xDx4)	f_{CK} / (2xDx8)	

APPLIED TERMINALS and CONDITIONS

Note 1) D_0-D_{15}, CSb, RS, RDb, WRb, P/S, SEL68, RESb
Note 2) D_0-D_{15}
Note 3) CL, FLM, FR, CLK
Note 4) CSb, RS, SEL68, RDb, WRb, P/S, RESb, OSC_1
Note 5) D_0-D_{15} in the high impedance

Note 6) $SEGA_0$-$SEGA_{127}$, $SEGB_0$-$SEGB_{127}$, $SEGC_0$-$SEGC_{127}$, COM_0-COM_{161}
- Defines the resistance between the COM/SEG terminals and each of the power supply terminals (V_{LCD}, V_1, V_2, V_3 and V_4) at the condition of 0.5V deference and 1/9 LCD bias ratio.

Note 7) V_{DD}
- The oscillator is halted, CSb="1" (disabled), No-load on the COM/SEG drivers

Note 8) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the variable gradation mode.

Note 9) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the fixed gradation mode.

Note 10) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the Black & White mode.

Note 11) V_{DD}=3V, Ta=25°C

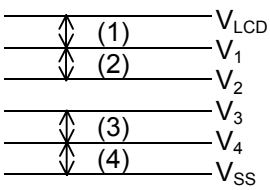
Note 12) V_{OUT}
- Applies to the condition when the internal voltage booster, the internal oscillator and internal power circuits are used.
- V_{EE}=2.4V to 3.3V, EVR= (1,1,1,1,1,1,1), 1/5 to 1/12 LCD bias, 1/163 duty cycle, No-load on COM/SEG drivers.
- RL=500KΩ between the V_{OUT} and the V_{SS}, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="1", AMPON="1"

Note 13) V_{DD}
- Applies to the condition when using the internal oscillator and internal power circuits, no access between the LSI and MPU.
- EVR= (1,1,1,1,1,1,1), All pixels turned-on or checkerboard display in gradation mode. No-load on the COM/SEG drivers.
- V_{DD}=V_{EE}, V_{REF}=0.9V_{EE}, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="1", AMPON="1", NLIN="0" 1/163 Duty cycle, Ta=25°C

Note 14) V_{BA}
- Applies to the condition that V_{BA}=V_{REF} and voltage booster N= 1. When DCON="0", V_{OUT}=13.5V input.

Note 15) V_{REG}
- V_{EE}=2.4V to 3.3V, V_{REF}=0.9V_{EE}, V_{OUT}=18V, 1/5 to 1/12 LCD bias ratio, 1/163 duty cycle, EVR=(1,1,1,1,1,1,1)
- Checkerboard display, No-load on the COM/SEG drivers, the voltage booster N=2 to 7 CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="0", AMPON="1", NLIN="0"

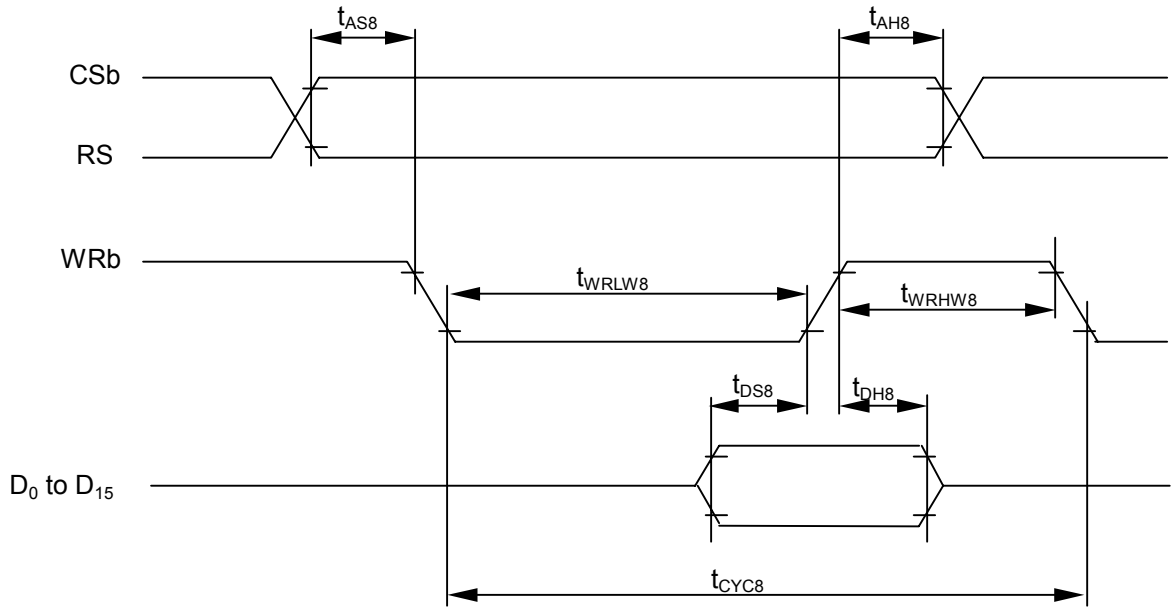
Note 16) V_{LCD}, V_1, V_2, V_3, V_4
- V_{EE}=3.0V, V_{REF}=0.9V_{EE}, V_{OUT}=15V, 1/5 to 1/12 LCD Bias, EVR= (1,1,1,1,1,1,1), Display OFF, No-load on the COM/SEG drivers, voltage booster N=5, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="0", AMPON="1"



V_{D12}: (1)-(2)
V_{D34}: (3)-(4)
V_{D24}: (2)-(4)

■ AC CHARACTERISTICS

- Write operation (80-type MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		90 35 35		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		30 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

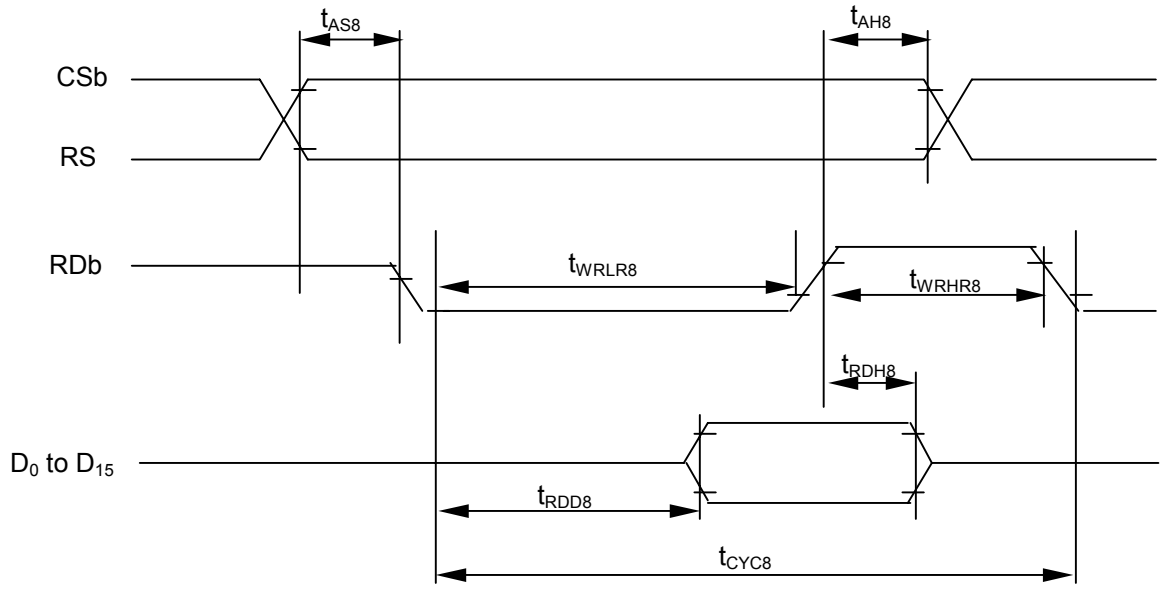
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		160 70 70		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		180 80 80		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		70 10		ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Read operation (80-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	T_{RDD8} T_{RDH8}	CL=15pF	 0	60	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

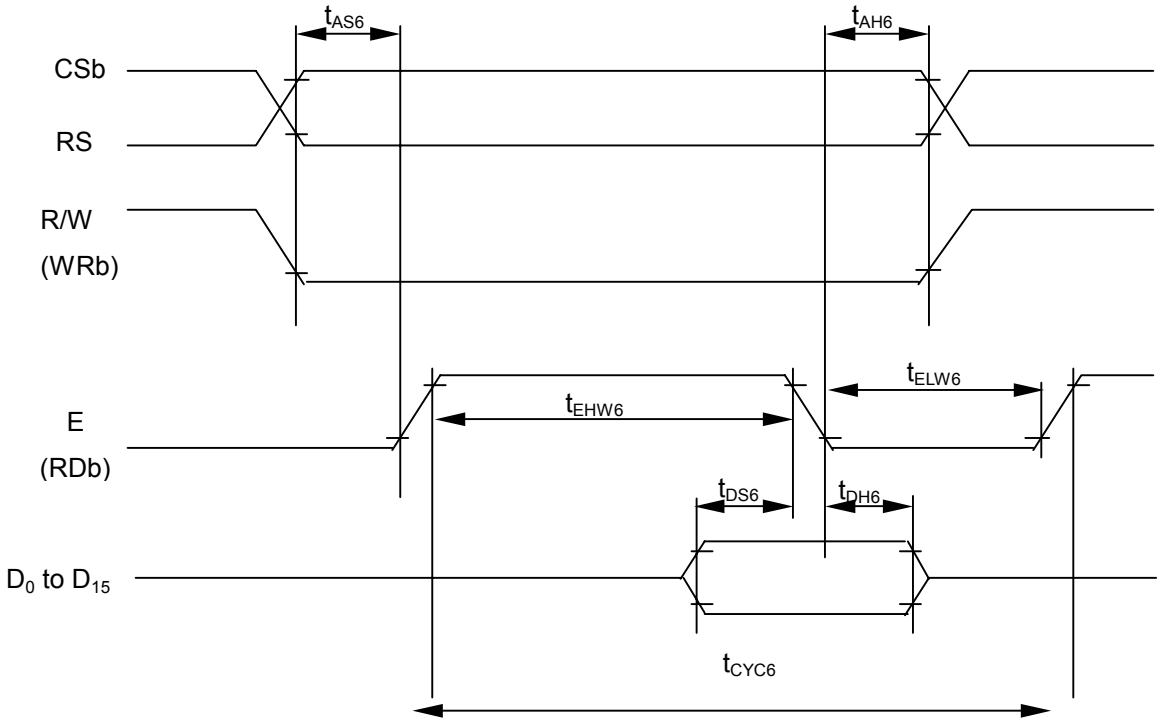
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	T_{RDD8} T_{RDH8}	CL=15pF	 0	60	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		250 120 120		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	110	ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Write operation (68-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		90 35 35		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

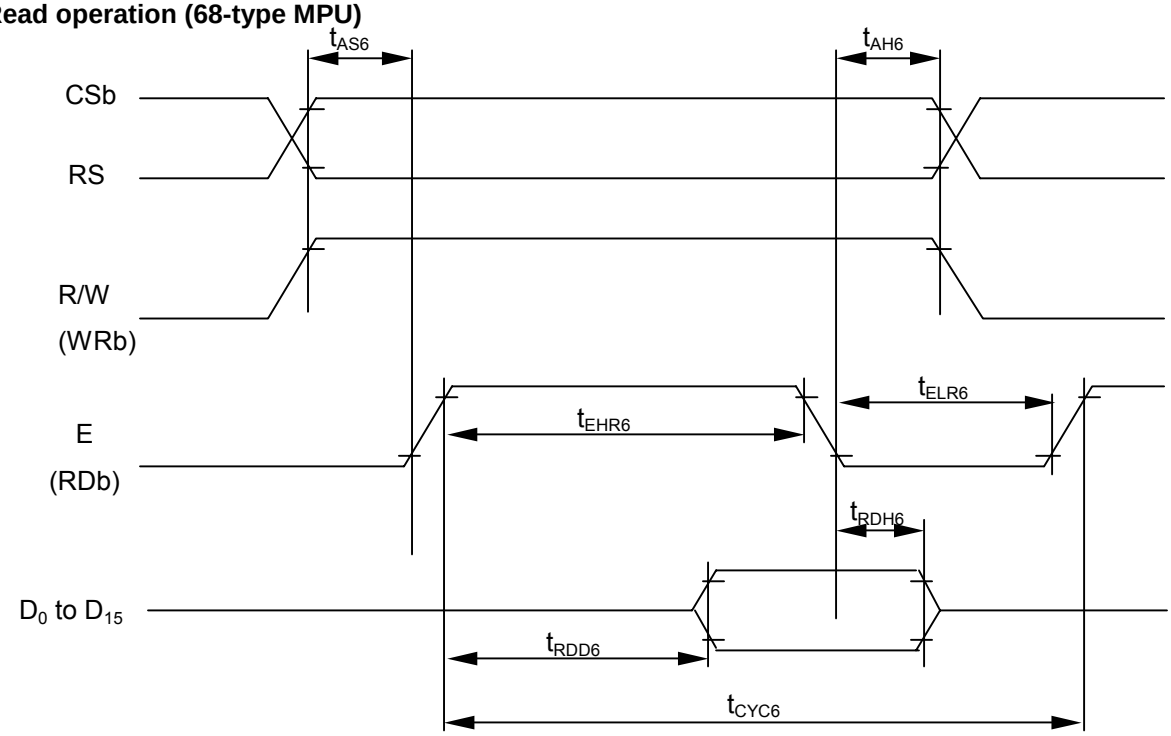
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		160 70 70		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		50 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		180 80 80		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		70 10		ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Read operation (68-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	70	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

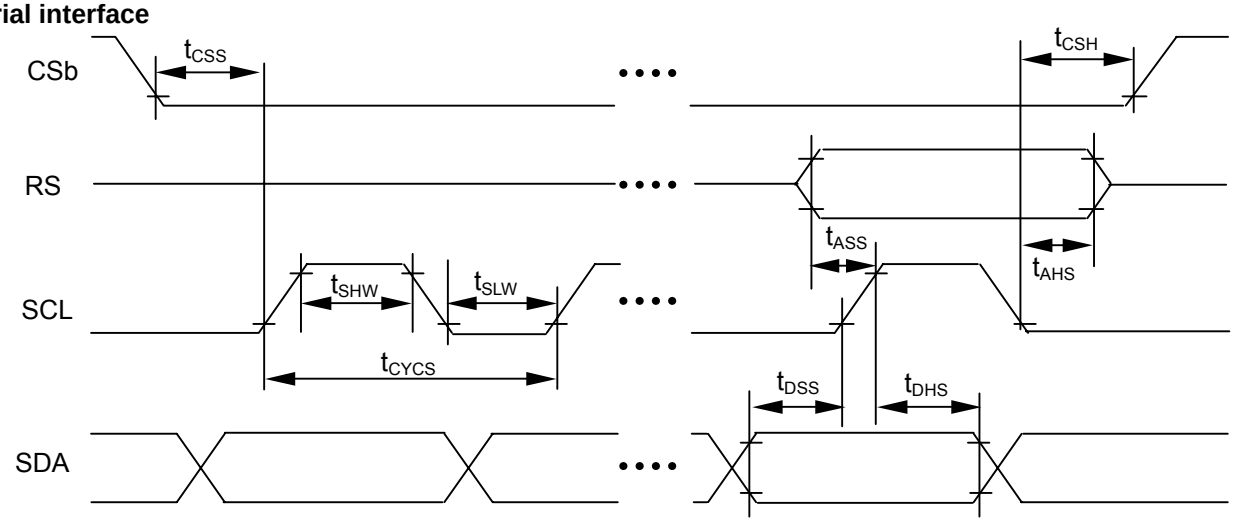
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	70	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		250 120 120		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	110	ns ns	D0 to D15

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Serial interface**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

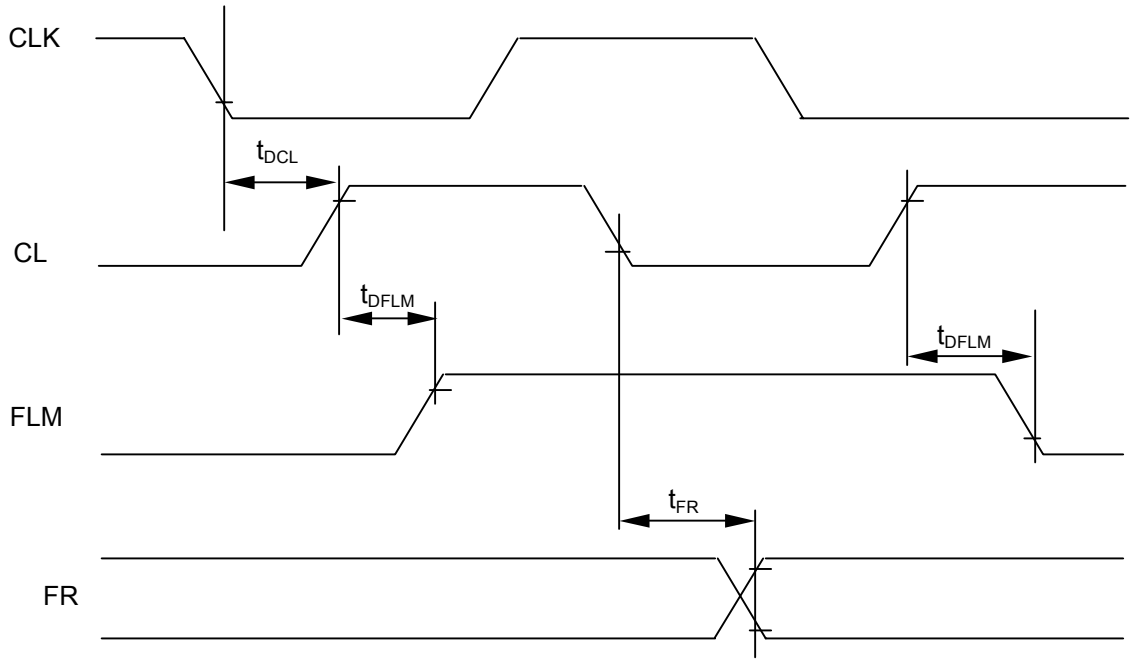
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	SCL
SCL "H" level pulse width	t_{SHW}		35		ns	
SCL "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Display control timing**



Output timing (V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

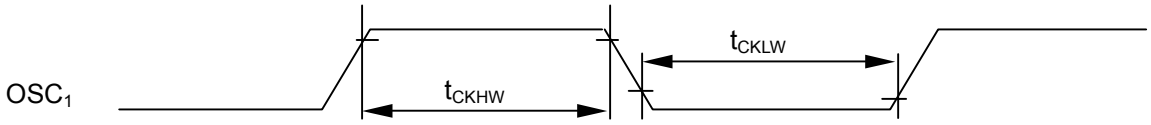
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Output timing (V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Input clock timing**

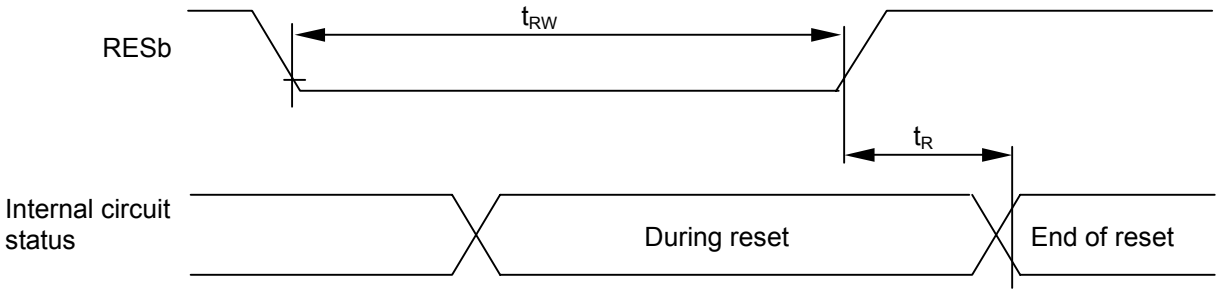


(V_{DD}=1.7 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC_1 "H" level pulse width (1)	t_{CKHW1}		0.555	0.800	μs	OSC_1
OSC_1 "L" level pulse width (1)	t_{CKLW1}		0.555	0.800	μs	*1
OSC_1 "H" level pulse width (2)	t_{CKHW2}		2.46	3.54	μs	OSC_1
OSC_1 "L" level pulse width (2)	t_{CKLW2}		2.46	3.54	μs	*2
OSC_1 "H" level pulse width (3)	t_{CKHW3}		16.9	24.4	μs	OSC_1
OSC_1 "L" level pulse width (3)	t_{CKLW3}		16.9	24.4	μs	*3

Note) Each timing is specified based on 20% and 80% of V_{DD}.
Note 1) Applied to the variable gradation mode / MON="0",PWM="0"
Note 2) Applied to the fixed gradation mode / MON="0",PWM="1"
Note 3) Applied to the B&W mode / MON="1"

- Reset input timing



(V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	µs	
RESb "L" level pulse width	t_{RW}		10.0		µs	RESb

(V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	µs	
RESb "L" level pulse width	t_{RW}		10.0		µs	RESb

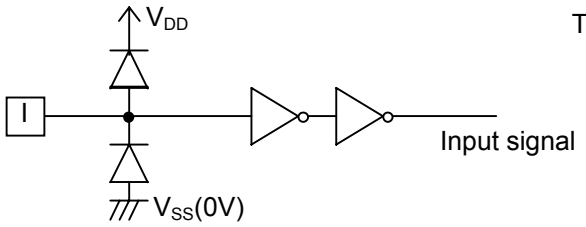
Note) Each timing is specified based on 20% and 80% of V_{DD}.

- Typical characteristic

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Basic delay time of gate	Ta=+25°C, V_{SS}=0V, V_{DD}=3.0V		10		ns

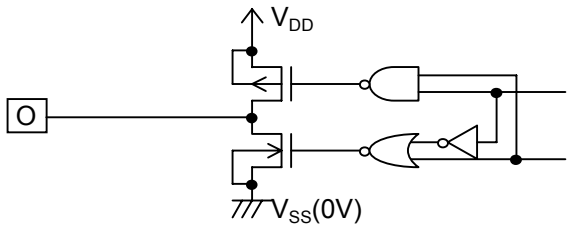
- Input output terminal type

(a) Input circuit



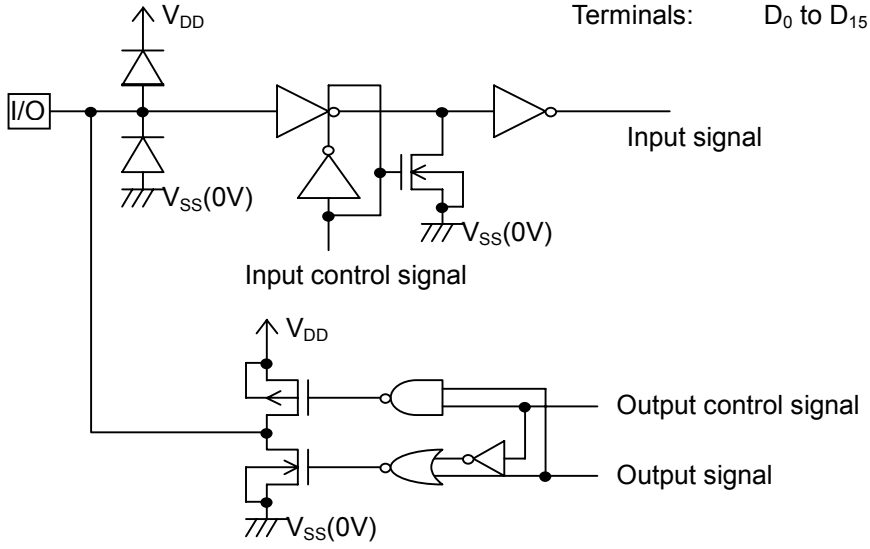
Terminals: CSb, RS, RDb, WRb, SEL68, P/S, RESb

(b) Output circuit



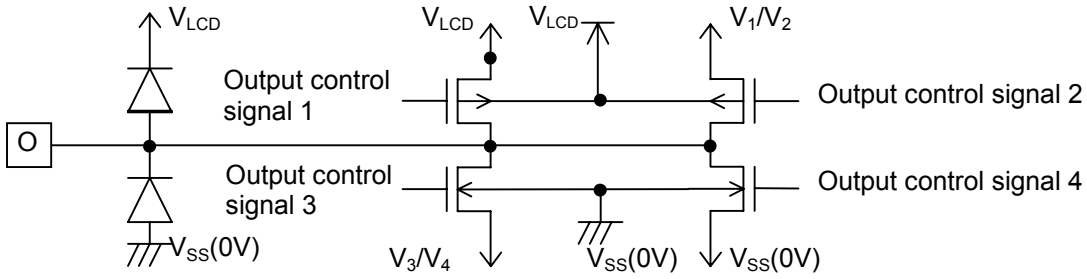
Terminals: FLM, CL, FR, CLK

(c) Input/Output circuit



Terminals: D_0 to D_{15}

(d) Display output circuit

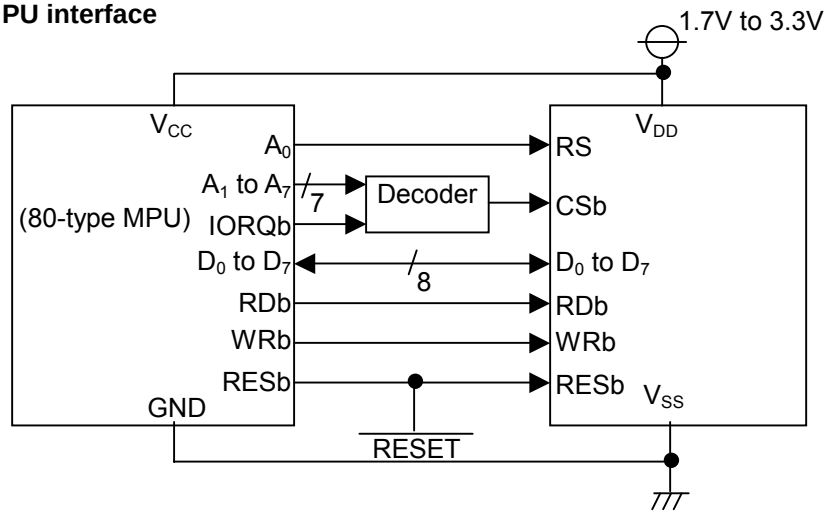


Terminals: $SEGA_0$ to $SEGA_{127}$
$SEGB_0$ to $SEGB_{127}$
$SEGC_0$ to $SEGC_{127}$
COM_0 to COM_{161}

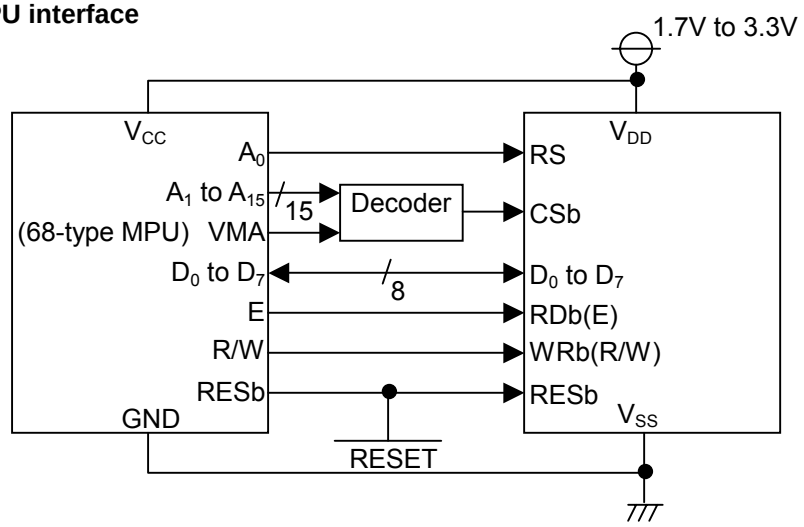
■ APPLICATION CIRCUIT EXAMPLES

(1) MPU Connections

80-type MPU interface



68-type MPU interface



Serial interface