

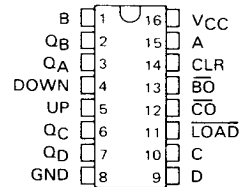
SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

D2661, DECEMBER 1982—REVISED MAY 1986

- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS192, SN54ALS193 . . . J PACKAGE
SN74ALS192, SN74ALS193 . . . D OR N PACKAGE

(TOP VIEW)



description

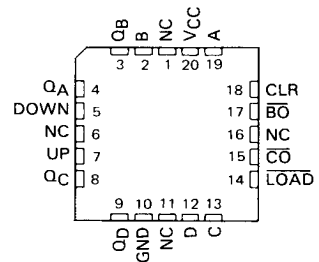
The 'ALS192 and 'ALS193 are synchronous, reversible up/down counters. The 'ALS192 is a 4-bit decade counter and the 'ALS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

SN54ALS192, SN54ALS193 . . . FK PACKAGE

(TOP VIEW)



NC — no internal connection.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output (\overline{CO}) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54ALS192 and SN54ALS193 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS192 and SN74ALS193 are characterized for operation from 0°C to 70°C .

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

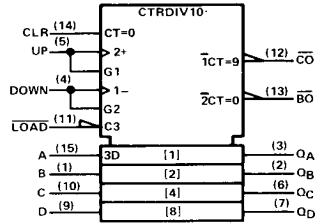
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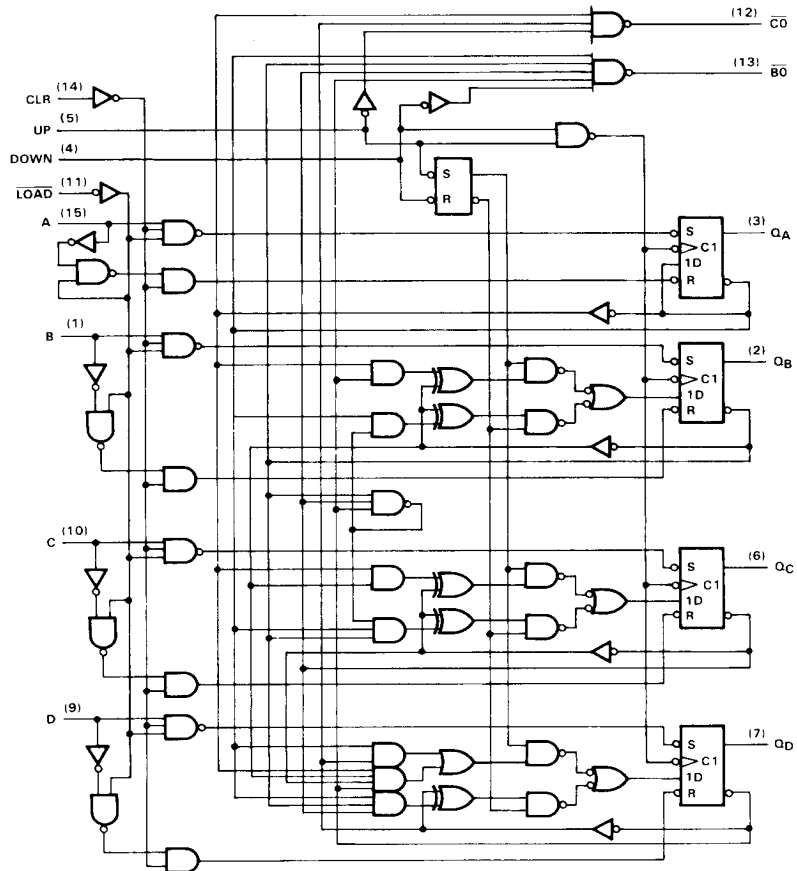
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SN54ALS192, SN74ALS192 SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS (DUAL CLOCK WITH CLEAR)

†ALS192 logic symbol†



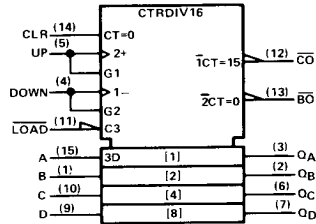
†ALS192 logic diagram (positive logic)



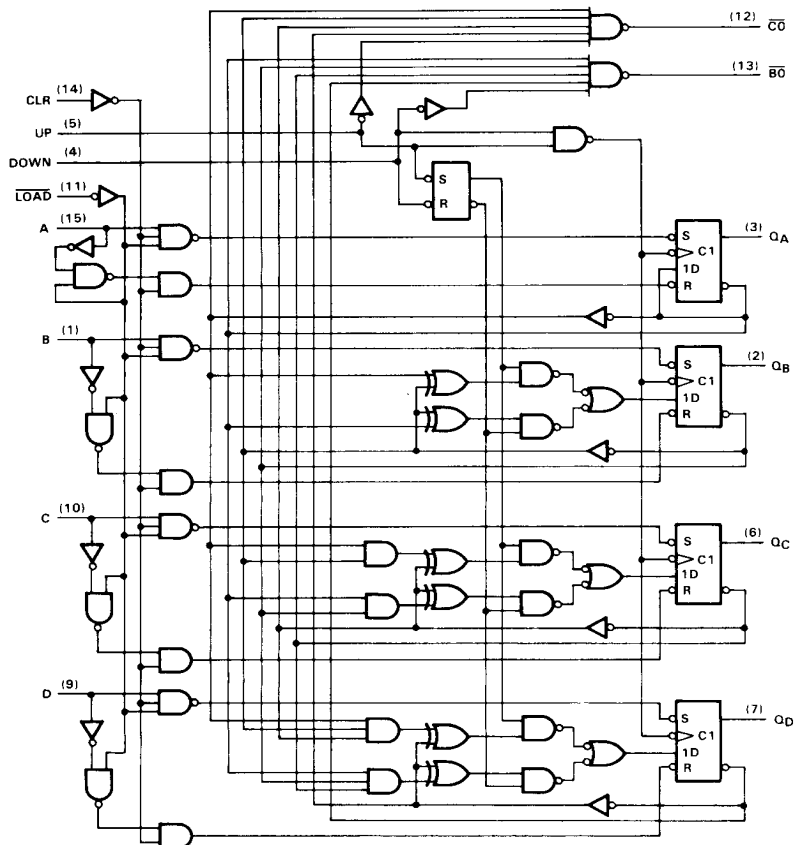
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS193, SN74ALS193 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS (DUAL CLOCK WITH CLEAR)

'ALS193 logic symbol†



'ALS193 logic diagrams (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91 1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

**TEXAS
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SN54ALS192, SN74ALS192 SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS (DUAL CLOCK WITH CLEAR)

typical clear, load, and count sequence

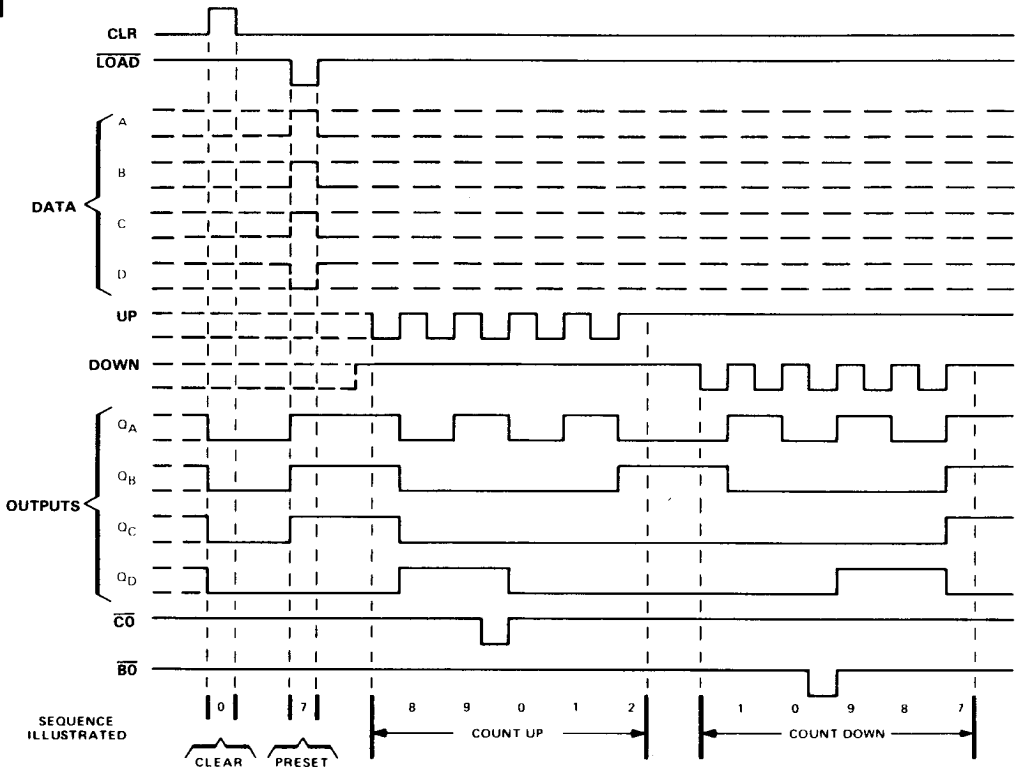
'ALS192

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.

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ALS and AS Circuits



- NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

'ALS193

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



B. When counting up, count-down input must be high; when counting down, count-up input must be high.

SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS192, SN54ALS193	-55 °C to 125 °C
SN74ALS192, SN74ALS193	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

					SN54ALS192 SN54ALS193			SN74ALS192 SN74ALS193			UNIT
					MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage				4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage				2			2			V
V _{IL}	Low-level input voltage						0.7			0.8	V
I _{OH}	High-level output current						−0.4			−0.4	mA
I _{OL}	Low-level output current						4			8	mA
f _{clock}	Clock frequency	'ALS192			0		20	0		25	MHz
		'ALS193			0		20	0		30	
t _w	Pulse duration	CLR high			10			10			ns
		LOAD low			25			20			
		UP or DOWN high or low			'ALS192			25			ns
					'ALS193			30		16.5	
t _{su}	Setup time	Data before LOAD ¹			25			20			ns
		CLR inactive before UP ¹ or DOWN ¹			20			20			
		LOAD inactive before UP ¹ or DOWN ¹			20			20			
t _h	Hold time	Data after LOAD ¹			5			5			ns
		UP high after DOWN ¹			0			0			
		DOWN high after UP ¹			0			0			
T _A	Operating free-air temperature				−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS192 SN54ALS193			SN74ALS192 SN74ALS193			UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}		$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$				-1.5			-1.5	V
V_{OH}		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$		$V_{CC}-2$			$V_{CC}-2$			V
V_{OL}		$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 4 \text{ mA}$			0.25	0.4		0.25	0.4	V
		$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 8 \text{ mA}$						0.35	0.5	
I_I		$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$				0.1			0.1	mA
I_{IH}		$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$				20			20	μA
I_{IL}	UP, DOWN	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$				-0.2			-0.2	mA
	All others					-0.1			-0.1	
I_{O}^{\dagger}		$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$		-30		-112	-30		-112	mA
I_{CC}		$V_{CC} = 5.5 \text{ V}$, See Note 1			12	22		12	22	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with the clear and load inputs grounded, and all other inputs at 4.5 V.

SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193 **SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)**

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, RL = 500 Ω, TA = MIN to MAX				UNIT
			SN54ALS192 SN54ALS193		SN74ALS192 SN74ALS193		
			MIN	MAX	MIN	MAX	
fmax		'ALS192	20		25		MHz
		'ALS193	25		30		
tPLH	Up	CO	3	20	4	16	ns
tPHL			3	21	5	18	
tPLH	Down	BO	4	20	4	16	ns
tPHL			5	22	5	18	
tPLH	Up or Down	Any Q	4	27	4	19	ns
tPHL			4	23	4	17	
tPLH	LOAD	Any Q	8	38	8	30	ns
tPHL			8	37	8	28	
tPHL	CLR	Any Q	5	20	5	17	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



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