

M66313FP

32-Bit LED Driver with Shift Register and Latch

REJ03F0179-0201

Rev.2.01

Mar 31, 2008

Description

The M66313FP is a semiconductor integrated circuit for LED array driver with 32-bit serial-input, parallel-output shift register, equipped with direct set input and output latches.

The M66313FP guarantees sufficient 24 mA output current to drive anode common LED, allowing 32-bit simultaneous and continuous current output.

The parallel outputs are open-drain outputs.

The M66313FP employs CMOS technology, allowing considerable reduction of power dissipation, compared to previous BIPOLAR or Bi-CMOS products.

In addition, the pin configuration is suitable for easy wiring on the printed circuit board.

Features

- High output current.
All parallel output $I_{OL} = +24$ mA, LEDs can be turned on simultaneously.
- Low power dissipation : 200 μ W/package (max)
($V_{CC} = 5$ V, $T_a = 25^\circ\text{C}$, quiescent state)
- High noise margin
Employment of Schmitt-trigger circuit on all inputs allows application with long wiring.
- Direct set input ($\overline{S_D}$)
- Open-drain output ($\overline{Q_1}$ to $\overline{Q_{32}}$)
- Serial data output for cascading (SQ_{32})
- Wide operating temperature range ($T_a = -40$ to $+85^\circ\text{C}$)
- Pin configuration for easy layout on PCB.
(Pin configuration allows easy cascade connection or LED connection)

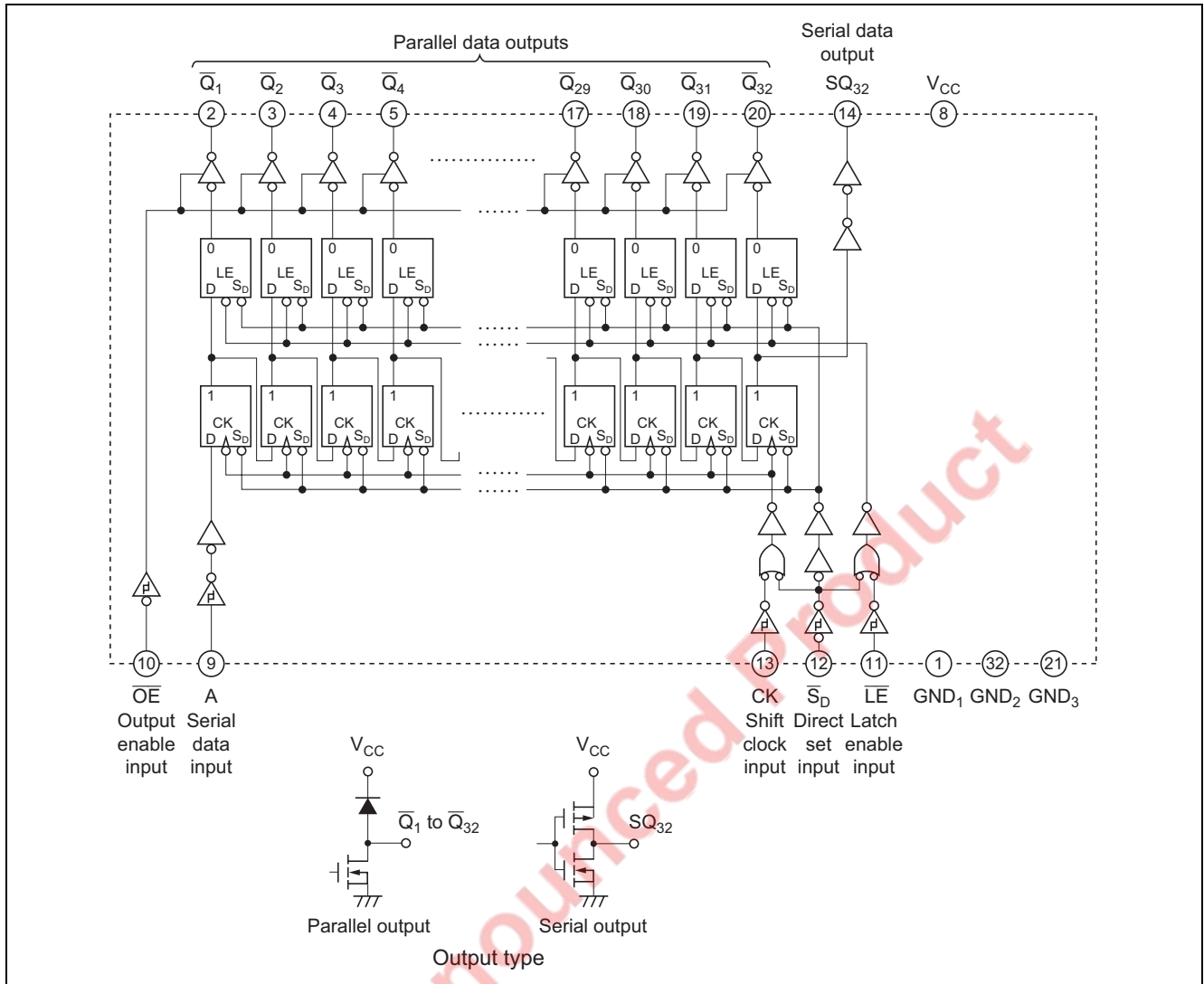
Application

LED array drive for eraser unit of a copying machine

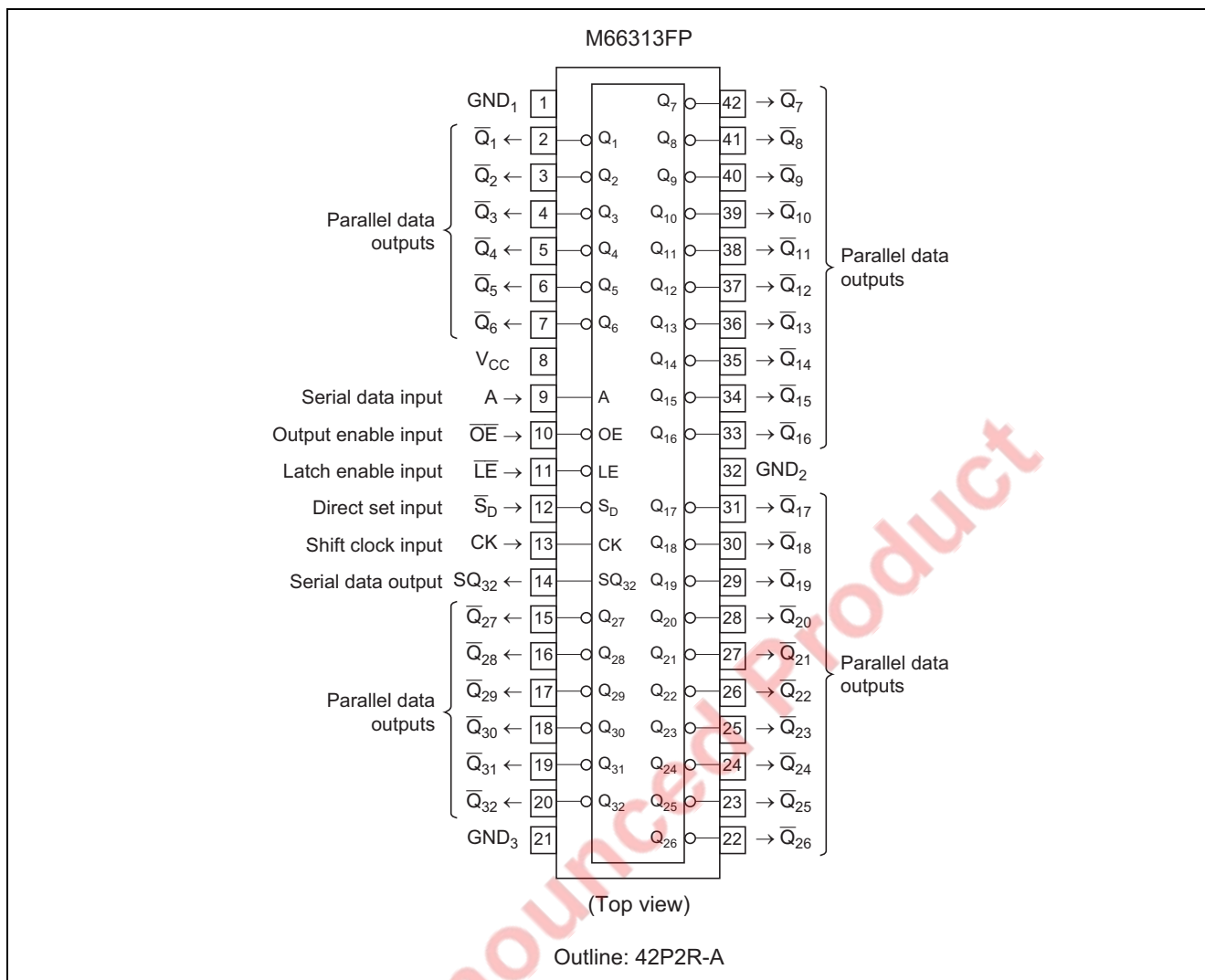
LED array drive of a button telephone set

Various LED modules

Block Diagram



Pin Arrangement



Functional Description

The employment of silicon gate CMOS process of the M66313FP guarantees low power dissipation and maintains high noise margin as well as high output current and high speed required to drive LEDs.

Each shift register bit consists of a flip-flop for shifting and an output latch.

The shift operation takes place when the clock input CK changes from low-level to high-level.

The serial data input A corresponds to the data input of the first-stage shift register, and the shift register is shifted in sequence when a pulse is applied to CK.

The parallel outputs \bar{Q}_1 to \bar{Q}_{32} are open-drain outputs.

If the latch-enable input \bar{LE} is turned high-level, the content of the shift register at that instant is latched.

To expand the number of bits, use the serial data output SQ_{32} which shows the output of the shift register of the 32nd bit.

If the direct set input \bar{S}_D is turned low-level, shift register and latches are set.

If the high-level input is applied to the output enable input \bar{OE} , \bar{Q}_1 to \bar{Q}_{32} are set to the high-impedance state, but SQ_{32} is not set to the high-impedance state. The shift operation is not affected when \bar{OE} is changed.

Note \uparrow : Transition from low-to-high-level.
 \overline{Q}^0 : Shows the status of output \overline{Q} before CK input changes.
 X: Irrelevant
 q^0 : The content of shift register before CK changes.
 q: The content of the shift register.
 Z: High-impedance state.

(Ta = -40 to +85°C, unless otherwise noted)

Recommended Operating Conditions

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Electrical Characteristics

(V_{CC} = 4.5 to 5.5 V, unless otherwise noted)

Item		Sym bol	Limits				Unit	Conditions		
			Ta = 25°C			Ta = -40 to +85°C				
			Min	Typ (Note1)	Max	Min				Max
Positive-going threshold voltage		V _{T+}	0.35×V _{CC}	2.8	0.7×V _{CC}	0.35×V _{CC}	0.7×V _{CC}	V	V _O = 0.1V, V _{CC} -0.1V I _O = 20μA	
Negative-going threshold voltage		V _{T-}	0.2×V _{CC}	2	0.55×V _{CC}	0.2×V _{CC}	0.55×V _{CC}	V	V _O = 0.1V, V _{CC} -0.1V I _O = 20μA	
High-level output voltage	SQ ₃₂	V _{OH}	V _{CC} -0.1	—	—	V _{CC} -0.1	—	V	V _I = V _{T+} , V _{T-} V _{CC} = 4.5V	I _{OH} = -20μA
			3.83	—	—	3.66	—			I _{OH} = -4mA
Low-level output voltage	Q ₁ to Q ₃₂	V _{OL}	—	—	0.1	—	0.1	V	V _I = V _{T+} , V _{T-} V _{CC} = 4.5V	I _{OL} = 20μA
			—	0.20	0.41	—	0.50			I _{OL} = 24mA
			—	0.25	0.48	—	0.55 (Note 2)			I _{OL} = 28mA
	SQ ₃₂		—	—	0.1	—	0.1			I _{OL} = 20μA
			—	—	0.44	—	0.53			I _{OL} = 4mA
High-level input current		I _{IH}	—	—	0.5	—	5.0	μA	V _I = V _{CC} , V _{CC} = 5.5V	
Low-level input current		I _{IL}	—	—	-0.5	—	-5.0	μA	V _I = GND, V _{CC} = 5.5V	
Maximum output leak current	Q ₁ to Q ₃₂	I _O	—	—	1.0	—	10.0	μA	V _I = V _{T+} , V _{T-} V _{CC} = 5.5V	V _O = V _{CC}
			—	—	-1.0	—	-10.0			V _O = GND
Quiescent state dissipation current		I _{CC}	—	—	40.0	—	400.0	μA	V _I = V _{CC} , GND, V _{CC} = 5.5V	

Note: 1. All typical values are at V_{CC} = 5 V, Ta = 25°C

2. Ta = -40 to +70°C

Switching Characteristics

(V_{CC} = 5V)

Item		Symbol	Limits					Unit	Conditions
			Ta = 25°C			Ta = −40 to +85°C			
			Min	Typ	Max	Min	Max		
Maximum clock frequency		f _{max}	5	30	—	4	—	MHz	C _L = 50 pF R _L = 1 kΩ (Note 2)
Output enable time to low-level	CK- \overline{Q}_1 to \overline{Q}_{32} (Turned on)	t _{PZL}	—	35	150	—	200	ns	
Output disable time from low-level	CK- \overline{Q}_1 to \overline{Q}_{32} (Turned off)	t _{PLZ}	—	35	200	—	250	ns	
Low-to-high, high-to-low output propagation time	CK-SQ ₃₂	t _{PLH}	—	35	100	—	130	ns	
		t _{PHL}	—	40	100	—	130	ns	
Output enable time to low-level	\overline{S}_D - \overline{Q}_1 to \overline{Q}_{32} (Turned on)	t _{PZL}	—	35	150	—	200	ns	
Low-to-high output propagation time	\overline{S}_D -SQ ₃₂	t _{PLH}	—	40	100	—	130	ns	
Output enable time to low-level	\overline{LE} - \overline{Q}_1 to \overline{Q}_{32} (Turned on)	t _{PZL}	—	30	100	—	130	ns	
Output disable time from low-level	\overline{LE} - \overline{Q}_1 to \overline{Q}_{32} (Turned off)	t _{PLZ}	—	35	150	—	200	ns	
Output enable time to low-level	\overline{OE} - \overline{Q}_1 to \overline{Q}_{32} (Turned on)	t _{PZL}	—	30	100	—	130	ns	
Output disable time from low-level	\overline{OE} - \overline{Q}_1 to \overline{Q}_{32} (Turned off)	t _{PLZ}	—	35	150	—	200	ns	
Input capacitance		C _I	—	3	10	—	10	pF	\overline{OE} -V _{CC}
Output capacitance		C _O	—	6	15	—	15	pF	
Power dissipation capacitance (Note 1)		C _{PD}	—	160	—	—	—	pF	

Note 1. C_{PD} is the equivalent capacitance of IC calculated by the operating power dissipation without load. The operating power dissipation without load is given as follows.

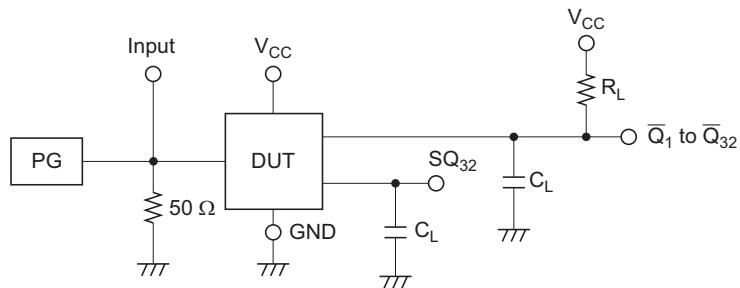
$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$$

Timing Requirements

(V_{CC} = 5V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = −40 to +85°C			
		Min	Typ	Max	Min	Max		
CK, $\overline{\text{LE}}$, $\overline{\text{S}}_{\text{D}}$ pulse width	t _W	100	16	—	130	—	ns	(Note 2)
Setup time A to CK	t _{su}	100	27	—	130	—	ns	
Hold time A to CK	t _h	10	5	—	15	—	ns	
Hold time $\overline{\text{LE}}$ to CK		50	15	—	70	—		
Recovery time CK to $\overline{\text{S}}_{\text{D}}$	t _{rec}	50	20	—	70	—	ns	

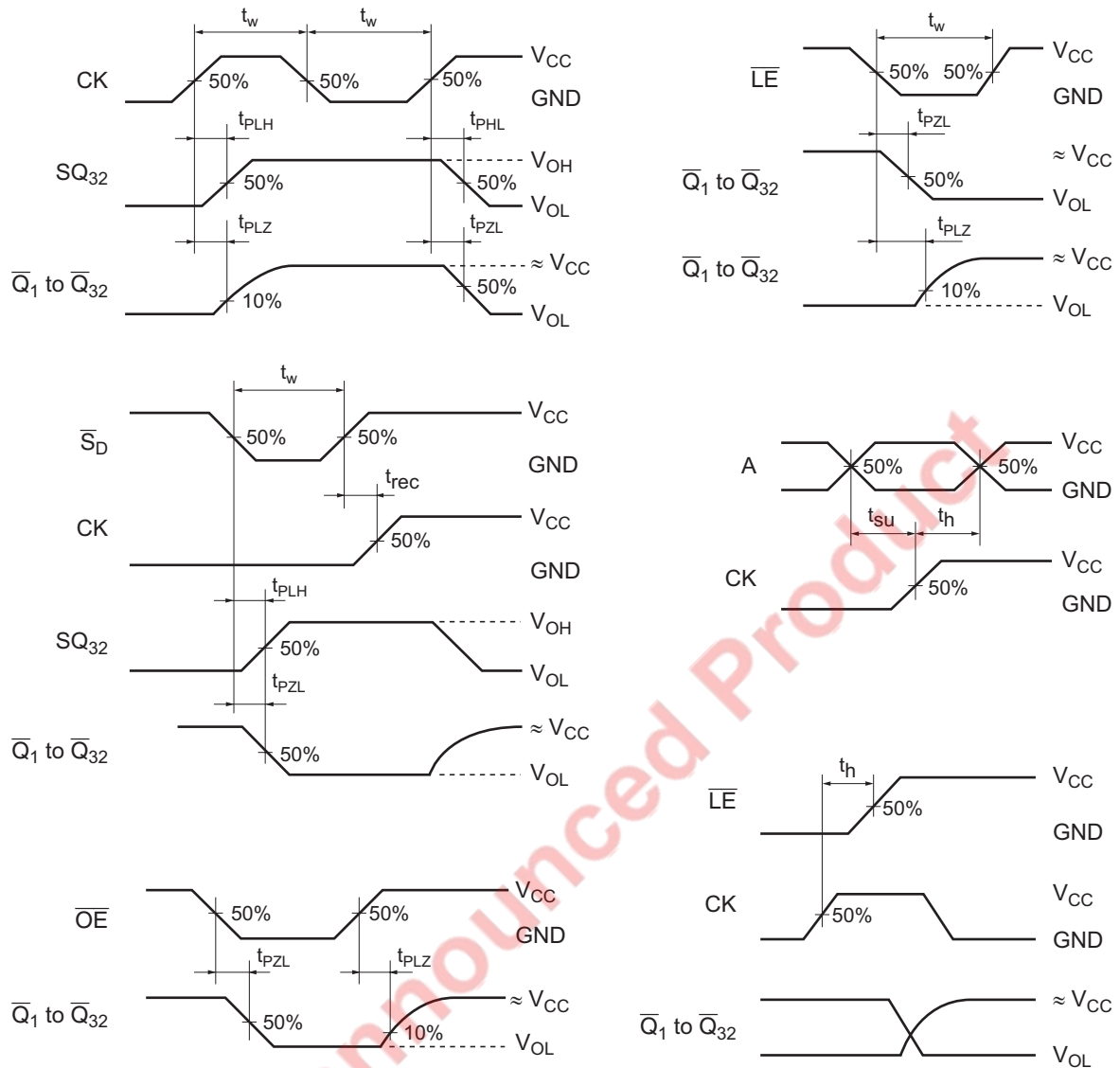
Note: 2. Test Circuit



(1) Characteristics of pulse generator (PG): tr = 6 ns, tf = 6 ns

(2) CL includes probe and stray capacitance.

Timing Chart



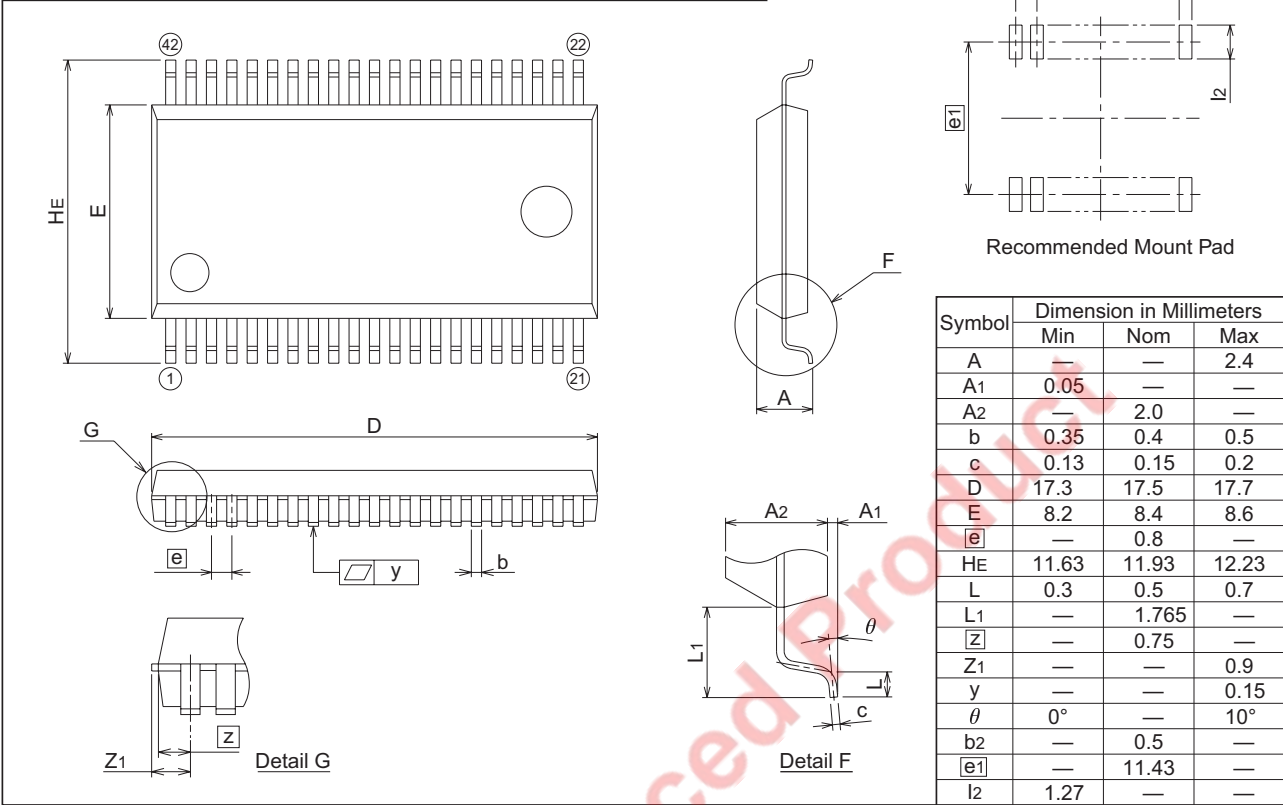
Package Dimensions

42P2R-A



Plastic 42pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	—	0.63	Alloy 42/Cu Alloy



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Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

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Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510