

**TC74LVX86F, TC74LVX86FN, TC74LVX86FT****QUAD EXCLUSIVE OR GATE**

The TC74LVX86 is a high speed CMOS EXCLUSIVE OR GATE fabricated with silicon gate C<sup>2</sup>MOS technology. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low voltage and battery operated systems.

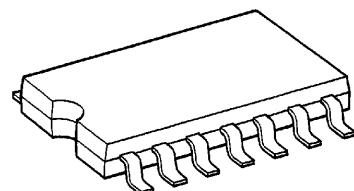
The internal circuit is includes on output buffer, which provide high noise immunity and stable output.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage.

This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

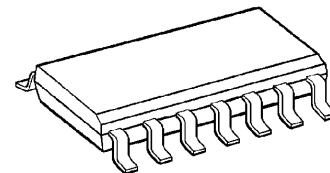
(Note) The JEDEC SOP (FN) is not available in Japan.

TC74LVX86F



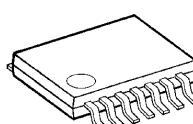
SOP14-P-300-1.27

TC74LVX86FN



SOL14-P-150-1.27

TC74LVX86FT



TSSOP14-P-0044-0.65

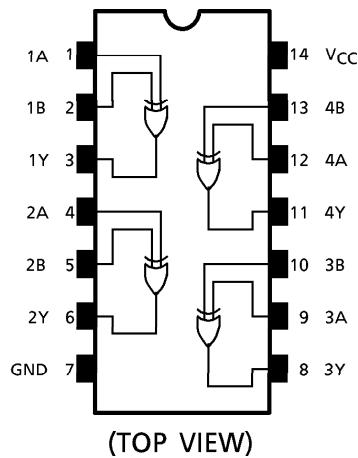
## Weight

SOP14-P-300-1.27	: 0.18g (Typ.)
SOL14-P-150-1.27	: 0.12g (Typ.)
TSSOP14-P-0044-0.65	: 0.06g (Typ.)

**FEATURES**

- High speed :  $t_{pd} = 5.8\text{ns}$  (Typ.) ( $V_{CC} = 3.3\text{V}$ )
- Low power dissipation :  $I_{CC} = 2\mu\text{A}$  (Max.) ( $T_a = 25^\circ\text{C}$ )
- Input voltage level :  $V_{IL} = 0.8\text{V}$  (Max.) ( $V_{CC} = 3\text{V}$ )  
 $V_{IH} = 2.0\text{V}$  (Min.) ( $V_{CC} = 3\text{V}$ )
- Power down protection is provided on all inputs.
- Balanced propagation delays :  $t_{pLH} \approx t_{pHL}$
- Low noise :  $V_{OLP} = 0.5\text{V}$  (Max.)
- Pin and function compatible with 74HC86

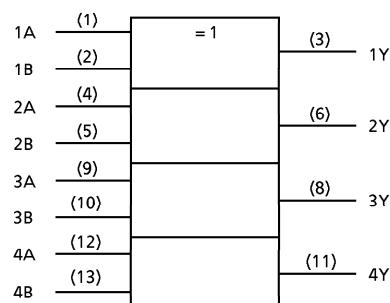
## PIN ASSIGNMENT



## TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

## IEC LOGIC SYMBOL



## MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}$ + 0.5	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ / Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	2.0~3.6	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise And Fall Time	$dt/dv$	0~100	ns/V

## ELECTRICAL CHARACTERISTICS

## DC characteristics

PARAMETER	SYM-BOL	TEST CONDITION	$V_{CC}$ (V)	Ta = 25°C			Ta = -40~85°C		UNIT		
				MIN.	TYP.	MAX.	MIN.	MAX.			
Input Voltage	"H" Level	$V_{IH}$		2.0	1.5	—	—	1.5	—	V	
				3.0	2.0	—	—	2.0	—		
				3.6	2.4	—	—	2.4	—		
	"L" Level	$V_{IL}$		2.0	—	—	0.5	—	0.5		
				3.0	—	—	0.8	—	0.8		
				3.6	—	—	0.8	—	0.8		
Output Voltage	"H" Level	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\mu A$	2.0	1.9	2.0	—	1.9	V	
				$I_{OH} = -50\mu A$	3.0	2.9	3.0	—	2.9		
				$I_{OH} = -4mA$	3.0	2.58	—	—	2.48		
	"L" Level	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\mu A$	2.0	—	0.0	0.1	—		
				$I_{OL} = 50\mu A$	3.0	—	0.0	0.1	—		
				$I_{OL} = 4mA$	3.0	—	—	0.36	—		
Input Leakage Current	$I_{IN}$	$V_{IN} = 5.5V$ or GND		3.6	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu A$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		3.6	—	—	2.0	—	20.0	$\mu A$	

AC characteristics (Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYM-BOL	TEST CONDITION	$V_{CC}$ (V)	$C_L$ (pF)	Ta = 25°C			Ta = - 40~85°C		UNIT	
					MIN.	TYP.	MAX.	MIN.	MAX.		
Propagation Delay Time	$t_{pLH}$	(Note 1)	2.7	15	—	7.5	14.5	1.0	17.5	ns	
				50	—	10.0	18.0	1.0	21.0		
	$t_{pHL}$		$3.3 \pm 0.3$	15	—	5.8	9.3	1.0	11.0		
				50	—	8.3	12.8	1.0	14.5		
Output To Output Skew	$t_{osLH}$		2.7	50	—	—	1.5	—	1.5	ns	
	$t_{osHL}$		$3.3 \pm 0.3$	50	—	—	1.5	—	1.5		
Input Capacitance	$C_{IN}$	(Note 2)			—	—	4	10	—	10	pF
Power Dissipation Capacitance	$C_{PD}$				—	—	18	—	—	—	pF

(Note 1) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

(Note 2) Parameter guaranteed by design.

(Note 3)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

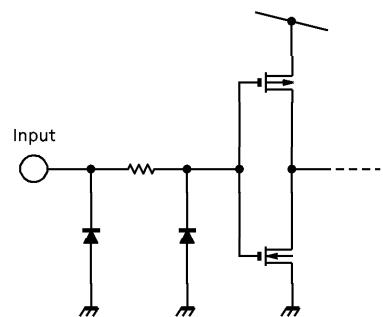
Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per Gate)}$$

Noise characteristics (Ta = 25°C, Input  $t_r = t_f = 3\text{ns}$ ,  $C_L = 50\text{pF}$ )

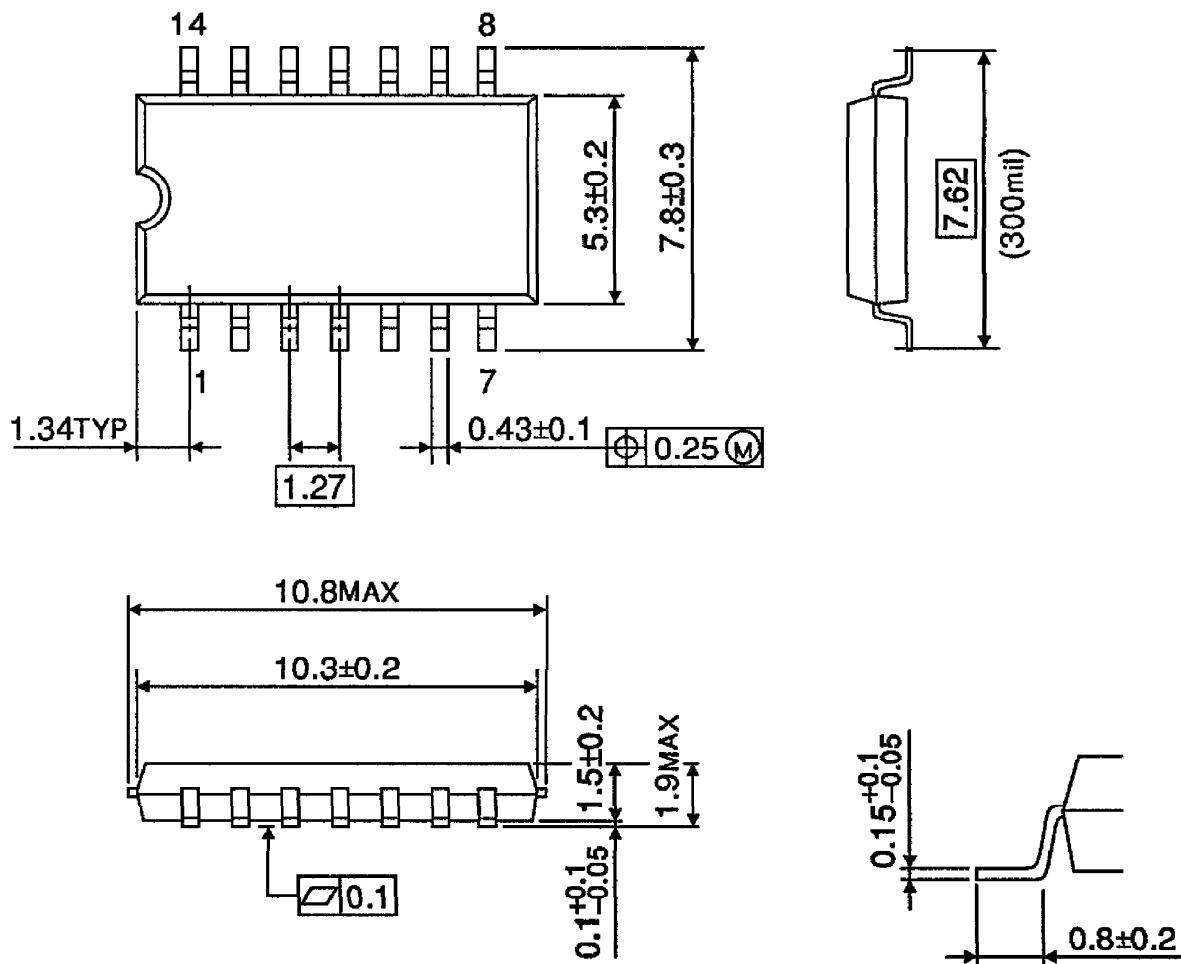
PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic $V_{OL}$	$V_{OLP}$		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic $V_{OL}$	$V_{OLV}$		3.3	-0.3	-0.5	V
Minimum High Level Dynamic Input Voltage	$V_{IH}$		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	$V_{IL}$		3.3	—	0.8	V

## INPUT EQUIVALENT CIRCUIT



**PACKAGE DIMENSIONS**  
SOP14-P-300-1.27

Unit : mm

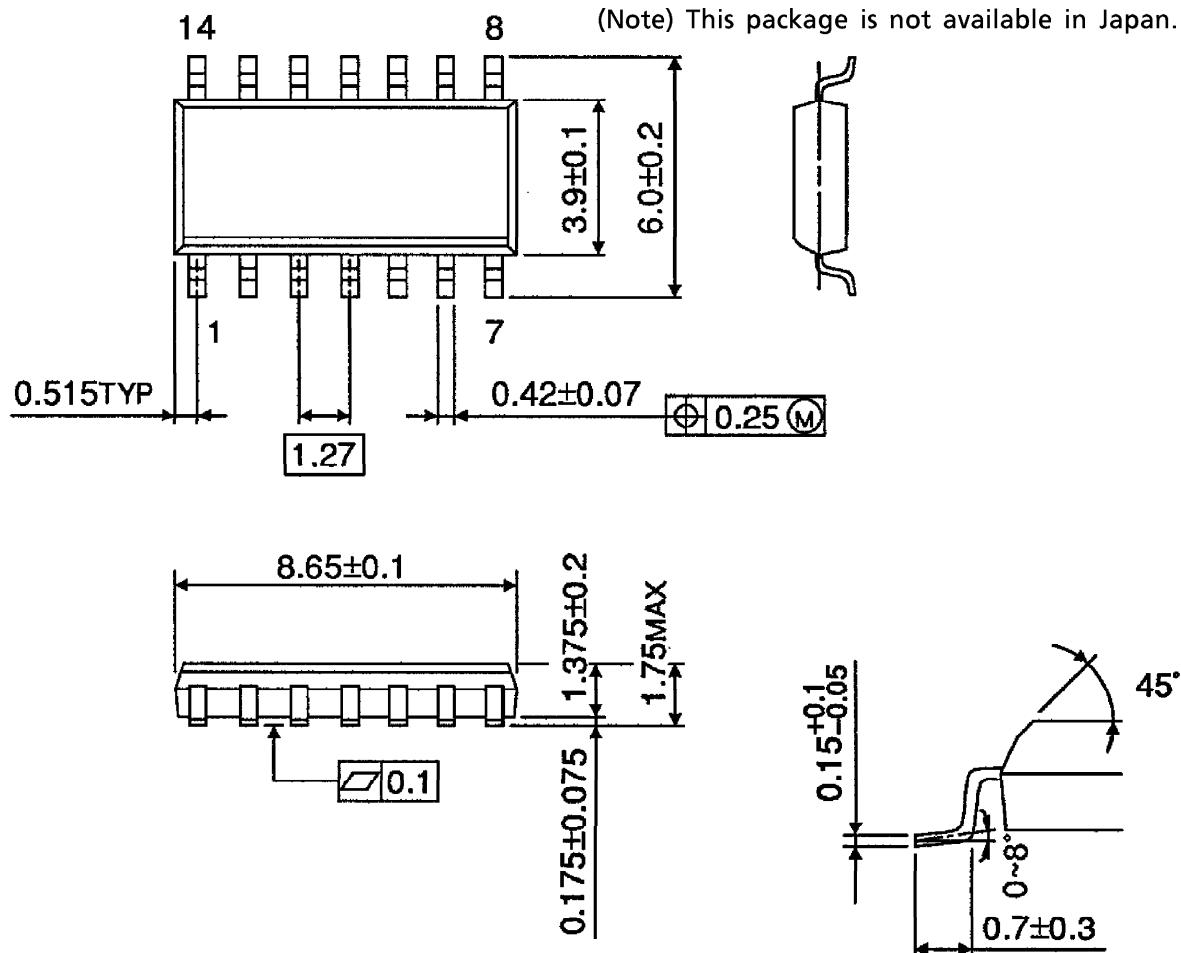


Weight : 0.18g (Typ.)

## PACKAGE DIMENSIONS

SOL14-P-150-1.27

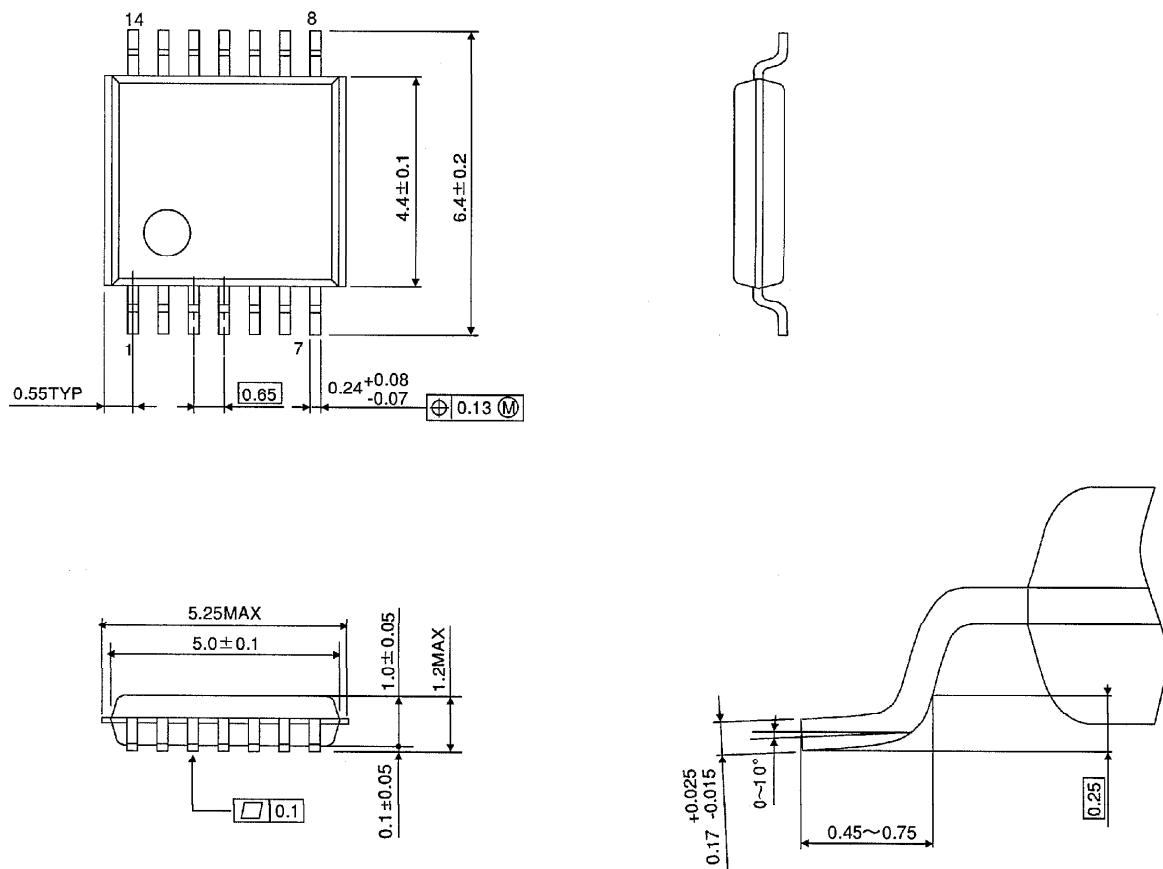
Unit : mm



Weight : 0.12g (Typ.)

**PACKAGE DIMENSIONS**  
TSSOP14-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)

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000707EBA

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