To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M35046-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35046-XXXSP/FP is a character pattern display control IC can display on the liquid crystal display and the plasma display. It uses a silicon gate CMOS process and it housed in a 20-pin shrink DIP package (M35046-XXXSP) or a 20-pin shrink SOP package (M35046-XXXFP).

For M35046-001SP/FP that is a standard ROM version of M35046-XXXSP/FP respectively, the character pattern is also mentioned.

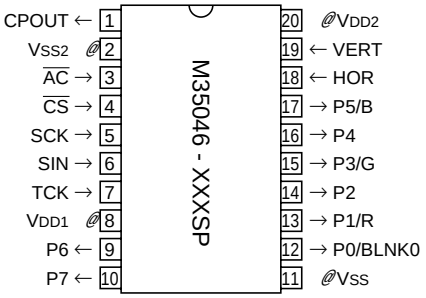
FEATURES

- Screen composition ..... 24 columns × 12 lines
- Number of characters displayed ..... 288 (Max.)
- Character composition ..... 12 × 18 dot matrix
- Characters available ..... 256 characters
- Character sizes available ..... 4 (horizontal) × 4 (vertical)
- Display locations available
  - Horizontal direction ..... 1000 locations
  - Vertical direction ..... 1023 locations
- Blinking ..... Character units
  - Cycle : division of vertical synchronization signal into 32 or 64
  - Duty : 25%, 50%, or 75%
- Data input ..... By the 16-bit serial input function
- Coloring
  - Character color ..... Character unit
  - Background coloring ..... Character unit
  - Matrix-outline (shadow) coloring ..... 8 colors (RGB output) Specified by register
  - Border coloring ..... 8 colors (RGB output) Specified by register
  - Raster coloring ..... 8 colors (RGB output) Specified by register
- Blanking
  - Character size blanking
  - Border size blanking
  - Matrix-outline blanking
  - All blanking (all raster area)
- Output ports
  - 4 shared output ports (toggled between RGB output)
  - 4 dedicated output ports
- Display RAM erase function
- Display input frequency range ..... F_{OSC} = 20MHz to 80MHz
- Horizontal synchronous input frequency ..... H.sync = 15 kHz to 130 kHz
- Display oscillation stop function

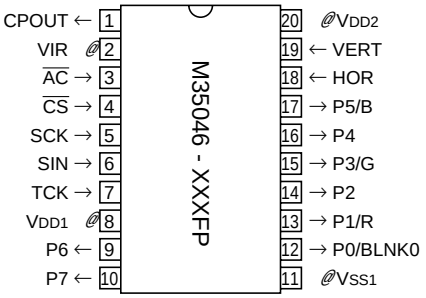
APPLICATION

Liquid crystal display, Plasma display, Video projecter

PIN CONFIGURATION (TOP VIEW)

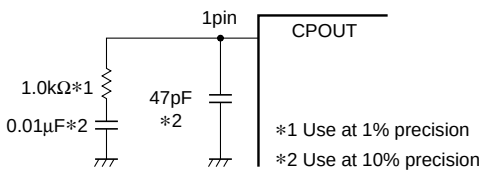


Outline 20P4B

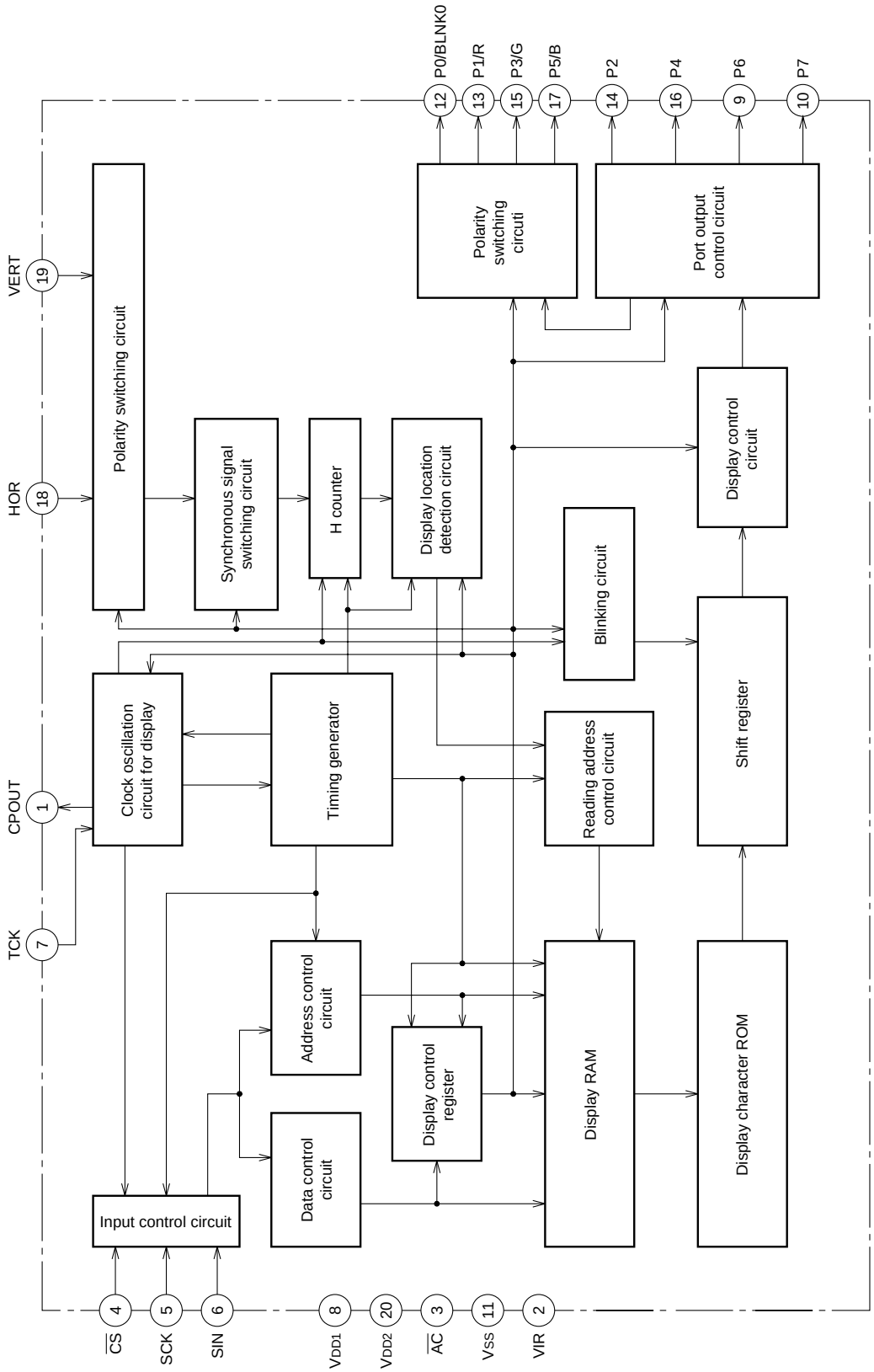


Outline 20P2Q-A

PIN DESCRIPTION

Pin Number	Symbol	Pin name	Input/ Output	Function
1	CPOUT	Phase difference	Output	Connect loop filter to this pin. 
2	V_{SS2}	Earthing pin	–	Connect to GND.
3	$\overline{AC}$	Auto-clear input	Input	When “L”, this pin resets the internal IC circuit. Hysteresis input. Built-in pull-up resistor.
4	$\overline{CS}$	Chip select input	Input	This is the chip select input pin, and when serial data transmission is being carried out, it goes to “L”. Hysteresis input. Built-in pull-up resistor.
5	SCK	Serial clock input	Input	When $\overline{CS}$ pin is “L”, SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor.
6	SIN	Serial data input	Input	This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Built-in pull-up resistor.
7	TCK	External clock	Input	This is the pin for external clock input.
8	V_{DD1}	Power pin	–	Please connect to +5V with the power pin.
9	P6	Port P6 output	Output	This is the output port. Port data is set by PTD6.
10	P7	Port P7 output	Output	This is the output port. Port data is set by PTD7.
11	V_{SS1}	Earthing pin	–	Please connect to GND using circuit earthing pin.
12	P0/BLNK0	Port P0 output	Output	This pin can be toggled between port pin output and BLNK0 signal output.
13	P1/R	Port P1 output	Output	This pin can be toggled between port pin output and R signal output.
14	P2	Port P2 output	Output	This is the output port. Port data is set by PTD2.
15	P3/G	Port P3 output	Output	This pin can be toggled between port pin output and G signal output.
16	P4	Port P4 output	Output	This is the output port. Port data is set by PTD4.
17	P5/B	Port P5 output	Output	This pin can be toggled between port pin output and B signal output.
18	HOR	Horizontal synchronous signal input	Input	This pin inputs the horizontal synchronous signal. Hysteresis input.
19	VERT	Vertical synchronous signal input	Input	This pin inputs the vertical synchronous signal. Hysteresis input.
20	V_{DD2}	Power pin	–	Please connect to +5V with the power pin.

BLOCK DIAGRAM



MEMORY CONSTITUTION

Address 000_{16} to $11F_{16}$ are assigned to the display RAM, address 120_{16} to 128_{16} are assigned to the display control registers. The internal circuit is reset and all display control registers (address 120_{16} to 128_{16}) are set to "0" when the $\overline{AC}$ pin level is "L". And then RAM is erased.

Memory constitution is shown in Figure 1.

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen constitution is shown in Figure 2.

	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000_{16}	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background coloring			Blink-ing	Character color			Character code							
$11F_{16}$	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
120_{16}	0	EXCK0	VJT	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
121_{16}	0	RSEL0	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
122_{16}	0	RSEL1	SPACE2	SPACE1	SPACE0	TEST9	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
123_{16}	0	EXCK1	TEST3	TEST2	TEST1	TEST0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
124_{16}	0	TEST14	TEST5	TEST4	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
125_{16}	0	TEST10	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
126_{16}	0	TEST11	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10
127_{16}	0	TEST12	HSZ21	HSZ20	HSZ11	HSZ10	BETA14	TEST8	TEST7	TEST6	FB	FG	FR	RB	RG	RR
128_{16}	0	TEST13	BLINK2	BLINK1	BLINK0	DSPON	STOP	RAMERS	SYAD	BLK1	BLK0	POLH	POLV	VMASK	B/$\overline{F}$	BCOL

Fig. 1 Memory constitution

Row / Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	000_{16}	001_{16}	002_{16}	003_{16}	004_{16}	005_{16}	006_{16}	007_{16}	008_{16}	009_{16}	$00A_{16}$	$00B_{16}$	$00C_{16}$	$00D_{16}$	$00E_{16}$	$00F_{16}$	010_{16}	011_{16}	012_{16}	013_{16}	014_{16}	015_{16}	016_{16}	017_{16}
2	018_{16}	019_{16}	$01A_{16}$	$01B_{16}$	$01C_{16}$	$01D_{16}$	$01E_{16}$	$01F_{16}$	020_{16}	021_{16}	022_{16}	023_{16}	024_{16}	025_{16}	026_{16}	027_{16}	028_{16}	029_{16}	$02A_{16}$	$02B_{16}$	$02C_{16}$	$02D_{16}$	$02E_{16}$	$02F_{16}$
3	030_{16}	031_{16}	032_{16}	033_{16}	034_{16}	035_{16}	036_{16}	037_{16}	038_{16}	039_{16}	$03A_{16}$	$03B_{16}$	$03C_{16}$	$03D_{16}$	$03E_{16}$	$03F_{16}$	040_{16}	041_{16}	042_{16}	043_{16}	044_{16}	045_{16}	046_{16}	047_{16}
4	048_{16}	049_{16}	$04A_{16}$	$04B_{16}$	$04C_{16}$	$04D_{16}$	$04E_{16}$	$04F_{16}$	050_{16}	051_{16}	052_{16}	053_{16}	054_{16}	055_{16}	056_{16}	057_{16}	058_{16}	059_{16}	$05A_{16}$	$05B_{16}$	$05C_{16}$	$05D_{16}$	$05E_{16}$	$05F_{16}$
5	060_{16}	061_{16}	062_{16}	063_{16}	064_{16}	065_{16}	066_{16}	067_{16}	068_{16}	069_{16}	$06A_{16}$	$06B_{16}$	$06C_{16}$	$06D_{16}$	$06E_{16}$	$06F_{16}$	070_{16}	071_{16}	072_{16}	073_{16}	074_{16}	075_{16}	076_{16}	077_{16}
6	078_{16}	079_{16}	$07A_{16}$	$07B_{16}$	$07C_{16}$	$07D_{16}$	$07E_{16}$	$07F_{16}$	080_{16}	081_{16}	082_{16}	083_{16}	084_{16}	085_{16}	086_{16}	087_{16}	088_{16}	089_{16}	$08A_{16}$	$08B_{16}$	$08C_{16}$	$08D_{16}$	$08E_{16}$	$08F_{16}$
7	090_{16}	091_{16}	092_{16}	093_{16}	094_{16}	095_{16}	096_{16}	097_{16}	098_{16}	099_{16}	$09A_{16}$	$09B_{16}$	$09C_{16}$	$09D_{16}$	$09E_{16}$	$09F_{16}$	$0A0_{16}$	$0A1_{16}$	$0A2_{16}$	$0A3_{16}$	$0A4_{16}$	$0A5_{16}$	$0A6_{16}$	$0A7_{16}$
8	$0A8_{16}$	$0A9_{16}$	$0AA_{16}$	$0AB_{16}$	$0AC_{16}$	$0AD_{16}$	$0AE_{16}$	$0AF_{16}$	$0B0_{16}$	$0B1_{16}$	$0B2_{16}$	$0B3_{16}$	$0B4_{16}$	$0B5_{16}$	$0B6_{16}$	$0B7_{16}$	$0B8_{16}$	$0B9_{16}$	$0BA_{16}$	$0BB_{16}$	$0BC_{16}$	$0BD_{16}$	$0BE_{16}$	$0BF_{16}$
9	$0C0_{16}$	$0C1_{16}$	$0C2_{16}$	$0C3_{16}$	$0C4_{16}$	$0C5_{16}$	$0C6_{16}$	$0C7_{16}$	$0C8_{16}$	$0C9_{16}$	$0CA_{16}$	$0CB_{16}$	$0CC_{16}$	$0CD_{16}$	$0CE_{16}$	$0CF_{16}$	$0D0_{16}$	$0D1_{16}$	$0D2_{16}$	$0D3_{16}$	$0D4_{16}$	$0D5_{16}$	$0D6_{16}$	$0D7_{16}$
10	$0D8_{16}$	$0D9_{16}$	$0DA_{16}$	$0DB_{16}$	$0DC_{16}$	$0DD_{16}$	$0DE_{16}$	$0DF_{16}$	$0E0_{16}$	$0E1_{16}$	$0E2_{16}$	$0E3_{16}$	$0E4_{16}$	$0E5_{16}$	$0E6_{16}$	$0E7_{16}$	$0E8_{16}$	$0E9_{16}$	$0EA_{16}$	$0EB_{16}$	$0EC_{16}$	$0ED_{16}$	$0EE_{16}$	$0EF_{16}$
11	$0F0_{16}$	$0F1_{16}$	$0F2_{16}$	$0F3_{16}$	$0F4_{16}$	$0F5_{16}$	$0F6_{16}$	$0F7_{16}$	$0F8_{16}$	$0F9_{16}$	$0FA_{16}$	$0FB_{16}$	$0FC_{16}$	$0FD_{16}$	$0FE_{16}$	$0FF_{16}$	100_{16}	101_{16}	102_{16}	103_{16}	104_{16}	105_{16}	106_{16}	107_{16}
12	108_{16}	109_{16}	$10A_{16}$	$10B_{16}$	$10C_{16}$	$10D_{16}$	$10E_{16}$	$10F_{16}$	110_{16}	111_{16}	112_{16}	113_{16}	114_{16}	115_{16}	116_{16}	117_{16}	118_{16}	119_{16}	$11A_{16}$	$11B_{16}$	$11C_{16}$	$11D_{16}$	$11E_{16}$	$11F_{16}$

ƒ The hexadecimal numbers in the boxes show the display RAM address.

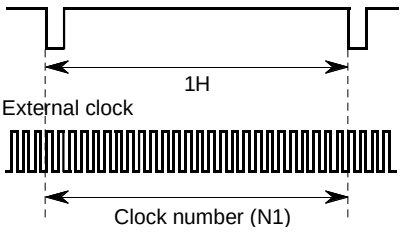
Fig. 2 Screen constitution

REGISTERS DESCRIPTION

(1) Address 120_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DIV0</td><td>0
1</td><td rowspan="12">Set external clock frequency value of horizontal oscillation frequency.

$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$
N1: frequency value

Horizontal synchronized signal
 
</td><td rowspan="12">Set display frequency by frequency value setting. Set N1 to be “N1=fOSC/fH”.
fOSC(MHz) : External clock frequency for TCK pin (=display frequency)
fH(kHz) : Horizontal synchronous signal frequency for HOR pin
Set registers DIVS0, DIVS1 (address 120_{16}), RSEL0 (address 121_{16}) and RSEL1 (address 122_{16}) according to external clock frequency.
For details, see (2) Setting display frequencies under Register Supplementary Description.

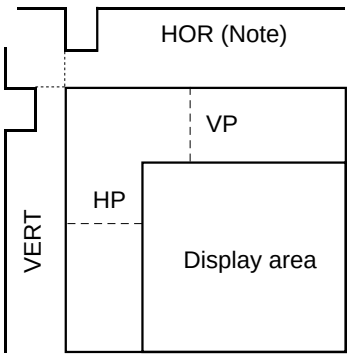
Any of this settings above is reguired only when EXCK1=1, EXCK0=1.</td></tr>
<tr><td>1</td><td>DIV1</td><td>0
1</td></tr>
<tr><td>2</td><td>DIV2</td><td>0
1</td></tr>
<tr><td>3</td><td>DIV3</td><td>0
1</td></tr>
<tr><td>4</td><td>DIV4</td><td>0
1</td></tr>
<tr><td>5</td><td>DIV5</td><td>0
1</td></tr>
<tr><td>6</td><td>DIV6</td><td>0
1</td></tr>
<tr><td>7</td><td>DIV7</td><td>0
1</td></tr>
<tr><td>8</td><td>DIV8</td><td>0
1</td></tr>
<tr><td>9</td><td>DIV9</td><td>0
1</td></tr>
<tr><td>A</td><td>DIV10</td><td>0
1</td></tr>
<tr><td>B</td><td>DIVS0</td><td>0
1</td><td rowspan="2">For details, see (2) Setting display frequencies under Register Supplementary Description.</td><td rowspan="2">Set display frequency area.</td></tr>
<tr><td>C</td><td>DIVS1</td><td>0
1</td></tr>
<tr><td>D</td><td>VJT</td><td>0
1</td><td>It should be fixed to “0”.
Alleviates continuous vertical jitters.</td><td></td></tr>
<tr><td>E</td><td>EXCK0</td><td>0
1</td><td><table><tr><th>EXCK1</th><th>EXCK0</th><th>Display clock input</th></tr><tr><td>0</td><td>0</td><td>20 to 30MHz</td></tr><tr><td>0</td><td>1</td><td>Do not set</td></tr><tr><td>1</td><td>0</td><td>Do not set</td></tr><tr><td>1</td><td>1</td><td>20 to 80MHz</td></tr></table></td><td>See setting External Clock Input Mode (to be input from the TCK terminal).
EXCK1 : address 123_{16}</td></tr>
</table>

(2) Address 121_{16}

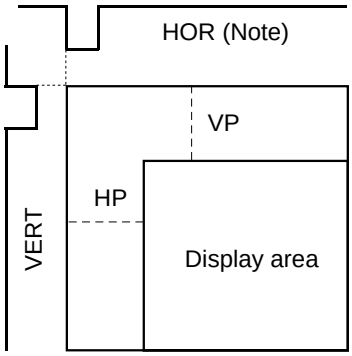
DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	0	P0 output (port P0). Port data is set by PTD0.	BLNK0 outputs blanking signal. Blanking status is determined by BLK0, BLK1, and DSP0 to DSP11 settings.
		1	BLNK0 output. Polarity is set by PTD0.	
1	PTC1	0	P1 output (port P1). Port data is set by PTD1.	
		1	R signal output. Polarity is set by PTD1.	
2	PTC2	0	P2 output (port P2). Port data is set by PTD2.	
		1	Can not be used.	
3	PTC3	0	P3 output (port P3). Port data is set by PTD3.	
		1	G signal output. Polarity is set by PTD3.	
4	PTC4	0	P4 output (port P4). Port data is set by PTD4.	
		1	Can not be used.	
5	PTC5	0	P5 output (port P5). Port data is set by PTD5.	
		1	B signal output. Polarity is set by PTD5.	
6	PTD0 (**Note**)	0	“L” output (P0 output) or negative polarity output (BLNK0 output).	P0 pin data control.
		1	“H” output (P0 output) or positive polarity output (BLNK0 output).	
7	PTD1 (**Note**)	0	“L” output (P1 output) or negative polarity output (R signal output).	P1 pin data control.
		1	“H” output (P1 output) or positive polarity output (R signal output).	
8	PTD2 (**Note**)	0	“L” output (P2 output).	P2 pin exclusive port output state control.
		1	“H” output (P2 output).	
9	PTD3 (**Note**)	0	“L” output (P3 output) or negative polarity output (G signal output).	P3 pin data control.
		1	“H” output (P3 output) or positive polarity output (G signal output).	
A	PTD4 (**Note**)	0	“L” output (P2 output).	P4 pin exclusive port output state control.
		1	“H” output (P2 output).	
B	PTD5 (**Note**)	0	“L” output (P5 output) or negative polarity output (B signal output).	P5 pin data control.
		1	“H” output (P5 output) or positive polarity output (B signal output).	
C	PTD6 (**Note**)	0	“L” output (P6 output).	P6 pin exclusive port output state control.
		1	“H” output (P6 output).	
D	PTD7 (**Note**)	0	“L” output (P7 output).	P7 pin exclusive port output state control.
		1	“H” output (P7 output).	
E	RSEL0	0	For details, see (2) Setting display frequencies under Register Supplementary Description.	Set display frequency area.
		1	To be used when EXCK0=1 and EXCK1=1.	

Note. To determined this register, input clock (at least one clock) to the external clock pin (TCK).

(3) Address 122_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>HP0
(LSB)</td><td>0
1</td><td rowspan="11">If HS is the horizontal display start location,
$HS = T \times \sum_{n=0}^{9} 2^n HP_n + 6$
T: The cycle of display frequency
1000 settings are possible.
 
</td><td rowspan="11">Horizontal display start location is specified using the 10 bits from HP9 to HP0.
HP9 to HP0 = (0000000000_2) and (0000010111_2) setting is forbidden.
Note : In case of B/$\overline{F}$ register is “0”.</td></tr>
<tr><td>1</td><td>HP1</td><td>0
1</td></tr>
<tr><td>2</td><td>HP2</td><td>0
1</td></tr>
<tr><td>3</td><td>HP3</td><td>0
1</td></tr>
<tr><td>4</td><td>HP4</td><td>0
1</td></tr>
<tr><td>5</td><td>HP5</td><td>0
1</td></tr>
<tr><td>6</td><td>HP6</td><td>0
1</td></tr>
<tr><td>7</td><td>HP7</td><td>0
1</td></tr>
<tr><td>8</td><td>HP8</td><td>0
1</td></tr>
<tr><td>9</td><td>HP9
(MSB)</td><td>0
1</td></tr>
<tr><td>A</td><td>TEST9</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>B</td><td>SPACE0</td><td>0
1</td><td rowspan="4">
<table>
<tr><th colspan="3">SPACE</th><th rowspan="2">Number of Lines and Space
(Œ represents space)</th></tr>
<tr><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>12</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1 Œ 10 Í 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2 Œ 8 Í 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3 Œ 6 Í 3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4 Œ 4 Í 4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5 Œ 2 Í 5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6 Œ 6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>6 Œ Í 6</td></tr>
</table>
Œ represents one line worth of spaces.</td><td rowspan="4">Leave one line worth of space in the vertical direction.
For example, 6 Œ 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7.
A line is 18 × N horizontal scan lines.
N is determined by the character size in the vertical direction as follows:
×1 ··· N = 1 ×2 ··· N = 2
×3 ··· N = 3 ×4 ··· N = 4</td></tr>
<tr><td>C</td><td>SPACE1</td><td>0
1</td></tr>
<tr><td>D</td><td>SPACE2</td><td>0
1</td></tr>
<tr><td>E</td><td>RSEL1</td><td>0
1</td><td>For details, see (2) Setting display frequencies under Register Supplementary Description.
To be used when EXCK0=1 and EXCK1=1.</td><td>Set display frequency area.</td></tr>
</table>

(4) Address 123_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	VP0 (LSB)	0	If VS is the vertical display start location, $VS = H \times \sum_{n=0}^{9} 2^n VP_n$ H: Cycle with the horizontal synchronizing pulse 1023 settings are possible.  	The vertical start location is specified using the 10 bits from VP9 to VP0. VP9 to VP0 = (0000000000_2) setting is forbidden. Note : In case of B/$\overline{F}$ register is “0”.
		1		
1	VP1	0		
		1		
2	VP2	0		
		1		
3	VP3	0		
		1		
4	VP4	0		
		1		
5	VP5	0		
		1		
6	VP6	0		
		1		
7	VP7	0		
		1		
8	VP8	0		
		1		
9	VP9 (MSB)	0		
		1		
A	TEST0	0	It should be fixed to “0”.	
		1	Can not be used.	
B	TEST1	0	It should be fixed to “0”.	
		1	Can not be used.	
C	TEST2	0	It should be fixed to “0”.	
		1	Can not be used.	
D	TEST3	0	It should be fixed to “0”.	
		1	Can not be used.	
E	EXCK1	0	For setting. See Register EXCK0 (address 120_{16}).	Sets input mode of external clock (input from TCK pin).
		1		

(5) Address 124_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	DSP0	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 1.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
1	DSP1	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 2.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
2	DSP2	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 3.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
3	DSP3	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 4.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
4	DSP4	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 5.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
5	DSP5	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 6.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
6	DSP6	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 7.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
7	DSP7	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 8.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
8	DSP8	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 9.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
9	DSP9	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 10.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
A	DSP10	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 11.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
B	DSP11	0	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 12.
		1	Blanking is in the display mode specified by except BLK0 and BLK1. (Note)	
C	TEST4	0	It should be fixed to “0”.	
		1	Can not be used.	
D	TEST5	0	It should be fixed to “0”.	
		1	Can not be used.	
E	TEST14	0	Can not be used.	
		1	It should be fixed to “1”.	

Note: Refer to DISPLAY FORM1.

(6) Address 125_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">LIN2</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 2nd line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">LIN3</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 3rd line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">LIN4</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 4th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">LIN5</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 5th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">LIN6</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 6th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">LIN7</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 7th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">LIN8</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 8th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">LIN9</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 9th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">V1SZ0</td><td>0</td><td rowspan="3">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>V1SZ1</th><th>V1SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="3">Character size setting in the vertical direction for the 1st line.
(display monitor 1 to 12 line)</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">V1SZ1</td><td>0</td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">VSZ1L0</td><td>0</td><td rowspan="3">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ1L1</th><th>VSZ1L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="3">Character size setting in the vertical direction (display monitor 1 line) at “0” state in register LIN2 to LIN17.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">VSZ1L1</td><td>0</td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">VSZ1H0</td><td>0</td><td rowspan="3">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ1H1</th><th>VSZ1H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="3">Character size setting in the vertical direction (display monitor 1 line) at “1” state in register LIN2 to LIN17.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">VSZ1H1</td><td>0</td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">E</td><td rowspan="2">TEST10</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Test mode</td></tr>
</table>

(7) Address 126_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">LIN10</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 10th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">LIN11</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 11th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">LIN12</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 12th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">LIN13</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 13th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">LIN14</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 14th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">LIN15</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 15th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">LIN16</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 16th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">LIN17</td><td>0</td><td>The first line is set by VSZ1L0 and VSZ1L1.
The second to 12th lines are set by VSZ2L0 and VSZ2L1.</td><td rowspan="2">Character size setting in the vertical direction for the 17th line.</td></tr>
<tr><td>1</td><td>The first line is set by VSZ1H0 and VSZ1H1.
The second to 12th lines are set by VSZ2H0 and VSZ2H1.</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">V18SZ0</td><td>0</td><td rowspan="3">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>V18SZ1</th><th>V18SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="3">Character size setting in the vertical direction for the 18th line.
(display monitor 1 to 12 line)</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">V18SZ1</td><td>0</td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">VSZ2L0</td><td>0</td><td rowspan="3">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ2L1</th><th>VSZ2L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="3">Character size setting in the vertical direction (display monitor for 2 to 12 line) at “0” state in register LIN2 to LIN17.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">VSZ2L1</td><td>0</td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">VSZ2H0</td><td>0</td><td rowspan="3">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ2H1</th><th>VSZ2H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="3">Character size setting in the vertical direction (display monitor for 2 to 12 line) at “1” state in register LIN2 to LIN17.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">VSZ2H1</td><td>0</td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">E</td><td rowspan="2">TEST11</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Test mode</td></tr>
</table>

(8) Address 127_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>RR</td><td>0
1</td><td rowspan="2"><table><tr><th>RB</th><th>RG</th><th>RR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="2">Sets the color of all blankings.</td></tr>
<tr><td>1</td><td>RG</td><td>0
1</td></tr>
<tr><td>2</td><td>RB</td><td>0
1</td><td></td><td></td></tr>
<tr><td>3</td><td>FR</td><td>0
1</td><td rowspan="3"><table><tr><th>BB</th><th>BG</th><th>BR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="3">Sets the blanking color of the Border size, or the shadow size.</td></tr>
<tr><td>4</td><td>FG</td><td>0
1</td></tr>
<tr><td>5</td><td>FB</td><td>0
1</td></tr>
<tr><td>6</td><td>TEST6</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>7</td><td>TEST7</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>8</td><td>TEST8</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>9</td><td>BETA14</td><td>0</td><td>Matrix-outline display (12 × 18 dot)</td><td rowspan="2">Set this register to the character font set by display RAM BR, BG and BB.</td></tr>
<tr><td></td><td>1</td><td>Matrix-outline display (14 × 18 dot)</td></tr>
<tr><td>A</td><td>HSZ10</td><td>0
1</td><td rowspan="2">T: Display frequency cycle<table><tr><th>HSZ11</th><th>HSZ10</th><th>Horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table></td><td rowspan="2">Character size setting in the horizontal direction for the first line.</td></tr>
<tr><td>B</td><td>HSZ11</td><td>0
1</td></tr>
<tr><td>C</td><td>HSZ20</td><td>0
1</td><td rowspan="2">T: Display frequency cycle<table><tr><th>VSZ21</th><th>HSZ20</th><th>Horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table></td><td rowspan="2">Character size setting in the horizontal direction for the 2nd line to 12th line.</td></tr>
<tr><td>D</td><td>HSZ21</td><td>0
1</td></tr>
<tr><td>E</td><td>TEST12</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td></td><td>1</td><td>Test mode</td></tr>
</table>

(9) Address 128_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BCOL</td><td>0</td><td>Blanking of BLK0, BLK1</td><td rowspan="2">Sets all raster blanking</td></tr>
<tr><td>1</td><td>All raster blanking</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">B/F</td><td>0</td><td>Synchronize with the leading edge of horizontal synchronization.</td><td rowspan="2">Synchronize with the front porch or back porch of the horizontal synchronazation signal.</td></tr>
<tr><td>1</td><td>Synchronize with the trailing edge of horizontal synchronization.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">VMASK</td><td>0</td><td>Do not mask by VERT input signal</td><td rowspan="2">This register has or do not have mask at phase comparison operating.</td></tr>
<tr><td>1</td><td>Mask by VERT input signal</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">POLV</td><td>0</td><td>VERT pin is negative polarity</td><td rowspan="2">Set VERT pin polarity.</td></tr>
<tr><td>1</td><td>VERT pin is positive polarity</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">POLH</td><td>0</td><td>HOR pin is negative polarity</td><td rowspan="2">Set HOR pin polarity.</td></tr>
<tr><td>1</td><td>HOR pin is positive polarity</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BLK0</td><td>0</td><td rowspan="4"><table><tr><th colspan="2">BLK</th><th rowspan="2">Blanking mode</th></tr><tr><th>1</th><th>0</th></tr><tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr></table></td><td rowspan="4">Set blanking mode. (Note 1)
An example of blanking mode at BCOL = “0”, DSPn = “0” (n = 0 to 11) shown left.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BLK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">SYAD</td><td>0</td><td>Border display of character</td><td rowspan="2">(Note 2)</td></tr>
<tr><td>1</td><td>Shadow display of character</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">RAMERS</td><td>0</td><td>RAM not erased</td><td rowspan="2">There is no need to reset because there is no register for this bit.</td></tr>
<tr><td>1</td><td>RAM erased</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">STOP</td><td>0</td><td>Oscillation of clock for display</td><td rowspan="2">R, G, B and BLNK0 output can be altered.</td></tr>
<tr><td>1</td><td>Stop the oscillation of clock for display</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">DSPON</td><td>0</td><td>Display OFF</td><td rowspan="2">Display can be altered.</td></tr>
<tr><td>1</td><td>Display ON</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">BLINK0</td><td>0</td><td rowspan="4"><table><tr><th colspan="2">BLINK</th><th rowspan="2">Duty</th></tr><tr><th>1</th><th>0</th></tr><tr><td>0</td><td>0</td><td>Blinking OFF</td></tr><tr><td>0</td><td>1</td><td>25%</td></tr><tr><td>1</td><td>0</td><td>50%</td></tr><tr><td>1</td><td>1</td><td>75%</td></tr></table></td><td rowspan="4">Blinking duty ratio can be altered.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">BLINK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">BLINK2</td><td>0</td><td>Divided into 64 of vertical synchronous signal</td><td rowspan="2">Blinking frequency can be altered.</td></tr>
<tr><td>1</td><td>Divided into 32 of vertical synchronous signal</td></tr>
<tr><td rowspan="2">E</td><td rowspan="2">TEST13</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Test mode</td></tr>
</table>

Notes 1: Refer to DISPLAY FORM 1 2: Refer to DISPLAY FORM 3

REGISTER SUPPLEMENTARY DESCRIPTION

(1) Setting external clock input mode (by use of EXCK0 (120_{16}) and EXCK1 (123_{16}))

Two modes given below are available for the external clock signal input. (the settings (EXCK1, EXCK0) = (0, 1), (1, 0) are forbidden.)

(a) When (EXCK1, EXCK0) = (0, 0), F_{OSC} = 20 to 30 MHz

Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronization signal. And input from HOR pin a constant-period continuous horizontal synchronous signal.

Never stop inputting the clock while displaying.

Do not have to set a display frequency because the clock just as it is entered from outside is used as the display clock.

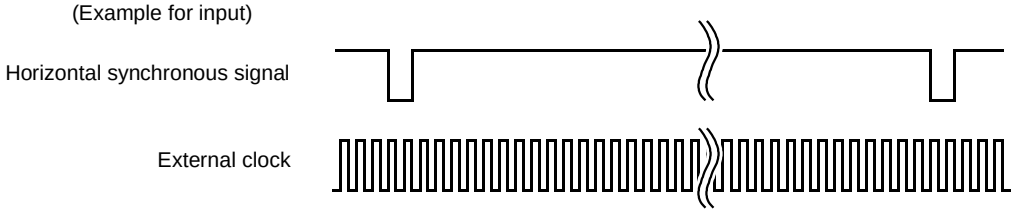
(b) When (EXCK1, EXCK0) = (1, 1), F_{OSC} = 20 to 80 MHz

Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronization signal.

Never stop inputting the clock while displaying.

Be sure to set a display frequency because the internal clock made to synchronize with the clock input from outside is used as the display clock (see the next page).

(Example for input)



(2) Setting display frequencies

Set a display frequency by setting a frequency value for the horizontal synchronization signal by use of DIV10 to DIV0 (120_{16}).

Set display frequency area in conformity with the frequency of the external clock signal.

Set display frequency area by use of DIVS0, DIVS1 (120_{16}), RSEL0 (121_{16}), and RSEL1 (122_{16}). Frequency area are as follows.

RSEL1	RSEL0	DIVS1	DIVS0	Display frequency area
0	1	0	0	70.0 to 80.0
0	0	0	0	63.0 to 70.0
1	0	0	1	56.6 to 63.0
0	1	0	1	46.6 to 56.6
0	0	0	1	45.0 to 46.6
1	0	1	0	42.5 to 45.0
0	1	1	0	35.0 to 42.5
0	0	1	0	31.5 to 35.0
1	0	1	1	28.3 to 31.5
0	1	1	1	23.3 to 28.3
0	0	1	1	20.0 to 23.3

Cautions in setting a display frequency

To change the external clock frequency or the horizontal synchronization frequency, follow the steps in sequence given below.

(a) Display OFF (DSPON = 0)

(b) Set the display frequency (Use DIV10 to DIV0 (120_{16}), DIVS0, DIVS1 (120_{16}), RSEL0 (121_{16}), and RSEL1 (122_{16}).)

(c) 20-ms waiting time with the horizontal synchronization signal and the external clock signal being input

(d) Display ON (DSPON = 1)

DISPLAY FORM1

Table 1 shows display form of blanking.

Table 1. Display mode

BCOL	Standard blanking		When the all of registers DSPn (Note 2) are set to "0"	When some of registers DSPn are set to "1"		BLNK0 output
	BLK1	BLK0		DSPn = 0	DSPn = 1	
0	0	0	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline display color set: display RAM (Note 3)	DSPn = "0" line, DSPn = "1" line ┐ Matrix-outline size
	0	1	Character	Character	Border display color set: display RAM (Note 3)	DSPn = "0" line→Character size DSPn = "1" line→Border size
	1	0	Border display color set: display RAM (Note 3)	Border display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	DSPn = "0" line→Border size DSPn = "1" line→Matrix-outline size
	1	1	Matrix-outline display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	Character	DSPn = "0" line→Matrix-outline size DSPn = "1" line→Character size
1 (Note 1)	0	0	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline display color set: display RAM (Note 3)	All blanking size
	0	1	Character	Character	Border display color set: display RAM (Note 3)	
	1	0	Border display color set: display RAM (Note 3)	Border display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	
	1	1	Matrix-outline display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	Character	

Notes 1: Color setting of raster area is set by register RR, RG and RB.
2: DSPn (n = 0 to 11)
3: Set by BR, BG and BB of display RAM.
4: Set border by register FR, FG and FB. Set matrix-outline by BR, BG and BB of display RAM.

DISPLAY FORM 2

M35046-XXXSP/FP has the following four display forms.

(1) Character size
: Blanking same as the character size.

(2) Border size
: Blanking the background as a size from character.

(3) Matrix-outline size
: Blanking the background 12 × 18 dot.
When set register BETA14 to "1", setting of blanking the background 14 × 18 dot is possible.

(4) All blanking size
: When set register BCOL to "1", all raster area is blanking.

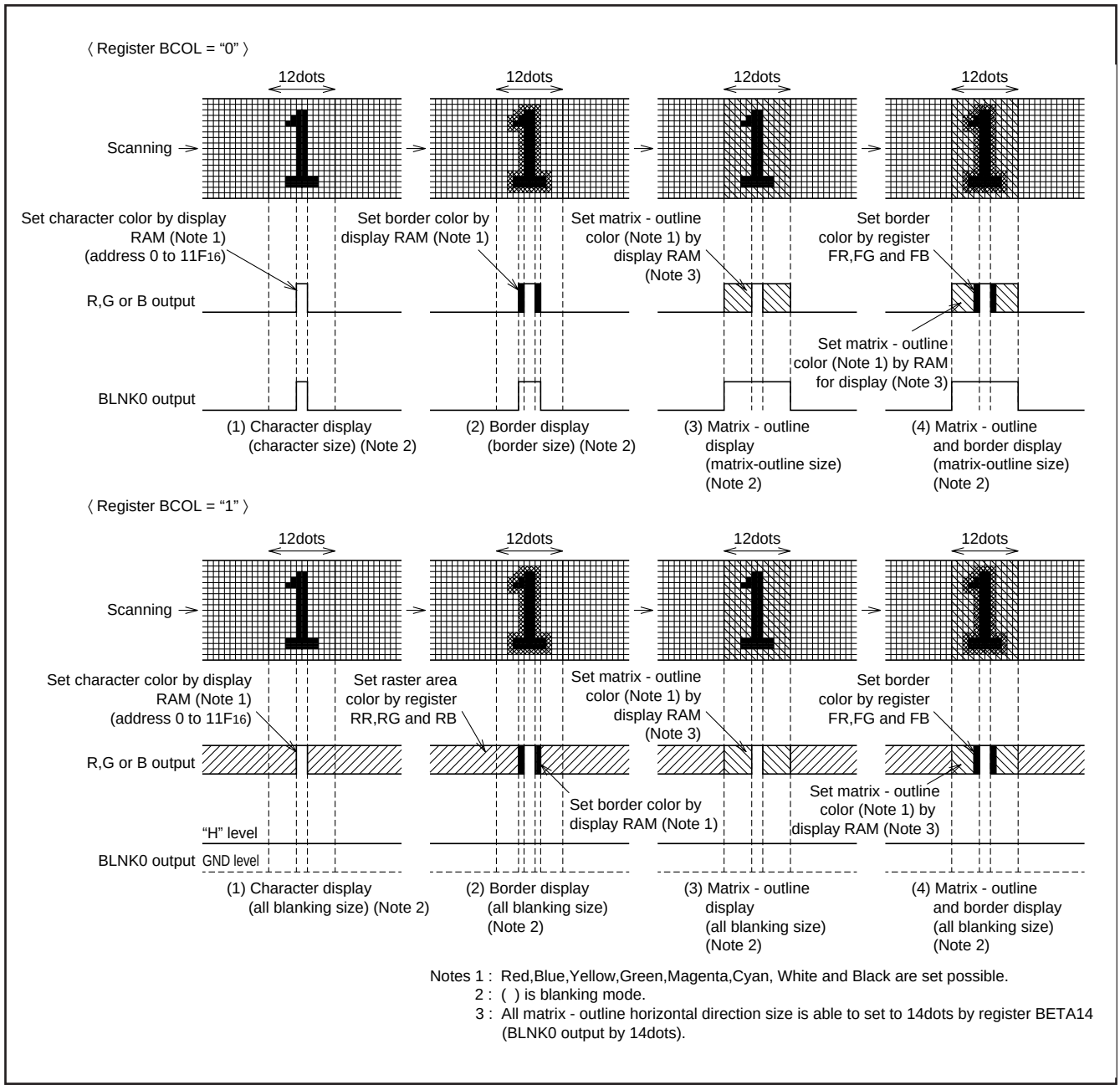


Fig. 3 Display form

DISPLAY FORM 3

When border display mode, if set SYAD = “0” to “1”, it change to shadow display mode.
Border and shadow display are shown below.

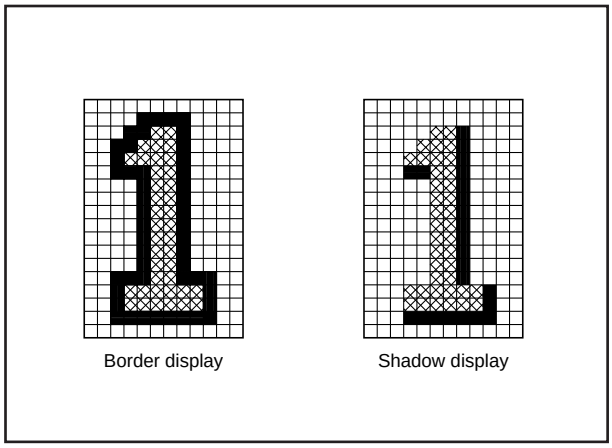


Fig. 4 Border and shadow display

Set shadow display color by display RAM or register FR, FG and FB.

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the serial input function. Example of data setting is shown in Figure 5 and Figure 6.

(1) At EXCK0 = “0”, EXCK1 = “0” setting

Example of data setting by the serial input function (M35046-XXXSP/FP)

		DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Addition
		200 msec hold																System set-up
1	address 120_{16}	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	Address set
2	data 120_{16}	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	(Note 1)
3	data 121_{16}	0	0	PTD7	PTD6	1	PTD4	1	PTD2	1	1	1	0	1	0	1	1	Output setting
4	data 122_{16}	0	0	0	0	0	0	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting
5	data 123_{16}	0	0	0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display location setting
6	data 124_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting
7	data 125_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
8	data 126_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
9	data 127_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Color, character size setting
10	data 128_{16}	0	0	0	0	0	0	0	1	0	1	1	POLH	POLV	0	0	0	Display OFF, display form (Note 2)
11	data 000_{16}	0	BB	BG	BR	BLINK	B	G	R	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	
12 ⋮ 297	⋮	⋮	Character background color			Blink-ing	Character color			Character code								Character setting
298	data $11F_{16}$	0	BB	BG	BR	BLINK	B	G	R	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	
299	address 128_{16}	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	Address setting
300	data 128_{16}	0	0	0	0	0	1	0	0	0	1	1	POLH	POLV	0	0	0	Display ON, display form (Note 2)

Notes 1 : Input the horizontal synchronous signal to the HOR pin and the vertical synchronous signal to the VERT pin. If serrated pulses are present in the vertical synchronous signal, set the register VMASK to 1.
2 : Matrix-outline display in this data.

Fig. 5 Example of data setting by the serial input function (1)

(2) At EXCK0 = “1”, EXCK1 = “1” setting

		DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Addition
		200 msec hold																System set-up
1	address 120_{16}	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	Address set
2	data 120_{16}	0	1	1	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	Set frequency value of horizontal synchronous frequency(Note 1)
3	data 121_{16}	0	RSEL0	PTD7	PTD6	1	PTD4	1	PTD2	1	1	1	0	1	0	1	1	Output setting Oscillation circuit setting
4	data 122_{16}	0	RSEL1	0	0	0	0	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting Oscillation circuit setting
5	data 123_{16}	0	1	0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display location setting
6	data 124_{16}	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting
7	data 125_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
8	data 126_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
9	data 127_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Color, character size setting
10	data 128_{16}	0	0	0	0	0	0	0	1	0	1	1	POLH	POLV	0	0	0	Display OFF, display form (Note 2)
		Hold the time length as 1V of vertical synchronous signal																
11	data 000_{16}	0	BB	BG	BR	BLINK	B	G	R	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	Character setting
12 ⋮ 297	⋮	⋮	Character background color			BLINK -ING	Character color			Character code								
298	data $11F_{16}$	0	BB	BG	BR	BLINK	B	G	R	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	
299	address 128_{16}	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	Address setting
300	data 128_{16}	0	0	0	0	0	1	0	0	0	1	1	POLH	POLV	0	0	0	Display ON, display form (Note 2)

Notes 1 : From this time, input clock to TCK pin. And, input the horizontal synchronous signal to the HOR pin and the vertical synchronous signal to the VERT pin. If serrated pulses are present in the vertical synchronous signal, set the register VMASK to 1.
2 : Matrix-outline display in this data.

Fig. 6 Example of data setting by the serial input function (2)

SERIAL DATA INPUT TIMING

(1) Serial data should be input with the LSB first.
(2) The address consists of 16 bits.
(3) The data consists of 16 bits.
(4) The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits. Therefore, it is not necessary to input the address from the second data.

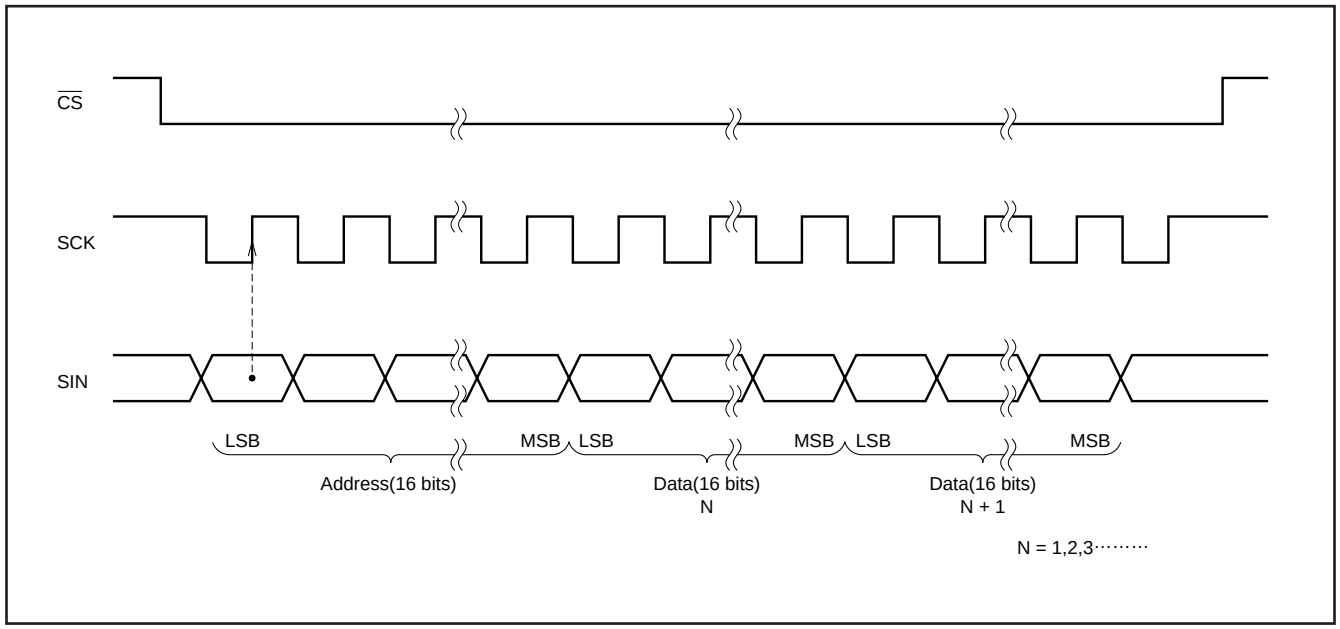


Fig. 7 Serial input timing

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

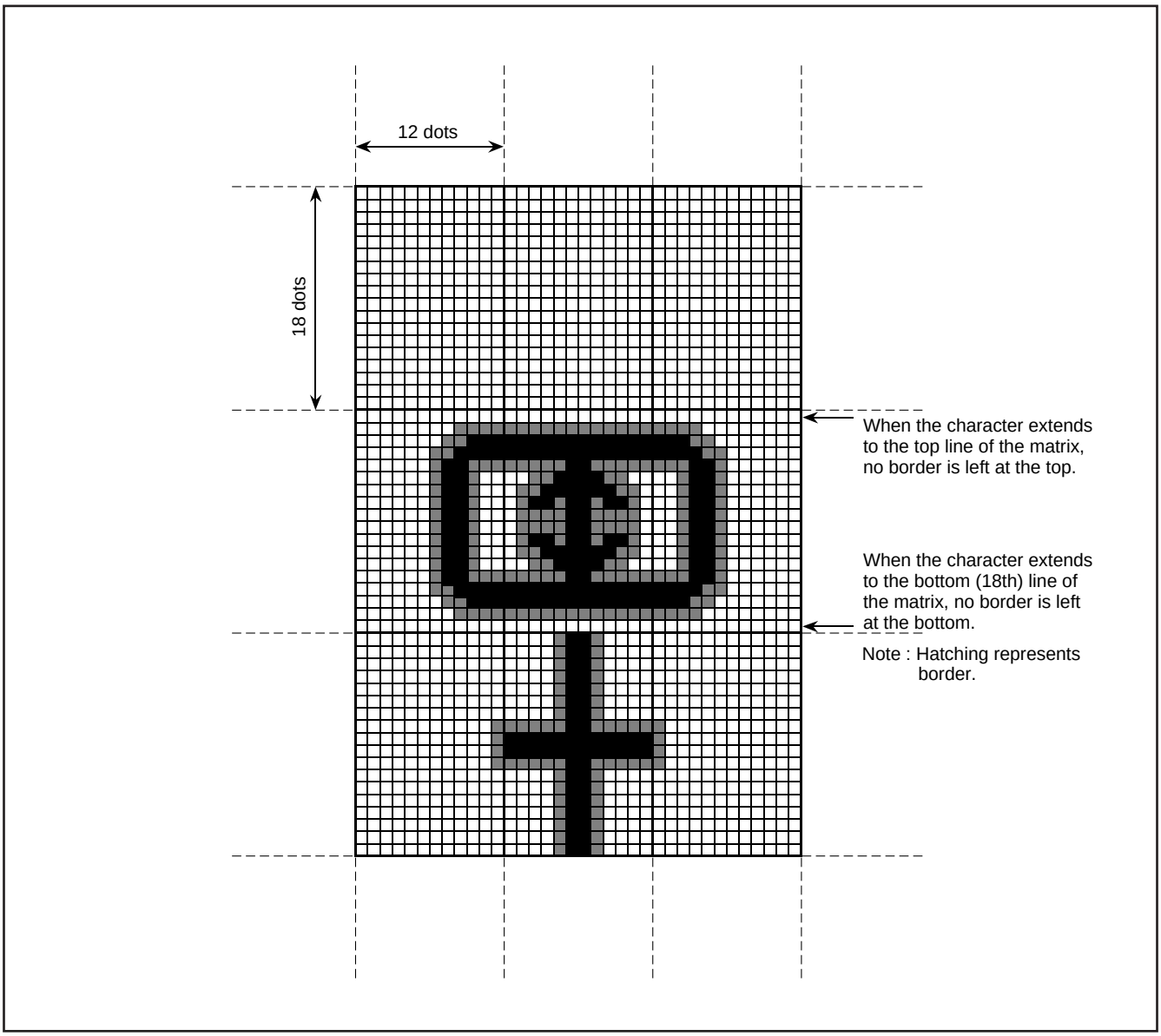


Fig. 8 Example for displaying a continuous pattern after combining characters in the horizontal or vertical direction

Character code FF_{16} is fixed as a blank without background. Therefore, cannot register a character font in this code.

TIMING REQUIREMENTS (Ta = –20°C to + 85°C, V_{DD} = 5±0.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_{w(SCK)}$	SCK width	200	—	—	ns	See Figure 9
$t_{su(\overline{CS})}$	$\overline{CS}$ setup time	200	—	—	ns	
$t_{h(\overline{CS})}$	$\overline{CS}$ hold time	2	—	—	μs	
$t_{su(SIN)}$	SIN setup time	200	—	—	ns	
$t_{h(SIN)}$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	10	—	—	μs	

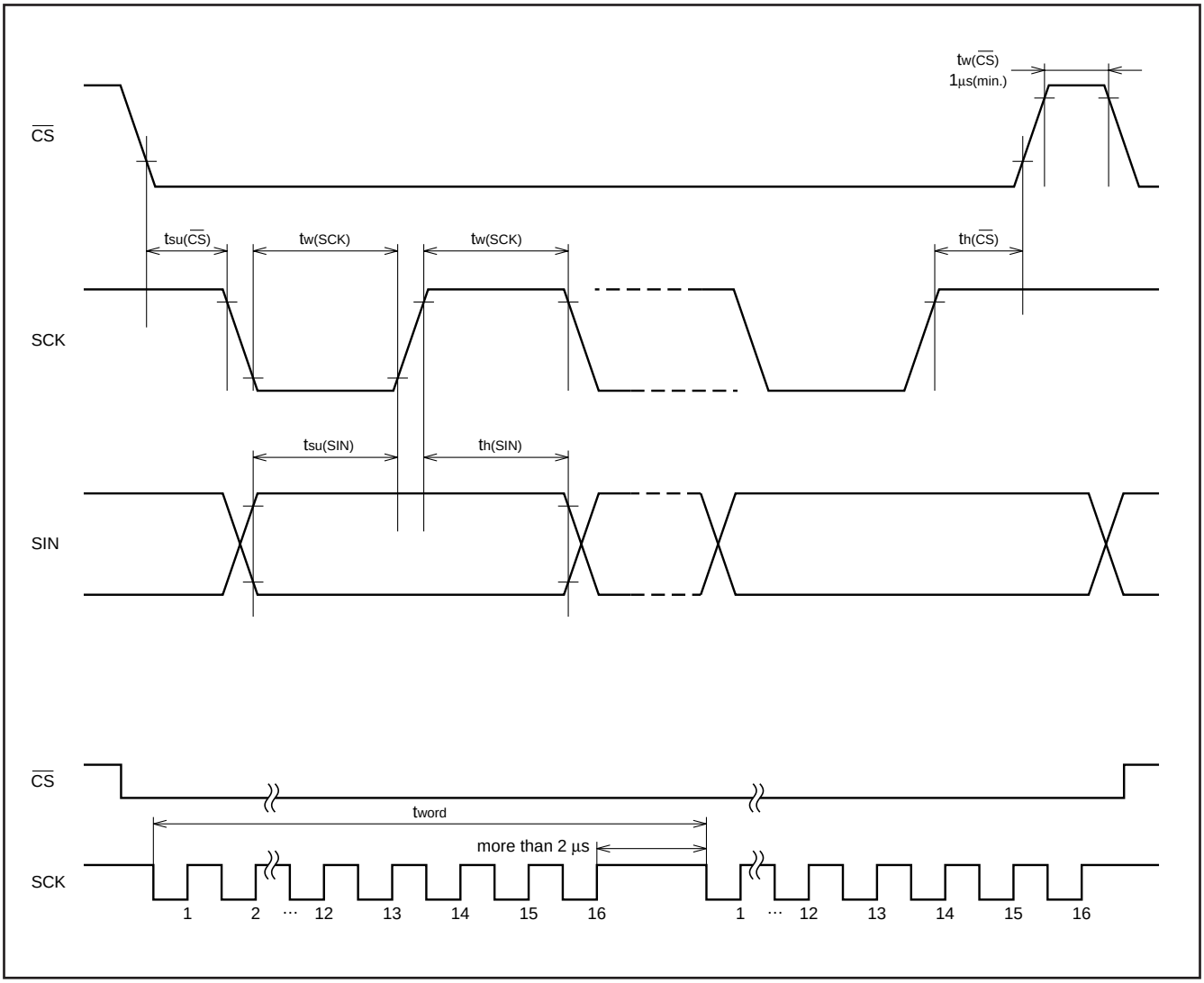


Fig. 9 Serial input timing requirements

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}.	–0.3 to +6.0	V
V_I	Input voltage		V_{SS} –0.3 ≤ V_I ≤ V_{DD} +0.3	V
V_O	Output voltage		V_{SS} ≤ V_O ≤ V_{DD}	V
P_d	Power dissipation	Ta = 25°C	300	mW
T_{opr}	Operating temperature		–20 to +85	°C
T_{stg}	Storage temperature		–40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5V, Ta = –20 to +85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{DD}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	“H” level input voltage SIN, SCK, $\overline{CS}$, $\overline{AC}$ HOR, VERT	0.8V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	“L” level input voltage SIN, SCK, $\overline{CS}$, $\overline{AC}$ HOR, VERT	0	0	0.2V_{DD}	V
F_{OSC}	Oscillating frequency for display	20.0	—	80.0	MHz
Hsync	Horizontal synchronous signal input frequeney	15.0	—	130.0	kHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage		Ta = –20 to +85°C	4.75	5.0	5.25	V
I_{DD}	Supply current		V_{DD} = 5.25V	—	30	50	mA
V_{OH}	“H” level output voltage	P0 to P7	V_{DD} = 4.75V, I_{OH} = 0.4mA	3.5	—	—	V
		CPOUT	V_{DD} = 4.75V, I_{OH} = 0.05mA				
V_{OL}	“L” level output voltage	P0 to P7	V_{DD} = 4.75V, I_{OL} = 0.4mA	—	—	0.4	V
		CPOUT	V_{DD} = 4.75V, I_{OL} = 0.05mA				
R_I	Pull-up resistance SCK, $\overline{AC}$, $\overline{CS}$, SIN		V_{DD} = 5.0V	10	30	100	kΩ
V_{TCK}	External clock input width		4.75V < V_{DD} ≤ 5.25V	0.7V_{DD}	—	0.9V_{DD}	V_{PP}

NOTE FOR SUPPLYING POWER

Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35046-XXXSP/FP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin in hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 11.

Timing of power supplying to V_{DD1} and V_{DD2}.

Supply power to V_{DD1} and V_{DD2} at the same time.

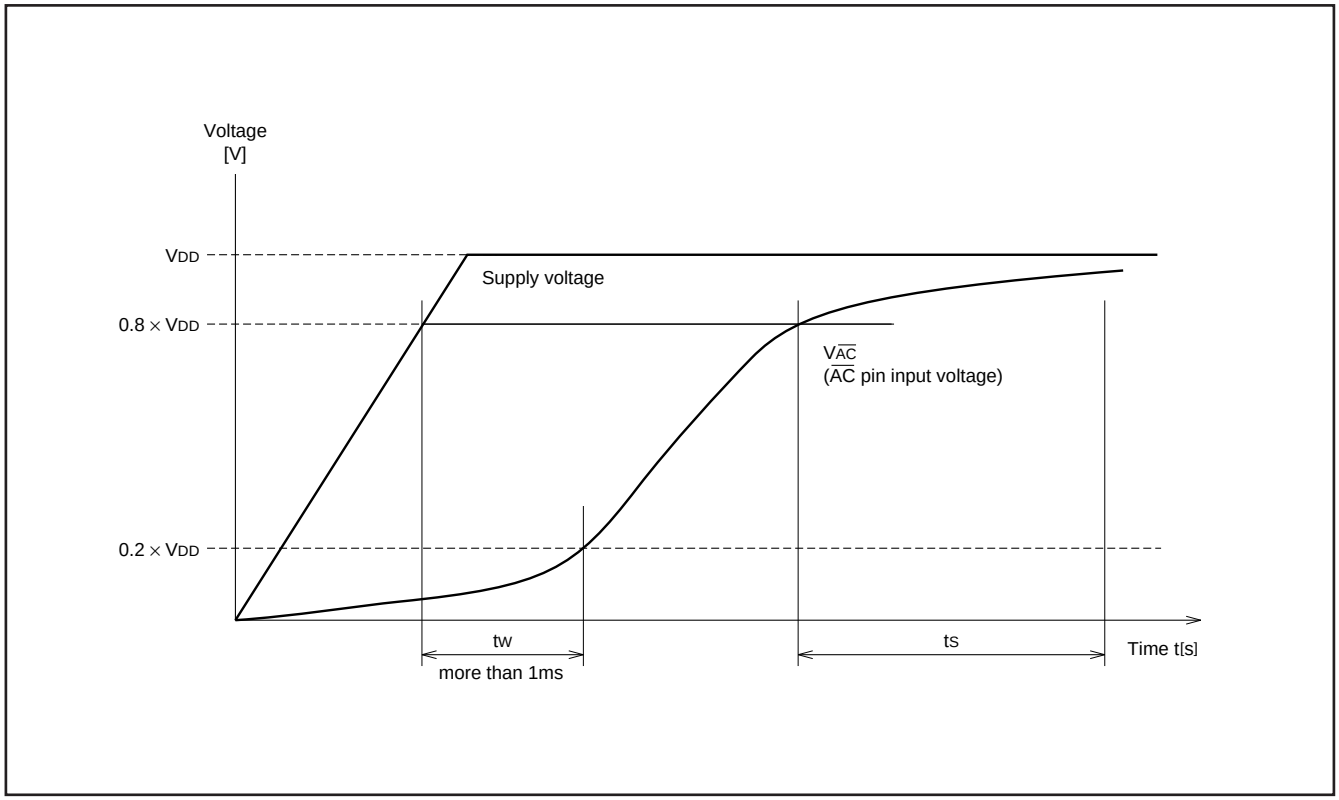


Fig. 11 Timing of power supplying to $\overline{AC}$ pin

After supplying the power (V_{DD} and V_{SS}) to M35046-XXXSP/FP and the supply voltage becomes more than $0.8 \times V_{DD}$, it needs to keep V_{IL} time; tw of the $\overline{AC}$ pin for more than 1ms.

Start inputting from microcomputer after $\overline{AC}$ pin supply voltage becomes more than $0.8 \times V_{DD}$ and keeping 200ms wait time.

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor (≈0.1μF) directly between the V_{DD1} pin and V_{SS} pin, and the V_{DD2} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

(1) M35046-XXXSP/FP mask ROM order confirmation form
(2) 20P4B mask specification form
(3) 20P2Q-A mask specification from
(4) ROM data (EPROM 3 sets)
(5) Floppy disks containing the character font generating program + character data

STANDARD ROM TYPE : M35046-001SP/FP

M35046-001SP/FP is a standard ROM type of M35046-XXXSP/FP. The character patterns are fixed to the contents of Figure 12 to 15.

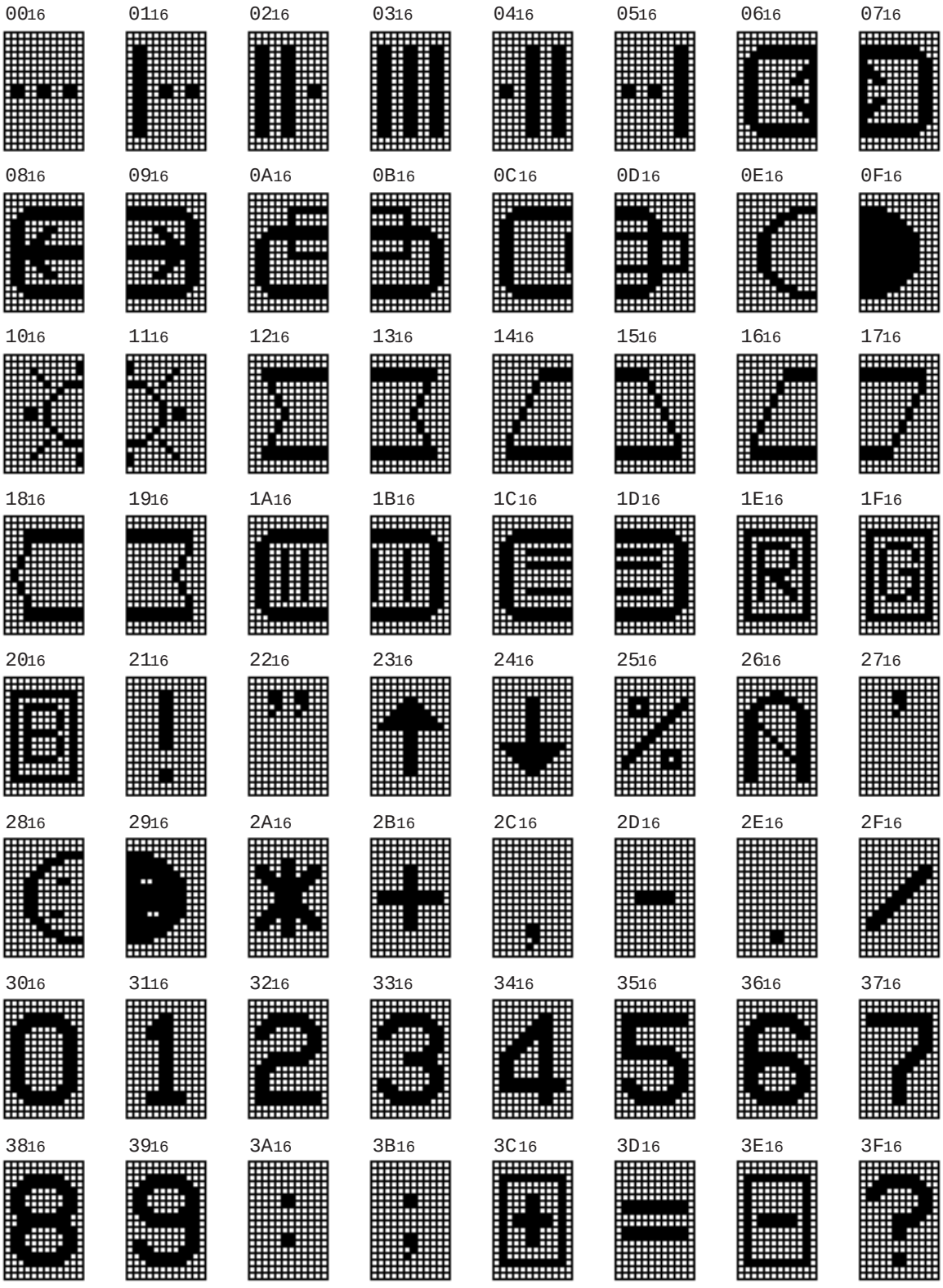


Fig. 12 M35046-001SP/FP character pattern (1)

Fig. 13 M35046-001SP/FP character pattern (2)

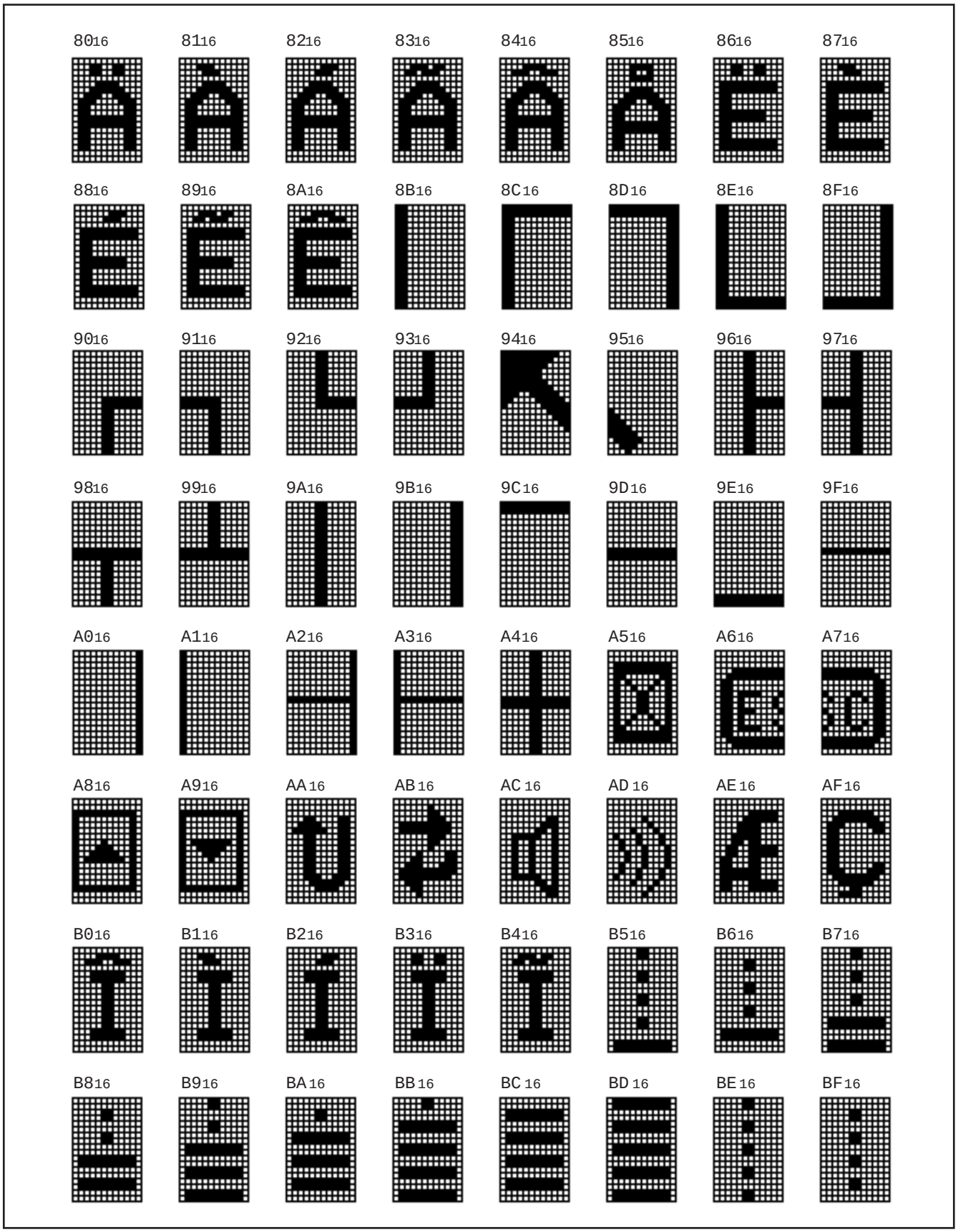


Fig. 14 M35046-001SP/FP character pattern (3)

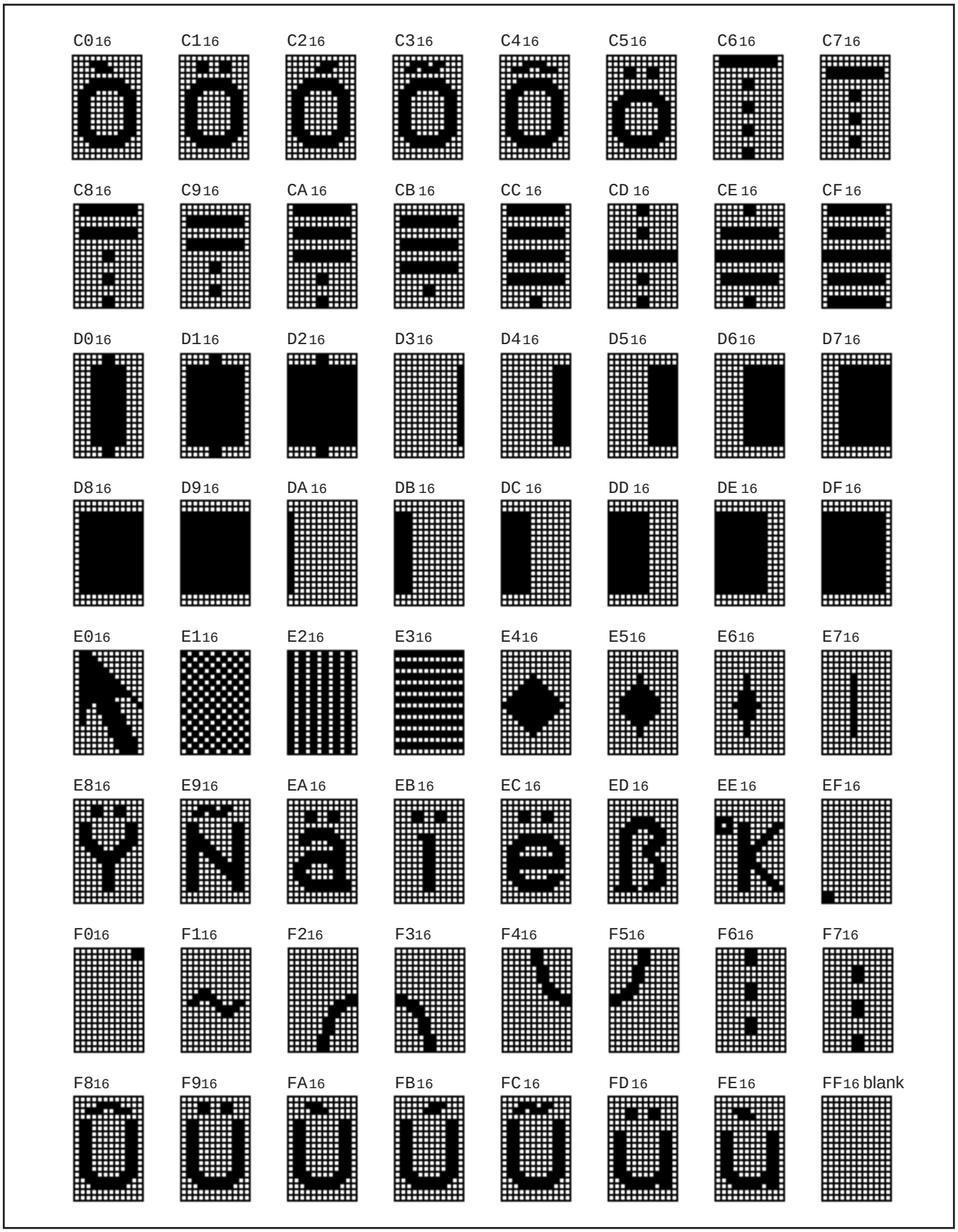


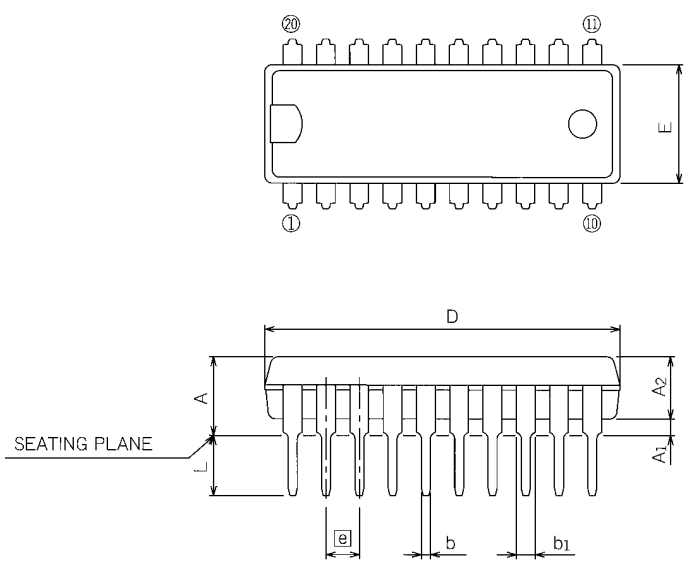
Fig. 15 M35046-001SP/FP character pattern (4)

PACKAGE OUTLINE

20P4B — Plastic 20pin 300mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP20-P-300-1.78	—	1.0	

Scale : 2.5/1

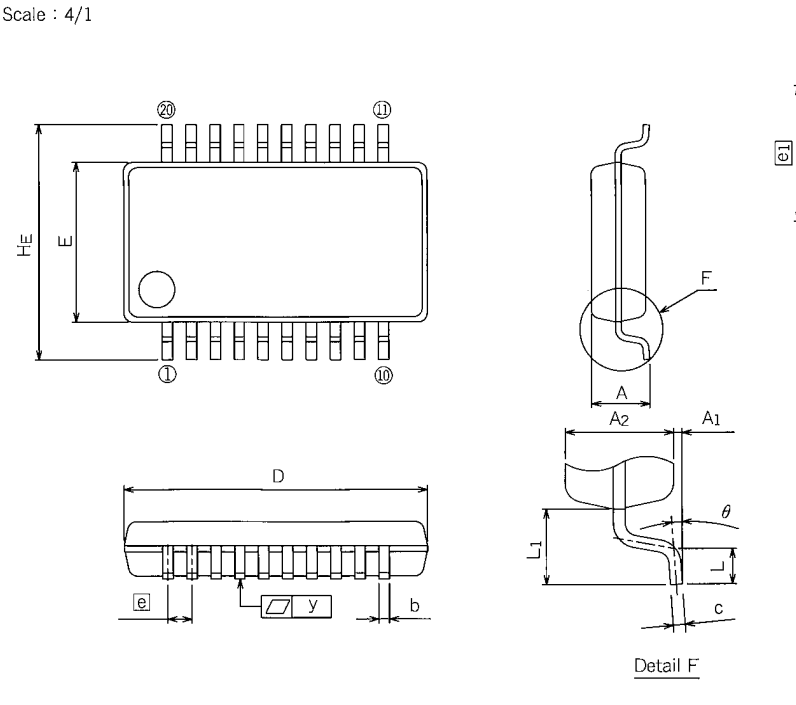


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.38	0.48	0.58
b_1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	—	1.778	—
e_1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

20P2Q−A — Plastic 20pin 300mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP020-P-0300	—	0.2	Cu Alloy

Scale : 4/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.1
A_1	0	0.1	0.2
A_2	—	1.8	—
b	0.3	0.35	0.45
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	—	0.8	—
H_E	7.5	7.8	8.1
L	0.4	0.6	0.8
L_1	—	1.25	—
y	—	—	0.1
θ	0°	—	8°
b_2	—	0.5	—
e_1	—	7.62	—
l_2	1.27	—	—

MITSUBISHI MICROCOMPUTERS

M35046-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

RENESAS
Renesas Technology Corp.

REVISION DESCRIPTION LIST	M35046-XXXSP/FP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	9902
1.1	Delete Mask ROM ORDER CONFIRMATION FORM and MASK SPECIFICATION FORM	0008