GS2964 Adaptive Cable Equalizer

Key Features

- SMPTE 424M, SMPTE 292M and SMPTE 259M compliant
- Automatic cable equalization
- Multi-standard operation from 143Mb/s to 2.97Gb/s
- Performance optimized for 270Mb/s, 1.485Gb/s and 2.97Gb/s. Typical equalized length of Belden 1694A cable:
  - 100m at 2.97Gb/s
  - 140m at 1.485Gb/s
  - 180m at 270Mb/s
- Supports DVB-ASI at 270Mb/s
- Manual bypass (useful for low data rates with slow rise/fall times)
- Programmable carrier detect with squelch threshold adjustment
- Standard EIA/JEDEC logic control and status signal levels
- Single 3.3V power supply operation
- 215mW power consumption (typical)
- Wide temperature range of -40°C to +85°C
- Small footprint QFN package (4mm x 4mm)
  - Drop-in compatible with the GS2974
- Pb-free and RoHS compliant

Applications

- SMPTE 424M, SMPTE 292M and SMPTE 259M coaxial cable serial digital interfaces

Description

The GS2964 is a high-speed BiCMOS integrated circuit designed to equalize and restore signals received over 75Ω coaxial cable.

The device is designed to support SMPTE 424M, SMPTE292M and SMPTE 259M, and is optimized for performance at 270Mb/s, 1.485Gb/s and 2.97Gb/s.

The GS2964 features DC restoration to compensate for the DC content of SMPTE pathological test patterns.

The Carrier Detect output pin ($\overline{CD}$) indicates whether a valid input signal has been detected. It can be connected directly to the MUTE pin to mute the output on loss of carrier. A voltage programmable threshold, which can be changed via the SQ_ADJ pin, forces $\overline{CD}$ high when the input signal amplitude falls below the threshold. This allows the GS2964 to distinguish between low-amplitude SDI signals and noise at the input of the device.

The equalizing and DC restore stages are disengaged when the BYPASS pin is HIGH. No equalization occurs in Bypass mode.

The differential outputs can be DC-coupled to Gennum 3.3V cable drivers and reclockers and to other industry-standard 3.3V CML logic.

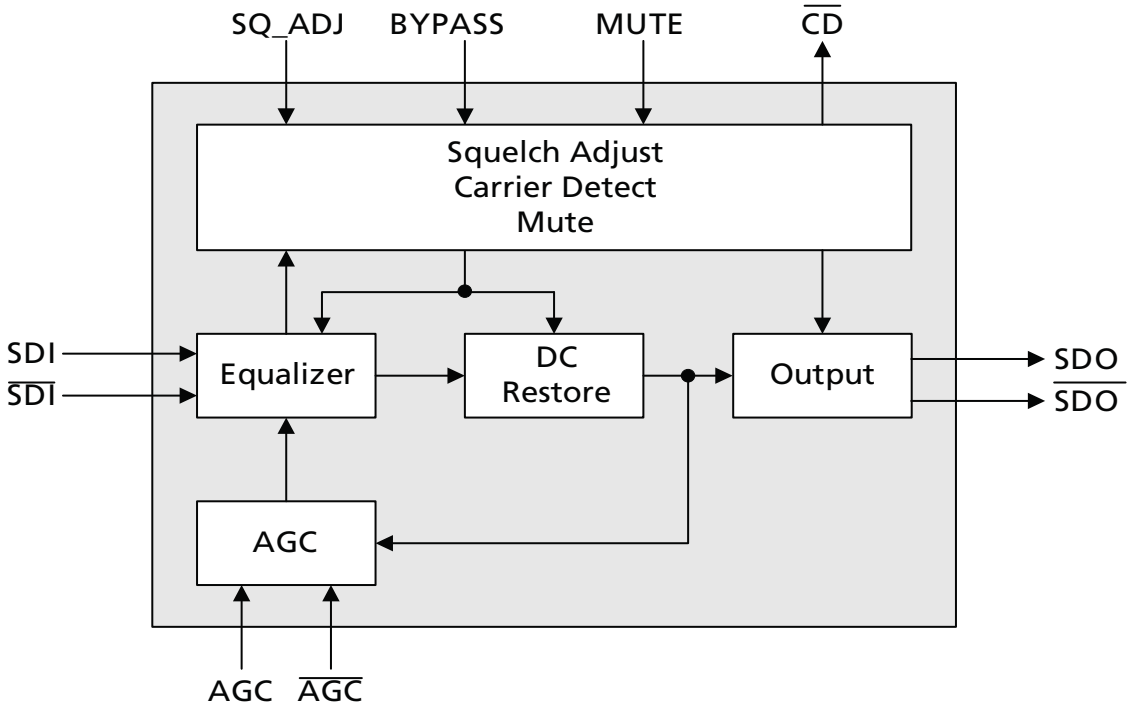
The GS2964 is footprint and drop-in compatible with existing GS2974 designs, with no additional application changes required.

The device is available in a 16-pin, 4mm x 4mm QFN package.

Power consumption of the GS2964 is typically 215mW.

The GS2964 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



GS2964 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
3	153913	54547	March 2010	Changed ESD rating from 6kV to 5kV in Section 2.1 Absolute Maximum Ratings.
2	152613	–	September 2009	Updates to Output Voltage Swing specifications in Table 2-2: AC Electrical Characteristics.
1	152312	–	July 2009	Converted to Data Sheet.
0	151929	–	May 2009	Conversion to Preliminary Data Sheet.
B	151798	–	April 2009	Updates.
A	151181	–	January 2009	New document.

Contents

1. Pin Out

1.1 GS2964 Pin Assignment

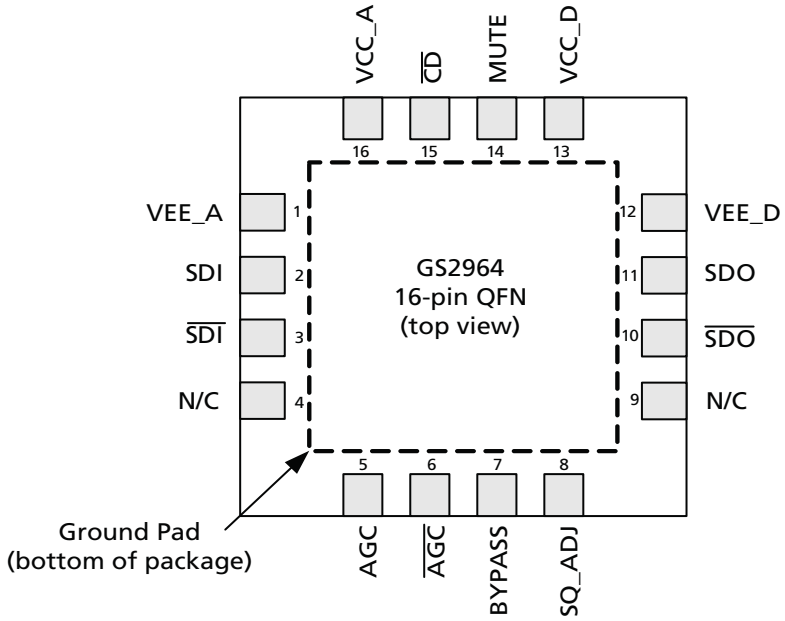


Figure 1-1: GS2964 Pin Out

1.2 GS2964 Pin Descriptions

Table 1-1: GS2964 Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	VEE_A	Analog	Power	Most negative power supply for analog circuitry. Connect to GND.
2, 3	SDI, $\overline{\text{SDI}}$	Analog	Input	Serial digital differential input.
4, 9	N/C	–	–	No Connect. Not bonded internally.
5, 6	AGC, $\overline{\text{AGC}}$	Analog	–	External AGC capacitor. Connect pin 5 and pin 6 together as shown in the Typical Application Circuit on page 13.
7	BYPASS	Not Synchronous	Input	Forces the Equalizing and DC RESTORE stages into bypass mode when HIGH. No equalization occurs in this mode. (Internal pull-down).
8	SQ_ADJ	Analog	Input	Squelch Adjust. Adjusts the approximate amount of cable equalized before $\overline{\text{CD}}$ goes low. See Section 4.4 and Section 4.5. (Internal pull-down).
10, 11	$\overline{\text{SDO}}$, SDO	Analog	Output	Equalized serial digital differential output.

Table 1-1: GS2964 Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
12	VEE_D	Analog	Power	Most negative power supply for the digital circuitry and output buffer. Connect to GND.
13	VCC_D	Analog	Power	Most positive power supply for the digital I/O pins of the device. Connect to +3.3V DC.
14	MUTE	Not Synchronous	Input	CONTROL SIGNAL INPUT levels are LVCMOS/LVTTL compatible. (3.3V Tolerant) Controls output behaviour on SDO and $\overline{\text{SDO}}$. (Internal pull-down). See Section 4.5.
15	$\overline{\text{CD}}$	Not Synchronous	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Indicates the presence of an input signal. See Section 4.5.
16	VCC_A	Analog	Power	Most positive power supply for the analog circuitry of the device. Connect to +3.3V DC.
–	Center Pad	–	Power	Internally bonded to VEE_A.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to +3.6V DC
Input ESD Voltage (HBM)	5kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V	±5%
Power Consumption	P_D	T_A = 25°C	–	215	–	mW	–
Supply Current	I_s	T_A = 25°C	–	65	–	mA	–
Output Common Mode Voltage	V_{CMOUT}	T_A = 25°C	–	V_{CC} - $\Delta V_{SDO}/2$	–	V	–
Input Common Mode Voltage	V_{CMIN}	T_A = 25°C	–	2.2	–	V	–
SQ_ADJ DC Voltage (to mute signal)	–	0m, T_A = 25°C	–	3.2	–	V	–
SQ_ADJ Range	–	T_A = 25°C	–	1	–	V	–
$\overline{CD}$ Output Voltage	$V_{\overline{CD}(OH)}$	Carrier not present	2.4	–	–	V	–
	$V_{\overline{CD}(OL)}$	Carrier present	–	–	0.4	V	–
Mute Input Voltage Required to Force Outputs to Mute	V_{Mute}	Min to Mute	2.0	–	–	V	–
Mute Input Voltage Required to Force Outputs Active	V_{Mute}	Max to Activate	–	–	0.8	V	–

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	143	–	2970	Mb/s	–
Input Voltage Swing	ΔV_{SDI}	T_A =25°C, differential, 270Mb/s and 1.485Gb/s	720	800	950	mV_{p-p}	1
		T_A =25°C, differential, 2.97Gb/s	720	800	880	mV_{p-p}	1
Output Voltage Swing	ΔV_{SDO}	100Ω load, T_A =25°C, differential	650	800	950	mV_{p-p}	–
Output Jitter of Various Cable Lengths and Data Rates	–	270Mb/s Belden 1694A: 0-180m	–	0.2	–	UI	2
	–	1.485Gb/s Belden 1694A: 0-140m	–	0.25	–	UI	2
	–	2.97Gb/s Belden 1694A: 0-100m	–	0.35	–	UI	2
Output Rise/Fall time	–	2.97Gb/s & 1.485Gb/s 20% - 80%	35	65	90	ps	–
		270Mb/s (see Section 4.6)					
Mismatch in rise/fall time	–	–	–	30	–	ps	–
Duty cycle distortion	–	–	–	–	30	ps	–
Overshoot	–	–	–	–	10	%	–
Input Return Loss	–	–	15	–	–	dB	3
Input Resistance	–	single ended	–	1.7	–	kΩ	–
Input Capacitance	–	single ended	–	1	–	pF	–
Output Resistance	–	single ended	–	50	–	Ω	–

NOTES:

1. 0m cable length.
2. Based on characterization data using the recommended applications circuit, at V_{CC} = 3.3V, T_A = 25°C and 800mV launch swing from the SDI cable driver.
3. Tested on GS2964 board from 5MHz to 3GHz.

2.4 Typical Performance Curves

VCC=3.3V, room temperature, 800mV launch swing

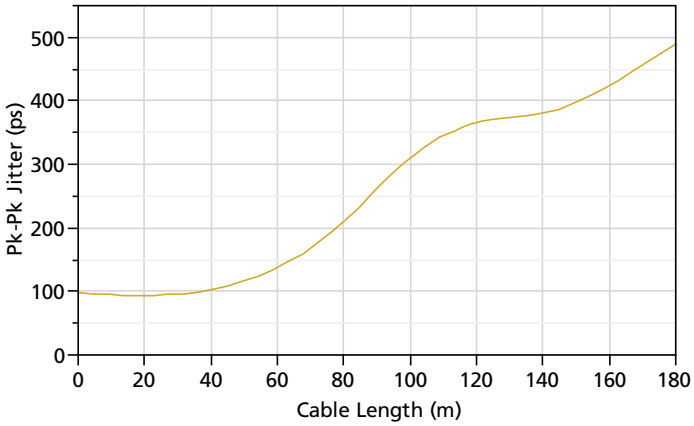


Figure 2-1: Jitter vs. Cable Length (270Mb/s)

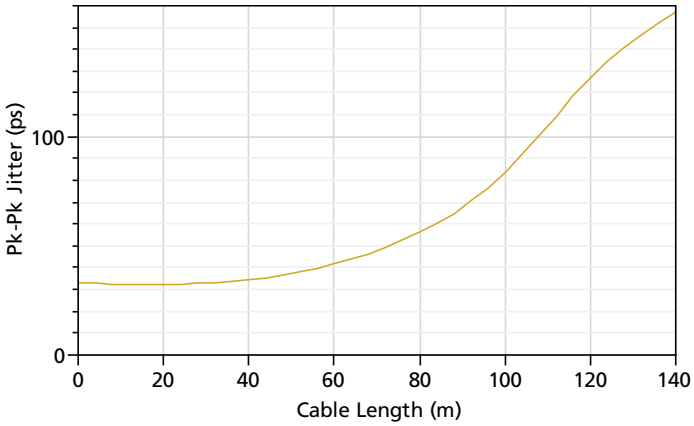


Figure 2-2: Jitter vs. Cable Length (1485Mb/s)

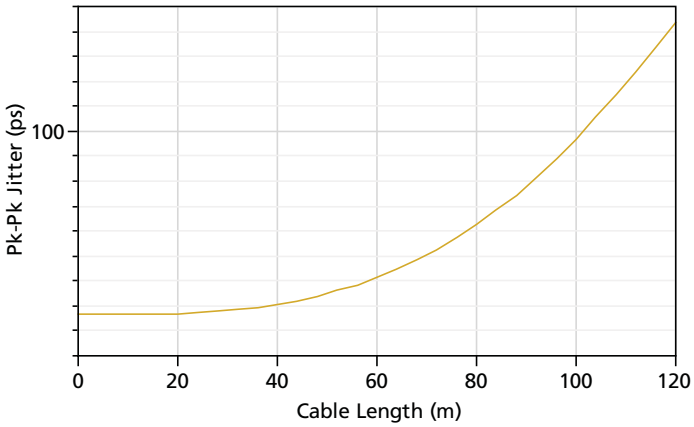


Figure 2-3: Jitter vs. Cable Length (2970Mb/s)

3. Input/Output Circuits

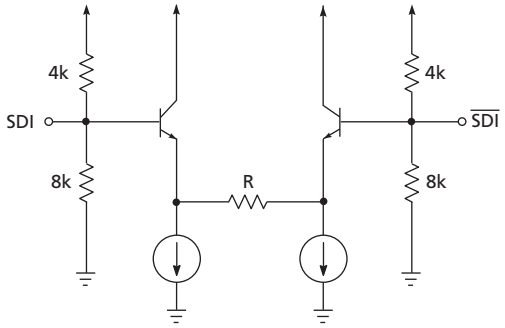


Figure 3-1: Input Equivalent Circuit

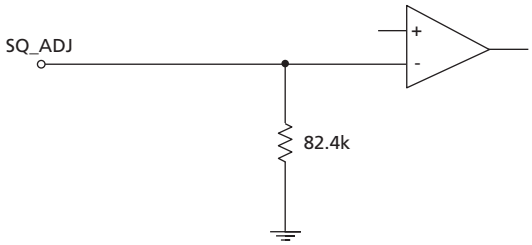


Figure 3-2: SQ_ADJ Equivalent Circuit

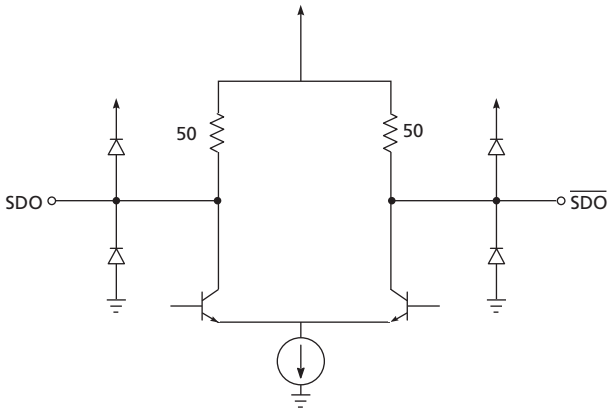


Figure 3-3: Output Circuit

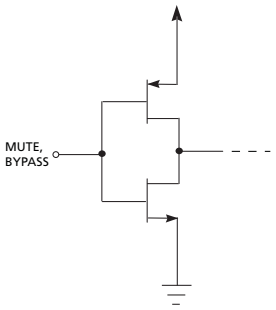


Figure 3-4: MUTE and BYPASS Circuits

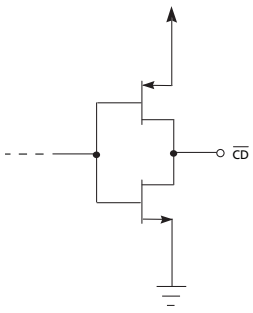


Figure 3-5: $\overline{CD}$ Circuit

4. Detailed Description

The GS2964 is a high-speed BiCMOS IC designed to equalize serial digital signals.

The GS2964 can equalize 3Gb/s, HD and SD serial digital signals, and will typically equalize 100m of Belden 1694A cable at 2.97Gb/s, 140m at 1.485Gb/s and 180m at 270Mb/s.The GS2964 is powered from a single +3.3V power supply and consumes approximately 215mW of power.

4.1 Serial Digital Inputs

The Serial Data Signal may be connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

4.2 Cable Equalization

The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse of the cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling.

4.3 Serial Digital Outputs

The digital output signals have a nominal voltage of 800mV$_{pp}$ differential, or 400mV$_{pp}$ single-ended when terminated with 50Ω as shown in Figure 4-1.

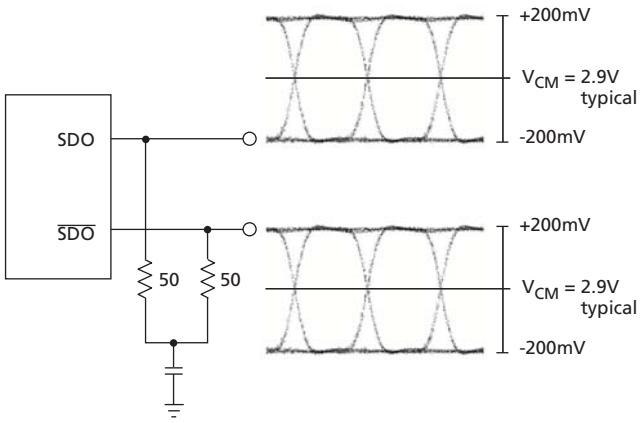


Figure 4-1: Typical Output Voltage Levels

4.4 Programmable Squelch Adjust (SQ_ADJ)

The GS2964 incorporates a programmable Squelch Adjust (SQ_ADJ) threshold.

This feature can be useful in applications where there are multiple input channels using the GS2964 and the maximum gain can be limited to avoid crosstalk.

The SQ_ADJ pin acts to change the threshold of the Carrier Detect ($\overline{CD}$) pin, through voltage level variances. When the input signal drops below a certain threshold, the $\overline{CD}$ pin will be driven high, indicating that there is not a valid input signal. In order to enable automatic muting of the output of the GS2964, the $\overline{CD}$ pin should be connected directly to the MUTE pin. In applications where programmable squelch adjust is not required, the SQ_ADJ pin may be left unconnected.

This feature has been designed for use in applications such as routers, where signal crosstalk and circuit noise cause the Equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem, since the signal to noise ratio on the circuit board could be significantly less than the default signal detection level set by the on chip reference.

4.5 Mute and Carrier Detect

The GS2964 includes a MUTE input pin that allows the application interface to mute the Serial Digital Output at any time. Set the MUTE pin HIGH to mute SDO and $\overline{SDO}$. In this case, the outputs will mute regardless of the setting of the BYPASS pin.

A Carrier Detect output pin ($\overline{CD}$) indicates the presence of a valid signal at the input of the GS2964. When $\overline{CD}$ is LOW, the device has detected a valid input on SDI and $\overline{SDI}$. When $\overline{CD}$ is HIGH, the device has not detected a valid input.

NOTE 1: $\overline{CD}$ will only detect loss of carrier for data rates greater than 19Mb/s. The $\overline{CD}$ output pin may be connected directly to the MUTE input pin to enable automatic muting of the GS2964 when no valid input signal has been detected.

NOTE 2: If the maximum cable length is exceeded (set by the SQ_ADJ pin) and the device is not in Bypass mode, the $\overline{CD}$ pin will not be driven low, even if a carrier is present.

Table 4-1: Mute Input Table

Mute	Function
0	SDO and $\overline{SDO}$ operate normally
1	SDO and $\overline{SDO}$ are forced to a steady state (either high or low)

Table 4-2: $\overline{CD}$ Output Table

$\overline{CD}$	Input Status
0	Valid Input on SDI, $\overline{SDI}$ pins
1	Input is not valid

4.6 Output Rise/Fall Times

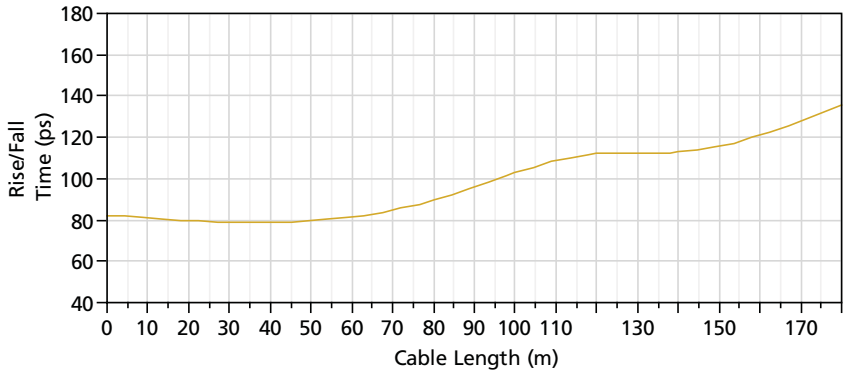


Figure 4-2: Typical Rise/Fall time for 270Mb/s data rate (VCC=3.3V, room temperature, 800mV launch swing)

The GS2964 was designed to limit bandwidth as cable length is increased. During 3G (2.97Gb/s) and HD (1.485Gb/s) operation, the impact of this is minimal on rise and fall time over the operating range. For SD (270Mb/s), the bandwidth limitation becomes more significant, particularly at longer cable lengths where a reduction in rise and fall time is observed. This means that for SD (270Mb/s) operation, rise and fall times slow as shown in Figure 4-2 above. This is beneficial because at 270Mb/s, one unit interval is equal to 3.7ns, therefore rise and fall times less than 100ps are not required, and slower rise and fall times actually help to reduce EMI.

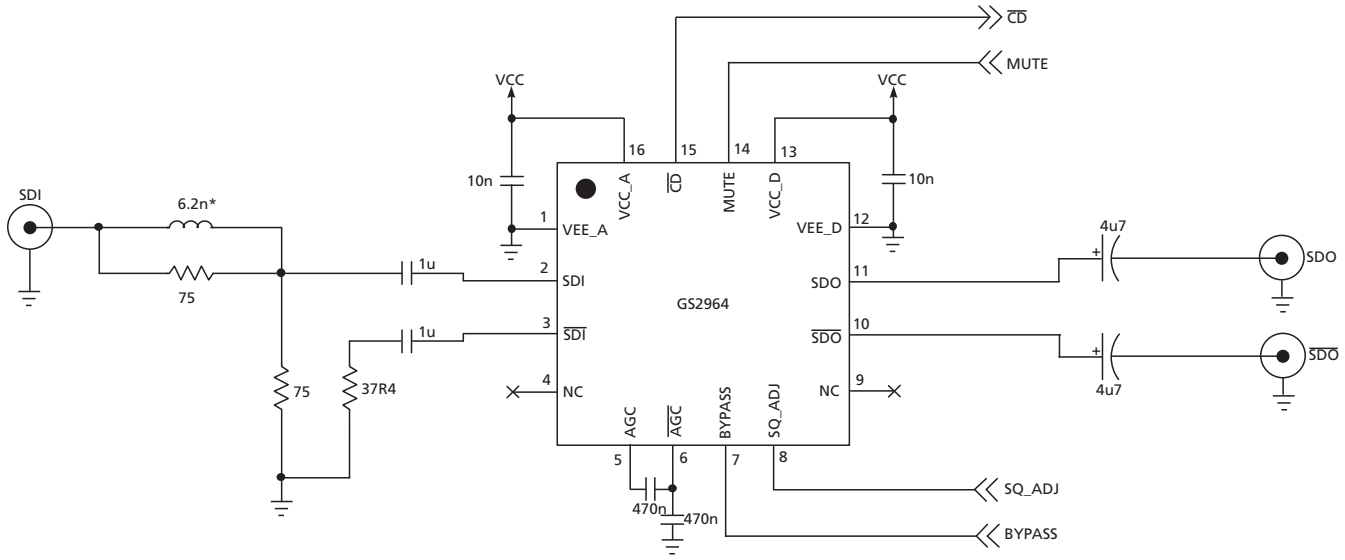
5. Application Information

5.1 PCB Layout

Special attention must be paid to component layout when designing Serial Digital Interfaces for HDTV. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for 3Gb/s rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- The PCB ground plane is removed under the GS2964 input components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GS2964 output components to minimize parasitic capacitance.
- High speed traces are curved to minimize impedance changes.

5.2 Typical Application Circuit

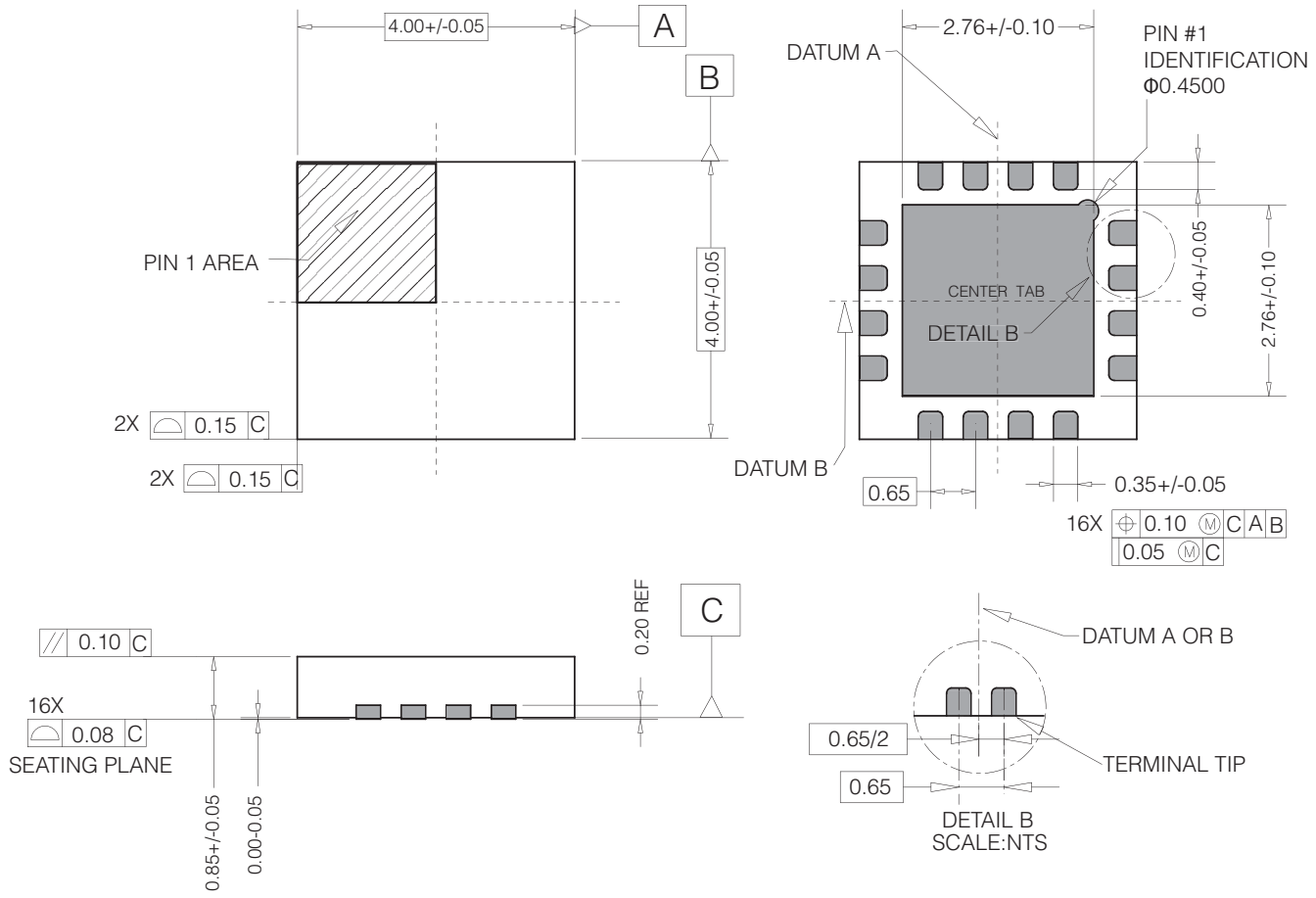


NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.
* Value dependent on layout

Figure 5-1: GS2964 Typical Application Circuit

6. Package & Ordering Information

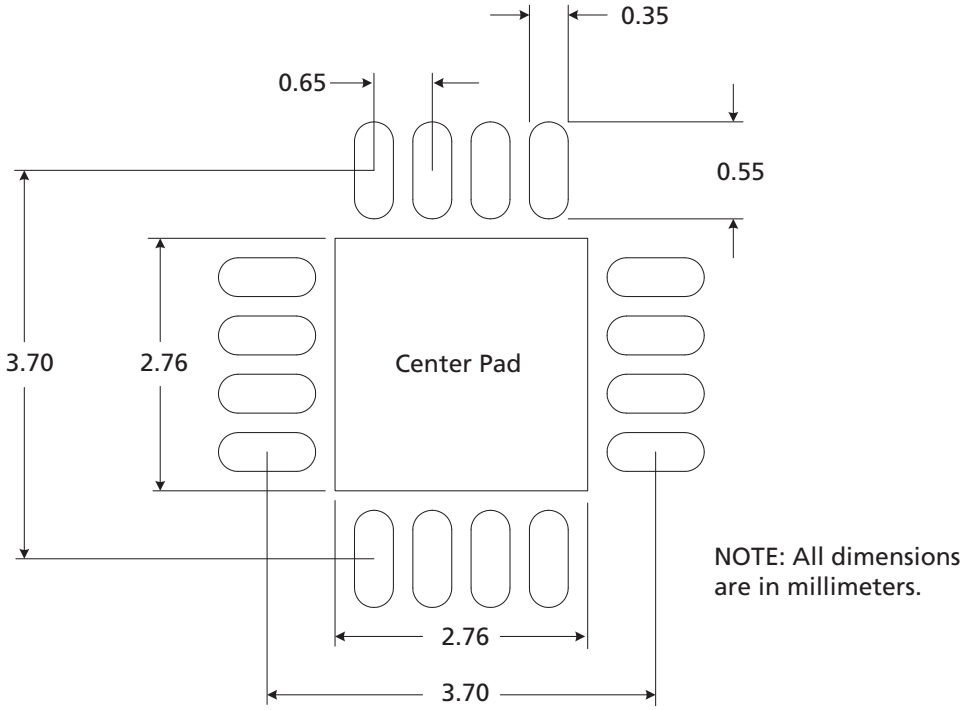
6.1 Package Dimensions



6.2 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, ψ	11.0°C/W
Pb-free and RoHS compliant	Yes

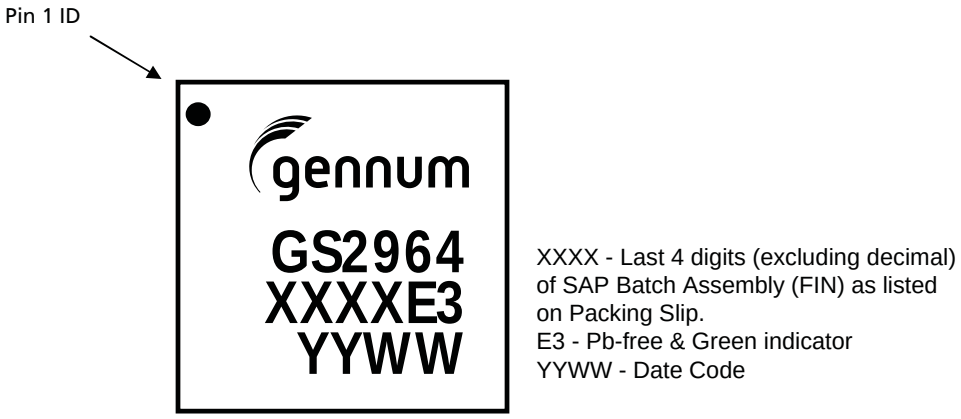
6.3 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane for analog circuitry in the device (VEE_A) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.4 Marking Diagram



6.5 Solder Reflow Profiles

The GS2964 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 6-1.

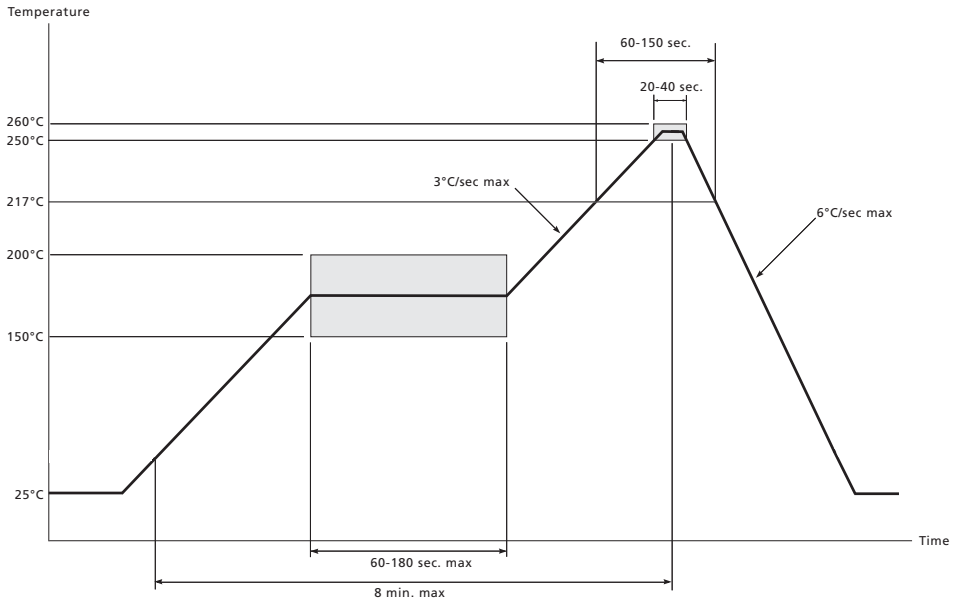


Figure 6-1: Maximum Pb-free Solder Reflow Profile

6.6 Ordering Information

	Part Number	Package	Temperature Range
GS2964	GS2964-INE3	16-pin QFN	-40°C to 85°C
GS2964	GS2964-INTE3	16-pin QFN Tape & Reel (250pcs)	-40°C to 85°C
GS2964	GS2964-INTE3Z	16-pin QFN Tape & Reel (2500pcs)	-40°C to 85°C

DOCUMENT IDENTIFICATION

DATA SHEET

The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

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