élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2021C
Monolithic Pin Driver

Features
- Wide range of programmable analog output levels
- 0.5 Ampere output drive with external transistors
- Programmable Slew Rate
- Low overshoot with large capacitive loads-stable with 500 pF
- 3-state output
- Power-down capability
- Wide supply range
- Overcurrent sense

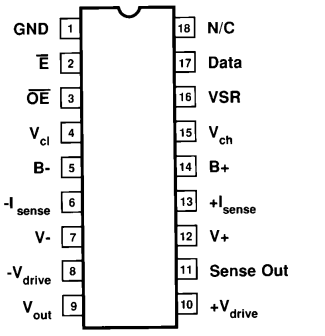
Applications
- Loaded circuit board testers
- Digital testers
- Programmable 4-quadrant power supplies

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2021CJ	0°C to +75°C	CerDIP	MDP0031

Connection Diagram

18-Pin DIP Package

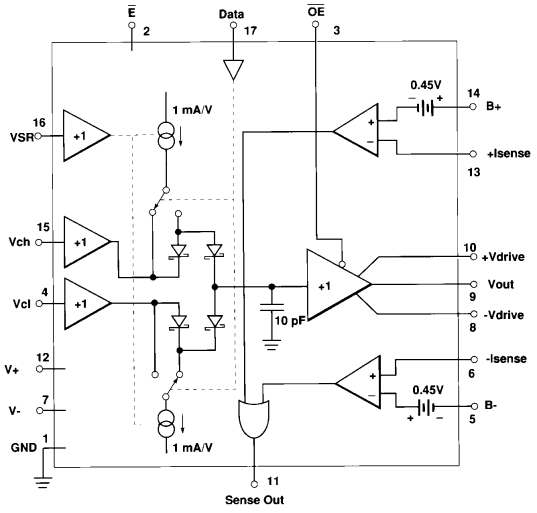


2021–1

Top View

General Description
The EL2021 is designed to drive programmed voltages into difficult loads. It has the required circuitry to be used as the pin driver electronics in board test systems. Capable of overpowering logic outputs, the part can accurately drive independently set high and low levels with programmed Slew Rates into reactive loads. It can also be placed into high impedance to monitor the load without having to disconnect. Previous board testers had multiplexing schemes to reduce the number of pin drivers required. With the small size and power consumption of the monolithic EL2021, a driver per node with little or no multiplexing becomes practical. Since only a few pins of "bed-of-nails" board testers need be active at any given time, the power-down feature saves substantial power in large systems.

Block Diagram



2021–2

Truth Table

$\overline{E}$	$\overline{OE}$	Data	V_{OUT}	Comments
0	0	0	V_{CL}	Active
0	0	1	V_{CH}	Active
0	1	X	High-Z	Third State
1	X	X	Undefined	Power-down

Absolute Maximum Ratings (T_A = 25°C)

V+	Supply Voltage	−0.3V to +16V	Sense Out	Output Current	−10 mA to +10 mA
V−	Supply Voltage	0.03V to −16V	V_{OUT}, Drive+, Drive−	Output Currents	−45 mA to +45 mA
B+, B−	Supply Voltages	V− to V+	T_J	Junction Temperature	150°C
Sense+	Input Voltages	(−2V + B+) to (0.3V + B+)	T_A	Operating Ambient Temperature Range	0°C to +75°C
Sense−	Input Voltages	(−0.3V + B−) to (2V + B−)	T_{ST}	Storage Temperature	−65°C to +150°C
$\overline{E}$, VSR, $\overline{OE}$, Data	Input Voltages	−0.3 to +6V	P_D	Power Dissipation (T_A = 25°C) (See Curves)	1.8W
V_{CH}, V_{CL}	Input Voltages	B− to B+ and V− to V+			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

T_A = 25°C, V+ = 15, V− = −10V, B+ = V_{CH} +3.6V, B− = V_{CL} −3.6V, No Load. Data and $\overline{OE}$ levels are: L = 2.0V and H = 3.0V (CMOS thresholds). $\overline{E}$ levels are: L = 1.5V and H = 3.5V. All tests done using 2N2222 and 2N2907 output transistors with Beta>40 @ I_C = 400 mA and Beta>27 @ I_C = 500 mA and V_{CE} = 3.1V. $\overline{OE}$ and $\overline{E}$ low.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
I_S	V+, -Supply Currents	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data = H or L	15	25	30	I	mA
		V_{CH} = 11V, V_{CL} = −6V, VSR = 5V, Data = H or L	21	33	45	IV	mA
		V_{CH} = −6V, V_{CL} = 11V, VSR+2.5V, Data = H or L	15	25	30	IV	mA
I_S, disabled	V+, -Supply Currents	V_{CH} = 5V, V_{CL} = 0V, VSR = 2.5V, Data = H or L, $\overline{E}$ = H	0	0.5	2.5	I	mA
I_{VCH}	V_{CH} Input Current	V_{CH} = −1V to +7.5V, V_{CL} = 0V, VSR = 5V, Data = H or L	−20	5	20	I	µA
I_{VCL}	V_{CL} Input Current	V_{CL} = −3.5V to +3.5V, V_{CH} = 0V, VSR = 5V, Data = H or L	−20	−5	20	I	µA
I_{Data}	Data Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = 0 or 5V	−50	5	50	I	µA
I_{OE}	$\overline{OE}$ Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = L, $\overline{OE}$ = 0V or 5V	−20	5	20	I	µA
I_E	$\overline{E}$ Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = L, $\overline{E}$ = 0V or 5V	−20	2	20	I	µA
I_{VSR}	VSR Input Current	V_{CH} = 5V, V_{CL} = 0V, Data = L, VSR = 0V or 5V	−20	2	20	I	µA
$\pm I_{sense}$	Sense Input Currents	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = 0V or 5V	−20	5	20	IV	µA
I_B+, I_B-	B+, B− Input Currents	V_{CH} = 5V, V_{CL} = 0V, Data = L, VSR = 5V	−20	5	20	IV	µA

TD is 1.1in

TD is 2.7in

DC Electrical Characteristics

T_A = 25°C, V+ = 15, V− = −10V, B+ = V_{CH} +3.6V, B− = V_{CL} −3.6V, No Load. Data and $\overline{OE}$ levels are: L = 2.0V and H = 3.0V (CMOS thresholds). $\overline{E}$ levels are: L = 1.5V and H = 3.5V. All tests done using 2N2222 and 2N2907 output transistors with Beta>40 @ I_C = 400 mA and Beta>27 @ I_C = 500 mA and V_{CE} = 3.1V. $\overline{OE}$ and $\overline{E}$ low. — Contd.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage	V+ = 14.5V, V− = −9.5V					
		V_{CH} = 5V, V_{CL} = 0, VSR = 1V, Data = L,					
		Output Current = −100 mA, 0 mA, or +100 mA	−50		50	I	mV
		Output Current = −400 mA or +400 mA	−300		300	I	mV
		Output Current = −500 mA or +500 mA	−600		600	I	mV
		V_{CH} = 5V, V_{CL} = 0, VSR = 1V, Data = H					
		Output Current = −100 mA, 0 mA, or +100 mA	4.95		5.05	I	V
		Output Current = −400 mA or +400 mA	4.7		5.3	I	V
		Output Current = −500 mA or +500 mA	4.4		5.6	I	V
		V_{CH} = 11V, V_{CL} = −6V, VSR = 1V, I_{OUT} = 0, Data = L	−6.1		−5.9	I	V
		V_{CH} = 11V, V_{CL} = −6V, VSR = 1V, I_{OUT} = 0, Data = H	10.9		11.1	I	V
I_{sense+}	+I_{sense} Threshold	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, R_{sense} = 1Ω, Data = H	400	450	600	I	mA
I_{sense-}	−I_{sense} Threshold	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, R_{sense} = 1Ω, Data = L	−400	−450	−600	I	mA
$V_{O, sense}$	Sense Out Levels	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data L or H,					
		Output Current = −350 mA or +350 mA	0		0.6	I	V
		Output Current = −550 mA or +550 mA	3.5		5.0	I	V
$I_{OUT,TRI}$	High-Impedance Output Leakage	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data = L, $\overline{OE}$ = H, Output Voltage = −2.5V or +7.5V	−100	5	100	I	μA

AC Electrical Characteristics

DC test conditions apply except where noted. For AC tests, R_L = 1k, C_L = 200 pF. Delay times are measured from $\overline{OE}$ or Data crossing 2.5V, V_{CH} = 5V, V_{CL} = 0.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
SR+	+Slew Rate	Data L to H, Output from 0.5V to 4.5V, VSR = 1V	80	100	120	I	V/μs
		VSR = 3V	150	240	360	I	V/μs
SR−	−Slew Rate	Data H to L, Output from 4.5V to 0.5V, VSR = 1V	−80	−100	−120	I	V/μs
		VSR = 3V	−150	−240	−360	I	V/μs
SRSYM	Slew Rate Symmetry	$\left[\frac{(SR+)-(SR-)}{(SR+)+(SR-)}\right]$ VSR = 1V	−10		10	I	%
		VSR = 2V	−20		20	IV	%
T_{pd}	Propagation Delay	Data L to H, Output to 0.2V, VSR = 2.5V	6.5	9	11.5	I	ns
		Data H to L, Output to 4.8V, VSR = 2.5V	6.5	9	11.5	I	ns
T_s	Settling Time	VSR = 5V, Data L to H, Output 4.5V to 5V ±0.2V			30	IV	ns
		VSR = 5V, Data H to L, Output 0.5V to ±0.2V			30	IV	ns
OS	Overshoot	VSR = 1V, Data L to H or H to L	−300		300	I	mV
		VSR = 1V, $\overline{OE}$ H to L, Data = L, R_L to 5V	−300		300	I	mV
		VSR = 1V, $\overline{OE}$ H to L, Data = H, R_L to 0V	−300		300	I	mV
T_{pda}	Propagation Delay, High-Z to Active	VSR = 2.5V, $\overline{OE}$ H to L, C_L = 50 pF					
		R_L to 5V, Data = L, Output to 3.5V			50	I	ns
		R_L to 0V, Data = H, Output to 1.5V			50	I	ns
T_{pdh}	Propagation Delay, Active to High-Z	VSR = 2.5V, $\overline{OE}$ L to H, C_L = 50 pF,					
		Data = L, R_L to 5V, Output to 0.5V			50	I	ns
		Data = H, R_L to 0V, Output to 4.5V			50	I	ns

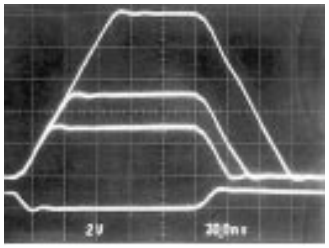
TD is 2.7in

TD is 3.2in

Pin Description Table

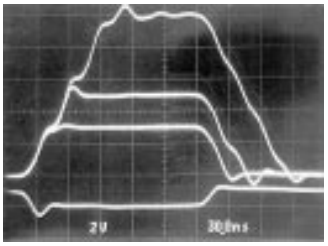
Pin #	Name	Description
1	GND	System ground.
2	$\overline{E}$	$\overline{\text{Enable}}$ control input. A logic low allows normal operation; a logic high puts the device into power down mode. No output levels are defined in powerdown nor does the output behave as a high impedance.
3	$\overline{OE}$	$\overline{\text{Output Enable}}$ input. A logic low sets the output to low-impedance driver mode; a logic high places the output into a high-impedance state.
4	V_{CL}	Lower analog control input. When Data = $\overline{OE}$ = $\overline{E}$ = L, the V_{CL} level is output as V_{OUT} (assuming $V_{CL} < V_{CH}$).
5	B−	System power supply. The EL2021 uses this pin as a negative output current monitor connection. Little current is drawn from this pin, transient or static.
6	$I_{sense}-$	Negative output current monitor input.
7	V−	Negative power supply. Because all negative output drive currents come from this pin (as much as 60 mA transiently), good bypassing is essential.
8	Drive−	Output to external pnp transistor base.
9	V_{OUT}	High-current input and output, depending on $\overline{OE}$.
10	Drive+	Output to external npn transistor base.
11	Sense Out	Logic output which signals that a high + or − output current is flowing.
12	V+	Positive power supply. Like V−, it should be well bypassed.
13	$I_{sense}+$	Positive output current monitor input.
14	B+	System power supply, similar to B−.
15	V_{CH}	Higher analog control input. When Data = H and $\overline{OE}$ = $\overline{E}$ = L, the V_{CH} level is output as V_{OUT} (assuming $V_{CH} > V_{CL}$).
16	VSR	Slew rate control input. A 1V level on this pin causes the output to slew at 100 V/μs, 0.5V causes a slew rate of 50 V/μs, etc.
17	Data	Output level control input. This pin digitally selects V_{CL} or V_{CH} as the output voltage when $\overline{OE}$ = $\overline{E}$ = L.
18	N/C	Not Connected.

Typical Performance Curves



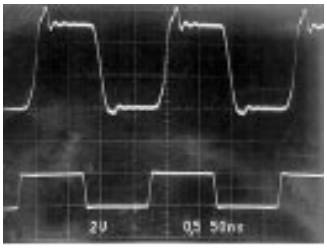
2021-3

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 50 pF, VSR = 1V.



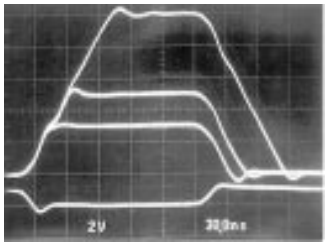
2021-4

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 200 pF, VSR = 1V.



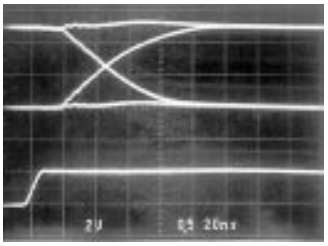
2021-5

Output waveshapes with 5 MHz data rate. C1 = 50 pF, VSR = 4V.



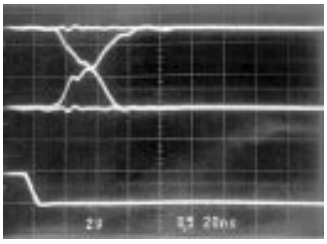
2021-6

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 200 pF, VSR = 1V, and overcompensated with 22 pF from each drive pin to ground.



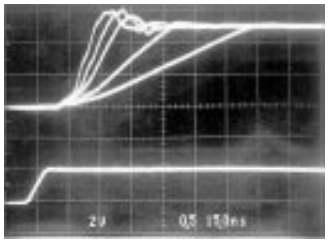
2021-7

Family of output waveshapes from active H, L to high-impedance H, L.



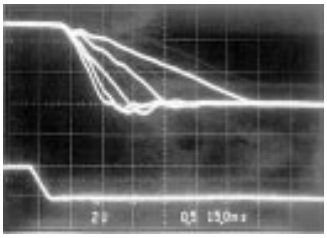
2021-8

Family of output waveshapes from high-impedance H, L to active H, L.



2021-9

Family of + output edges, 0V to 5V for VSR = 0.5V, 1V, 2V, 3V, 5V.

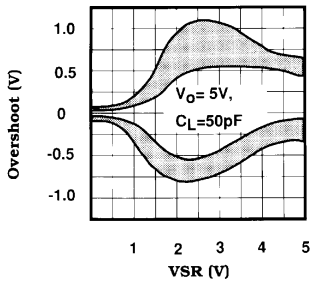


2021-10

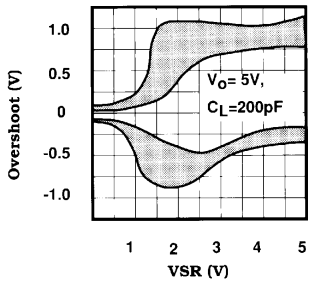
Family of—output edges, 5V to 0V or VSR = 0.5V, 1V, 2V, 3V, 5V.

Typical Performance Curves — Contd.

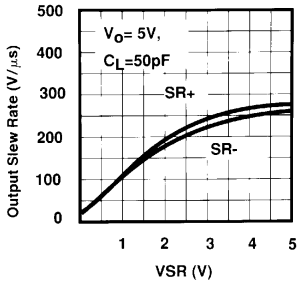
Overshoot vs VSR



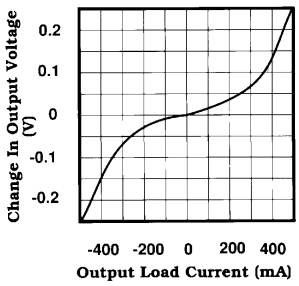
Overshoot vs VSR



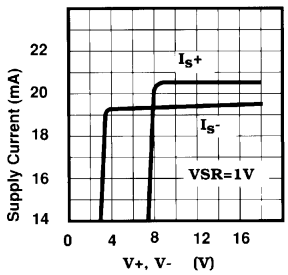
Slew Rate vs VSR



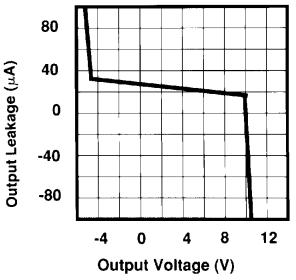
V_{OUT} vs Load Current



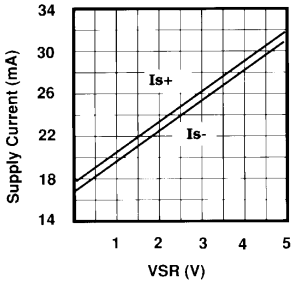
Supply Current vs Supply Voltage



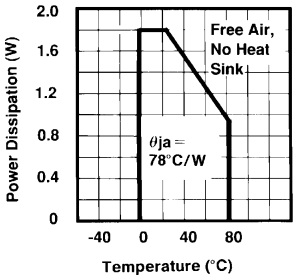
Tri-State Leakage vs Output Voltage



Supply Current vs VSR



Power Dissipation vs Temperature



2021-11

Applications Information

Output Stage

To meet the requirements of low output impedance, wide bandwidth, and large capacitive load driving capability, the EL2021 has a fairly exotic output stage. Figure 1 shows a simplified schematic of the circuit, only applicable in normal, low impedance mode. External transistors are used to handle the large load currents and peak power dissipations. Since there is no need for good AC crossover distortion performance in a pin driver, the output transistors are operated class C. That is, for small output currents, neither output transistor will conduct bias current, and when load currents do flow, one of the devices is off. This is accomplished by biasing the output transistors from Schottky diodes D1 and D2. In operation, the diode forward voltage is about 0.4V, whereas the "on" output transistor will have a V_{BE} of 0.6V. This leaves only 0.2V across the "off" transistor's base-emitter junction, not nearly enough to cause bias currents to flow in it. Schottky diodes have a temperature drift similar to silicon transistors, so the class C bias maintains over temperature. One caution is that the diodes are in the IC package and are thermally separate from the transistors, so there can exist temperature differences between packages that can cause thermal runaway. Runaway is avoided as long as the external transistors are not hotter than the EL2021 package by more than 80°C. The only way runaway has been induced as of this writing is to use "freeze spray" on the IC package while the output transistors are very hot.

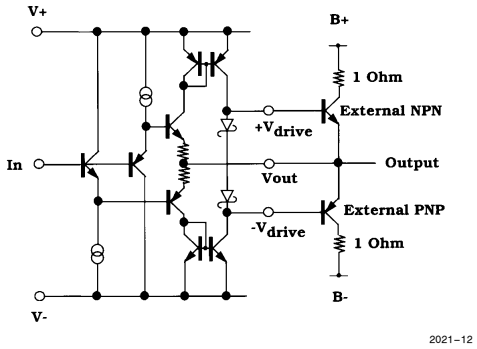


Figure 1. Simplified Output Stage (Normal Mode)

This circuit allows the external transistors to run from B+ and B− supplies that are of less voltage than V+ and V− to conserve power. Reducing B± supplies also reduces dissipations in the output devices themselves. B+ is typically made K volts more than V_{CH} and B− made K volts more negative than V_{CL}. Ideally K is made as small as possible to minimize output transistor dissipation, but two factors limit how small K can be. These factors are both related to the fact that transistors have two collector resistance numbers: "hard" and "soft" saturation resistance. As a transistor begins to saturate at high collector currents and small collector-emitter voltages, minority carriers begin to be generated from the base-collector junction. These carriers act as more collector dopant and actually reduce effective series collector resistance. At conditions of heavy saturation, the collector is flooded with minority carriers and exhibits minimum collector resistance. In this way, small geometry transistors like the 2N2222 and 2N2907 devices have excellent collector-emitter voltage drops at high currents, but are actually still in heavy saturation for 1V-2V drops. This "soft" saturation shows up as reduced beta at high currents and moderate V_{CE}'s as well as very poor AC performance. A transistor may exhibit an f_t of only 2 MHz in soft saturation when, like the 2N2222, it gives 300 MHz in non-saturated mode. The EL2021 requires the output transistors to have an f_t of at least 200 MHz to prevent degradation in overshoot, slew rate into heavy loads, and tolerance of heavy output capacitance. With a K of 3.2V and 1Ω collector resistors, almost all 2N2222 and 2N2907 devices perform well, but we have obtained devices from some vendors where the beta does indeed fall permaturely at reduced V_{CE} and high currents. It is important to characterize the external devices for the service that the EL2021 will be expected to provide.

The output stage of the EL2021 does not ring appreciably into a capacitive load in quiescent conditions, but it does ring while it slews. This is an unusual characteristic, but the output slews monotonically and the slew "ripple" does not cause problems in use. The slew ripple does cause a similar "ripple" in the overshoot-vs-VSR characteristic: the overshoot may decrease for slightly increasing VSR, then increase again for larger VSR's again. The overshoot-vs-VSR graphs

Applications Information — Contd.

presented in this data sheet thus reflect the range of overshoot rather than one particular device's wavy curve.

The typical 2N2222 and 2N2907 will deliver 750 mA into a short-circuit. This puts four watts of dissipation into the 2N2222 for V_{CH} = 5V. The npn can dissipate this power for a few tenths of a second as long as a metal-base TO-39 package is used. The small or non-metal-based packages have short thermal time constants and high thermal resistances, so they should withstand shorts for only a few milliseconds. The Sense Out signal should be used to control $\overline{OE}$ or reduce V_{CH} and V_{CL} to relieve the output devices from overcurrent conditions.

Transistors such as the MJE200 and MJE210 have very much improved collector resistances and high-current beta compared to the 2N2222 and 2N2907. Their f_t's are almost as good and sustain at higher currents, and high-current output accuracy will improve. They allow a K of 2V to reduce dissipations further, but short-circuit currents will be as much as two amperes! The geometries of these transistors are larger, and the added transistor capacitances will slow the maximum Slew Rates that the EL2021 can provide.

If transistors with f_t's less than 200 MHz are used, the EL2021 will need to be overcompensated. This is accomplished by connecting equal capacitors from the Drive pins to ground. These capacitors will range from 10 pF to 50 pF. The overcompensation will slow the maximum slew rate, but it will improve the overshoot and reactive load driving capability, and can be considered a useful technique.

Figure 2 shows the equivalent output stage schematic when the circuit is in high-impedance mode ($\overline{OE}$ = H). The external transistors have their base-emitter junctions each reverse-biased by a Schottky diode drop. A buffer amplifier copies the output voltage to give a bootstrapped bias for the Schottky stack. This scheme guarantees that the external transistors will be off for any output level, and the output leakage current is simply the bias current of the buffer.

The circuit works properly for AC signals up to 500 V/μs. Above this slew rate, the buffer cannot keep up and the external transistors may turn on transiently. Because of the bootstrap action, the output capacitance is less than 10 pF up to 10 MHz of small-signal bandwidth and 300 V/μs slew rate, increasing beyond these values. Adding overcompensation capacitors will degrade the slew rate that the output can withstand before current is drawn.

It is sometime necessary to provide a "snubber" network-a series R and C— to provide a local R.F. impedance for the buffer to look into. 330Ω and 56 pF should serve. Also, it is well to provide some DC path to ground (47k for instance) to bias the output stage when no actual circuit is connected to the EL2021 in high-impedance mode.

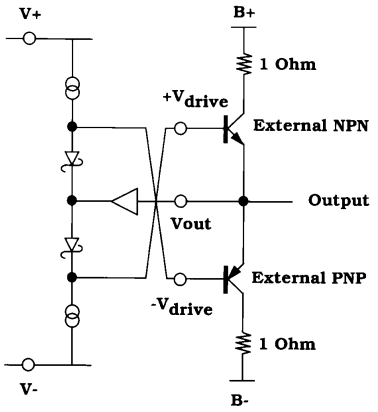


Figure 2. Simplified Output Stage (High-Impedance Mode)

Power Supplies

In typical operation, V+ and V— can be as much as ±15V and as little as V_{CH} +3V and V_{CL} —3V, respectively. When driving heavy output currents, however, it is wise to have 5V of headroom above V_{CH} and below V_{CL} to ensure no saturation of devices within the EL2021 and attendent waveshape distortions. Thus, for V_{CH} = 5V and V_{CL} = —2V, minimum operating voltages are +10, —7V. It is very important to bypass the supply terminals with low-inductance

Applications Information — Contd.

capacitors to ground, since the full base drive currents of the output transistors are derived from these supplies. Because the pulse currents can reach 60 mA, the capacitors should be at least a microfarad; 4.7 μF tantalum are ideal and require no small bypasses in parallel.

B+ and B− can be any voltage within V+ and V− and some amount previously discussed above V_{CH} and below V_{CL}. If V_{CH} or V_{CL} exceeds B+ or B−, very large internal fault currents can flow when the EL2021 attempts to bring an output transistor's base beyond the collector voltage. The bypassing care of the V± lines apply to the B± lines, as well as the fact that ampere currents can occur. Large (100 μF–500 μF) capacitors should be used to bypass perhaps every tenth EL2021.

The V_{CH}, V_{CL}, Data and $\overline{OE}$ lines should be driven locally so as to not pick up magnetic interference from the output. The inductance of interconnects to these lines can allow coupling to cause waveshape anomalies or even oscillations. If long lines are unavoidable, local 1k resistors or 50 pF–100 pF capacitors to ground can also serve the purpuse.

Data Pin

The slew rate of the input to the Data pin should be kept less than 1000 V/μs. Some feedthrough can occur for large Slew Rates which will distort the output waveshape. A 1k–2k resistor in series with the data pin will reduce feedthrough.

Current Sense

The output current is sensed by comparing the voltage dropped across the external shunt resistors to an internal 0.45V reference. The center of the trip level is adjusted for the particular output transistor betas listed in the data specifications. Transistors with less beta at high currents will cause the sense comparators to trip at slightly higher output currents. The 1Ω shunt resistors should be non-inductive. The family of wirewound resistors called "non-inductive" are too inductive for these shunts.

The response of the Sense Out can be thought of as slow attack and fast decay. A continuous overcurrent condition must last for at least 2 μs before Sense Out will go high, but will clear to low only about 200 ns after the overcurrent is withdrawn. This allows transient currents due to slewing capacitive load to not generate a flag. On the other hand, the output transistors will not be damaged with only a 2 μs system reaction time to a short-circuit.

Construction Practices

The major cautions in connecting to the EL2021 involve magnetic rather than capacitive parasitic concerns. The circuits can output as much as 100 A/μs. Even with normal Slew Rates and moderately large capacitive loads, the dI/dT can cause magnetic fields in harmless looking wires to fill adjacent lines with noise, and sometimes ringing or even sustained feedback. Thus, rules for wiring the EL2021 are:

(a) Keep leads short and large. Short wires are less inductive, as are wires with large surface area. The large surface area also reduces skin resistance at high frequencies, important at high currents (at 100 MHz, current penetrates only a few microns in metals).

(b) Use a ground plane. Due to inductance and skin effect, "ground" voltages will be different only inches apart on a copper ground plane. Individual wires do not create ground at high frequencies. The common "star" ground is a very bad idea for high-current and high-frequency circuits.

(c) Dress all wires against the ground plane. The magnetic fields that the wires would have generated will be intercepted by the ground plane and absorbed, thus reducing the wire's effective inductance. The capacitance added by this method is not important to EL2021 operation.

(d) The external transistors should have short interconnects to the EL2021, the collector shunt resistors, and the bypass capacitors. As previously stated, the shunt resistors must not be wire wound because of their inductance.

Applications Information — Contd.

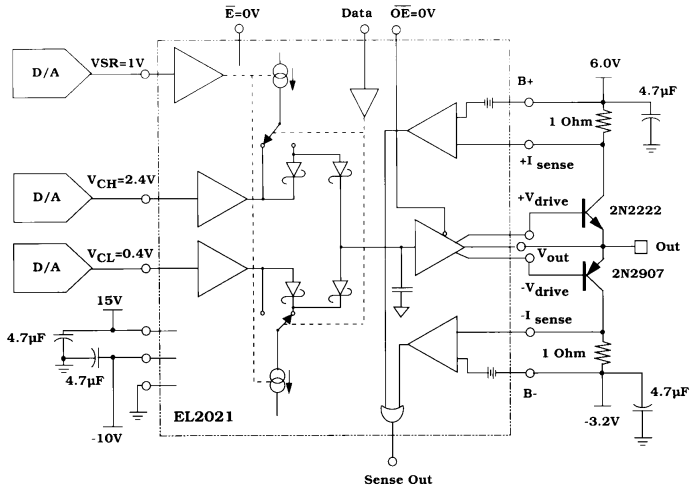
(e) The bypass capacitors should have low series resistance and inductance, but should not have a high Q. This may seem contradictory, but a 4.7 μF tantalum capacitor seems to work the best. An electrolytic capacitor should be added to help bolster the supply levels in the 0.1 μs–1 μs after a transition. No small capacitors are needed in parallel with the tantalums. The bypasses' ground returns are best connected to the area of ground inside the package outline to reduce the circulating current path length, if possible.

Using the EL2021 without External Transistors

By connecting both drive pins to the output pin, the EL2021 can be used as a stand-alone driver, not requiring the external transistors. The EL2021 is good for more than 50 mA in this mode. The output impedance rises to 12Ω, however, and the current sense and high-impedance mode are not available. The ripple seen in slew edges using the external transistors is largely absent from the standalone waveshapes; and overshoot is markedly improved at VSR > 1V, especially with large capacitive loads.

Typical Applications

100 V/μs High-Current Pin Driver Outputting TTL Levels



2021–14

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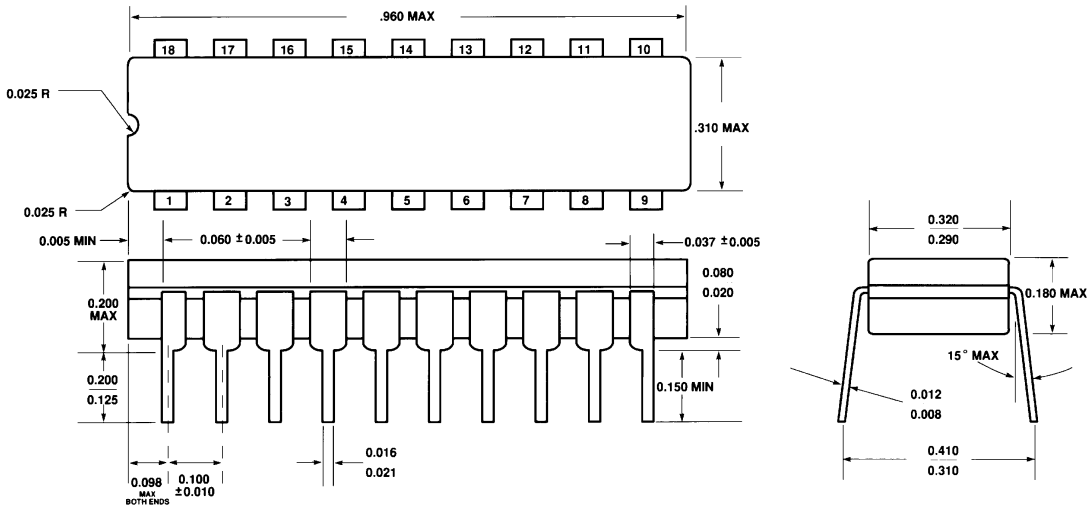
EL2021C
Monolithic Pin Driver

Package Outline



MDP0025 Rev. A
18-Lead CerDIP

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec, Inc.
1996 Tarob Court
Milpitas, CA 95035
Telephone: (408) 945-1323
(800) 333-6314
Fax: (408) 945-9305
European Office: 44-71-482-4596

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