



Integrated Device Technology, Inc.

## HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821AT/BT/CT  
IDT54/74FCT823AT/BT/CT/DT  
IDT54/74FCT825AT/BT/CT

### FEATURES:

#### • Common features:

- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility
  - $V_{OH} = 3.3\text{V}$  (typ.)
  - $V_{OL} = 0.3\text{V}$  (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPAC and LCC packages

#### • Features for FCT821T/FCT823T/FCT825T:

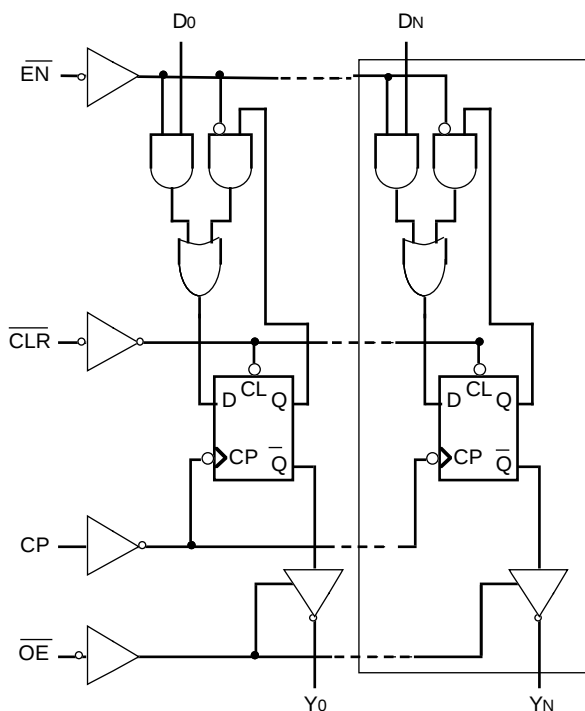
- A, B, C and D speed grades
- High drive outputs (-15mA  $I_{OH}$ , 48mA  $I_{OL}$ )
- Power off disable outputs permit "live insertion"

### DESCRIPTION:

The FCT82xT series is built using an advanced dual metal CMOS technology. The FCT82xT series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT821T are buffered, 10-bit wide versions of the popular FCT374T function. The FCT823T are 9-bit wide buffered registers with Clock Enable ( $\overline{EN}$ ) and Clear ( $\overline{CLR}$ ) – ideal for parity bus interfacing in high-performance microprogrammed systems. The FCT825T are 8-bit buffered registers with all the FCT823T controls plus multiple enables ( $\overline{OE1}$ ,  $\overline{OE2}$ ,  $\overline{OE3}$ ) to allow multi-user control of the interface, e.g.,  $\overline{CS}$ , DMA and  $\text{RD}/\overline{\text{WR}}$ . They are ideal for use as an output port requiring high  $I_{OL}/I_{OH}$ .

The FCT82xT high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

### FUNCTIONAL BLOCK DIAGRAM



2567 drw 01

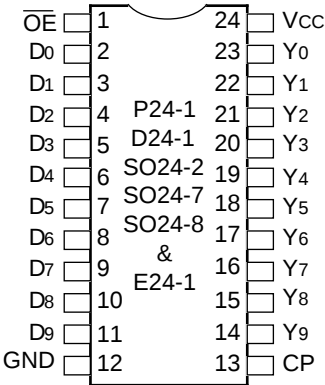
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

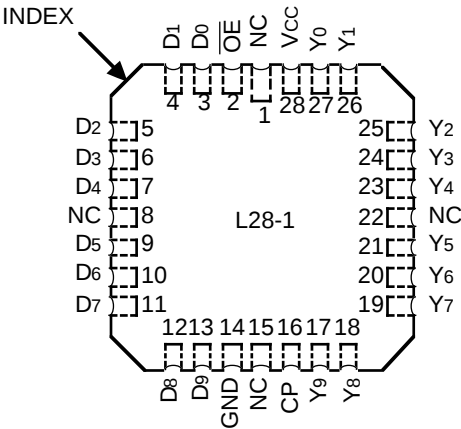
AUGUST 1995

PIN CONFIGURATIONS

FCT821 10-BIT REGISTER



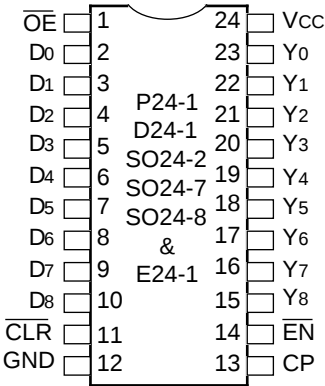
DIP/SOIC/SSOP/QSOP/CERPACK  
TOP VIEW



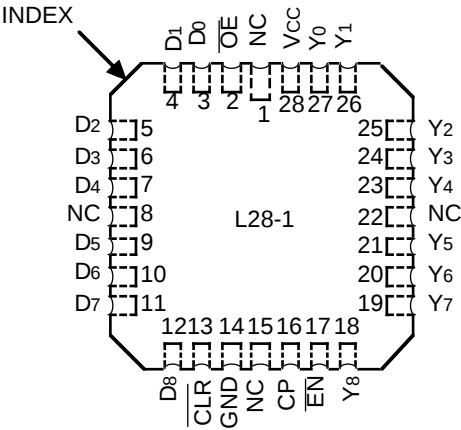
LCC  
TOP VIEW

2567 drw 02

FCT823 9-BIT REGISTER



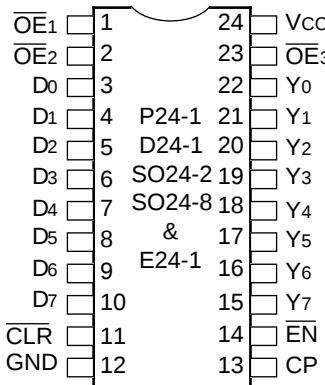
DIP/SOIC/SSOP/QSOP/CERPACK  
TOP VIEW



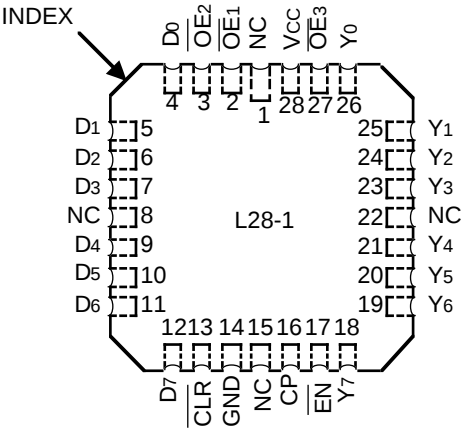
LCC  
TOP VIEW

2567 drw 03

FCT825 8-BIT REGISTER



DIP/SOIC/QSOP/CERPACK  
TOP VIEW



LCC  
TOP VIEW

2567 drw 04

## PIN DESCRIPTION

| Names                   | I/O | Description                                                                                                                                                                                                                                                                                     |
|-------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D <sub>I</sub>          | I   | The D flip-flop data inputs.                                                                                                                                                                                                                                                                    |
| $\overline{\text{CLR}}$ | I   | When the clear input is LOW and $\overline{\text{OE}}$ is LOW, the Q <sub>I</sub> outputs are LOW. When the clear input is HIGH, data can be entered into the register.                                                                                                                         |
| CP                      | I   | Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.                                                                                                                                                                                                      |
| Y <sub>I</sub>          | O   | The register 3-state outputs.                                                                                                                                                                                                                                                                   |
| $\overline{\text{EN}}$  | I   | Clock Enable. When the clock enable is LOW, data on the D <sub>I</sub> input is transferred to the Q <sub>I</sub> output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q <sub>I</sub> outputs do not change state, regardless of the data or clock input transitions. |
| $\overline{\text{OE}}$  | I   | Output Control. When the $\overline{\text{OE}}$ input is HIGH, the Y <sub>I</sub> outputs are in the high-impedance state. When the $\overline{\text{OE}}$ input is LOW, the TRUE register data is present at the Y <sub>I</sub> outputs.                                                       |

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## FUNCTION TABLE<sup>(1)</sup>

| Inputs                 |                         |                        |                |    | Internal/Outputs |                | Function |
|------------------------|-------------------------|------------------------|----------------|----|------------------|----------------|----------|
| $\overline{\text{OE}}$ | $\overline{\text{CLR}}$ | $\overline{\text{EN}}$ | D <sub>I</sub> | CP | Q <sub>I</sub>   | Y <sub>I</sub> |          |
| H                      | H                       | L                      | L              | ↑  | L                | Z              | High Z   |
| H                      | H                       | L                      | H              | ↑  | H                | Z              |          |
| H                      | L                       | X                      | X              | X  | L                | Z              | Clear    |
| L                      | L                       | X                      | X              | X  | L                | L              |          |
| H                      | H                       | H                      | X              | X  | NC               | Z              | Hold     |
| L                      | H                       | H                      | X              | X  | NC               | NC             |          |
| H                      | H                       | L                      | L              | ↑  | L                | Z              | Load     |
| H                      | H                       | L                      | H              | ↑  | H                | Z              |          |
| L                      | H                       | L                      | L              | ↑  | L                | L              |          |
| L                      | H                       | L                      | H              | ↑  | H                | H              |          |

### NOTE:

- H = HIGH  
L = LOW  
X = Don't Care  
NC = No Change  
↑ = LOW-to-HIGH Transition  
Z = High Impedance

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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol                           | Rating                               | Commercial                   | Military                     | Unit |
|----------------------------------|--------------------------------------|------------------------------|------------------------------|------|
| V <sub>TERM</sub> <sup>(2)</sup> | Terminal Voltage with Respect to GND | −0.5 to +7.0                 | −0.5 to +7.0                 | V    |
| V <sub>TERM</sub> <sup>(3)</sup> | Terminal Voltage with Respect to GND | −0.5 to V <sub>CC</sub> +0.5 | −0.5 to V <sub>CC</sub> +0.5 | V    |
| T <sub>A</sub>                   | Operating Temperature                | 0 to +70                     | −55 to +125                  | °C   |
| T <sub>BIAS</sub>                | Temperature Under Bias               | −55 to +125                  | −65 to +135                  | °C   |
| T <sub>STG</sub>                 | Storage Temperature                  | −55 to +125                  | −65 to +150                  | °C   |
| P <sub>T</sub>                   | Power Dissipation                    | 0.5                          | 0.5                          | W    |
| I <sub>OUT</sub>                 | DC Output Current                    | −60 to +120                  | −60 to +120                  | mA   |

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Input and V<sub>CC</sub> terminals only.
- Outputs and I/O terminals only.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

| Symbol           | Parameter <sup>(1)</sup> | Conditions            | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 6    | 10   | pF   |
| C <sub>OUT</sub> | Output Capacitance       | V <sub>OUT</sub> = 0V | 8    | 12   | pF   |

### NOTE:

- This parameter is measured at characterization but not tested.

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## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ; Military:  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol    | Parameter                                                             | Test Conditions <sup>(1)</sup>                             |                     | Min. | Typ. <sup>(2)</sup> | Max.    | Unit          |
|-----------|-----------------------------------------------------------------------|------------------------------------------------------------|---------------------|------|---------------------|---------|---------------|
| $V_{IH}$  | Input HIGH Level                                                      | Guaranteed Logic HIGH Level                                |                     | 2.0  | —                   | —       | V             |
| $V_{IL}$  | Input LOW Level                                                       | Guaranteed Logic LOW Level                                 |                     | —    | —                   | 0.8     | V             |
| $I_{IH}$  | Input HIGH Current <sup>(4)</sup>                                     | $V_{CC} = \text{Max.}$                                     | $V_I = 2.7\text{V}$ | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{IL}$  | Input LOW Current <sup>(4)</sup>                                      |                                                            | $V_I = 0.5\text{V}$ | —    | —                   | $\pm 1$ |               |
| $I_{OZH}$ | High Impedance Output Current<br>(3-State Output pins) <sup>(4)</sup> | $V_{CC} = \text{Max.}$                                     | $V_O = 2.7\text{V}$ | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{OZL}$ |                                                                       |                                                            | $V_O = 0.5\text{V}$ | —    | —                   | $\pm 1$ |               |
| $I_I$     | Input HIGH Current <sup>(4)</sup>                                     | $V_{CC} = \text{Max.}$ , $V_I = V_{CC} (\text{Max.})$      |                     | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $V_{IK}$  | Clamp Diode Voltage                                                   | $V_{CC} = \text{Min.}$ , $I_{IN} = -18\text{mA}$           |                     | —    | -0.7                | -1.2    | V             |
| $V_H$     | Input Hysteresis                                                      | —                                                          |                     | —    | 200                 | —       | mV            |
| $I_{CC}$  | Quiescent Power Supply Current                                        | $V_{CC} = \text{Max.}$ , $V_{IN} = \text{GND}$ or $V_{CC}$ |                     | —    | 0.01                | 1       | mA            |

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## OUTPUT DRIVE CHARACTERISTICS FOR FCT821/823/825T

| Symbol    | Parameter                                     | Test Conditions <sup>(1)</sup>                             |                                                                | Min. | Typ. <sup>(2)</sup> | Max.    | Unit          |
|-----------|-----------------------------------------------|------------------------------------------------------------|----------------------------------------------------------------|------|---------------------|---------|---------------|
| $V_{OH}$  | Output HIGH Voltage                           | $V_{CC} = \text{Min.}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$    | $I_{OH} = -6\text{mA MIL.}$                                    | 2.4  | 3.3                 | —       | V             |
|           |                                               |                                                            | $I_{OH} = -8\text{mA COM'L.}$                                  |      |                     |         |               |
|           |                                               |                                                            | $I_{OH} = -12\text{mA MIL.}$<br>$I_{OH} = -15\text{mA COM'L.}$ | 2.0  | 3.0                 | —       | V             |
| $V_{OL}$  | Output LOW Voltage                            | $V_{CC} = \text{Min.}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$    | $I_{OL} = 32\text{mA MIL.}$<br>$I_{OL} = 48\text{mA COM'L.}$   | —    | 0.3                 | 0.5     | V             |
| $I_{OS}$  | Short Circuit Current                         | $V_{CC} = \text{Max.}$ , $V_O = \text{GND}$ <sup>(3)</sup> |                                                                | -60  | -120                | -225    | mA            |
| $I_{OFF}$ | Input/Output Power Off Leakage <sup>(5)</sup> | $V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 4.5\text{V}$  |                                                                | —    | —                   | $\pm 1$ | $\mu\text{A}$ |

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### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^\circ\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .
- This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

| Symbol          | Parameter                                         | Test Conditions <sup>(1)</sup>                                                                                                                                                                           |                                            | Min. | Typ. <sup>(2)</sup> | Max.                | Unit       |
|-----------------|---------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|------|---------------------|---------------------|------------|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC} = \text{Max.}$<br>$V_{IN} = 3.4V^{(3)}$                                                                                                                                                          |                                            | —    | 0.5                 | 2.0                 | mA         |
| $I_{CCD}$       | Dynamic Power Supply Current <sup>(4)</sup>       | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$\overline{OE} = \overline{EN} = \text{GND}$<br>One Input Toggling<br>50% Duty Cycle                                                                           | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 0.15                | 0.25                | mA/<br>MHz |
| $I_C$           | Total Power Supply Current <sup>(6)</sup>         | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$<br>50% Duty Cycle<br>$\overline{OE} = \overline{EN} = \text{GND}$<br>One Bit Toggling<br>at $f_i = 5\text{MHz}$<br>50% Duty Cycle      | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 1.5                 | 3.5                 | mA         |
|                 |                                                   | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$<br>50% Duty Cycle<br>$\overline{OE} = \overline{EN} = \text{GND}$<br>One Bit Toggling<br>at $f_i = 5\text{MHz}$<br>50% Duty Cycle      | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —    | 2.0                 | 5.5                 |            |
|                 |                                                   | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$<br>50% Duty Cycle<br>$\overline{OE} = \overline{EN} = \text{GND}$<br>Eight Bits Toggling<br>at $f_i = 2.5\text{MHz}$<br>50% Duty Cycle | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 3.8                 | 7.3 <sup>(5)</sup>  |            |
|                 |                                                   | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$<br>50% Duty Cycle<br>$\overline{OE} = \overline{EN} = \text{GND}$<br>Eight Bits Toggling<br>at $f_i = 2.5\text{MHz}$<br>50% Duty Cycle | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —    | 6.0                 | 16.3 <sup>(5)</sup> |            |

### NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$   
 All currents are in milliamperes and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol       | Parameter                                                          | Condition <sup>(1)</sup>               | FCT821/823/825AT    |      |                     |      | FCT821/823/825BT    |      |                     |      | Unit |
|--------------|--------------------------------------------------------------------|----------------------------------------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|------|
|              |                                                                    |                                        | Com'l.              |      | Mil.                |      | Com'l.              |      | Mil.                |      |      |
|              |                                                                    |                                        | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. |      |
| tPLH<br>tPHL | Propagation Delay<br>CP to Y <sub>I</sub> ( $\overline{OE}$ = LOW) | CL = 50pF<br>RL = 500Ω                 | 1.5                 | 10.0 | 1.5                 | 11.5 | 1.5                 | 7.5  | 1.5                 | 8.5  | ns   |
|              |                                                                    | CL = 300pF <sup>(4)</sup><br>RL = 500Ω | 1.5                 | 20.0 | 1.5                 | 20.0 | 1.5                 | 15.0 | 1.5                 | 16.0 |      |
| tSU          | Set-up Time HIGH or LOW<br>DI to CP                                | CL = 50pF<br>RL = 500Ω                 | 4.0                 | —    | 4.0                 | —    | 3.0                 | —    | 3.0                 | —    | ns   |
| tH           | Hold Time HIGH or LOW<br>DI to CP                                  |                                        | 2.0                 | —    | 2.0                 | —    | 1.5                 | —    | 1.5                 | —    | ns   |
| tSU          | Set-up Time HIGH or LOW<br>$\overline{EN}$ to CP                   |                                        | 4.0                 | —    | 4.0                 | —    | 3.0                 | —    | 3.0                 | —    | ns   |
| tH           | Hold Time HIGH or LOW<br>$\overline{EN}$ to CP                     |                                        | 2.0                 | —    | 2.0                 | —    | 0                   | —    | 0                   | —    | ns   |
| tPHL         | Propagation Delay, $\overline{CLR}$ to Y <sub>I</sub>              |                                        | 1.5                 | 14.0 | 1.5                 | 15.0 | 1.5                 | 9.0  | 1.5                 | 9.5  | ns   |
| tREM         | Recovery Time $\overline{CLR}$ to CP                               |                                        | 6.0                 | —    | 7.0                 | —    | 6.0                 | —    | 6.0                 | —    | ns   |
| tw           | Clock Pulse Width<br>HIGH or LOW                                   |                                        | 7.0                 | —    | 7.0                 | —    | 6.0                 | —    | 6.0                 | —    | ns   |
| tw           | $\overline{CLR}$ Pulse Width LOW                                   |                                        | 6.0                 | —    | 7.0                 | —    | 6.0                 | —    | 6.0                 | —    | ns   |
| tPZH<br>tPZL | Output Enable Time $\overline{OE}$ to Y <sub>I</sub>               | CL = 50pF<br>RL = 500Ω                 | 1.5                 | 12.0 | 1.5                 | 13.0 | 1.5                 | 8.0  | 1.5                 | 9.0  | ns   |
|              |                                                                    | CL = 300pF <sup>(4)</sup><br>RL = 500Ω | 1.5                 | 23.0 | 1.5                 | 25.0 | 1.5                 | 15.0 | 1.5                 | 16.0 |      |
| tPHZ<br>tPLZ | Output Disable Time $\overline{OE}$ to Y <sub>I</sub>              | CL = 5pF <sup>(4)</sup><br>RL = 500Ω   | 1.5                 | 7.0  | 1.5                 | 8.0  | 1.5                 | 6.5  | 1.5                 | 7.0  | ns   |
|              |                                                                    | CL = 50pF<br>RL = 500Ω                 | 1.5                 | 8.0  | 1.5                 | 9.0  | 1.5                 | 7.5  | 1.5                 | 8.0  |      |

### NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not tested.
- This condition is guaranteed but not tested.

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# SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol       | Parameter                                                          | Condition <sup>(1)</sup>               | FCT821/823/825CT    |      |                     |      | FCT823DT            |      | Unit |
|--------------|--------------------------------------------------------------------|----------------------------------------|---------------------|------|---------------------|------|---------------------|------|------|
|              |                                                                    |                                        | Com'l.              |      | Mil.                |      | Com'l.              |      |      |
|              |                                                                    |                                        | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. |      |
| tPLH<br>tPHL | Propagation Delay<br>CP to Y <sub>I</sub> ( $\overline{OE}$ = LOW) | CL = 50pF<br>RL = 500Ω                 | 1.5                 | 6.0  | 1.5                 | 7.0  | 1.5                 | 5.0  | ns   |
|              |                                                                    | CL = 300pF <sup>(4)</sup><br>RL = 500Ω | 1.5                 | 12.5 | 1.5                 | 13.5 | 1.5                 | 8.5  |      |
| tSU          | Set-up Time HIGH or LOW<br>DI to CP                                | CL = 50pF<br>RL = 500Ω                 | 3.0                 | —    | 3.0                 | —    | 2.0                 | —    | ns   |
| tH           | Hold Time HIGH or LOW<br>DI to CP                                  |                                        | 1.5                 | —    | 1.5                 | —    | 1.0                 | —    | ns   |
| tSU          | Set-up Time HIGH or LOW<br>$\overline{EN}$ to CP                   |                                        | 3.0                 | —    | 3.0                 | —    | 3.0                 | —    | ns   |
| tH           | Hold Time HIGH or LOW<br>$\overline{EN}$ to CP                     |                                        | 0                   | —    | 0                   | —    | 0                   | —    | ns   |
| tPHL         | Propagation Delay, $\overline{CLR}$ to Y <sub>I</sub>              |                                        | 1.5                 | 8.0  | 1.5                 | 8.5  | 1.5                 | 5.0  | ns   |
| tREM         | Recovery Time $\overline{CLR}$ to CP                               |                                        | 6.0                 | —    | 6.0                 | —    | 3.0                 | —    | ns   |
| tw           | Clock Pulse Width<br>HIGH or LOW <sup>(3)</sup>                    |                                        | 6.0                 | —    | 6.0                 | —    | 3.0                 | —    | ns   |
| tw           | $\overline{CLR}$ Pulse Width LOW <sup>(3)</sup>                    |                                        | 6.0                 | —    | 6.0                 | —    | 3.0                 | —    | ns   |
| tpZH<br>tpZL | Output Enable Time $\overline{OE}$ to Y <sub>I</sub>               | CL = 50pF<br>RL = 500Ω                 | 1.5                 | 7.0  | 1.5                 | 8.0  | 1.5                 | 4.8  | ns   |
|              |                                                                    | CL = 300pF <sup>(4)</sup><br>RL = 500Ω | 1.5                 | 12.5 | 1.5                 | 13.5 | 1.5                 | 9.0  |      |
| tpHZ<br>tPLZ | Output Disable Time $\overline{OE}$ to Y <sub>I</sub>              | CL = 5pF <sup>(4)</sup><br>RL = 500Ω   | 1.5                 | 6.0  | 1.5                 | 6.0  | 1.5                 | 4.0  | ns   |
|              |                                                                    | CL = 50pF<br>RL = 500Ω                 | 1.5                 | 6.5  | 1.5                 | 6.5  | 1.5                 | 4.0  |      |

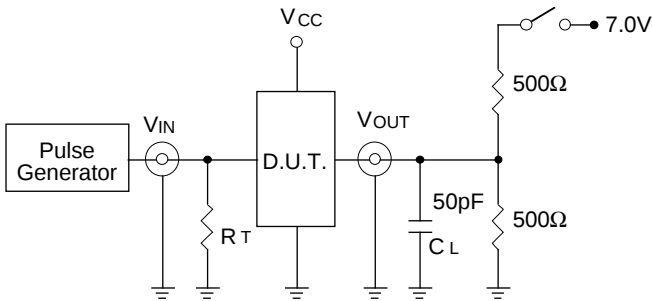
## NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not tested.
- This condition is guaranteed but not tested.

2567 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



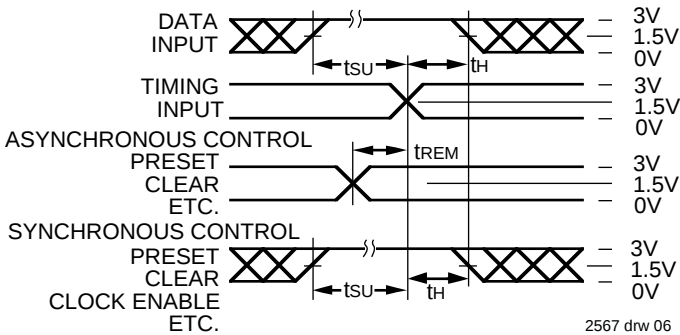
2567 drw 05

SWITCH POSITION

| Test                                    | Switch |
|-----------------------------------------|--------|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests                         | Open   |

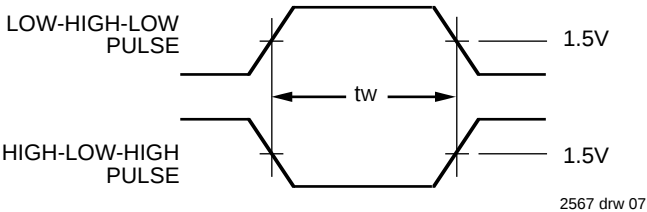
**DEFINITIONS:** 2567 Ink 10  
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



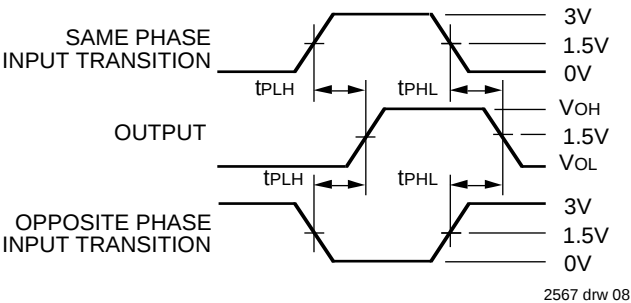
2567 drw 06

PULSE WIDTH



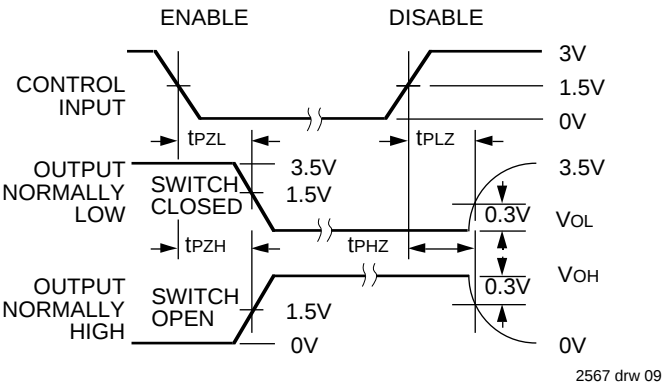
2567 drw 07

PROPAGATION DELAY



2567 drw 08

ENABLE AND DISABLE TIMES



2567 drw 09

- NOTES:**
- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
  - Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

ORDERING INFORMATION

| IDT | XX<br>Temp. Range | XXXX<br>Device Type | X<br>Package | X<br>Process |       |                                    |
|-----|-------------------|---------------------|--------------|--------------|-------|------------------------------------|
|     |                   |                     |              |              | Blank | Commercial                         |
|     |                   |                     |              |              | B     | MIL-STD-883, Class B               |
|     |                   |                     |              |              | P     | Plastic DIP                        |
|     |                   |                     |              |              | D     | CERDIP                             |
|     |                   |                     |              |              | E     | CERPACK                            |
|     |                   |                     |              |              | L     | Leadless Chip Carrier              |
|     |                   |                     |              |              | SO    | Small Outline IC                   |
|     |                   |                     |              |              | PY    | Shrink Small Outline Package       |
|     |                   |                     |              |              | Q     | Quarter-size Small Outline Package |
|     |                   |                     |              |              | 821AT | 10-Bit Non-Inverting Register      |
|     |                   |                     |              |              | 823AT | 9-Bit Non-Inverting Register       |
|     |                   |                     |              |              | 825AT | 8-Bit Non-Inverting Register       |
|     |                   |                     |              |              | 821BT |                                    |
|     |                   |                     |              |              | 823BT |                                    |
|     |                   |                     |              |              | 825BT |                                    |
|     |                   |                     |              |              | 821CT |                                    |
|     |                   |                     |              |              | 823CT |                                    |
|     |                   |                     |              |              | 825CT |                                    |
|     |                   |                     |              |              | 823DT |                                    |
|     |                   |                     |              |              | 54    | −55°C to +125°C                    |
|     |                   |                     |              |              | 74    | 0°C to +70°C                       |

2567 drw 10