

# Complementary Darlington Power Transistors

## DPAK For Surface Mount Applications

### MJD112 (NPN), MJD117 (PNP)

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

#### Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Electrically Similar to Popular TIP31 and TIP32 Series
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant\*

SILICON  
POWER TRANSISTORS  
2 AMPERES  
100 VOLTS, 20 WATTS

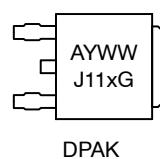


DPAK  
CASE 369C

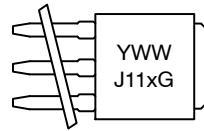


DPAK-3  
CASE 369D

#### MARKING DIAGRAMS



DPAK



DPAK-3

A = Assembly Location  
Y = Year  
WW = Work Week  
X = 2 or 7  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MJD112 (NPN), MJD117 (PNP)

## MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5	Vdc
Collector Current Continuous Peak	$I_C$	2 4	Adc
Base Current	$I_B$	50	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	W W/ $^\circ\text{C}$
Total Power Dissipation (Note1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	6.25	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	$^\circ\text{C}/\text{W}$

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

## MJD112 (NPN), MJD117 (PNP)

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage (Note 2) ( $I_C = 30 \text{ mA}_\text{dc}$ , $I_B = 0$ )	$V_{\text{CEO}(\text{sus})}$	100	–	Vdc
Collector Cutoff Current ( $V_{\text{CE}} = 50 \text{ Vdc}$ , $I_B = 0$ )	$I_{\text{CEO}}$	–	20	$\mu\text{A}_\text{dc}$
Collector Cutoff Current ( $V_{\text{CB}} = 100 \text{ Vdc}$ , $I_E = 0$ )	$I_{\text{CBO}}$	–	20	$\mu\text{A}_\text{dc}$
Emitter Cutoff Current ( $V_{\text{BE}} = 5 \text{ Vdc}$ , $I_C = 0$ )	$I_{\text{EBO}}$	–	2	$\text{mA}_\text{dc}$
Collector-Cutoff Current ( $V_{\text{CB}} = 80 \text{ Vdc}$ , $I_E = 0$ )	$I_{\text{CBO}}$	–	10	$\mu\text{A}_\text{dc}$
Emitter-Cutoff Current ( $V_{\text{BE}} = 5 \text{ Vdc}$ , $I_C = 0$ )	$I_{\text{EBO}}$	–	2	$\text{mA}_\text{dc}$
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 0.5 \text{ Adc}$ , $V_{\text{CE}} = 3 \text{ Vdc}$ ) ( $I_C = 2 \text{ Adc}$ , $V_{\text{CE}} = 3 \text{ Vdc}$ ) ( $I_C = 4 \text{ Adc}$ , $V_{\text{CE}} = 3 \text{ Vdc}$ )	$h_{\text{FE}}$	500 1000 200	– 12,000 –	–
Collector-Emitter Saturation Voltage ( $I_C = 2 \text{ Adc}$ , $I_B = 8 \text{ mA}_\text{dc}$ ) ( $I_C = 4 \text{ Adc}$ , $I_B = 40 \text{ mA}_\text{dc}$ )	$V_{\text{CE}(\text{sat})}$	– –	2 3	Vdc
Base-Emitter Saturation Voltage ( $I_C = 4 \text{ Adc}$ , $I_B = 40 \text{ mA}_\text{dc}$ )	$V_{\text{BE}(\text{sat})}$	–	4	Vdc
Base-Emitter On Voltage ( $I_C = 2 \text{ Adc}$ , $V_{\text{CE}} = 3 \text{ Vdc}$ )	$V_{\text{BE}(\text{on})}$	–	2.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current-Gain – Bandwidth Product ( $I_C = 0.75 \text{ Adc}$ , $V_{\text{CE}} = 10 \text{ Vdc}$ , $f = 1 \text{ MHz}$ )	$f_T$	25	–	MHz
Output Capacitance ( $V_{\text{CB}} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 0.1 \text{ MHz}$ ) MJD117, NJVMJD117T4G MJD112, NJVMJD112G, NJVMJD112T4G	$C_{\text{ob}}$	– –	200 100	pF

2. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

\*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

## MJD112 (NPN), MJD117 (PNP)

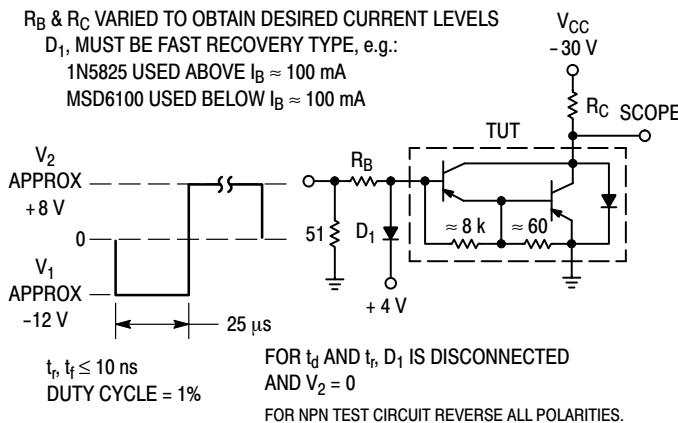


Figure 1. Switching Times Test Circuit

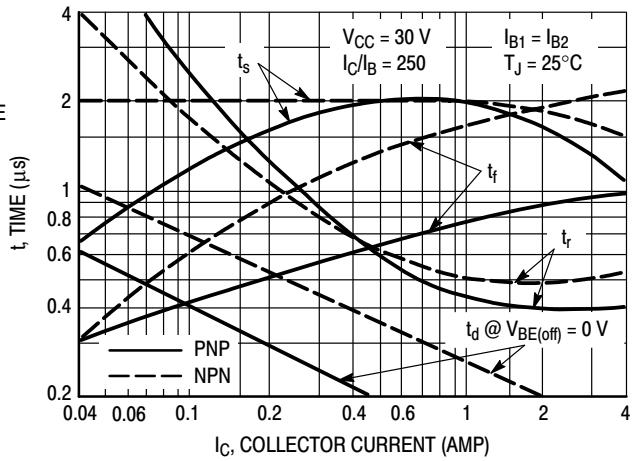


Figure 2. Switching Times

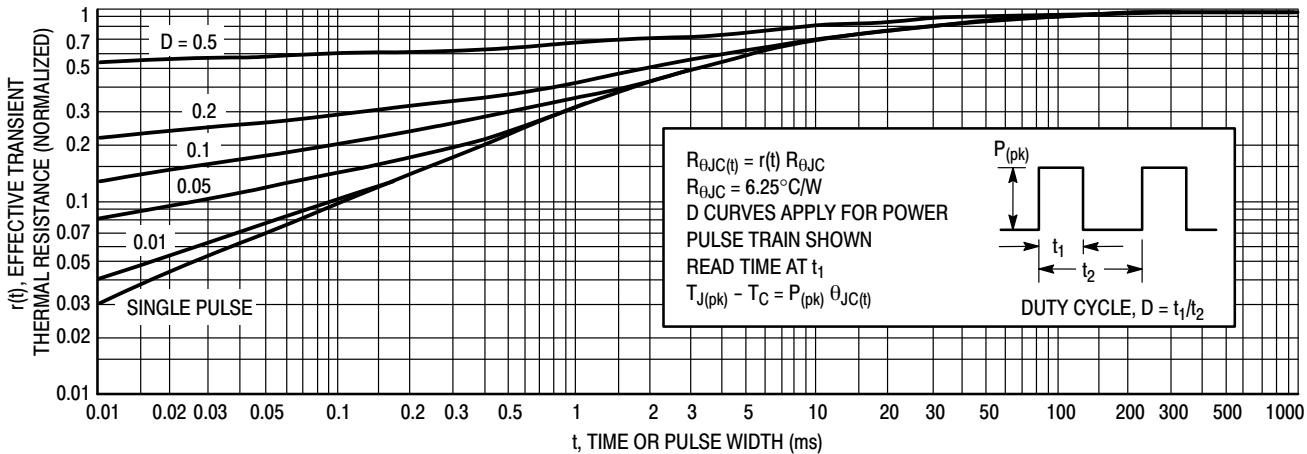
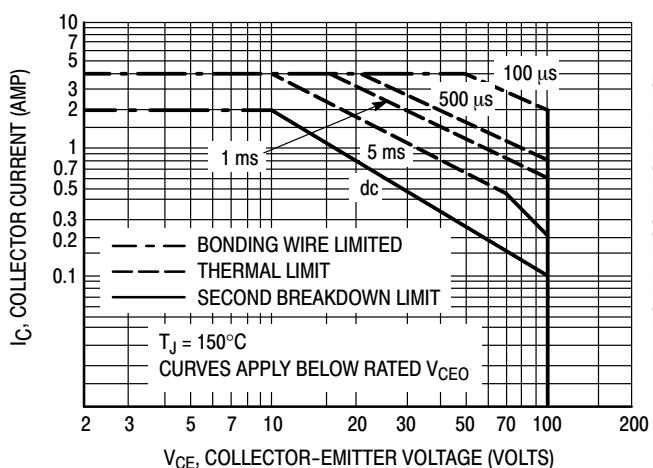


Figure 3. Thermal Response

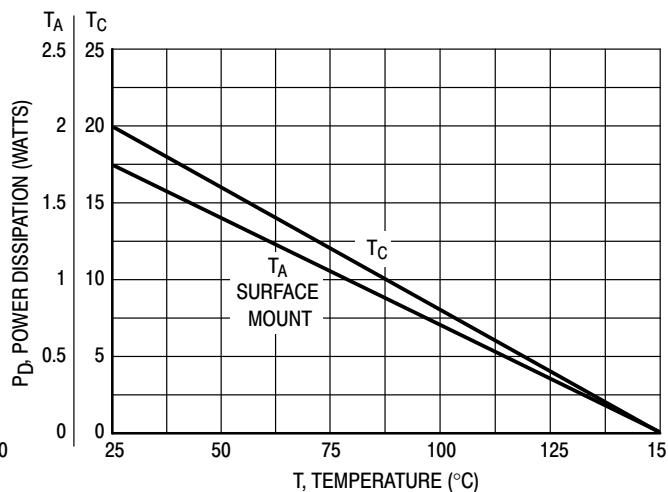
**ACTIVE-REGION SAFE-OPERATING AREA**



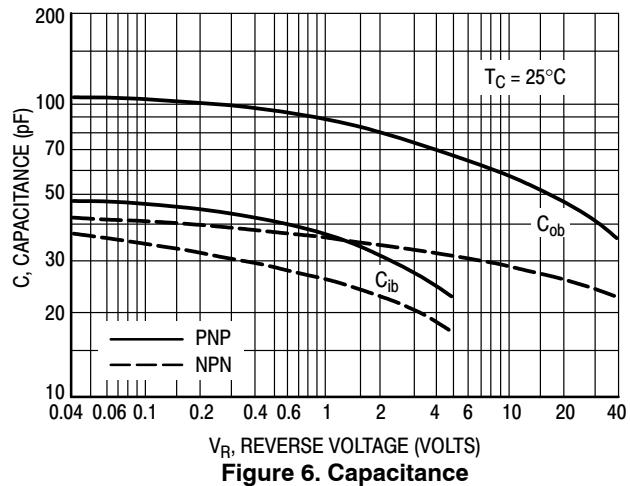
**Figure 4. Maximum Rated Forward Biased Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 5. Power Derating**



**Figure 6. Capacitance**

# MJD112 (NPN), MJD117 (PNP)

## TYPICAL ELECTRICAL CHARACTERISTICS

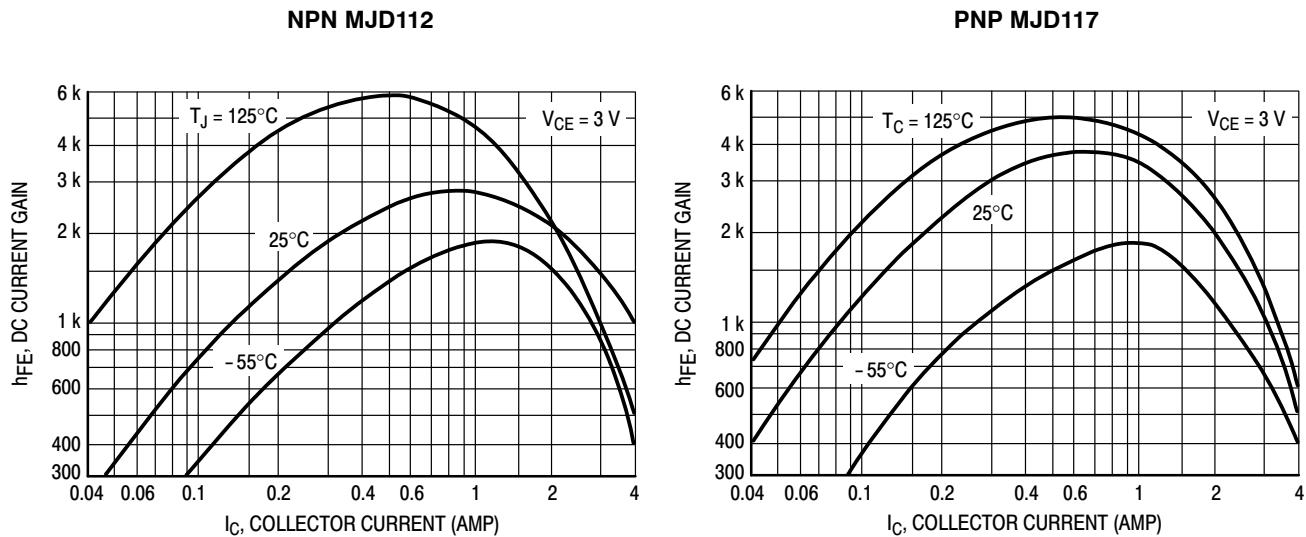


Figure 7. DC Current Gain

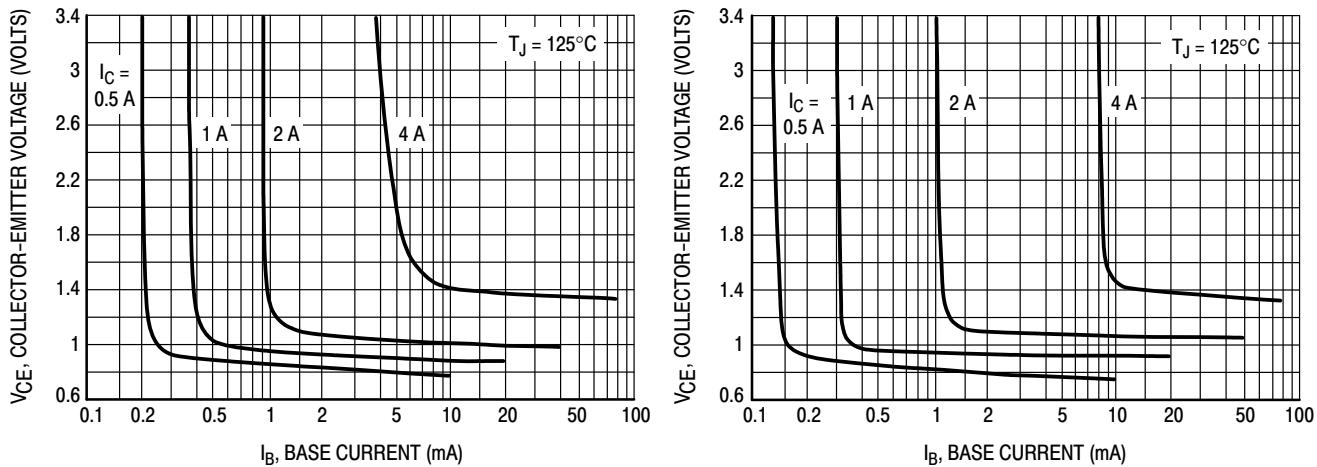


Figure 8. Collector Saturation Region

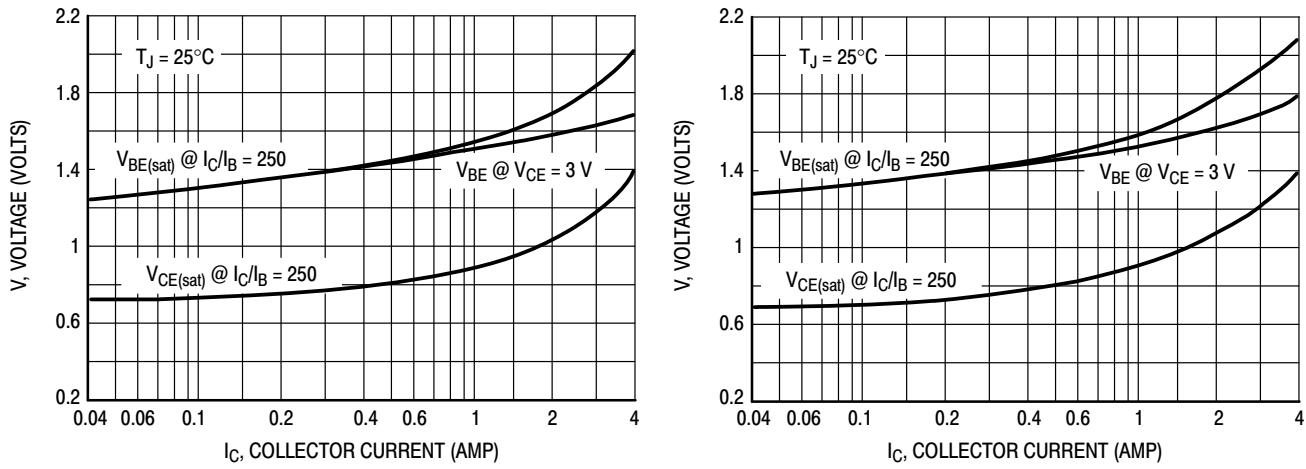
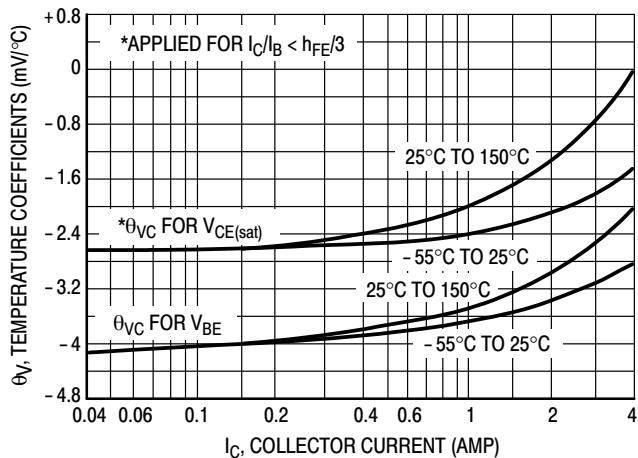


Figure 9. "On" Voltages

## MJD112 (NPN), MJD117 (PNP)

NPN MJD112



PNP MJD117

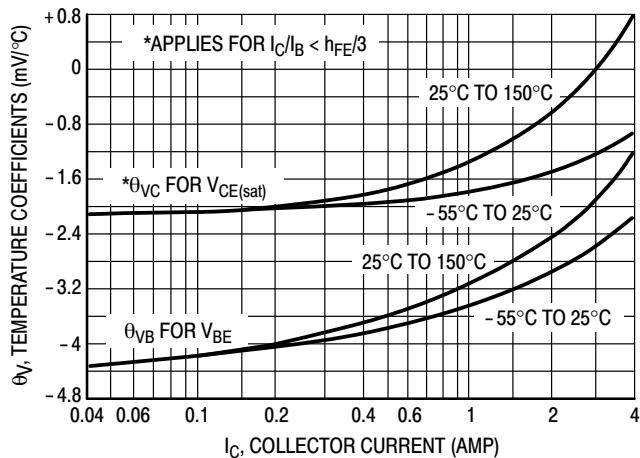


Figure 10. Temperature Coefficients

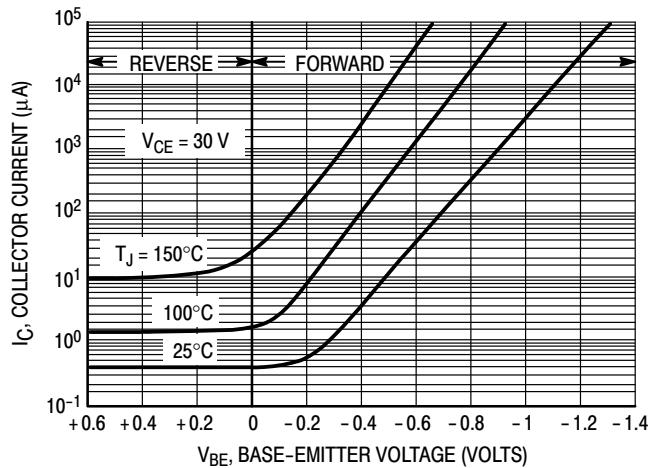
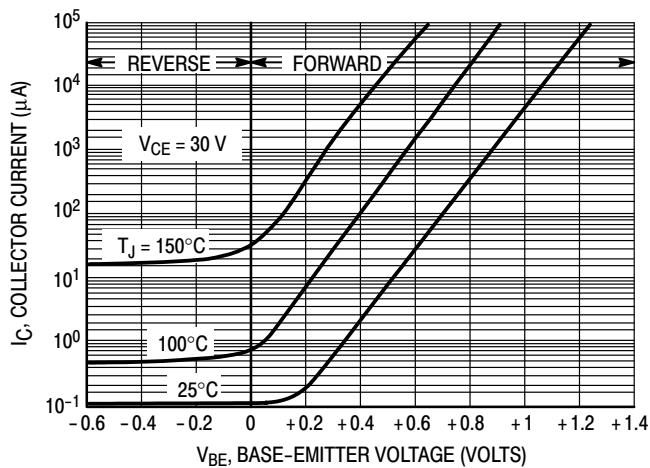


Figure 11. Collector Cut-Off Region

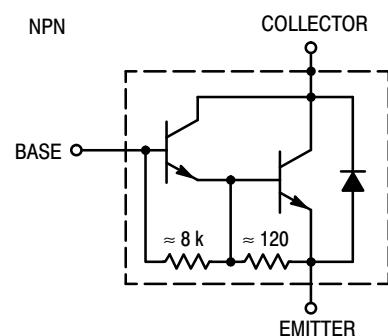
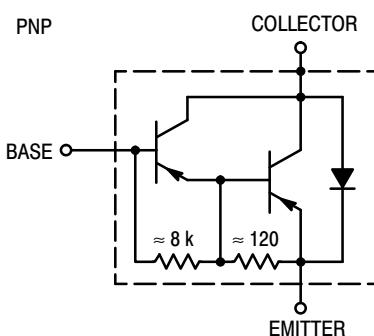


Figure 12. Darlington Schematic

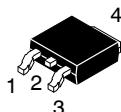
## MJD112 (NPN), MJD117 (PNP)

### ORDERING INFORMATION

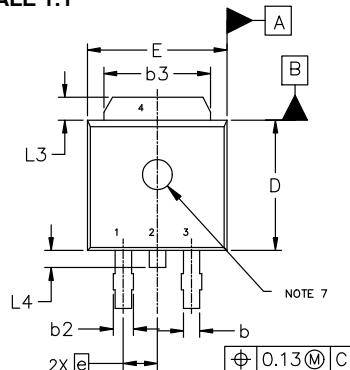
Device	Package Type	Package	Shipping <sup>†</sup>
MJD112G	DPAK (Pb-Free)	369C	75 Units / Rail
NJVMJD112G*	DPAK (Pb-Free)	369C	75 Units / Rail
MJD112-1G	DPAK-3 (Pb-Free)	369D	75 Units / Rail
MJD112RLG	DPAK (Pb-Free)	369C	1,800 Tape & Reel
MJD112T4G	DPAK (Pb-Free)	369C	2,500 Tape & Reel
NJVMJD112T4G*	DPAK (Pb-Free)	369C	2,500 Tape & Reel
MJD117G	DPAK (Pb-Free)	369C	75 Units / Rail
MJD117-1G	DPAK-3 (Pb-Free)	369D	75 Units / Rail
MJD117RLG	DPAK (Pb-Free)	369C	1,800 Tape & Reel
MJD117T4G	DPAK (Pb-Free)	369C	2,500 Tape & Reel
NJVMJD117T4G*	DPAK (Pb-Free)	369C	2,500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



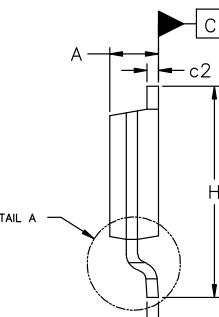
SCALE 1:1



TOP VIEW

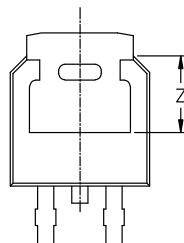
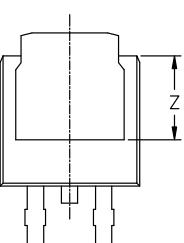
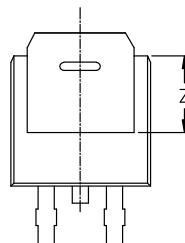
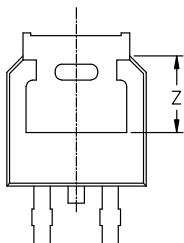
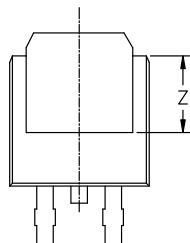
**DPAK3 6.10x6.54x2.28, 2.29P**  
CASE 369C  
ISSUE J

DATE 12 AUG 2025



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29	BSC	
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90	REF	
L2	0.51	BSC	
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---

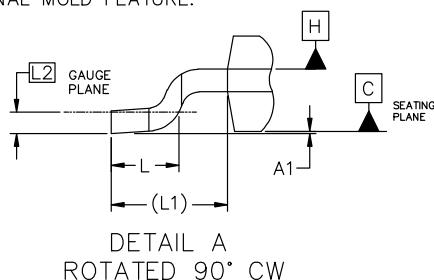
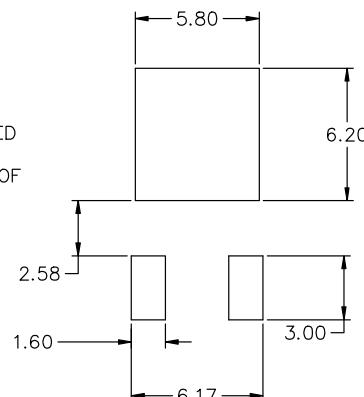


BOTTOM VIEW

ALTERNATE CONSTRUCTIONS

## NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DETAIL A  
ROTATED 90° CW

RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

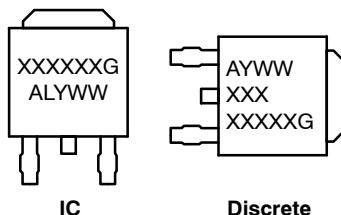
DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 1 OF 2

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**DPAK3 6.10x6.54x2.28, 2.29P**  
**CASE 369C**  
**ISSUE J**

DATE 12 AUG 2025

## GENERIC MARKING DIAGRAM\*



XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

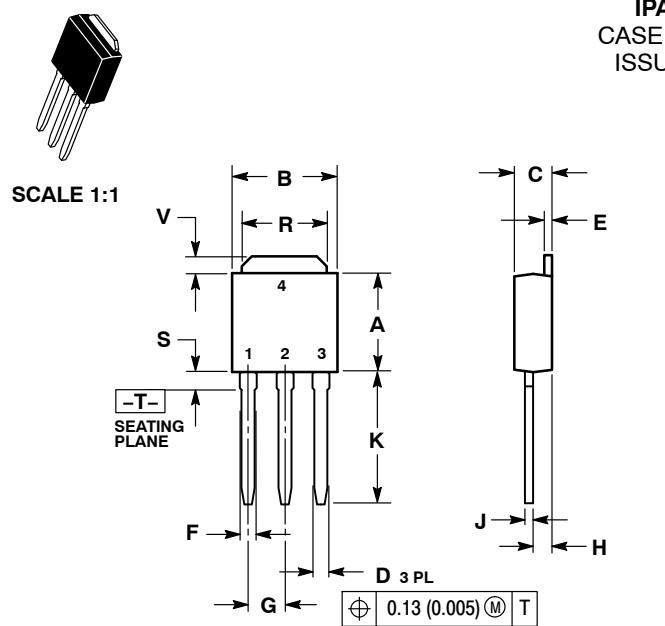
STYLE 1: PIN 1. BASE	STYLE 2: PIN 1. GATE	STYLE 3: PIN 1. ANODE	STYLE 4: PIN 1. CATHODE	STYLE 5: PIN 1. GATE
2. COLLECTOR	2. DRAIN	2. CATHODE	2. ANODE	2. ANODE
3. Emitter	3. SOURCE	3. ANODE	3. GATE	3. CATHODE
4. COLLECTOR	4. DRAIN	4. CATHODE	4. ANODE	4. ANODE

STYLE 6: PIN 1. MT1	STYLE 7: PIN 1. GATE	STYLE 8: PIN 1. N/C	STYLE 9: PIN 1. ANODE	STYLE 10: PIN 1. CATHODE
2. MT2	2. COLLECTOR	2. CATHODE	2. CATHODE	2. ANODE
3. GATE	3. Emitter	3. ANODE	3. RESISTOR ADJUST	3. CATHODE
4. MT2	4. COLLECTOR	4. CATHODE	4. CATHODE	4. ANODE

<b>DOCUMENT NUMBER:</b>	<b>98AON10527D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DPAK3 6.10x6.54x2.28, 2.29P</b>	<b>PAGE 2 OF 2</b>

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DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	----	3.93	----

### GENERIC MARKING DIAGRAMS

STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. Emitter  
4. COLLECTOR

STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

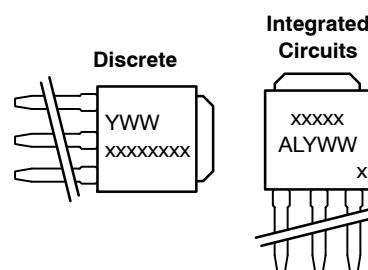
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PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE

STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE

STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE

STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2

STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. Emitter  
4. COLLECTOR



xxxxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON10528D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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