

TLC1549C, TLC1549I, TLC1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

- 10-Bit-Resolution A/D Converter
- Inherent Sample and Hold
- Total Unadjusted Error . . . ± 1 LSB Max
- On-Chip System Clock
- Terminal Compatible With TLC549 and TLV1549
- CMOS Technology

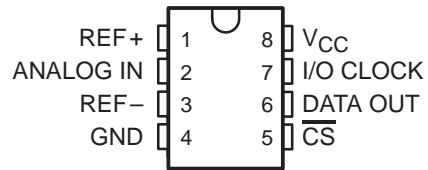
description

The TLC1549C, TLC1549I, and TLC1549M are 10-bit, switched-capacitor, successive-approximation analog-to-digital converters. These devices have two digital inputs and a 3-state output [chip select (\overline{CS}), input-output clock (I/O CLOCK), and data output (DATA OUT)] that provide a three-wire interface to the serial port of a host processor.

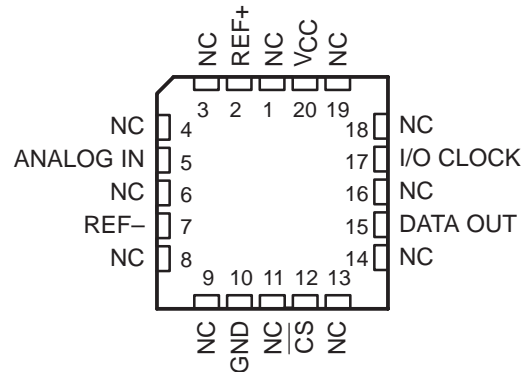
The sample-and-hold function is automatic. The converter incorporated in these devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The TLC1549C is characterized for operation from 0°C to 70°C. The TLC1549I is characterized for operation from -40°C to 85°C. The TLC1549M is characterized for operation over the full military temperature range of -55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T _A	PACKAGE			
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	TLC1549CD	—	—	TLC1549CP
-40°C to 85°C	TLC1549ID	—	—	TLC1549IP
-55°C to 125°C	—	TLC1549MFK	TLC1549MJG	—



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

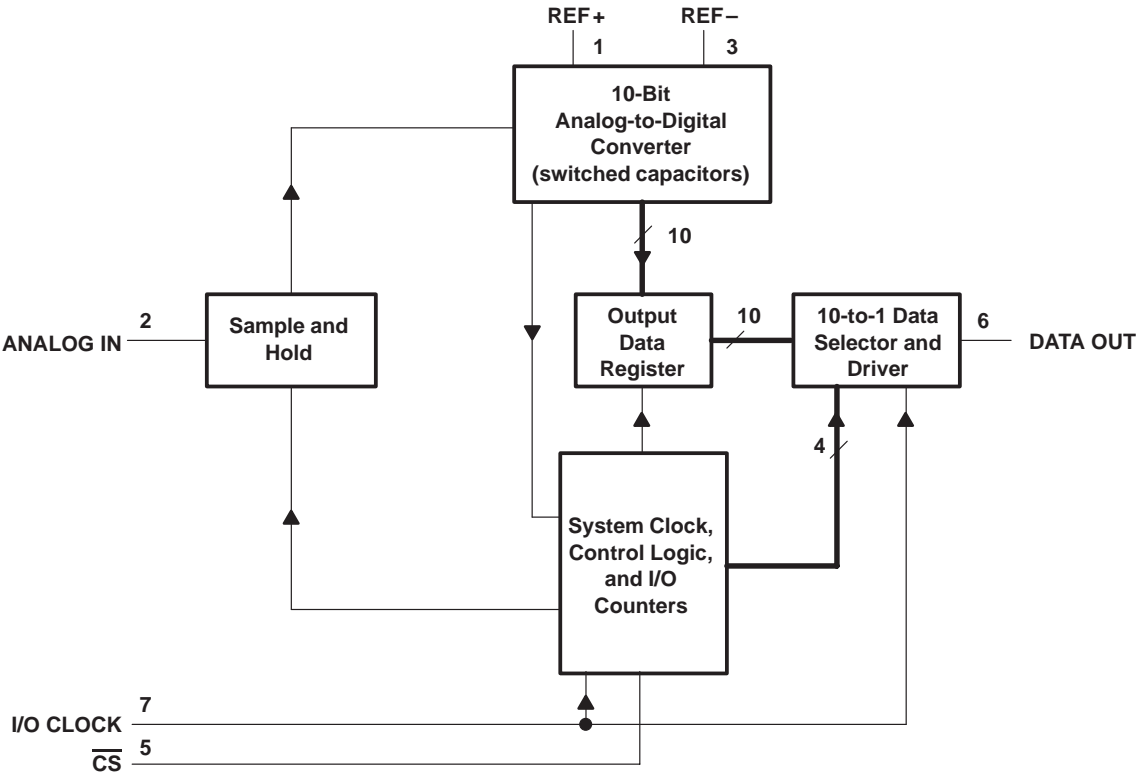
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

TLC1549C, TLC1549I, TLC1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

functional block diagram



Terminal numbers shown are for the D, JG, and P packages only.

typical equivalent inputs

INPUT CIRCUIT IMPEDANCE DURING SAMPLING MODE	INPUT CIRCUIT IMPEDANCE DURING HOLD MODE
<p>ANALOG IN — $1\text{ k}\Omega\text{ TYP}$ — $C_i = 60\text{ pF TYP}$ (equivalent input capacitance)</p>	<p>ANALOG IN — $5\text{ M}\Omega\text{ TYP}$</p>

TLC1549C, TLC1549I, TLC1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANALOG IN	2	I	Analog signal input. The driving source impedance should be $\leq 1\text{ k}\Omega$. The external driving source to ANALOG IN should have a current capability $\geq 10\text{ mA}$.
$\overline{\text{CS}}$	5	I	Chip select. A high-to-low transition on $\overline{\text{CS}}$ resets the internal counters and controls and enables DATA OUT and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	6	O	This 3-state serial output for the A/D conversion result is in the high-impedance state when $\overline{\text{CS}}$ is high and active when $\overline{\text{CS}}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATAOUT to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
GND	4		The ground return for internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	7	I	Input/output clock. I/O CLOCK receives the serial I/O CLOCK input and performs the following three functions: 1) On the third falling edge of I/O CLOCK, the analog input voltage begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 2) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 3) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF +	1	I	The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to REF+ and the voltage applied to REF–.
REF –	3	I	The lower reference voltage value (nominally ground) is applied to REF–.
V_{CC}	8		Positive supply voltage

detailed description

With chip select ($\overline{\text{CS}}$) inactive (high), I/O CLOCK is initially disabled and DATA OUT is in the high impedance state. When the serial interface takes $\overline{\text{CS}}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and the removal of DATA OUT from the high-impedance state. The serial interface then provides the I/O CLOCK sequence to I/O CLOCK and receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first ten I/O clocks provide the control timing for sampling the analog input.

There are six basic serial interface timing modes that can be used with the TLC1549. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{\text{CS}}$ as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and $\overline{\text{CS}}$ inactive (high) between transfers, (2) a fast mode with a 10-clock transfer and $\overline{\text{CS}}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{\text{CS}}$ inactive (high) between transfers, (4) a fast mode with a 16-bit transfer and $\overline{\text{CS}}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{\text{CS}}$ inactive (high) between transfers, and (6) a slow mode with a 16-clock transfer and $\overline{\text{CS}}$ active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{\text{CS}}$ in mode 1, mode 3, and mode 5, within 21 μs from the falling edge of the tenth I/O CLOCK in mode 2 and mode 4, and following the sixteenth clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of $\overline{\text{CS}}$, the number of I/O serial transfer clocks that can be used, and the timing on which the MSB of the previous conversion appears at the output.



TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

detailed description

Table 1. Mode Operation

MODES		\overline{CS}	NO. OF I/O CLOCKS	MSB AT Terminal 6†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	\overline{CS} falling edge	Figure 6
	Mode 2	Low continuously	10	Within 21 μ s	Figure 7
	Mode 3	High between conversion cycles	11 to 16‡	\overline{CS} falling edge	Figure 8
	Mode 4	Low continuously	16‡	Within 21 μ s	Figure 9
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	\overline{CS} falling edge	Figure 10
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 11

† This timing also initiates serial interface communication.

‡ No more than 16 clocks should be used.

All the modes require a minimum period of 21 μ s after the falling edge of the tenth I/O CLOCK before a new transfer sequence can begin. During a serial I/O CLOCK data transfer, \overline{CS} must be active (low) so that I/O CLOCK is enabled. When \overline{CS} is toggled between data transfers (modes 1, 3, and 5), the transitions at \overline{CS} are recognized as valid only if the level is maintained for a minimum period of 1.425 μ s after the transition. If the transfer is more than ten I/O clocks (modes 3, 4, 5, and 6), the rising edge of the eleventh clock must occur within 9.5 μ s after the falling edge of the tenth I/O CLOCK; otherwise, the device could lose synchronization with the host serial interface and \overline{CS} has to be toggled to restore proper operation.

fast modes

The TLC1549 is in a fast mode when the serial I/O CLOCK data transfer is completed within 21 μ s from the falling edge of the tenth I/O CLOCK. With a ten-clock serial transfer, the device can only run in a fast mode.

mode 1: fast mode, \overline{CS} inactive (high) between transfers, 10-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, \overline{CS} active (low) continuously, 10-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. Within 21 μ s after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

mode 3: fast mode, \overline{CS} inactive (high) between transfers, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, \overline{CS} active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. Within 21 μ s after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

slow modes

In a slow mode, the serial I/O CLOCK data transfer is completed after 21 μ s from the falling edge of the tenth I/O CLOCK.



mode 5: slow mode, \overline{CS} inactive (high) between transfers, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, \overline{CS} active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16 clock transfer initiated by the serial interface.

analog input sampling

Sampling of the analog input starts on the falling edge of the third I/O CLOCK, and sampling continues for seven I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are determined.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

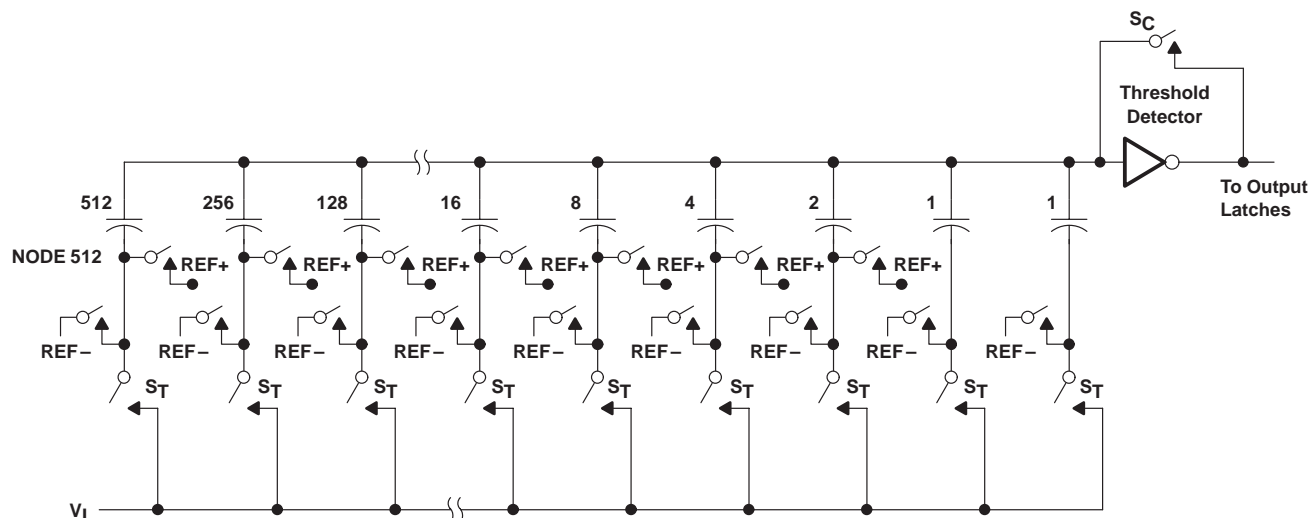


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of \overline{CS} starts all modes of operation, and \overline{CS} can abort a conversion sequence in any mode. A high-to-low transition on \overline{CS} within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Care should be exercised to prevent \overline{CS} from being taken low close to completion of conversion because the output data may be corrupted.

reference voltage inputs

There are two reference inputs used with the TLC1549: REF+ and REF-. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF-.

TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1):	TLC1549C, TLC1549I	–0.5 V to 6.5 V
	TLC1549M	–0.5 V to 6 V
Input voltage range, V_I (any input)		–0.3 V to $V_{CC} + 0.3$ V
Output voltage range, V_O		–0.3 V to $V_{CC} + 0.3$ V
Positive reference voltage, V_{ref+}		$V_{CC} + 0.1$ V
Negative reference voltage, V_{ref-}		–0.1 V
Peak input current (any input)		±20 mA
Peak total input current (all inputs)		±30 mA
Operating free-air temperature range, T_A :	TLC1549C	0°C to 70°C
	TLC1549I	–40°C to 85°C
	TLC1549M	–55°C to 125°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.5	5	5.5	V
Positive reference voltage, V _{ref+} (see Note 2)		V _{CC}			V
Negative reference voltage, V _{ref−} (see Note 2)		0			V
Differential reference voltage, V _{ref+} − V _{ref−} (see Note 2)		2.5	V _{CC}	V _{CC} +0.2	V
Analog input voltage (see Note 2)		0	V _{CC}		V
High-level control input voltage, V _{IH}	V _{CC} = 4.5 V to 5.5 V	2			V
Low-level control input voltage, V _{IL}	V _{CC} = 4.5 V to 5.5 V			0.8	V
Clock frequency at I/O CLOCK (see Note 3)		0	2.1		MHz
Setup time, \overline{CS} low before first I/O CLOCK↑, t _{su} (CS) (see Note 4)		1.425			μs
Hold time, \overline{CS} low after last I/O CLOCK↓, t _h (CS)		0			ns
Pulse duration, I/O CLOCK high, t _{wH} (I/O)		190			ns
Pulse duration, I/O CLOCK low, t _{wL} (I/O)		190			ns
Transition time, I/O CLOCK, t _t (I/O) (see Note 5 and Figure 5)				1	μs
Transition time, \overline{CS} , t _t (CS)				10	μs
Operating free-air temperature, T _A	TLC1549C	0	70		°C
	TLC1549I	−40	85		
	TLC1549M	−55	125		

- NOTES:
- Analog input voltages greater than that applied to REF+ convert as all ones (111111111), while input voltages less than that applied to REF– convert as all zeros (000000000). The TLC1549 is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.
 - For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V) at least 1 I/O CLOCK rising edge (≥ 2 V) must occur within 9.5 μs.
 - To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after \overline{CS} ↓ before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum \overline{CS} setup time has elapsed.
 - This is the time required for the clock input signal to fall from V_{IHmin} to V_{ILmax} or to rise from V_{ILmax} to V_{IHmin} . In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 μs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.5 \text{ V to } 5.5 \text{ V}$, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -1.6 \text{ mA}$	2.4			V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -20 \mu\text{A}$	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 1.6 \text{ mA}$			0.4	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OL} = 20 \mu\text{A}$			0.1	
I_{OZ}	Off-state (high-impedance-state) output current	$V_O = V_{CC}$, \overline{CS} at V_{CC}			10	μA
		$V_O = 0$, \overline{CS} at V_{CC}			-10	
I_{IH}	High-level input current	$V_I = V_{CC}$		0.005	2.5	μA
I_{IL}	Low-level input current	$V_I = 0$		-0.005	-2.5	μA
I_{CC}	Operating supply current	\overline{CS} at 0 V		0.8	2.5	mA
Analog input leakage current		$V_I = V_{CC}$			1	μA
		$V_I = 0$			-1	
Maximum static analog reference current into $REF+$		$V_{ref+} = V_{CC}$, $V_{ref-} = \text{GND}$			10	μA
C_i	Input capacitance	TLC1549C, I (Analog) During sample cycle		30	55	pF
		TLC1549M (Analog) During sample cycle		30		
		TLC1549C, I (Control)		5	15	
		TLC1549M (Control)		5		

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

TLC1549C, TLC1549I, TLC1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

operating characteristics over recommended operating free-air temperature range,
 $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$, I/O CLOCK frequency = 2.1 MHz

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
E_L	Linearity error (see Note 6)			± 1	LSB
E_{ZS}	Zero-scale error (see Note 7)	See Note 2		± 1	LSB
E_{FS}	Full-scale error (see Note 7)	See Note 2		± 1	LSB
	Total unadjusted error (see Note 8)			± 1	LSB
t_{conv}	Conversion time	See Figures 6–10		21	μs
t_c	Total cycle time (access, sample, and conversion)	See Figures 6–10, See Note 9		21 + 10 I/O CLOCK periods	μs
t_v	Valid time, DATA OUT remains valid after I/O CLOCK \downarrow	See Figure 5	10		ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK \downarrow to DATA OUT valid	See Figure 5		240	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}\downarrow$ to DATA OUT (MSB driven)	See Figure 3		1.3	μs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}\uparrow$ to DATA OUT (high impedance)	See Figure 3		180	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 5		300	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 5		300	ns
$t_{d(I/O-CS)}$	Delay time, tenth I/O CLOCK \downarrow to $\overline{CS}\downarrow$ to abort conversion (see Note 10)			9	μs

- NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (11111111), while input voltages less than that applied to REF– convert as all zeros (00000000). The TLC1549 is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero, and full-scale errors.
9. I/O CLOCK period = $1/(\text{I/O CLOCK frequency})$. Sampling begins on the falling edge of the third I/O CLOCK, continues for seven I/O CLOCK periods, and ends on the falling edge of the 10th I/O CLOCK (see Figure 5).
10. Any transitions of \overline{CS} are recognized as valid only if the level is maintained for a minimum of a setup time plus two falling edges of the internal clock (1.425 μs) after the transition.



TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

PARAMETER MEASUREMENT INFORMATION

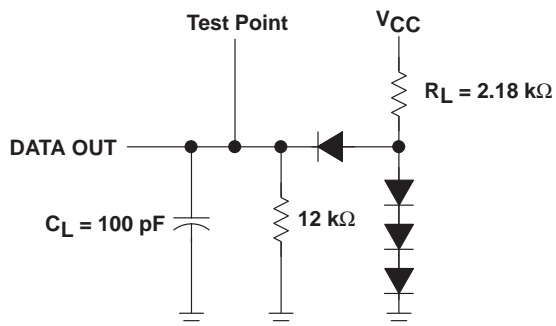


Figure 2. Load Circuit

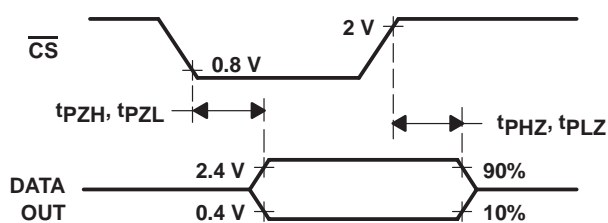


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

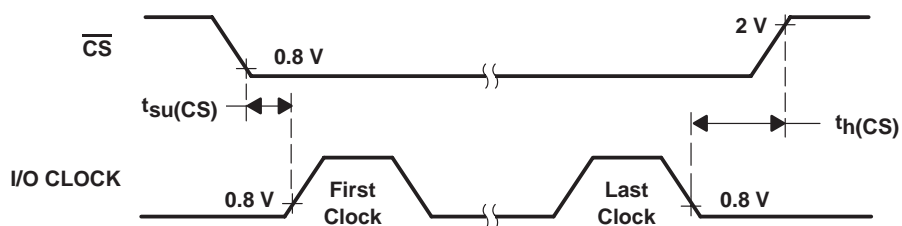


Figure 4. CS to I/O CLOCK Voltage Waveforms

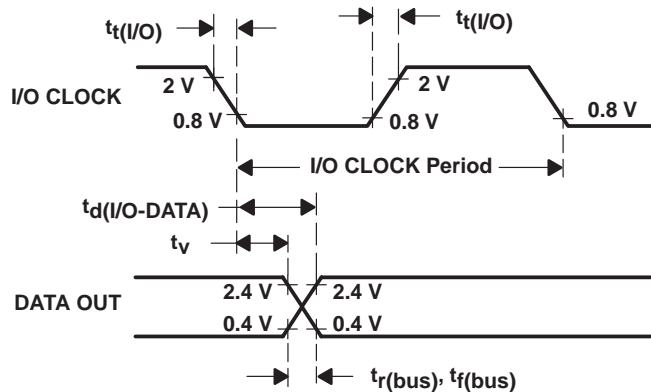


Figure 5. I/O CLOCK and DATA OUT Voltage Waveforms

TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

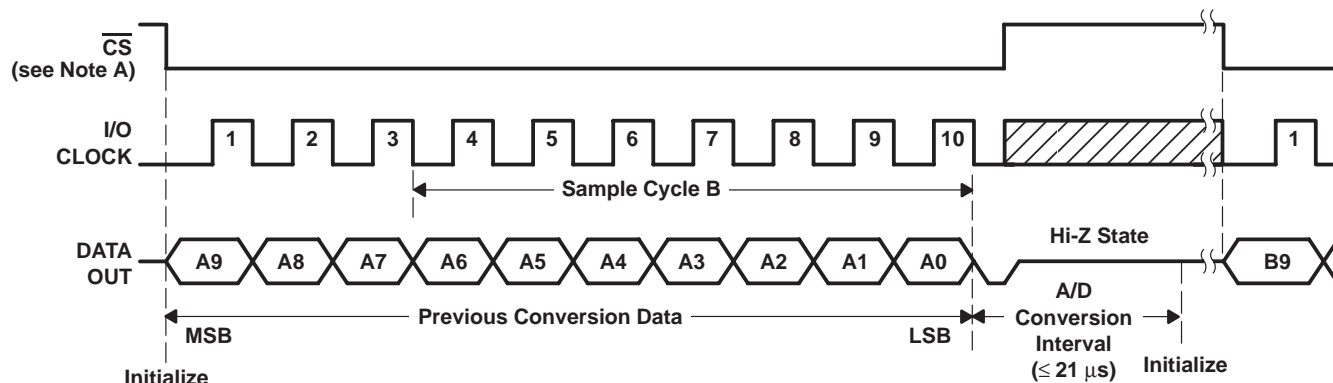


Figure 6. Timing for 10-Clock Transfer Using $\overline{\text{CS}}$

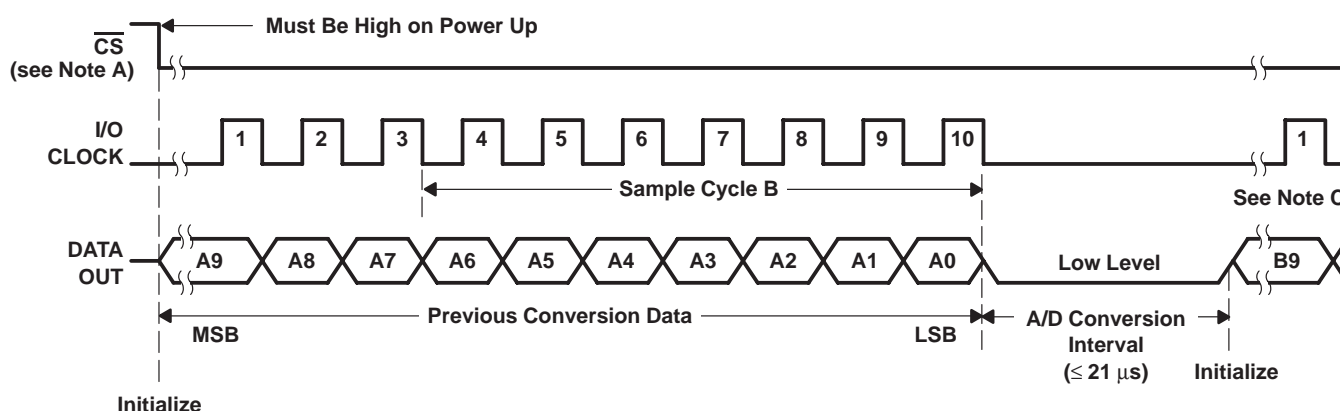


Figure 7. Timing for 10-Clock Transfer Not Using $\overline{\text{CS}}$

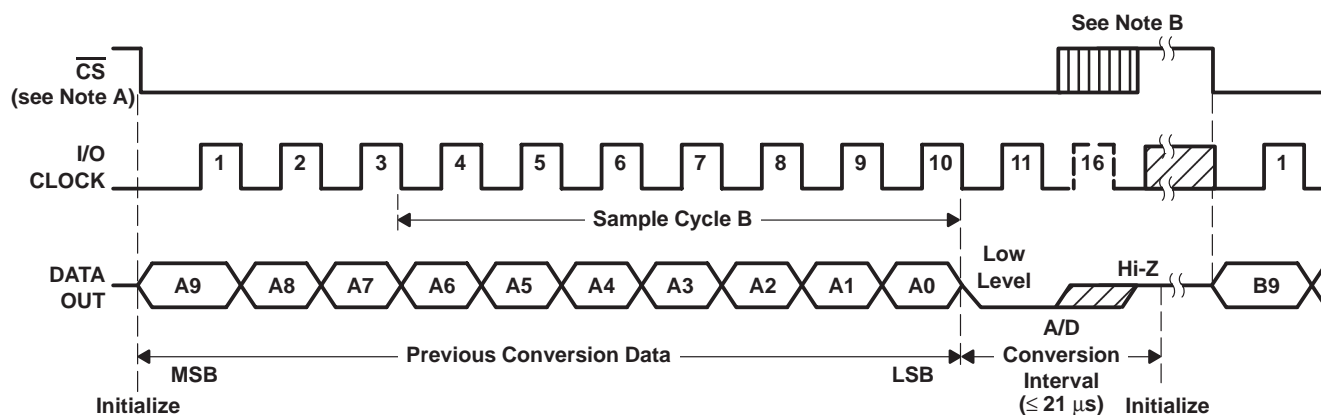


Figure 8. Timing for 11- to 16-Clock Transfer Using $\overline{\text{CS}}$ (Serial Transfer Completed Within 21 μs)

- NOTES:
- A. To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{\text{CS}} \downarrow$ before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum $\overline{\text{CS}}$ setup time has elapsed.
 - B. A low-to-high transition of $\overline{\text{CS}}$ disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.
 - C. The first I/O CLOCK must occur after the end of the previous conversion.

TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

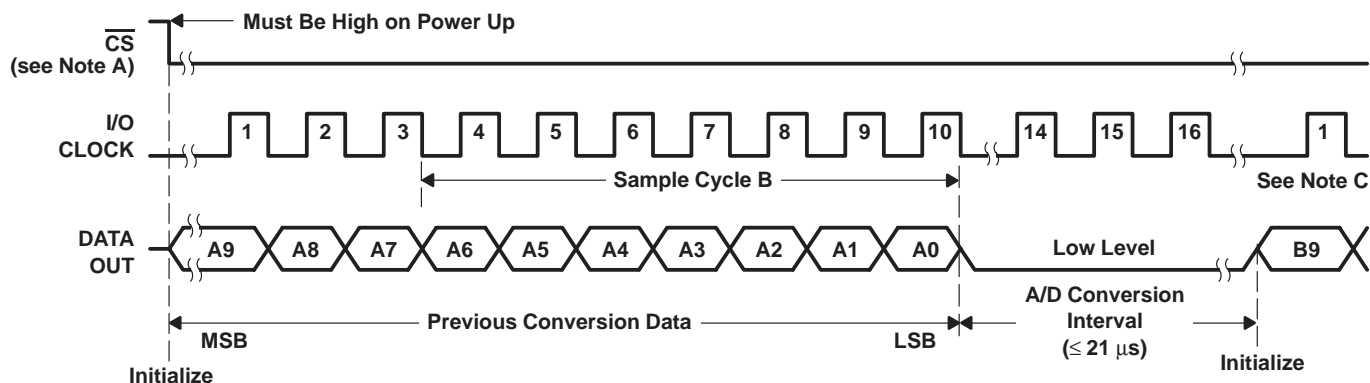


Figure 9. Timing for 16-Clock Transfer Not Using \overline{CS} (Serial Transfer Completed Within 21 μs)

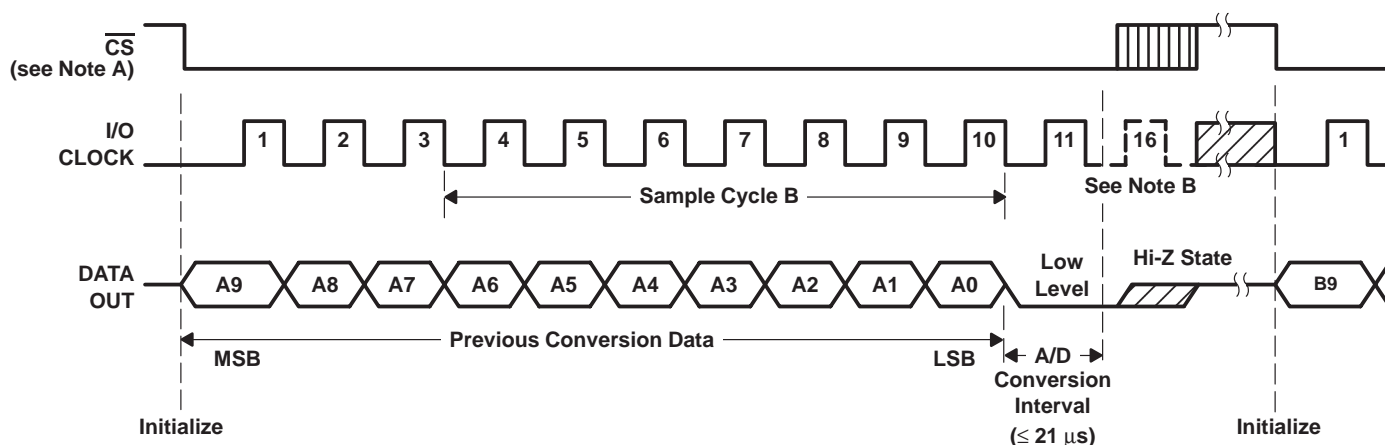


Figure 10. Timing for 11- to 16-Clock Transfer Using \overline{CS} (Serial Transfer Completed After 21 μs)

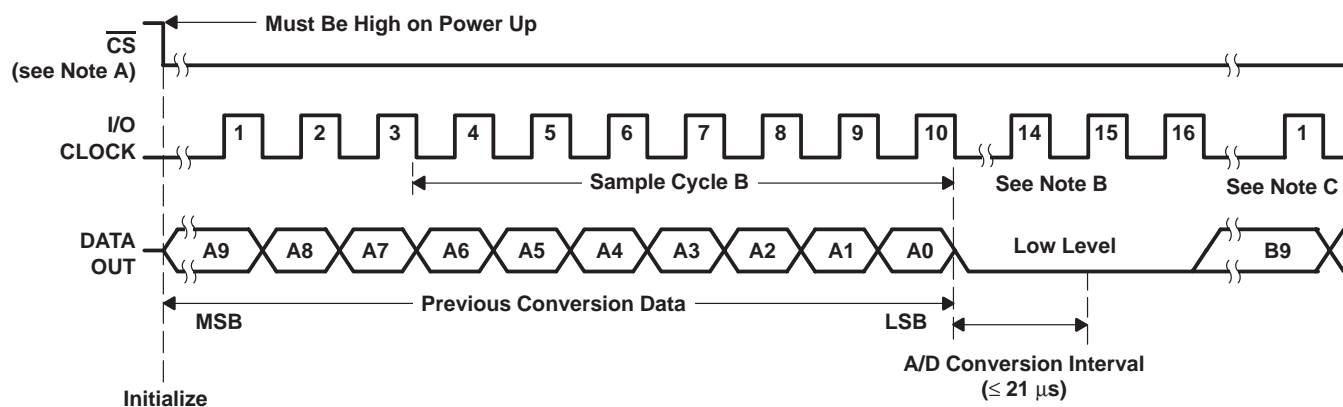
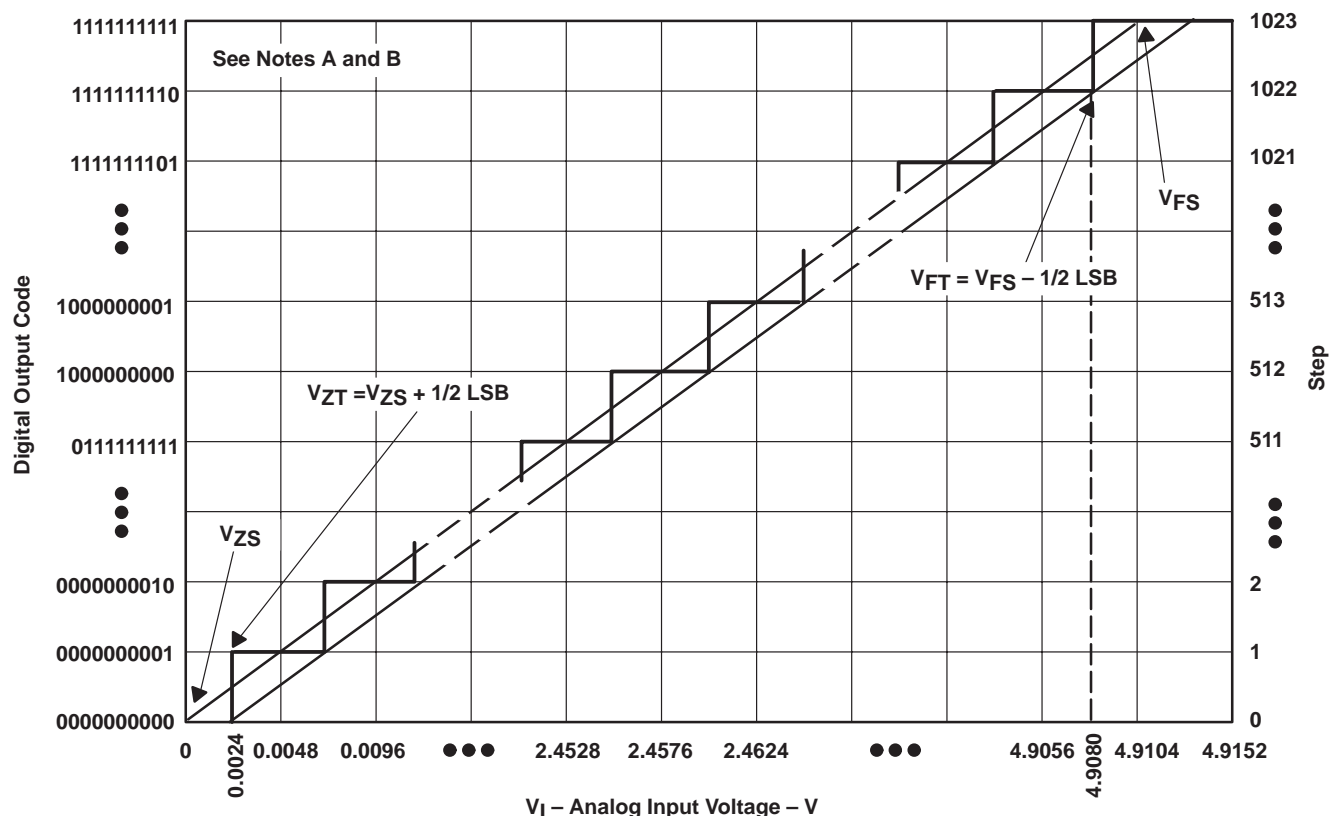


Figure 11. Timing for 16-Clock Transfer Not Using \overline{CS} (Serial Transfer Completed After 21 μs)

- NOTES:
- To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum \overline{CS} setup time has elapsed.
 - A low-to-high transition of \overline{CS} disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.
 - The first I/O CLOCK must occur after the end of the previous conversion.

APPLICATION INFORMATION



- NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.
- B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 12. Ideal Conversion Characteristics

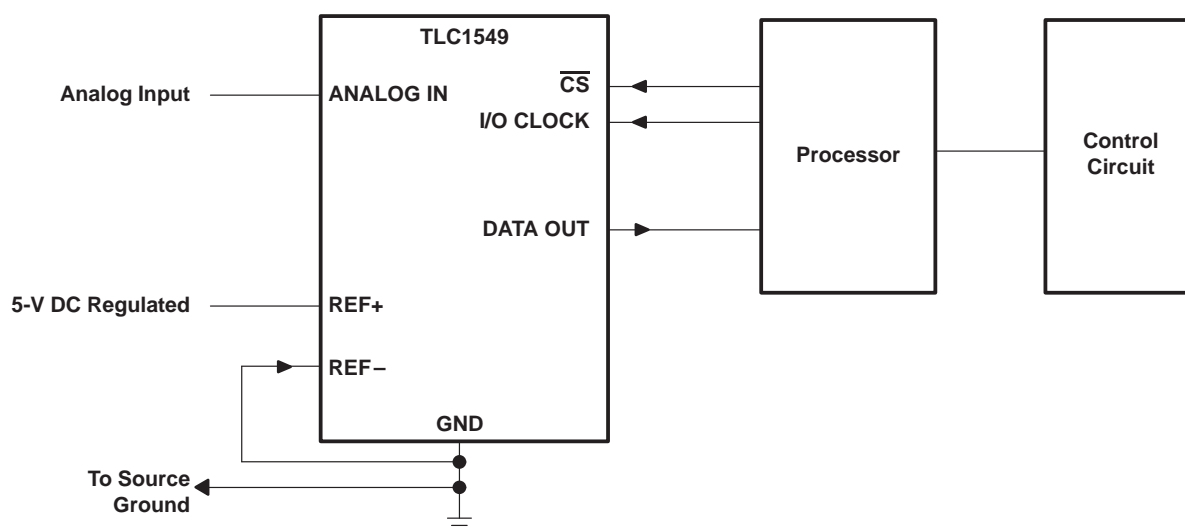


Figure 13. Typical Serial Interface

TLC1549C, TLC1549I, TLC1549M

10-BIT ANALOG-TO-DIGITAL CONVERTERS

WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 14, the time required to charge the analog input capacitance from 0 V to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (1)$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S / 2048) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S / 2048) = V_S \left(1 - e^{-t_c / R_t C_i} \right) \quad (3)$$

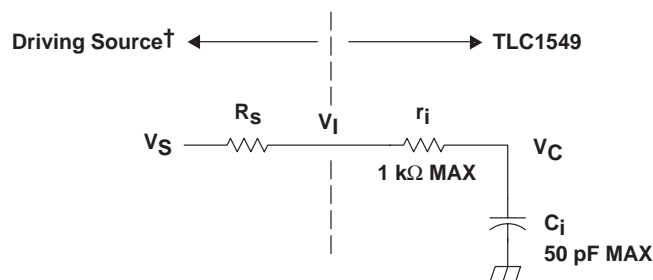
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(2048) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_S + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(2048) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at ANALOG IN
 V_S = External Driving Source Voltage
 R_S = Source Resistance
 r_i = Input Resistance
 C_i = Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 14. Equivalent Input Circuit Including the Driving Source

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC1549CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C1549C	Samples
TLC1549CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C1549C	Samples
TLC1549CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C1549C	Samples
TLC1549CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C1549C	Samples
TLC1549CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC1549CP	Samples
TLC1549ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C1549I	Samples
TLC1549IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C1549I	Samples
TLC1549IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C1549I	Samples
TLC1549IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C1549I	Samples
TLC1549IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC1549IP	Samples
TLC1549IPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC1549IP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com