



POWER MANAGEMENT

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

| Parameter | Symbol | Maximum | Units |
|---|-----------------|----------------------|-------|
| Input Supply Voltage | V_{CC} | 18 | V |
| BST to GND | V_{BST} | 40 | V |
| BST to PN | V_{BST_PN} | 10 | V |
| PN to GND | V_{PN} | -1 to 30 | V |
| PN to GND Negative Pulse ($t_{pulse} < 20ns$) | V_{PN_PULSE} | -5 | V |
| DL to GND | V_{DL} | -1 to +10 | V |
| DL to GND Negative Pulse ($t_{pulse} < 20ns$) | V_{DL_PULSE} | -3 | V |
| DH to PN | V_{DH_PN} | -1 to +10 | V |
| DH to PN Negative Pulse ($t_{pulse} < 20ns$) | V_{DH_PULSE} | -3 | V |
| DRV to GND | V_{DRV} | 10 | V |
| Operating Ambient Temperature Range | T_A | -25 to 85 | °C |
| Operating Junction Temperature | T_J | -25 to 125 | °C |
| Thermal Resistance Junction to Ambient | θ_{JA} | 100 (SO-14, QSOP-16) | °C/W |
| | | 48 (MLP-16) | |
| Thermal Resistance Junction to Case | θ_{JC} | 32 (SO-14, QSOP-16) | °C/W |
| | | 15 (MLP-16) | |
| Lead Temperature (Soldering) 10s | T_{LEAD} | 300 (SO-14, QSOP-16) | °C |
| | | 260 (MLP-16) | |
| Storage Temperature | T_{STG} | -65 to 150 | °C |

Electrical Characteristics

Unless specified: $V_{CC} = 5V$ to $16V$; $V_{FB} = V_O$; $V_{BST} - V_{PN} = 5V$ to $8.2V$; $T_A = -25^{\circ}C$ to $85^{\circ}C$

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------|---------------|--|-----|-----|-----|-------|
| General | | | | | | |
| VCC Supply Voltage | V_{CC} | | 4 | | 16 | V |
| VCC Quiescent Current | I_{QVCC} | $V_{CC} = 12V$, $V_{BST} - V_{PN} = 8.2V$ | | 5 | 7 | mA |
| VCC Under Voltage Lockout | UV_{VCC} | $V_{HYST} = 100mV$ | | 4 | | V |
| BST to PN Supply Voltage | V_{BST_PN} | | 4 | | 10 | V |
| BST Quiescent Current | I_{QBST} | $V_{CC} = 12V$, $V_{BST} - V_{PN} = 8.2V$ | | | 3 | mA |
| Internal LDO | | | | | | |
| LDO Output | V_{DRV} | $8.6V < V_{CC} < 16V$ | | 8.2 | | V |
| Dropout Voltage | V_{DROP} | $4V < V_{CC} < 8.6V$ | | 0.4 | | V |

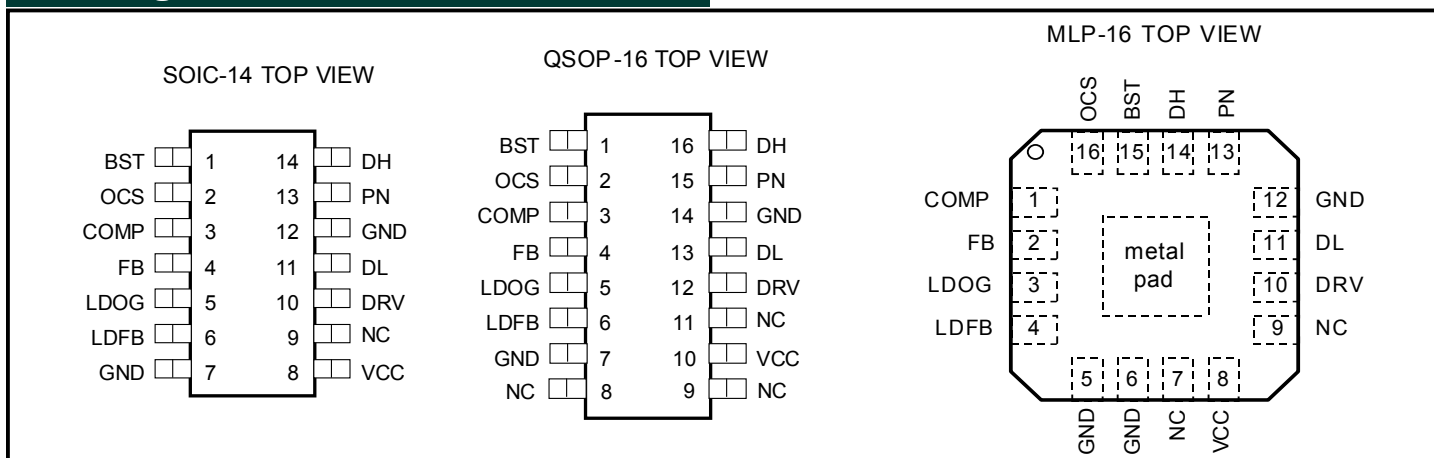
POWER MANAGEMENT
Electrical Characteristics

Unless specified: $V_{CC} = 5V$ to $16V$; $V_{FB} = V_O$; $V_{BST} - V_{PN} = 5V$ to $8.2V$; $T_A = -25^{\circ}C$ to $85^{\circ}C$

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-------------------------------------|----------------|--|-------|-------|-------|-------|
| Linear Section | | | | | | |
| Reference Voltage | V_{OL} | $LDFB = V_{OL}$, $T_A = 25^{\circ}C$, $V_{CC} = 12V$ | 0.495 | 0.500 | 0.505 | V |
| Gain ⁽²⁾ | A_{OLL} | LDFB to LDOG | | 70 | | dB |
| Load Regulation | | $I_O = 0$ to $1A$, $V_{IN} = 3.3V$, $V_{CC} = 12V$ | | | 0.4 | % |
| Line Regulation | | $V_{IN} = 3.2V$ to $3.4V$, $V_{CC} = 12V$ | | | 0.4 | % |
| VCC Supply Rejection | | $V_{IN} = 3.3V$, $V_{CC} = 10V$ to $14V$ | | | 0.4 | % |
| Gate Sourcing Current | | $V_{GATE} = 6.5V$ | | 1 | | mA |
| Gate Sinking Current | | $V_{GATE} = 6.5V$ | | 1 | | mA |
| LDFB Input Bias Current | | LDFB = 0.5V | | -0.2 | -1.0 | uA |
| Soft Start Time | | $V_{IN} = 3.3V$, $V_{CC} = 12V$, $T_A = 25^{\circ}C$ | | 1.5 | | ms |
| Switching Section | | | | | | |
| Reference Voltage | V_{REF} | $T_A = 25^{\circ}C$, $V_{CC} = 12V$ | 0.495 | 0.500 | 0.505 | V |
| Load Regulation | | $I_O = 0.2$ to $4A$ | | 0.4 | | % |
| Line Regulation | | $V_{CC} = 10V$ to $14V$ | | 0.4 | | % |
| Operating Frequency | F_S | | 400 | 450 | 525 | kHz |
| Ramp Amplitude ⁽²⁾ | V_m | | | 0.8 | | V |
| Maximum Duty Cycle ⁽²⁾ | D_{MAX} | | | 97 | | % |
| DH Rising/Falling Time | t_{SRC_DH} | 6V Swing at $C_L = 3.3nF$ $V_{BST} - V_{PN} = 8.2V$ | | 41 | | ns |
| | t_{SINK_DH} | | | 27 | | |
| DL Rising/Falling Time | t_{SRC_DL} | 6V Swing at $C_L = 3.3nF$ $V_{DRV} = 8.2V$ | | 29 | | ns |
| | t_{SINK_DL} | | | 42 | | |
| DH, DL Nonoverlapping Time | | | | 30 | | ns |
| Soft Start Time | | $T_A = 25^{\circ}C$, $V_{CC} = 12V$ | | 1.5 | | ms |
| Voltage Error Amplifier | | | | | | |
| Input Offset Voltage ⁽²⁾ | | | | 2 | | mV |
| Input Offset Current ⁽²⁾ | | | | 40 | | nA |
| Open Loop Gain ⁽²⁾ | | | | 80 | | dB |
| Unity Gain Bandwidth ⁽²⁾ | | | | 10 | | MHz |
| Output Source Current | | | | 0.9 | | mA |
| Output Sink Current | | | | 0.9 | | mA |
| Slew Rate ⁽²⁾ | | For $C_L = 500pF$ Load | | 1.2 | | V/us |

Notes:

- (1) This device is ESD sensitive. Use of standard ESD handling precautions is required.
 (2) Guaranteed by design, not tested in production.

POWER MANAGEMENT
Pin Configuration

Ordering Information

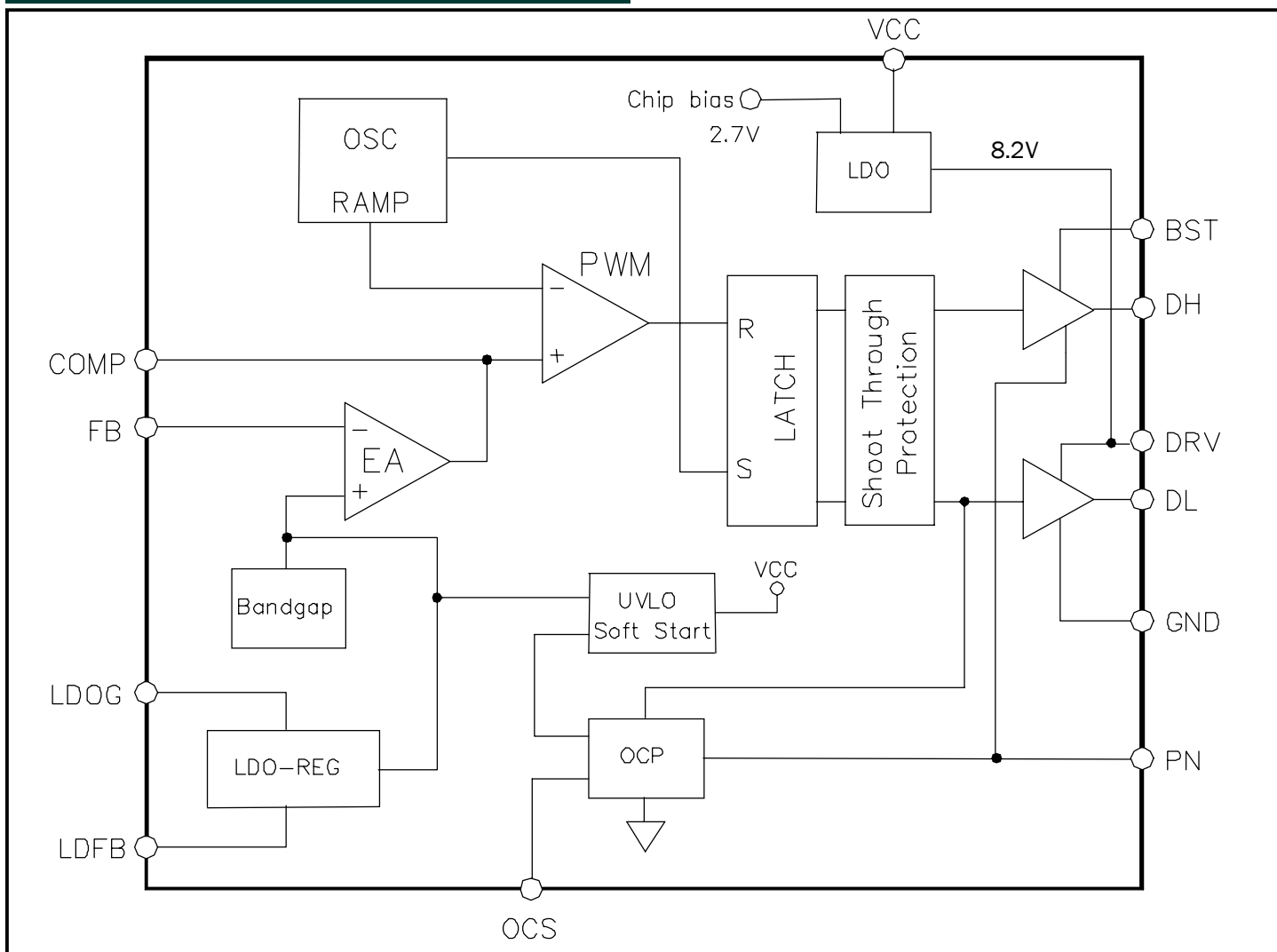
| Part Numbers | Package |
|-----------------------------------|---------|
| SC2621ASTRT ⁽¹⁾⁽²⁾ | SO-14 |
| SC2621AQSTRT ⁽¹⁾⁽²⁾⁽³⁾ | QSOP-16 |
| SC2621AMLTRT ⁽¹⁾⁽²⁾⁽³⁾ | MLP-16 |
| SC2621A EVB | |

Note:

- (1) Only available in tape and reel packaging. A reel contains 2500 devices.
- (2) Lead free products. This product is fully WEEE and RoHS compliant.
- (3) Contact factory for availability.

Pin Descriptions

| SO-14 | QSOP-16 | MLP-16 | Pin Name | Pin Function |
|-------|---------|--------|----------|--|
| 1 | 1 | 15 | BST | Boost input for top gate drive bias. |
| 2 | 2 | 16 | OCS | Current limit setting. Connect a resistor from this pin to ground to program the trip point of load current. |
| 3 | 3 | 1 | COMP | Error amplifier output for compensation. |
| 4 | 4 | 2 | FB | Voltage feed back of synchronous buck converter. |
| 5 | 5 | 3 | LDOG | External LDO gate drive. Connect this pin to the external N-MOSFET gate. |
| 6 | 6 | 4 | LDFB | External LDO feed back. Connect this pin to the linear regulator output. |
| 7 | 7 | 5,6 | GND | Chip ground. |
| 8 | 10 | 8 | VCC | Chip input power supply. |
| 9 | 8,9,11 | 7,9 | NC | No connection. |
| 10 | 12 | 10 | DRV | Internal LDO output. Connect a 1uF ceramic capasitor from this pin to ground for decoupling. This voltage is used for chip bias, including gate drivers. |
| 11 | 13 | 11 | DL | Gate drive for bottom MOSFET. |
| 12 | 14 | 12 | GND | Chip ground. |
| 13 | 15 | 13 | PN | Phase node. Connect this pin to bottom N-MOSFET drain. |
| 14 | 16 | 14 | DH | Gate drive for top MOSFET. |
| | | PAD | PAD | Exposed pad must be soldered to power ground plane. |

POWER MANAGEMENT
Block Diagram


THEORY OF OPERATION

The SC2621A integrates a high-speed, voltage mode PWM controller with a linear controller into a single package. It is designed to control two independent output voltages for high performance graphic card applications.

As shown in the block diagram of the SC2621A, the voltage-mode PWM controller consists of an error amplifier, a 450kHz ramp generator, a PWM comparator, a RS latch circuit, and two MOSFET drivers. The buck converter output voltage is fed back to the error amplifier negative input and is regulated to a reference voltage level. The error amplifier output is compared with the ramp to generate a PWM wave, which is amplified and used to drive the MOSFETs in the buck converter. The PWM wave at the phase node with the amplitude of V_{in} is filtered out to get a DC output. The linear controller is an error amplifier. It provides the gate drive and output voltage control for a linear regulator. Both PWM controller and linear controller work with soft-start and fault monitoring circuitry to meet application requirement.

UVLO, Start Up and Shut Down

To initiate the SC2621A, a supply voltage is applied to Vcc pin. The top gate (DH) and bottom gate (DL) are held low until Vcc voltage exceed UVLO (Under Voltage Lock Out) threshold, typically 4.0V. Then the internal Soft-Start (SS) capacitor begins to charge, the top gate remains low, and the bottom gate is pulled high to turn on the bottom MOSFET. When the SS voltage at the capacitor reaches 0.4V, the linear controller is enabled and the LDO output is turned on. Meanwhile, the top and bottom gates of PWM controller begin to switch. The switching regulator output is slowly ramping up for a soft turn-on. Refer to output soft start waveforms in Typical Performance Characteristics section on page 5.

If the supply voltages at Vcc pin falls below UVLO threshold during a normal operation, the SS capacitor begins to discharge. When the SS voltage reaches 0.4V, the PWM controller controls the switching regulator output to ramp down slowly for a soft turn-off. Meanwhile, the linear controller is disabled and LDO output is turned off.

Hiccup Mode Short Circuit Protection

The SC2621 uses low-side MOSFET $R_{ds(on)}$ sensing for over current protection. In every switching cycle, after the bottom MOSFET is on for 150ns, the SC2621 detects the phase node voltage and compares it with an internal setting voltage. If the phase node is lower than

the setting voltage, an overcurrent condition occurs. The SC2621 will discharge the internal SS capacitor and shut-down both outputs. After waiting for around 5 milliseconds, the SC2621 begins to charge SS capacitor again and initiates a fresh startup. The startup and shutdown cycle will repeat until the short circuit is removed. This is called a hiccup mode short circuit protection.

To program a load trip point for short circuit protection, it is recommended to connect a 3.3k resistor from the OCS pin to the ground, and a resistor R_{set} from the OCS pin to the DRV pin, as shown in Fig. 1.

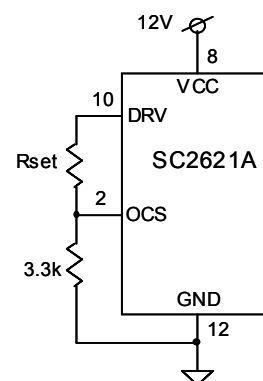


Fig. 1. Programming load trip point

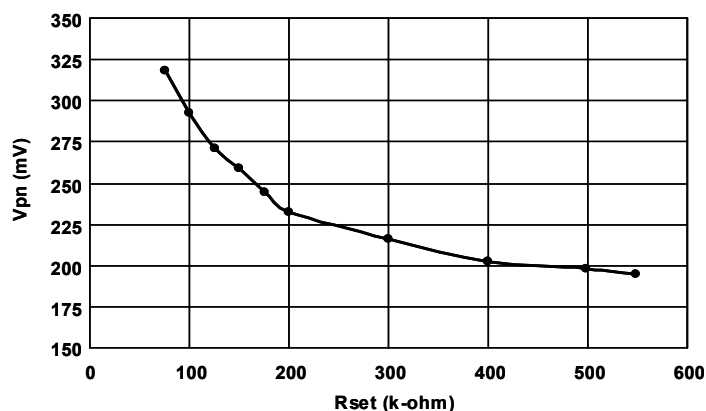


Fig. 2. Pull up resistor (R_{set}) vs. trip voltage V_{pn}

The resistor R_{set} can be found in Fig. 2 for a given phase node voltage V_{pn} at the load trip point. This voltage is the product of the inductor peak current at the load trip point and the $R_{ds(on)}$ of the low-side MOSFET:

$$V_{pn} = I_{peak} \times R_{ds_on}$$

Applications Information (Cont.)

The soft start time of the SC2621 is fixed at around 1.5ms. Therefore, the maximum soft start current is determined by the output inductance and output capacitance. The values of output inductor and output bulk capacitors have to be properly selected so that the soft start peak current does not exceed the load trip point of the short circuit protection.

Internal LDO for Gate Drive

An internal LDO is designed in the SC2621A to lower the 12V supply voltage for gate drive. An 1uF external ceramic capacitor connected in between DRV pin to the ground is needed to support the LDO. The LDO output is connected to low gate drive internally, and has to be connected to high gate drive through an external bootstrap circuit. The LDO output voltage is set at 8.2V. The manufacture data and bench tested results show that, for low $R_{ds(on)}$ MOSFETs run at applied load current, the optimum gate drive voltage is around 8.2V, where the total power losses of power MOSFETs are minimized.

COMPONENT SELECTION

General design guideline of switching power supplies can be applied to the component selection for the SC2621A.

Inductor and MOSFETs

The selection of inductor and MOSFETs should meet thermal requirement because they are power loss dominant components. Pick an inductor with as high inductance as possible without adding extra cost and size. The higher inductance, the lower ripple current, the smaller core loss and the higher efficiency will be. However, too high inductance slows down output transient response. It is recommended to choose the inductance that gives the inductor ripple current to be approximate 20% of maximum load current. So choose inductor value from:

$$L = \frac{5}{I_O \cdot f_{osc}} \cdot V_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$$

The MOSFETs are selected from their $R_{ds(on)}$, gate charge, and package. The SC2621A provides 1.5A gate drive current. To drive a 50nC gate charge MOSFET gives 50nC/1.5A=33ns switching time. The switching time t_s contributes to the top MOSFET switching loss:

$$P_S = I_O \cdot V_{IN} \cdot t_s \cdot f_{OSC}$$

There is no significant switching loss for the bottom MOSFET because of its zero voltage switching. The conduction losses of the top and bottom MOSFETs are given by:

$$P_{C_TOP} = I_O^2 \cdot R_{ds(on)} \cdot D$$

$$P_{C_BOT} = I_O^2 \cdot R_{ds(on)} \cdot (1 - D)$$

If the requirement of total power losses for each MOSFET is given, the above equations can be used to calculate the values of $R_{ds(on)}$ and gate charge can be calculated using above equations, then the devices can be determined accordingly. The solution should ensure the MOSFET is within its maximum junction temperature at highest ambient temperature.

Output Capacitor

The output capacitors should be selected to meet both output ripple and transient response criteria. The output capacitor ESR causes output ripple V_{RIPPLE} during the inductor ripple current flowing in. To meet output ripple criteria, the ESR value should be:

$$R_{ESR} < \frac{L \cdot f_{OSC} \cdot V_{RIPPLE}}{V_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The output capacitor ESR also causes output voltage transient V_T during a transient load current I_T flowing in. To meet output transient criteria, the ESR value should be:

$$R_{ESR} < \frac{V_T}{I_T}$$

To meet both criteria, the smaller one of above two ESRs is required.

The output capacitor value also contributes to load transient response. Based on a worst case where the inductor energy 100% dumps to the output capacitor during the load transient, the capacitance then can be calculated by:

$$C > L \cdot \frac{I_T^2}{V_T^2}$$

POWER MANAGEMENT

Applications Information (Cont.)

Input Capacitor

The input capacitor should be chosen to handle the RMS ripple current of a synchronous buck converter. This value is given by:

$$I_{RMS} = \sqrt{(1-D) \cdot I_{IN}^2 + D \cdot (I_o - I_{IN})^2}$$

where I_o is the load current, I_{IN} is the input average current, and D is the duty cycle. Choosing low ESR input capacitors will help maximize ripple rating for a given size.

MOSFET for Linear Regulator

The MOSFET in linear regulator operates in linear region with really high power loss. A device with a suitable package has to be selected to handle the loss. To prevent too high load current during short circuit, the $R_{ds(on)}$ of the MOSFET should not be selected too low. A good choice is to select a MOSFET so that it is almost fully turned on at maximum load current. For example, in a LDO design with 3.3V in and 1.5V/2A out, a MOSFET with 600 to 800m-ohm $R_{ds(on)}$ can be chosen.

Bootstrap Circuit

The SC2621A uses an external bootstrap circuit to provide a voltage at BST pin for the top MOSFET drive. This voltage, referring to the Phase Node, is held up by a bootstrap capacitor. Typically, it is recommended to use a 1uF ceramic capacitor with 16V rating and a commonly available diode IN4148 for the bootstrap circuit.

Filters for Supply Power

For each pin of DRV and Vcc, it is recommended to use a 1uF/16V ceramic capacitor for decoupling. In addition, place a small resistor (10 ohm) in between Vcc pin and the supply power for noise reduction.

CONTROL LOOP DESIGN

The goal of compensation is to shape the frequency response characteristics of the buck converter to achieve a better DC accuracy and a faster transient response for the output voltage, while maintaining the loop stability.

The block diagram in Fig. 3 represents the control loop of a buck converter designed with the SC2621A. The control loop consists of a compensator, a PWM modulator, and a LC filter.

The LC filter and PWM modulator represent the small signal model of the buck converter operating at fixed

switching frequency. The transfer function of the model is given by:

$$\frac{V_o}{V_c} = \frac{V_{IN}}{V_m} \cdot \frac{1 + sR_{ESR}C}{1 + sL/R + s^2LC}$$

where V_{IN} is the power rail voltage, V_m is the amplitude of the 500kHz ramp, and R is the equivalent load.

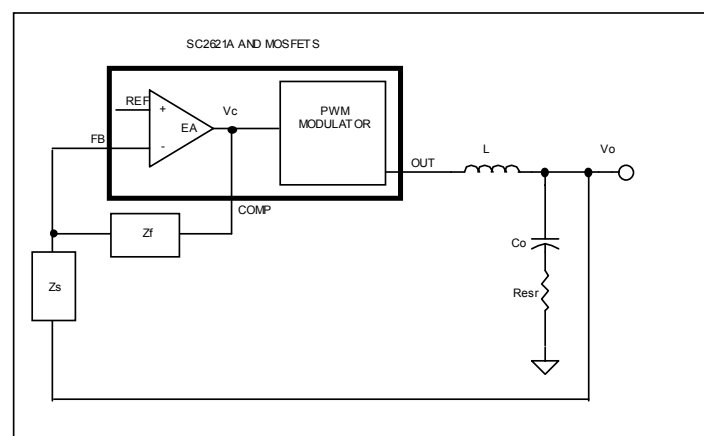


Fig. 3. Block diagram of the control loop

The model is a second order system with a finite DC gain, a complex pole pair at F_o , and an ESR zero at F_z , as shown in Fig. 4. The locations of the poles and zero are determined by:

$$F_o = \frac{1}{\sqrt{LC}}$$

$$F_z = \frac{1}{R_{ESR}C}$$

The compensator in Fig. 3 includes an error amplifier and impedance networks Z_f and Z_s . It is implemented by the circuit in Fig. 5. The compensator provides an integrator, double poles and double zeros. As shown in Fig. 4, the integrator is used to boost the gain at low frequency. Two zeros are introduced to compensate excessive phase lag at the loop gain crossover due to the integrator (-90deg) and complex pole pair (-180deg). Two high frequency poles are designed to compensate the ESR zero and attenuate high frequency noise.

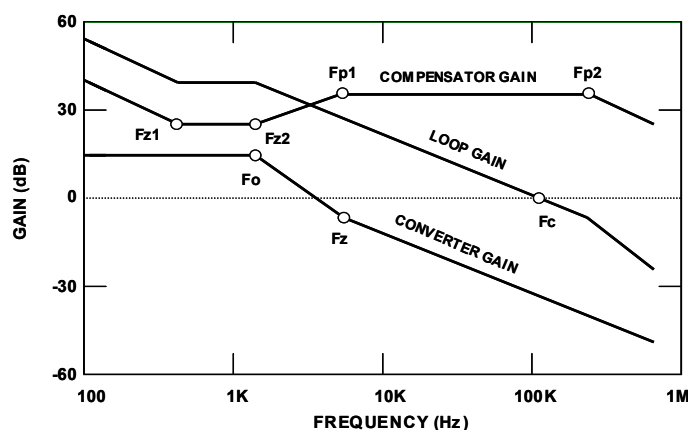


Fig. 4. Bode plots for control loop design

(2). Select the open loop crossover frequency F_c located at 10% to 20% of the switching frequency. At F_c , find the required DC gain.

(3). Use the first compensator pole F_{p1} to cancel the ESR zero F_z .

(4). Have the second compensator pole F_{p2} at half the switching frequency to attenuate the switching ripple and high frequency noise.

(5). Place the first compensator zero F_{z1} at or below 50% of the power stage resonant frequency F_o .

(6). Place the second compensator zero F_{z2} at or below the power stage resonant frequency F_o .

A MathCAD program is available upon request for the calculation of the compensation parameters.

LAYOUT GUIDELINES

The switching regulator is a high di/dt power circuit. Its Printed Circuit Board (PCB) layout is critical. A good layout can achieve an optimum circuit performance while minimizing the component stress, resulting in better system reliability. During PCB layout, the SC2621A controller, MOSFETs, inductor, and power decoupling capacitors have to be considered as a unit.

The following guidelines are typically recommended for using the SC2621A controller.

(1). Place a 4.7 μ F to 10 μ F ceramic capacitor close to the drain of top MOSFET for the high frequency and high current decoupling. The loop formed by the capacitor, the top and bottom MOSFETs must be as small as possible. Keep the input bulk capacitors close to the drain of the top MOSFETs.

(2). Place the SC2621A over a quiet ground plane to avoid pulsing current noise. Keep the ground return of the gate drive short.

(3). Connect bypass capacitors as close as possible to the decoupling pins (DRV and Vcc) to the ground pin GND. The trace length of the decoupling capacitor on DRV pin should be no more than 0.2" (5mm).

(4). Locate the components of the bootstrap circuit close to the SC2621A.

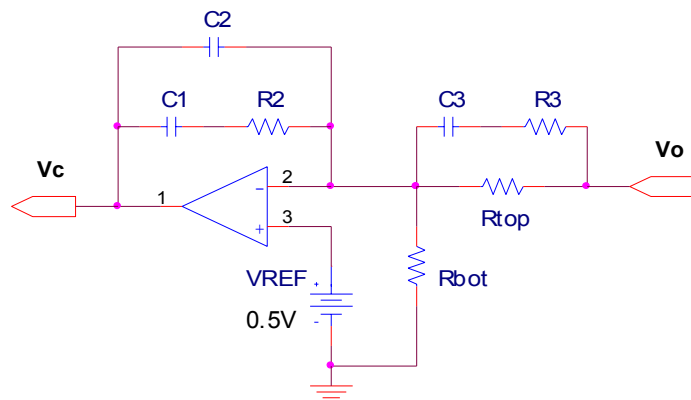


Fig. 5. Compensation network

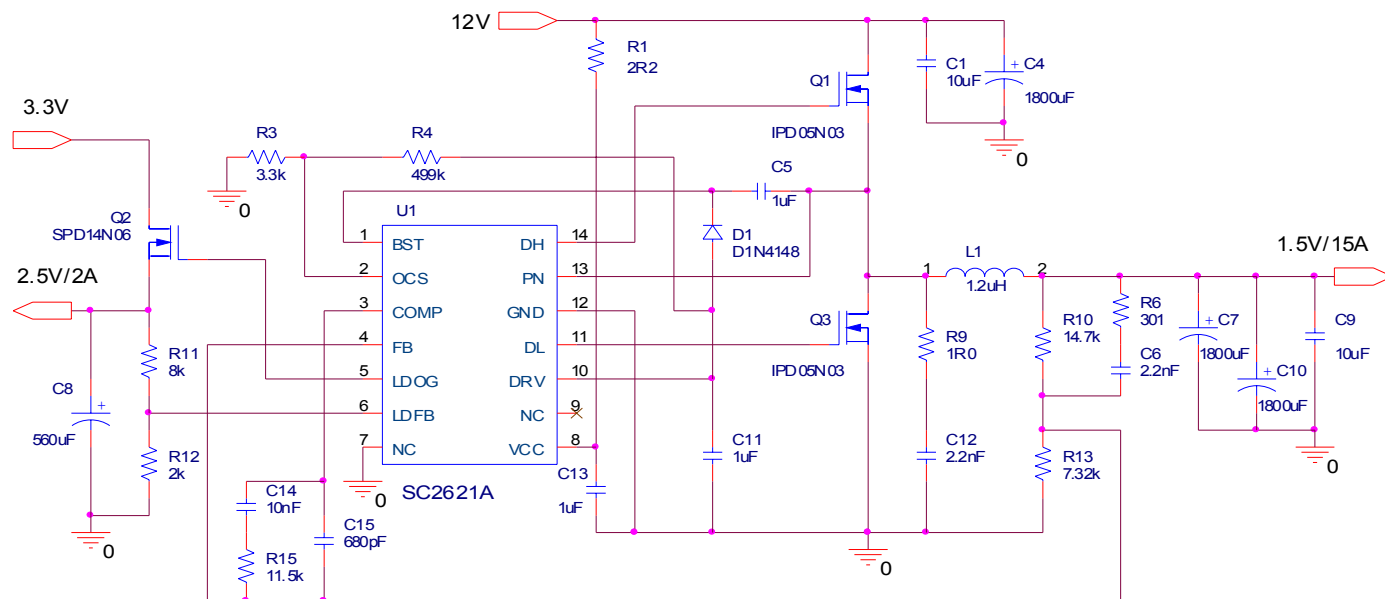
The top resistor R_{top} of the voltage divider in Fig. 5 can be chosen from 1k to 5k. Then the bottom resistor R_{bot} is found from:

$$R_{bot} = \frac{0.5V}{V_o - 0.5V} \cdot R_{top}$$

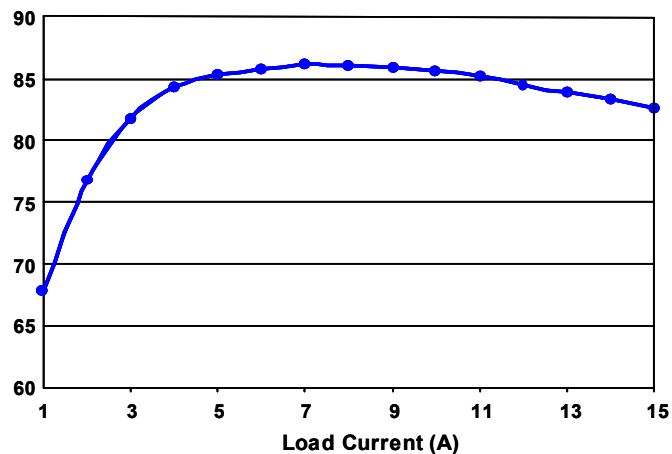
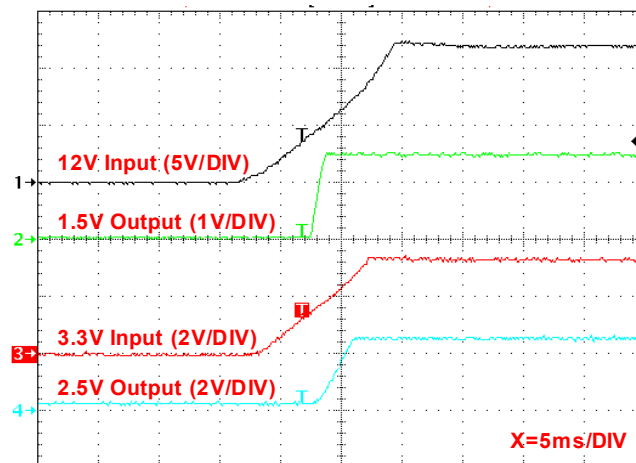
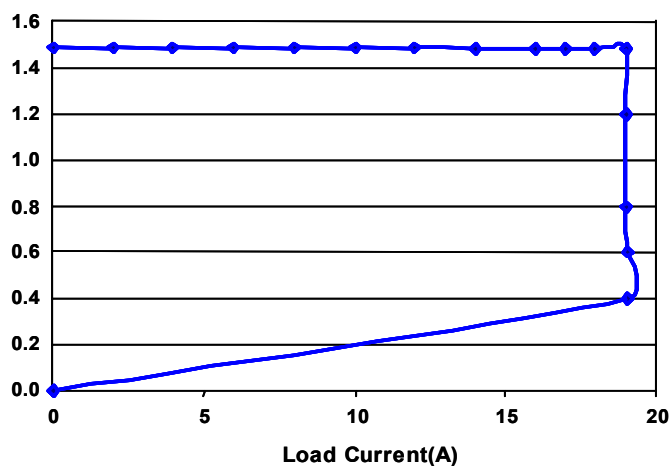
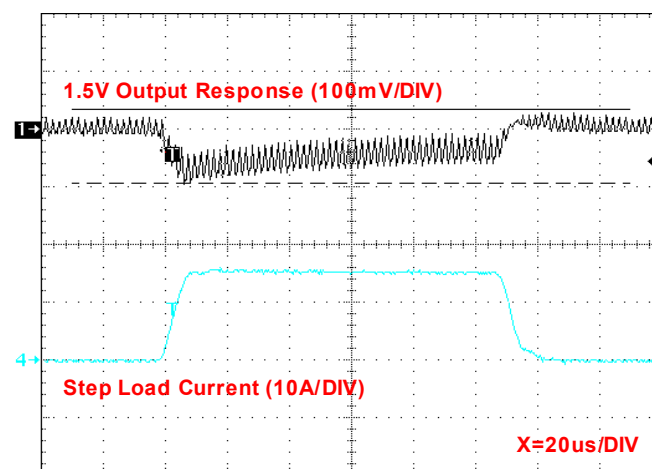
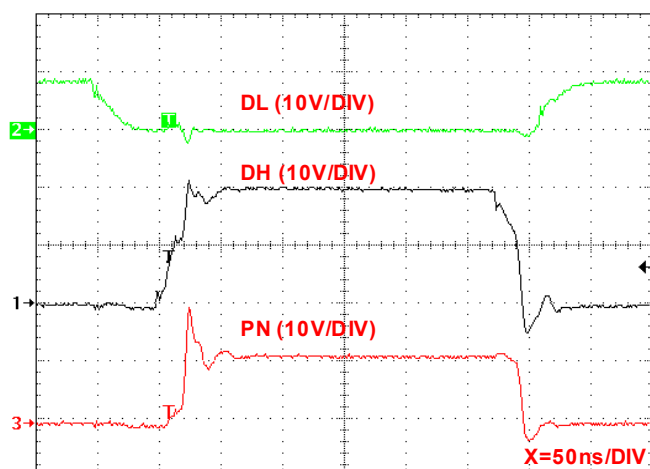
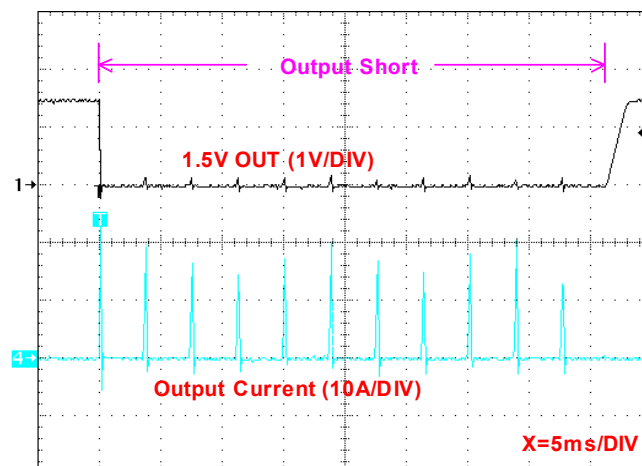
where 0.5V is the internal reference voltage of the SC2621A.

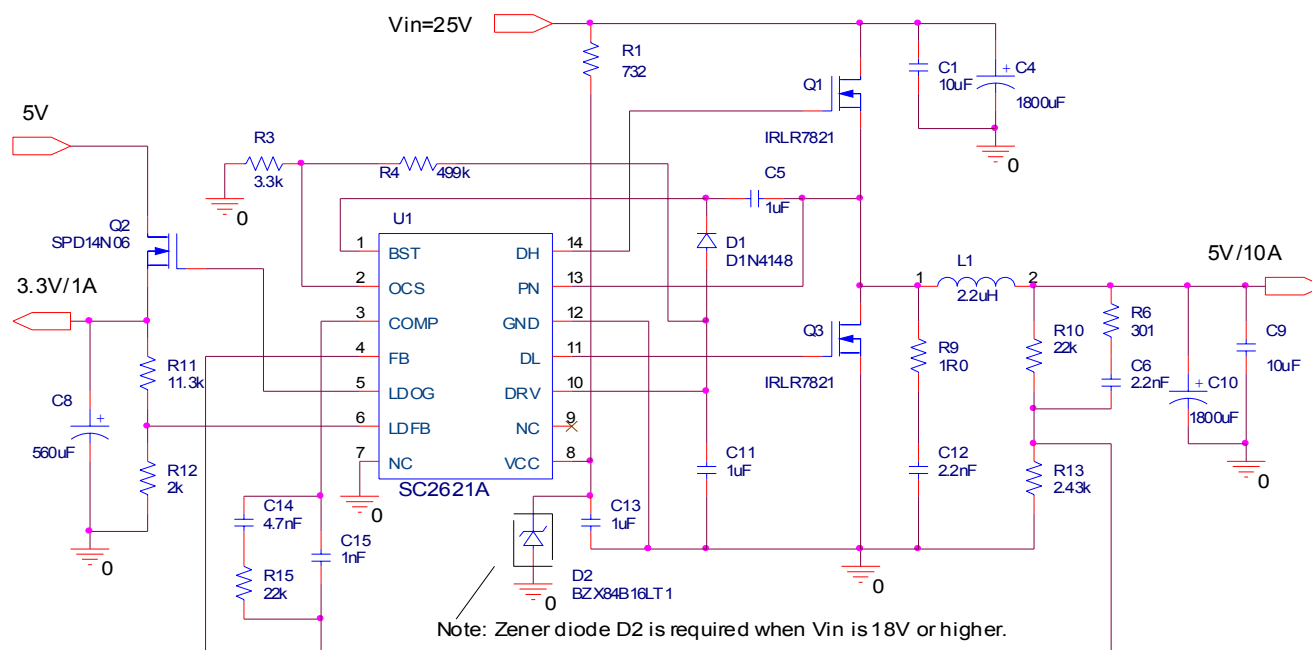
The other components of the compensator can be calculated using following design procedure:

(1). Plot the converter gain, including LC filter and PWM modulator.

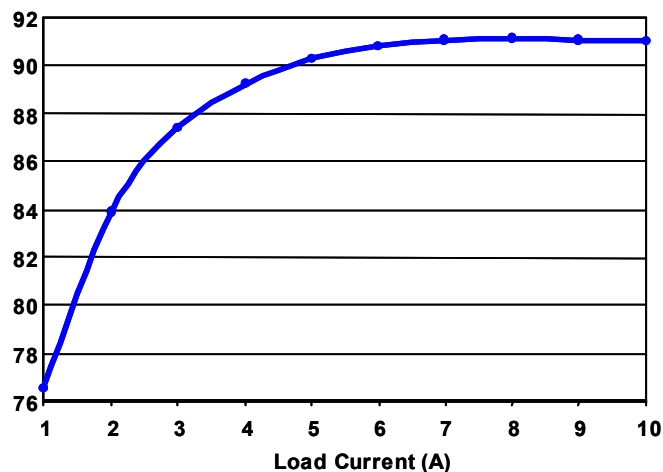
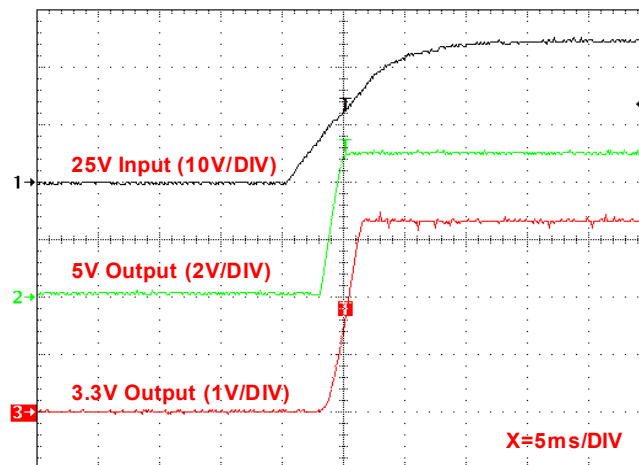
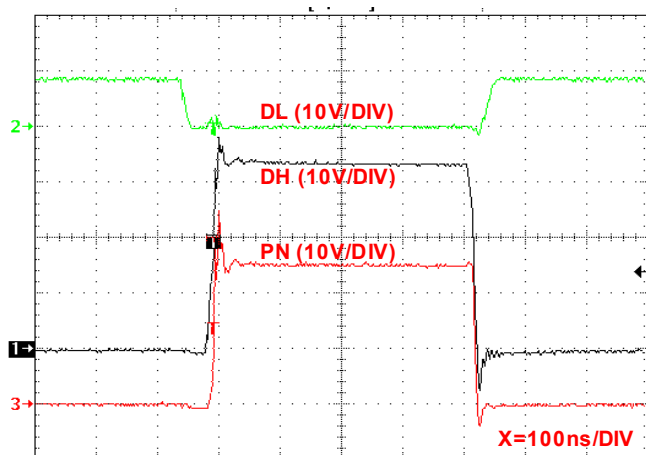
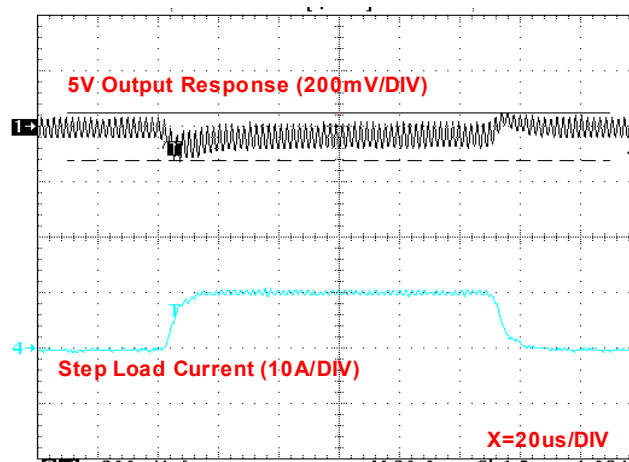
POWER MANAGEMENT
Applications Information (Cont.)
Typical Application Schematics for PCI-Express with 12V Input

Bill of Materials (12V Input)

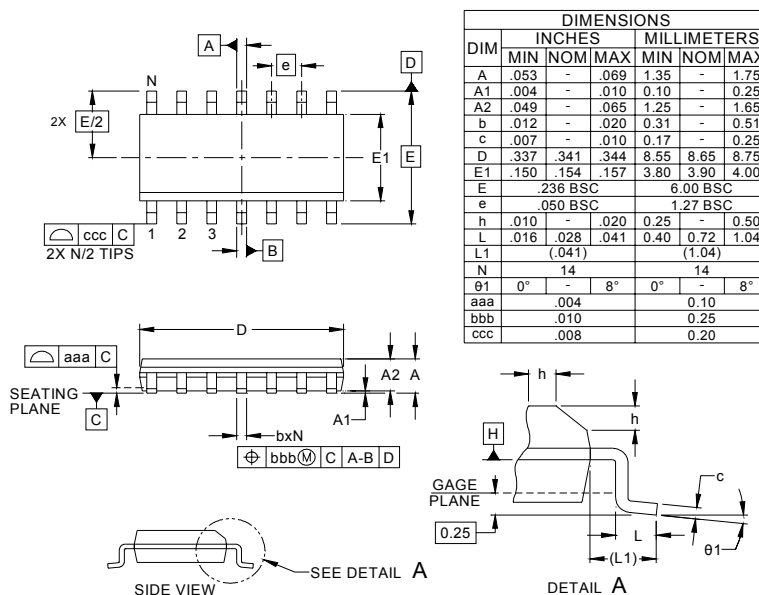
| Item | Quantity | Reference | Part | Vendor |
|------|----------|------------|-------------|---------------------|
| 1 | 1 | C1 | 10uF/16V | Vishay |
| 2 | 1 | C9 | 10uF/6.3V | Vishay |
| 3 | 1 | C4 | 1800uF/16V | Rubycon, MBZ |
| 4 | 2 | C7,C10 | 1800uF/6.3V | Rubycon, MBZ |
| 5 | 3 | C5,C11,C13 | 1uF | Vishay |
| 6 | 1 | C6 | 2.2nF | Vishay |
| 7 | 1 | C8 | 560uF | Sanyo |
| 8 | 1 | C12 | 2.2nF | Vishay |
| 9 | 1 | C14 | 10nF | Vishay |
| 10 | 1 | C15 | 680pF | Vishay |
| 11 | 1 | D1 | D1N4148 | Any |
| 12 | 1 | L1 | 1.2uH | Cooper Electr. Tech |
| 13 | 2 | Q3,Q1 | IPD05N03 | Infineon |
| 14 | 1 | Q2 | SPD14N06 | Infineon |
| 15 | 1 | R1 | 2R2 | Vishay |
| 16 | 1 | R3 | 3.3k | Vishay |
| 17 | 1 | R4 | 499k | Vishay |
| 18 | 1 | R6 | 301 | Vishay |
| 19 | 1 | R9 | 1R0 | Vishay |
| 20 | 1 | R10 | 14.7k | Vishay |
| 21 | 1 | R11 | 8k | Vishay |
| 22 | 1 | R12 | 2k | Vishay |
| 23 | 1 | R13 | 7.32k | Vishay |
| 24 | 1 | R15 | 11.5k | Vishay |
| 25 | 1 | U1 | SC2621A | SEMTECH |

Performance Characteristics (12V Input)
Efficiency (%) vs Load Current

Start up

Load Characteristics (Output vs Load Current)

Transient Response

Gate Waveforms (Io=15A)

Short Circuit Protection


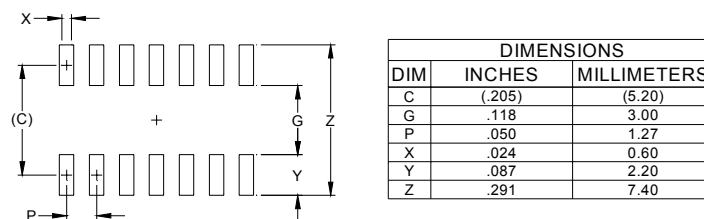
POWER MANAGEMENT
Applications Information (Cont.)
Typical Application Schematics with 25V Input

Bill of Materials (25V Input)

| Item | Quantity | Reference | Part | Vendor |
|------|----------|------------|-------------|---------------------|
| 1 | 1 | C1 | 10uF/35V | Murata |
| 2 | 1 | C9 | 10uF/6.3V | Vishay |
| 3 | 1 | C4 | 1500uF/35V | Rubycon |
| 4 | 1 | C10 | 1500uF/6.3V | Rubycon, MBZ |
| 5 | 3 | C5,C11,C13 | 1uF | Vishay |
| 6 | 1 | C6,C12 | 2.2nF | Vishay |
| 7 | 1 | C8 | 560uF | Sanyo |
| 8 | 1 | C14 | 4.7nF | Vishay |
| 9 | 1 | C15 | 1nF | Vishay |
| 10 | 1 | D1 | D1N4148 | Any |
| 11 | 1 | D2 | BZX84B16LT1 | ON Semi |
| 12 | 1 | L1 | 2.2uH | Cooper Electr. Tech |
| 13 | 2 | Q3,Q1 | IRLR7821 | IR |
| 14 | 1 | Q2 | SPD14N06 | Infineon |
| 15 | 1 | R1 | 732 | Vishay |
| 16 | 1 | R3 | 3.3k | Vishay |
| 17 | 1 | R4 | 499k | Vishay |
| 18 | 1 | R6 | 301 | Vishay |
| 19 | 1 | R9 | 1R0 | Vishay |
| 20 | 1 | R10,R15 | 22k | Vishay |
| 21 | 1 | R11 | 11.3k | Vishay |
| 22 | 1 | R12 | 2k | Vishay |
| 23 | 1 | R13 | 2.43k | Vishay |
| 24 | 1 | U1 | SC2621A | SEMTECH |

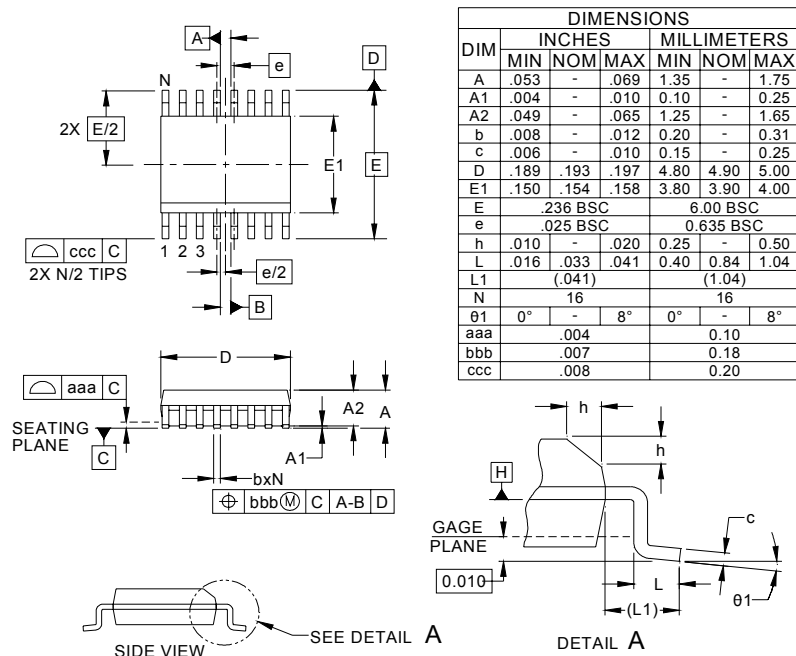
Performance Characteristics (25V Input)
Efficiency (%) vs Load Current

Start up

Gate Waveforms (I_o=10A)

Transient Response


POWER MANAGEMENT
Outline Drawing - SO-14

NOTES:

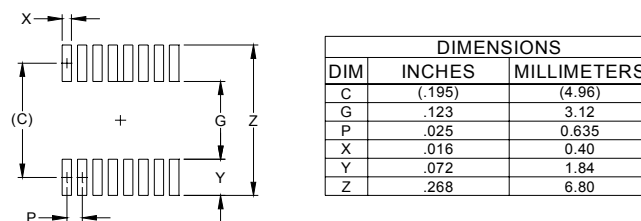
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **[A-]** AND **[B-]** TO BE DETERMINED AT DATUM PLANE **[H-]**.
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AB.

Land Pattern - SO-14

NOTES:

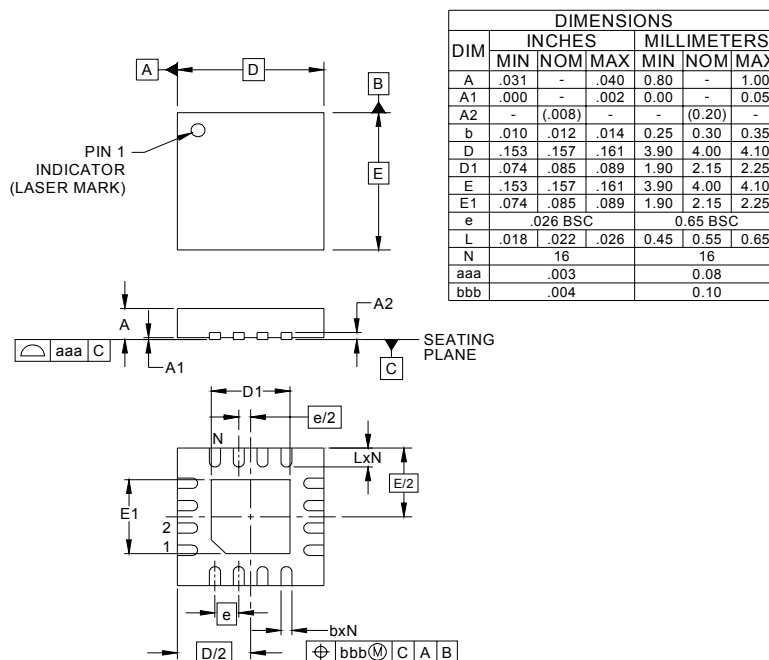
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 302A.

Outline Drawing - QSOP-16

NOTES:

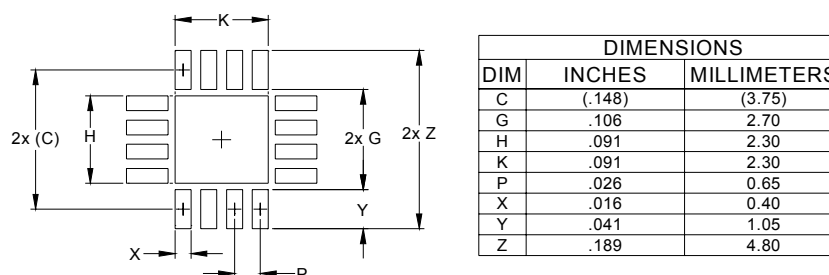
1. CONTROLLING DIMENSIONS ARE IN INCHES (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-137, VARIATION AB.

Land Pattern - QSOP-16

NOTES:

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POWER MANAGEMENT
Outline Drawing - MLP-16

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLP-16

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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