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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

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DESCRIPTION

R8A66160 is a LED array driver having a 16-bit serial input and parallel output shift register function with direct coupled reset input and output latch function.

This product guarantees the output current of 24mA ($V_{CC}=5V$ case) which is sufficient for cathode common LED drive, capable of following 16-bits continuously at the same time. Parallel output is open drain output. In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products. Furthermore, pin layout ensures the realization of an easy printed circuit. R8A66160 is the succession product of M66310.

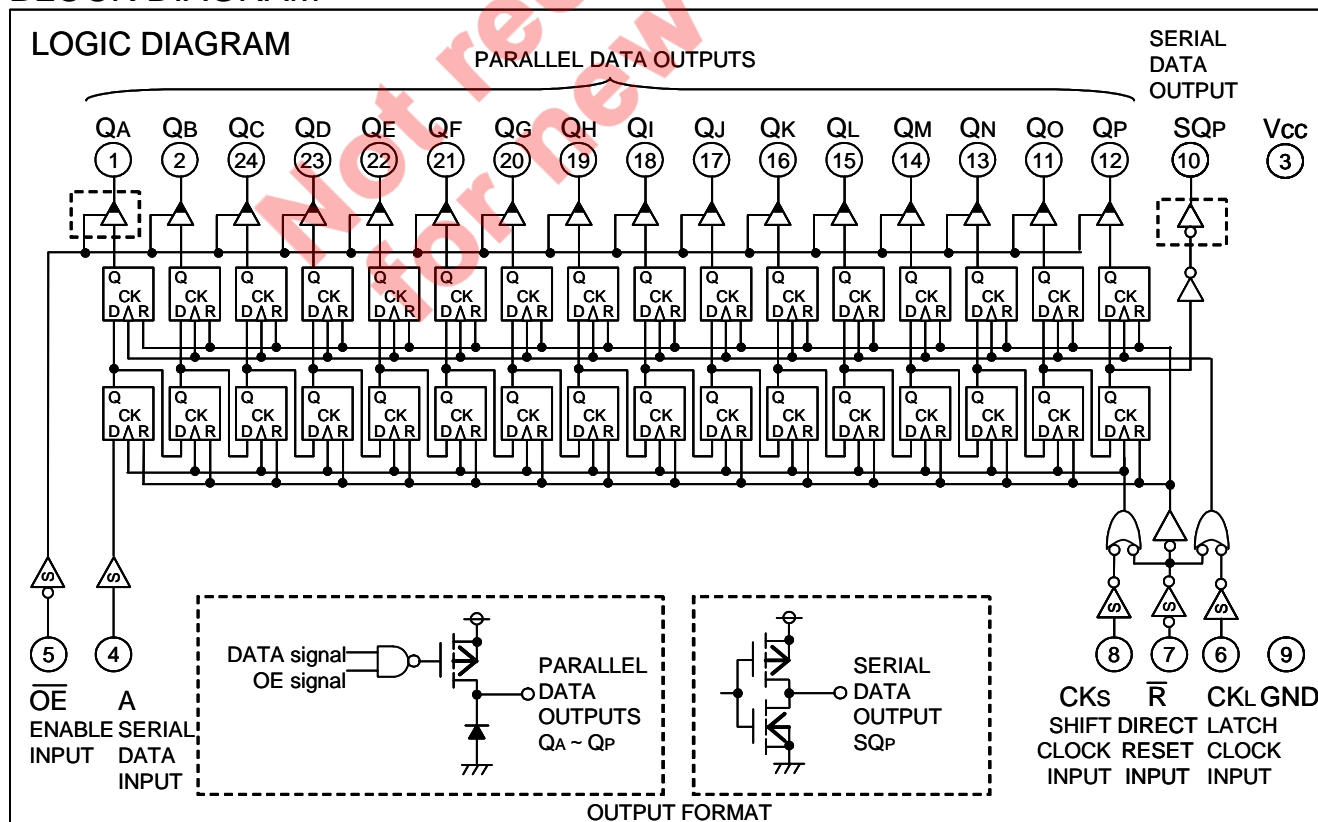
FEATURES

- Cathode common LED drive
- V_{CC} 5V or 3.3V single power supply
- High output current: all parallel outputs $Q_A \sim Q_P$ $I_{OH} = -24mA$ (at $V_{CC} = 5.0V$) $I_{OH} = -12mA$ (at $V_{CC} = 3.3V$) simultaneous lighting available
- Low power dissipation: 100uW/package (max) ($V_{CC}=5.0V$, $T_a=25^\circ C$, quiescent state)
- High noise margin: Schmitt input circuit provides responsiveness to a long line length
- Equipped with direct-coupled reset
- Open drain output: (except serial data output SQP)
- Wide operating temperature range: $T_a = -40^\circ C \sim +85^\circ C$
- Pin layout facilitates printed circuit wiring. (This layout facilitates cascade connection and LED connection)

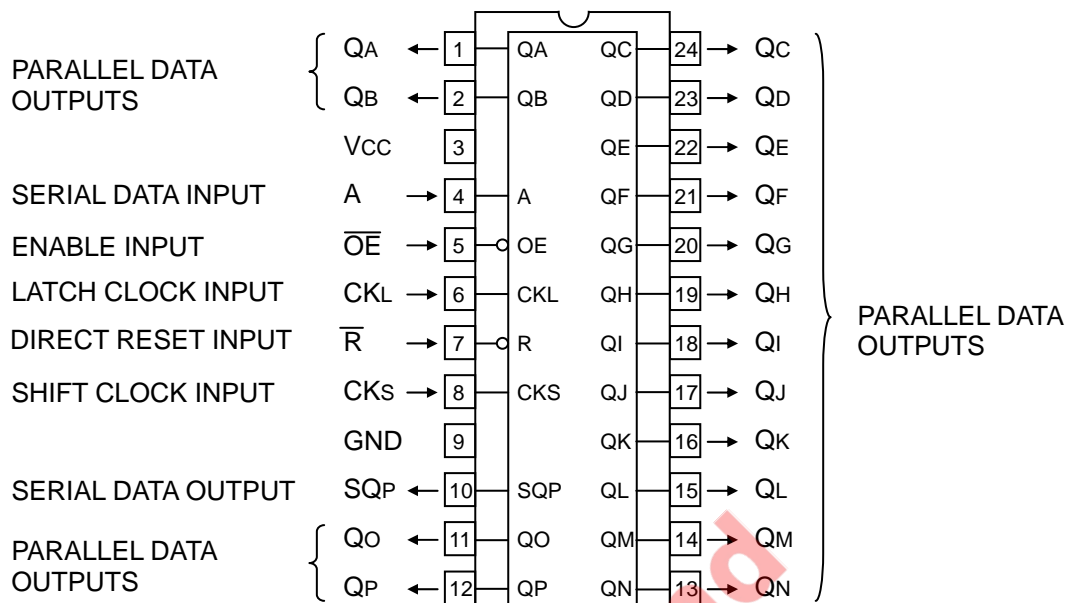
APPLICATION

- LED array drive, The various LED display modules
- PPC, Printer, VCR, Mini-compo, Button-Telephone etc. All of LED display equipment

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



FUNCTIONAL DESCRIPTION

As R8A66160 uses silicon gate CMOS process. It realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shift register consists of two flip-flop having independent clocks for shifting and latching.

As for clock input, shift clock input CKs and latch clock input CKL are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shift register and the signal of A shifts shifting registers one by one when a pulse is impressed to CKs. When A is "L", the signal of "L" shifts.

When the pulse is impressed to CKL, the contents of the shifting register at that time are stored in a latching register, and they appear in the parallel data outputs from QA ~ QP.

Outputs QA ~ QP are open drain outputs.

To extend the number of bits, use the serial data output SGP which shows the output of the shifting register of the 16th bit.

When reset input \overline{R} is changed to "L", QA ~ QP and SGP are reset. In this case, shifting and latching register are reset.

If "H" is impressed to output enable input \overline{OE} , QA ~ QP reaches the high impedance state, but SGP does not reach the high impedance state. Furthermore, change in OE does not affect shift operation.

FUNCTION TABLE (Note: 1)

Operation mode		Input					Parallel data output																Serial data output SGP	Remarks
		\overline{R}	CKs	CKL	A	\overline{OE}	QA	QB	QC	QD	QE	QF	QG	QH	QI	QJ	QK	QL	QM	QN	QO	QP		
Reset		L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	L	—
Shift Latch operation	Shift t ₁	H		X	H	L	Q ⁰ _A	Q ⁰ _B	Q ⁰ _C	Q ⁰ _D	Q ⁰ _E	Q ⁰ _F	Q ⁰ _G	Q ⁰ _H	Q ⁰ _I	Q ⁰ _J	Q ⁰ _K	Q ⁰ _L	Q ⁰ _M	Q ⁰ _N	Q ⁰ _O	Q ⁰ _P	q ⁰	Output lighting "H"
	Latch t ₂	H	X		X	L	H	q ⁰ _A	q ⁰ _B	q ⁰ _C	q ⁰ _D	q ⁰ _E	q ⁰ _F	q ⁰ _G	q ⁰ _H	q ⁰ _I	q ⁰ _J	q ⁰ _K	q ⁰ _L	q ⁰ _M	q ⁰ _N	q ⁰ _O	q ⁰	
	Shift t ₁	H		X	L	L	Q ⁰ _A	Q ⁰ _B	Q ⁰ _C	Q ⁰ _D	Q ⁰ _E	Q ⁰ _F	Q ⁰ _G	Q ⁰ _H	Q ⁰ _I	Q ⁰ _J	Q ⁰ _K	Q ⁰ _L	Q ⁰ _M	Q ⁰ _N	Q ⁰ _O	Q ⁰ _P	q ⁰	Output lights-out "L"
	Latch t ₂	H	X		X	L	Z	q ⁰ _A	q ⁰ _B	q ⁰ _C	q ⁰ _D	q ⁰ _E	q ⁰ _F	q ⁰ _G	q ⁰ _H	q ⁰ _I	q ⁰ _J	q ⁰ _K	q ⁰ _L	q ⁰ _M	q ⁰ _N	q ⁰ _O	q ⁰ _P	q ⁰
Output disable		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q ⁰ _P	—

Note1: : Change from low-level to high-level

Q⁰ : Output state Q before CKL changed

X : Irrelevant

q⁰ : Contents of shift register before CKs changed

q : Contents of shift register

t₁, t₂ : t₂ is set after t₁ is set

Z : High Impedance

ABSOLUTE MAXIMUM RATINGS (Ta=-40~+85°C, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
VCC	Supply voltage			-0.5 ~ +7.0	V
VI	Input voltage			-0.5 ~ VCC+0.5	V
VO	Output voltage			-0.5 ~ VCC+0.5	V
IO	Output current per output pin	QA ~ QP		-50	mA
		SQP		±25	
ICC	Supply / GND current		VCC, GND	-410, +20	mA
Pd	Power dissipation		(Note 2)	500	mW
Tstg	Storage temperature range			-65 ~+150	°C

Note 2: R8A66160SP; Ta=-40~+70°C, Ta=+70~+85°C are derated at -6mW/°C.

RECOMMENDED OPERATING CONDITIONS (Ta=-40~+85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VCC	Supply voltage	5.0V support	4.5	5.0	5.5	V
		3.3V support	3.0	3.3	3.6	V
VI	Input voltage		0		VCC	V
VO	Output voltage		0		VCC	V
Topr	Operating temperature range		-40		+85	°C

Not recommended
for new design

ELECTRICAL CHARACTERISTICS

■5.0V version support specifications (Ta=-40~+85°C, Vcc=4.5V~5.5V, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
VT+	Positive-going threshold voltage		VO=0.1V, VCC=0.1V IO =20uA		0.35xVCC		0.70xVCC	V
VT-	Negative-going threshold voltage		VO=0.1V, VCC=0.1V IO =20uA		0.20xVCC		0.55xVCC	V
VOH	High-level output voltage	QA ~ QP	VI=VT+, VT- VCC=4.5V (Note3)	IOH= -20uA	VCC-0.1			V
				IOH= -24mA	3.66			
				IOH= -40mA	3.25			
VOH	High-level output voltage	SQP	VI=VT+, VT- VCC=4.5V	IOH= -20uA	VCC-0.1			V
				IOH= -4mA	3.66			
VOL	Low-level output voltage	SQP	VI=VT+, VT- VCC=4.5V	IOL= 20uA			0.10	V
				IOL= 4mA			0.53	
IIH	High-level input current		VI=VCC, VCC=5.5V				5	uA
IIL	Low-level input current		VI=GND, VCC=5.5V				-5	uA
IO	Maximum output leakage current	QA ~ QP	VI=VT+, VT- VCC=5.5V	VO=VCC			10	uA
				VO=GND			-10	
ICC	Quiescent supply current		VI=VCC,GND, VCC=5.5V				200	uA

Note 3: R8A66160 is used under the condition of an output current IOH=-40mA, the number of simultaneous drive outputs is restricted as shown in the Duty Cycle – IOH of TYPICAL CHARACTERISTICS.

■3.3V version support specifications (Ta=-40~+85°C, Vcc=3.0V~3.6V, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
VT+	Positive-going threshold voltage		VO=0.1V, VCC=0.1V IO =20uA		0.35xVCC		0.70xVCC	V
VT-	Negative-going threshold voltage		VO=0.1V, VCC=0.1V IO =20uA		0.20xVCC		0.55xVCC	V
VOH	High-level output voltage	QA ~ QP	VI=VT+, VT- VCC=3.0V	IOH= -20uA	VCC-0.1			V
				IOH= -12mA	2.34			
				IOH= -20mA	2.08			
VOH	High-level output voltage	SQP	VI=VT+, VT- VCC=3.0V	IOH= -20uA	VCC-0.1			V
				IOH= -2mA	2.60			
VOL	Low-level output voltage	SQP	VI=VT+, VT- VCC=3.0V	IOL= 20uA			0.10	V
				IOL= 2mA			0.40	
IIH	High-level input current		VI=VCC, VCC=3.6V				5	uA
IIL	Low-level input current		VI=GND, VCC=3.6V				-5	uA
IO	Maximum output leakage current	QA ~ QP	VI=VT+, VT- VCC=3.6V	VO=VCC			10	uA
				VO=GND			-10	
ICC	Quiescent supply current		VI=VCC,GND, VCC=3.6V				200	uA

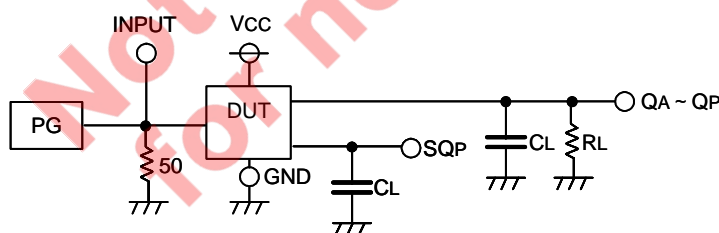
SWITCHING CHARACTERISTICS (Ta=-40~+85°C, Vcc=5.0V or 3.3V)

Symbol	Parameter		Test conditions	5.0V specification			3.3V specification			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
fmax	Maximum clock frequency		CL=50pF RL=1KΩ (Note 4)			4			3.3	MHz
tPLH	Output "L"-"H" and "H"-"L" propagation time	CKS - SQP				125			150	ns
tPHL		CKS - SQP				125			150	ns
tPHL	Output "H"-"L" propagation time	\overline{R} - SQP				125			150	ns
tPHZ		\overline{R} - QA ~ QP (turned off)				200			220	ns
tPZH	Output "Z"-"H" propagation time	CKL - QA ~ QP (turned on)				125			150	ns
tPHZ		CKL - QA ~ QP (turned off)				200			220	ns
tPZH	Output "Z"-"H" propagation time	\overline{OE} - QA ~ QP (turned on)				125			150	ns
tPHZ		\overline{OE} - QA ~ QP (turned off)				200			220	ns
CI	Input capacitance					10			10	pF

TIMING REQUIREMENTS (Ta=-40~+85°C, Vcc=5.0V or 3.3V)

Symbol	Parameter	Test conditions	5.0V specification			3.3V specification			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
tw	CKS, CKL, \overline{R} pulse width	(Note 4)	125			150			ns
tsu	A setup time with respect to CKS		125			150			ns
tsu	CKS setup time with respect to CKL		125			150			ns
th	A hold time with respect to CKS		15			20			ns
trec	\overline{R} recovery time with respect to CKS, CKL		70			80			ns

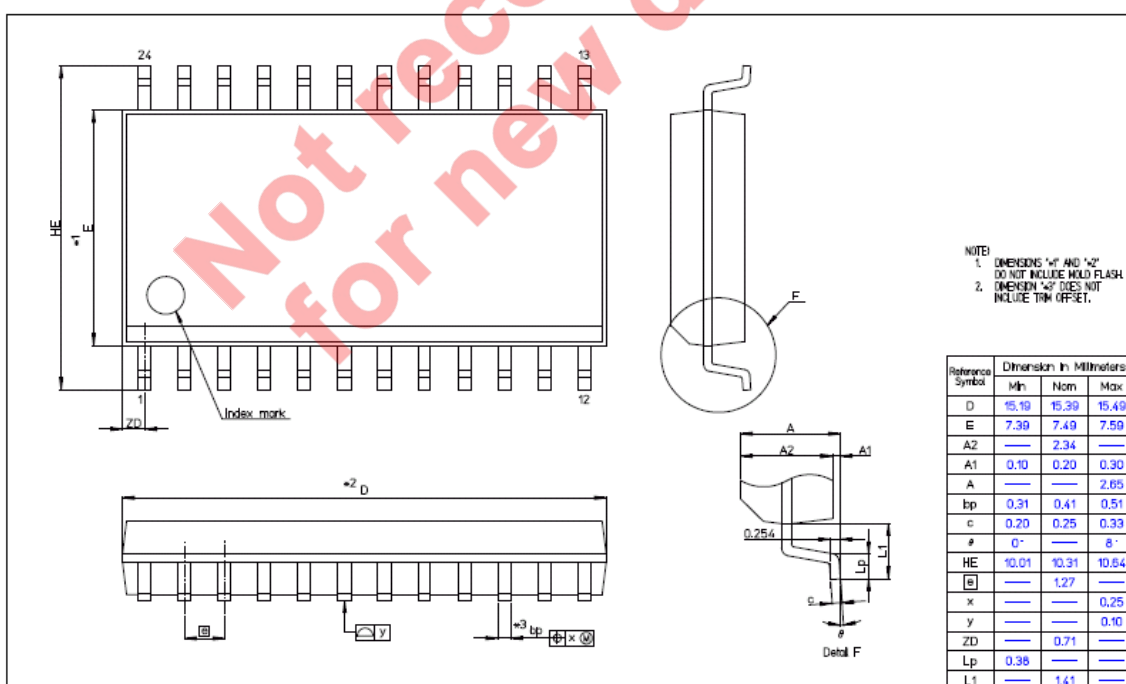
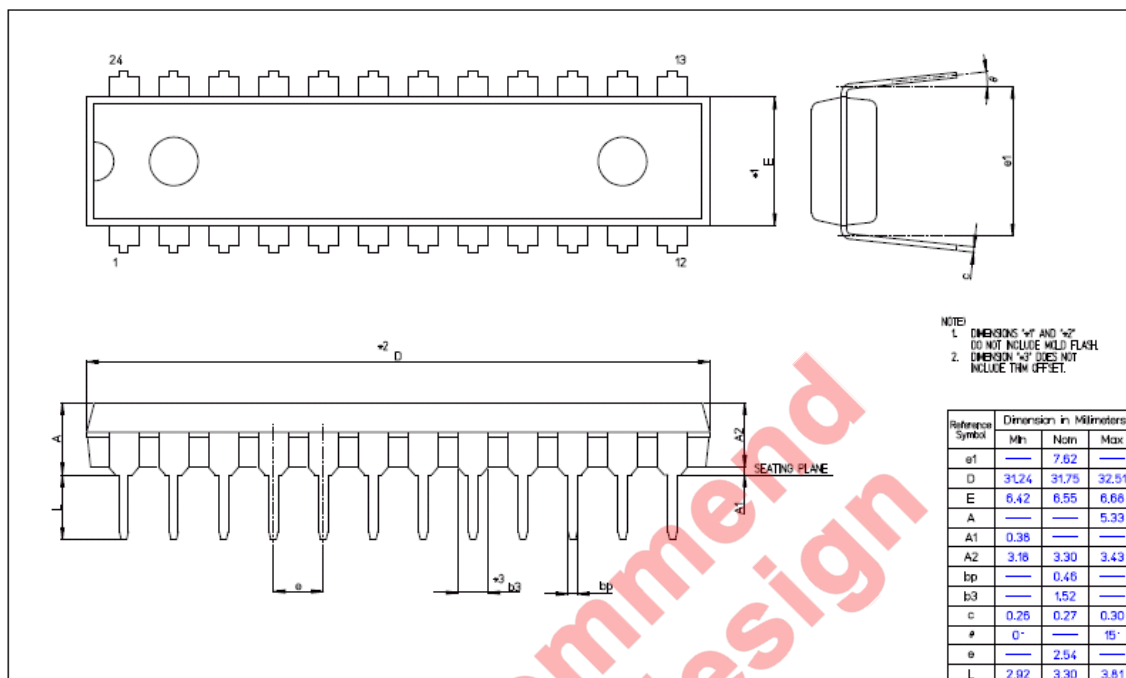
Note4 : Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%) : tr=6ns,tf=6ns
- (2) The capacitance CL includes stray wiring capacitance and the probe input capacitance.

PACKAGE OUTLINE

Product name	Package	RENESAS Code	Previous Code
R8A66160DD	24pin DIP	PRDP0024AF-A	24P4X-A
R8A66160SP	24pin SOP	PRSP0024DF-A	24P2X-B



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