9-BIT ECL-TO-TTL WITH 3-STATE ENABLE

SY10H601
SY100H601

FEATURES

- **9-bit ideal for byte-parity applications**
- **3-state TTL outputs**
- **Flow-through configuration**
- **Extra TTL and ECL power/ground pins to minimize switching noise**
- **ECL and TTL 3-state control inputs**
- **4.8ns max. delay into 50pF, 9.6ns into 200pF (all outputs switching)**
- **PNP TTL inputs for low loading**
- **Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)**
- **Fully compatible with MC10H/100H601**
- **Available in 28-pin PLCC package**

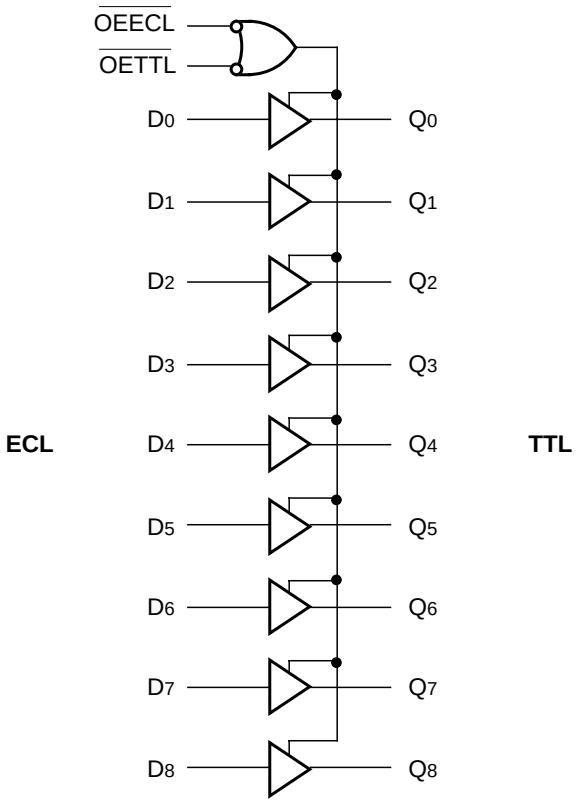
DESCRIPTION

The SY10/100H601 are 9-bit, dual supply ECL-to-TTL translators. Devices in the Micrel 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The devices feature a 48mA TTL output stage and AC performance is specified into both a 50pF and 200pF load capacitance. For the 3-state output disable, both ECL and TTL control inputs are provided, allowing maximum design flexibility.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

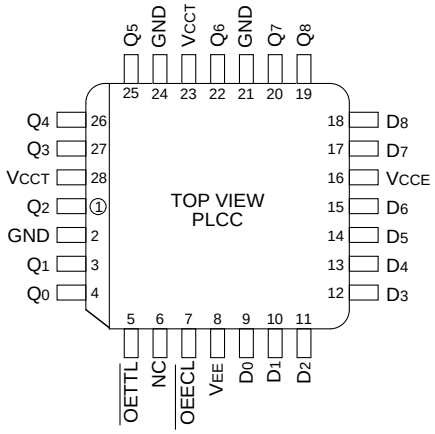
BLOCK DIAGRAM



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
V_{CCE}	ECL V_{CC} (0V)
V_{CCT}	TTL Supply (+5.0V)
V_{EE}	ECL Supply (–5.2/–4.5V)
D_0–D_8	Data Inputs (ECL)
Q_0–Q_8	Data Outputs (TTL)
$\overline{OEECL}$	3-State Control (ECL)
$\overline{OETTL}$	3-State Control (TTL)

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10H601JC	J28-1	Commercial	SY10H601JC	Sn-Pb
SY10H601JCTR[2]	J28-1	Commercial	SY10H601JC	Sn-Pb
SY100H601JC	J28-1	Commercial	SY100H601JC	Sn-Pb
SY100H601JCTR[2]	J28-1	Commercial	SY100H601JC	Sn-Pb
SY10H601JZ[3]	J28-1	Commercial	SY10H601JZ with Pb-Free bar-line indicator	Matte-Sn
SY10H601JZTR[2, 3]	J28-1	Commercial	SY10H601JZ with Pb-Free bar-line indicator	Matte-Sn
SY100H601JZ[3]	J28-1	Commercial	SY100H601JZ with Pb-Free bar-line indicator	Matte-Sn
SY100H601JZTR[2, 3]	J28-1	Commercial	SY100H601JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLE

$\overline{OEECL}$	$\overline{OETTL}$	D	Q
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

DC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –4.75V to –5.5V (10H Version); V_{EE} = –4.2V to –5.5V (100H Version)

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current, ECL	—	46	—	46	—	50	mA	—
I_{CCH} I_{CCL} I_{CCZ}	Power Supply Current, TTL	— — —	110 110 105	— — —	110 110 105	— — —	110 110 105	mA	—
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V
I_{OZH}	Output Disable Current HIGH	—	50	—	50	—	50	µA	V_{OUT} = 2.7V
I_{OZL}	Output Disable Current LOW	—	–50	—	–50	—	–50	µA	V_{OUT} = 0.5V

AC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –4.75V to –5.5V (10H Version); V_{EE} = –4.2V to –5.5V (100H Version)

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output	1.7 3.4	4.8 9.6	1.7 3.4	4.8 9.6	1.7 3.4	4.8 9.6	ns	C_L = 50pF C_L = 200pF
t_{PLZ} t_{PHZ}	Output Disable Time, $\overline{OEECL}$	3.7 5.4	6.5 13	3.7 5.4	6.5 13	3.7 5.4	6.5 13	ns	C_L = 50pF C_L = 200pF
t_{PLZ} t_{PHZ}	Output Disable Time, $\overline{OETTL}$	4.3 7.0	7.5 15	4.3 7.0	7.5 15	4.3 7.0	7.5 15	ns	C_L = 50pF C_L = 200pF
t_{PZL} t_{PZH}	Output Enable Time, $\overline{OEECL}$	3.5 5.0	6.0 12	3.5 5.0	6.0 12	3.5 5.0	6.0 12	ns	C_L = 50pF C_L = 200pF
t_{PZL} t_{PZH}	Output Enable Time, $\overline{OETTL}$	4.2 6.0	7.0 14	4.2 6.0	7.0 14	4.2 6.0	7.0 14	ns	C_L = 50pF C_L = 200pF
t_r t_f	Output Rise/Fall Time 1.0V – 2.0V	— —	1.2 3.0	— —	1.2 3.0	— —	1.2 3.0	ns	C_L = 50pF C_L = 200pF

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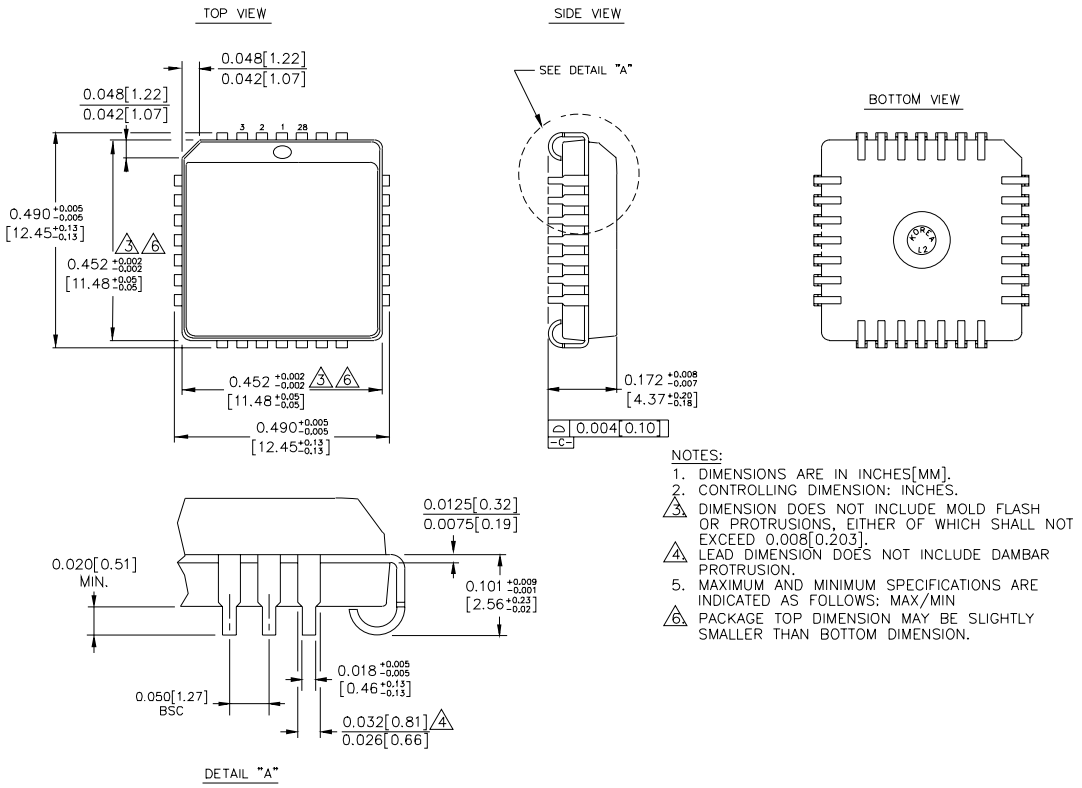

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