SC475A
Synchronous Buck Controller with Dual-Level VOUT Transition Support

POWER MANAGEMENT

Description

The SC475A is a versatile, constant on-time synchronous buck, pseudo-fixed-frequency, PWM controller intended for notebook computers and other battery operated portable devices. The SC475A contains all the features needed to provide cost-effective control of system elements needing voltage slewing. An integrated switch provides two resistor-programmable DC output voltages controlled by the G0 input.

The output voltage is adjustable from 0.75V to 5V. Additional features include cycle-by-cycle current limit, voltage soft-start, under-voltage protection, programmable over-current protection, soft shutdown, automatic power save and non-overlapping gate drive. The SC475A provides an enable input and a power good output which is automatically blanked during output voltage transitions.

The constant on-time topology provides fast dynamic response. The excellent transient response means that SC475A based solutions require less output capacitance than competing fixed-frequency converters. Switching frequency is constant until a step in load or line voltage occurs, at which time the pulse density and frequency will increase or decrease to counter the change in output voltage. After the transient event, the controller frequency returns to steady state operation. At light loads, the automatic power save mode reduces the SC475A frequency for improved efficiency.

Features

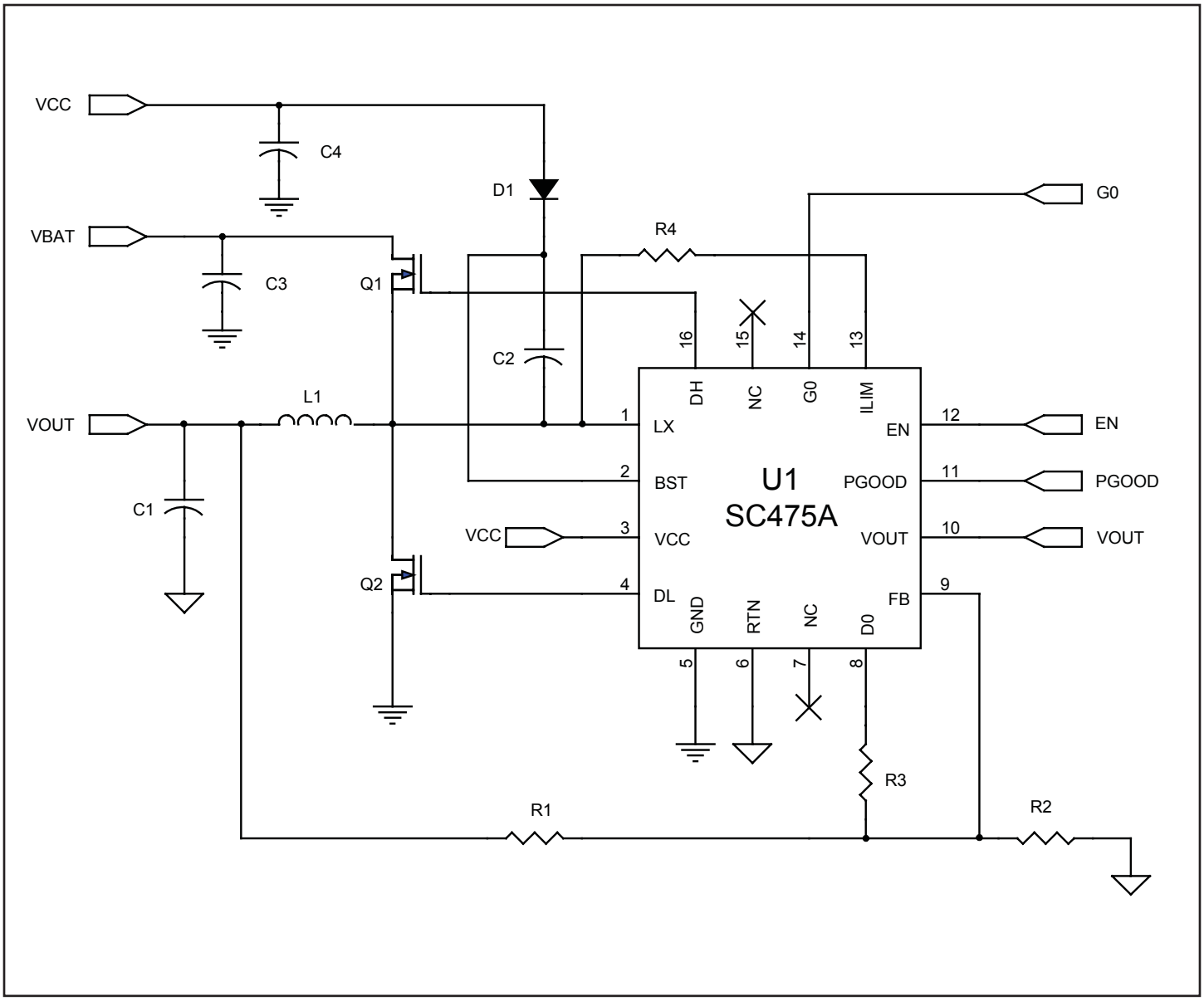
- V_{OUT} Programmable 0.75V to 5.25V with Integrated Transition Support
- V_{BAT} Range 3V to 25V
- Soft Shutoff at Output
- Current Sense Using Low-side $R_{DS(ON)}$ or Resistor Sensing
- Adjustable Cycle-by-Cycle Valley Current Limit
- 325kHz Fixed-Frequency
- Constant On-Time for Fast Dynamic Response and Reduced Output Capacitance
- Automatic Smart Power Save†
- Internal Soft-Start
- Over-Voltage/Under-Voltage Fault Protection
- Power Good Output with Transition Blanking
- 1µA Typical Shutdown Current
- 500µA Typical Operating Current
- Tiny 3×3mm, 16 Pin MLP Package
- Low External Part Count
- Industrial Temperature Range
- 0.85% Internal Reference
- 1A/3A Non-Overlapping Gate Drive with SmartDriver™ Technology
- High Efficiency > 90%
- Device is Fully WEEE and RoHS Compliant

†Patent Pending

Applications

- Notebook/Sub-Notebook Graphics Voltage Controllers
- Tablet PCs
- Embedded Applications

Typical Application Circuit



Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Min	Max	Units
DH, BST to GND (DC) DH, BST to GND (transient - 100nsec max)		-0.3 -2.0	+30 +33	V
DL to GND (DC) DL to GND (transient - 100nsec max)		-0.3 -2.0	+6.0 +6.0	V
LX to GND (DC) LX to GND (transient - 100nsec max)		-0.3 -2.0	+25 +28	V
BST to LX		-0.3	+6.0	V
RTN to GND		-0.3	+0.3	V
VCC to RTN		-0.3	+6.0	V
D0, EN, FB, G0, ILIM, PGOOD, VOUT to RTN		-0.3	VCC + 0.3	V
Operating Junction Temperature Range	T_J	-40	+125	°C
Storage Temperature Range	T_{STG}	-60	+150	°C
Thermal Resistance, Junction to Ambient(1)	θ_{JA}	45		°C/Watt
Peak IR Reflow Temperature, (10-40sec)	T_{PKG}		+260	°C
ESD Rating (Human Body Model)		2		kV

Note:

1) Calculated from package in still air, mounted 3" to 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Test Conditions: V_{BAT} = 15V, V_{OUT} = 1.5V, T_A = 25 °C, 0.1% resistor dividers; VCC = 5.0V.

Parameter	Conditions	25°C			-40° to 85°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VBAT Input Voltage		3.0		25			V
VCC Input Voltage		4.5		5.5			V
VCC Shutdown Current	EN = 0V		1			5	µA
VCC Operating Current	FB > 0.8V		500			1000	µA
Controller							
FB On-Time Threshold	0 to 85°C		0.75		0.7436	0.7564	V
	-40 to 85°C				0.7425	0.7575	
Output Voltage Adjust Range(1)					0.75	5.25	V
D0 Pull-Down Resistance	D0 to RTN; G0 = RTN		15			40	Ω

Electrical Characteristics *(continued)*

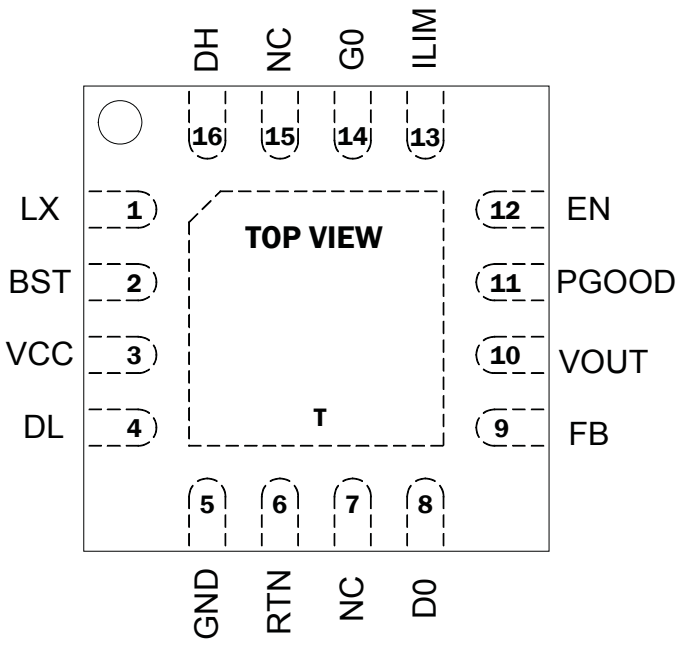
Parameter	Conditions	25°C			-40° to 85°C		Units
		Min	Typ	Max	Min	Max	
Regulation							
Line Regulation Error	Typical Application Circuit		0.04				%/V
Load Regulation Error	Typical Application Circuit		0.3				%
Timing							
On-Time	VOUT = 1.1V		250		225	275	ns
Minimum On-Time			100				ns
Minimum Off-Time			350				ns
Maximum Duty Cycle	$V_{BAT} = V_{OUT} + 0.2$ FB < 0.7V		85		80		%
Soft-Start							
Soft-Start Time	$I_{OUT} = I_{LIM}/2$		1000				µs
Analog Inputs/Outputs							
VOUT Input Resistance			500				kΩ
FB Input Bias Current					-1	+1	µA
Current Sense							
Zero Crossing Detector Threshold	LX - GND		0		-7	+7	mV
Power Good							
Power Good Threshold	1% Hysteresis Typical		-20%		-17%	-23%	V
Threshold Delay Time(1)			5				µs
Voltage Transition Blank Time(1)	G0 Transition		32				clks
Leakage						1	µA
Fault Protection							
ILIM Source Current			10		9	11	µA
ILIM Comparator Offset			0		-10	+10	mV
Current Limit (Negative)	LX - GND		80		60	100	mV
Output Under-Voltage Fault	FB with Respect to Nominal		-30		-35	-25	%

Electrical Characteristics *(continued)*

Parameter	Conditions	25°C			-40° to 85°C		Units
		Min	Typ	Max	Min	Max	
Fault Protection (continued)							
Steady-State Over-Voltage Fault	FB with Respect to Nominal		+20		+17	+23	%
Steady-State Over-Voltage Fault Delay	FB Forced 50mV Above Over-Voltage Fault Threshold		5				µs
G0 Transition Over-Voltage Fault	FB with Respect to Nominal; Valid for 32 cycles after G0 Transition		+50				%
Smart Power Save Threshold	FB with Respect to Nominal		+8				%
Over-Temperature Shutdown(1)	Latching, >10°C Hysteresis		160				°C
Logic Inputs/Outputs							
Logic Input High Voltage	EN, G0				1.2		V
Logic Input Low Voltage	EN, G0					0.4	V
EN Input Bias Current	EN = 5V				-1	+1	µA
G0 Input Bias Current	G0 = 5V		5		0	10	µA
Power Good Output Low Voltage	R_{PWRGD} = 10kΩ to VCC					0.4	V
Gate Drivers							
Shoot-Through Protection Delay(1)	DH or DL Rising		30				ns
DL Pull-Down Resistance			0.8			1.6	Ω
DL Sink Current	V_{DL} = 2.5V		3.1				A
DL Pull-Up Resistance			2			4	Ω
DL Source Current	V_{DL} = 2.5V		1.3				A
DH Pull-Down Resistance	BST - LX = 5V		2			4	Ω
DH Pull-Up Resistance(2)	BST - LX = 5V		2			4	Ω
DH Sink/Source Current	V_{DH} = 2.5V		1.3				A

Notes:
1) Guaranteed by design.
2) Semtech's SmartDriver™ FET drive first pulls DH high with a pull-up resistance of 10Ω (typical) until LX = 1.5V (typical). At this point, an additional pull-up device is activated, reducing the resistance to 2Ω (typical). This negates the need for an external gate or boost resistor.

Pin Configuration



MLPQ16: 3X3 16 LEAD

Ordering Information

Device	Package[2]
SC475AMLTRT[1]	MLPQ-16 3X3
SC475AEVB	Evaluation Board

Notes:
1) Available in tape and reel packaging only. A reel contains 3000 devices.
2) Available in lead-free packaging only. This product is fully WEEE, RoHS and J-TD-020B compliant. This component and all homogenous subcomponents are RoHS compliant.

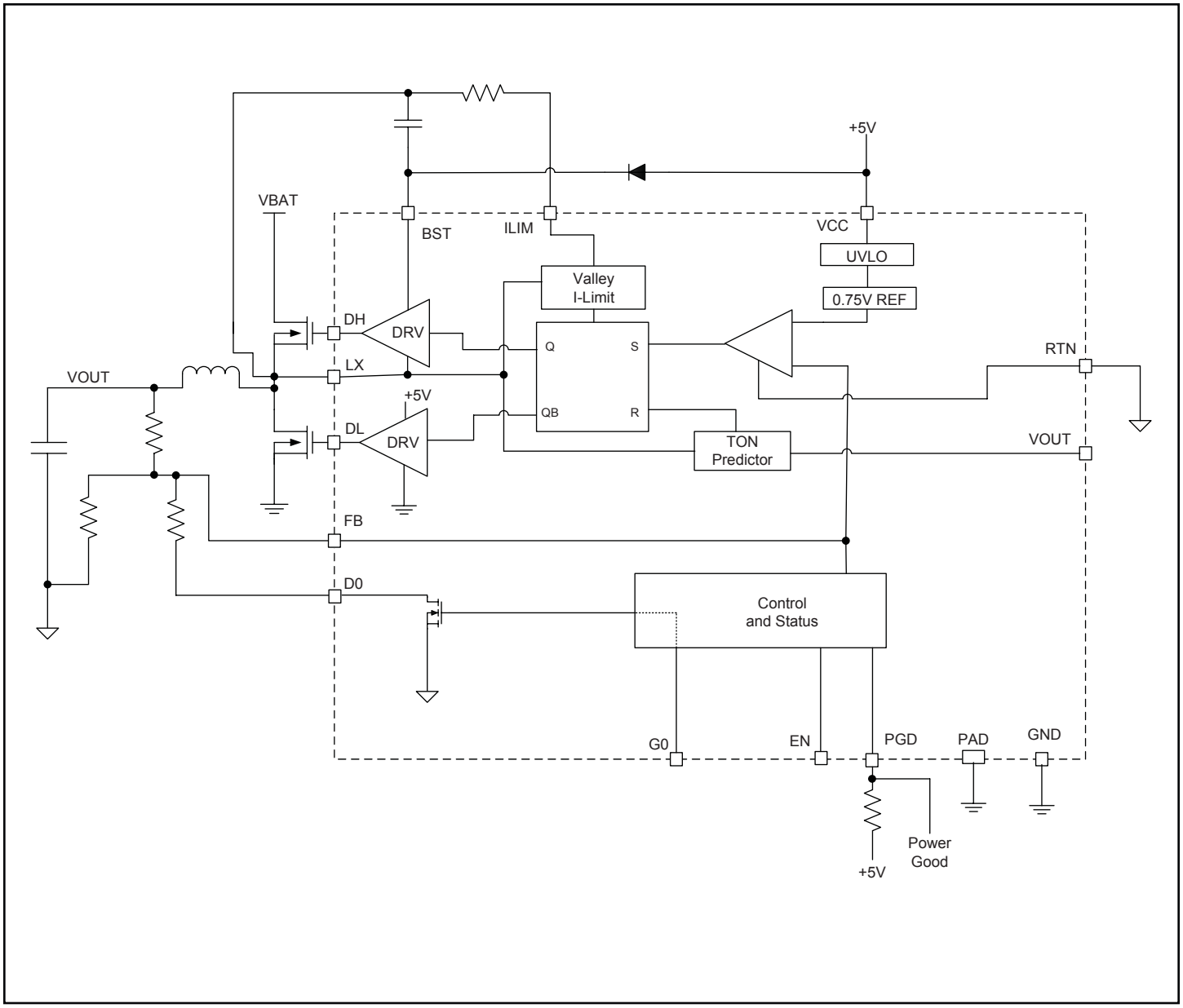
Marking Information

Marking for the 3x3mm MLPQ 16 Lead Package
nnn = Part Number (Example: 475A)
yyww = Date Code (Example: E652)
xxxx = Semtech Lot No. (Example: E901)

Pin Descriptions

Pin	Pin Name	Pin Function
1	LX	Switching (phase) node.
2	BST	Boost capacitor connection for high-side gate drive.
3	VCC	5V power input for the internal circuits and gate drive outputs.
4	DL	Gate drive output for the low-side external MOSFET.
5	GND	Power ground. This is the return point for the DL driver output, and the reference point for the ILIM and zero cross circuits.
6	RTN	Return or analog ground for the FB input and FB resistor divider . Connect to GND directly at the IC. All feedback components should connect to this ground.
7	NC	Not connected internally — leave unconnected or connect to GND.
8	D0	Drain of the internal MOSFET which is controlled by G0.
9	FB	Feedback sense point. The FB threshold is 0.75V; the resistor divider ratio between VOUT and FB sets the output voltage. This ratio can be modified using the G0 input to switch a resistor in or out at D0.
10	VOUT	Output voltage sense point for determining On-Time.
11	PGOOD	Open-drain power good indicator - a high impedance indicates power is good. An external pull-up resistor is required.
12	EN	Enable input - connect EN to RTN to disable the SC475A.
13	ILIM	Current limit sense point — to program the current limit connect a resistor from ILIM to LX or to a current sense resistor.
14	G0	Control input for the D0 MOSFET. A logic low energizes the D0 MOSFET, pulling D0 to ground.
15	NC	Not connected internally — leave unconnected or connect to GND.
16	DH	Gate drive output for the high-side external MOSFET.
T	PAD	Mounting pad. Not connected internally - connect to system ground plane through preferably one large vias or multiple smaller vias.

Block Diagram



Applications Information

SC475A Synchronous Buck Controller

The SC475A is a synchronous power supply controller which simplifies the task of designing a dual-level power supply suitable for controlling video chip sets and other dual-voltage circuits. The SC475A provides an input (G0) which controls an internal pull-down transistor used to select from two adjustable output voltages.

Battery and +5V Bias Supplies

The SC475A requires an external +5V bias supply in addition to the VBAT supply. If stand-alone capability is required, the +5V bias supply can be generated with an external linear regulator.

Pseudo-Fixed-Frequency Constant On-Time PWM Controller

The PWM control method is a constant-on-time, pseudo-fixed-frequency PWM controller, see Figure 1. The ripple voltage seen across the output capacitor's ESR provides the PWM ramp signal, eliminating the need for a current sense resistor. The on-time is determined by an internal one-shot whose period is proportional to output voltage, and inversely proportional to input voltage. A separate one-shot sets the minimum off-time (typically 350ns).

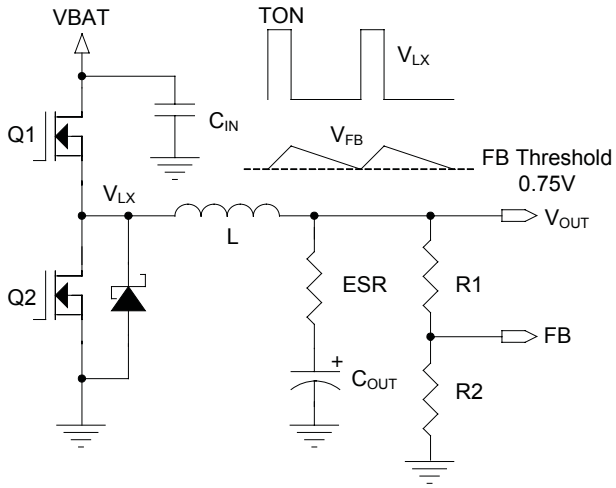


Figure 1

On-Time One-Shot (T_{ON})

The internal on-time one-shot comparator has two inputs. One input senses output voltage via the VOUT pin, while the other input samples VBAT via the LX pin and creates a proportional current which charges an internal capacitor. The TON time is the time required for this capacitor to charge from zero volts to VOUT, thereby making TON directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a fairly constant switching frequency without the need of a clock generator. The internal frequency is optimized for 325kHz. The general equation for the on-time is:

$$TON\ (nsec) = 2560 \bullet (V_{OUT}/V_{BAT}) + 35$$

Immediately after the DH on-time, the DL output drives high to energize the low-side MOSFET. DL has a minimum high time of typically 350nsec, after which DL will continue to stay high until one of the following occur:

- FB drops to the 0.75V reference
- The Zero Cross detector trips if power save is active
- The Negative Current Limit detector trips

The Zero Cross detector monitors the voltage across the low-side MOSFET and trips when it reaches zero. If this occurs on eight consecutive cycles, then DL will subsequently shut off when the Zero Cross detector trips. See the PSAVE Operation section. Both MOSFETS will then stay off until FB drops to 0.75V, which will begin the next DH on-time. This is normal operation at light load.

The Negative Current Limit detector trips when the drain voltage at the low-side MOSFET reaches typically +80mV, indicating a large negative current is being drawn through the inductor from VOUT. When this occurs, DL drives low. Both MOSFETS will then stay off until FB drops to 0.75V, which will begin the next DH on-time. Tripping the Negative Current detector is rare.

If DL drives low because FB has dropped to the 0.75V reference, then another DH on-time is started: this is normal operation at heavy load. If DL drives low because of the

Applications Information *(continued)*

Zero Cross detector, then both DH and DL will remain low until FB drops to the 0.75V reference, at which point the next DH on-time will begin. This is normal operation at light load.

The typical operating frequency is 325kHz. It is possible to raise the frequency by placing a resistor divider between the output and the VOUT pin, see Figure 2. This reduces the voltage at the VOUT pin which is used to generate the on-time according to the previous equation. Note that this places a small minimum load on the output. The new frequency is approximated by the following equation:

$$FREQ\ (kHz) = 325 \cdot (1 + R1/R2)$$

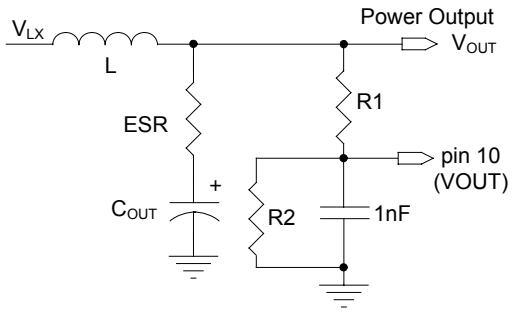


Figure 2

It is also possible to lower the frequency using a resistive divider to the 5V bias supply, see Figure 3. This raises the voltage at the VOUT pin which will increase the on-time. Note that this results in a small leakage path from the 5V supply to the output voltage. The resistor values should be fairly large (>50kOhm) large to prevent the output voltage from drifting up during shutdown conditions. Note that the feedback resistors act as a dummy load to limit how far the output can rise.

The new operating frequency is approximated by the equation:

$$FREQ\ (kHz) = 325 \cdot ((R1 + R2) / (R1 + R2 \cdot V_{CC}/V_{OUT}))$$

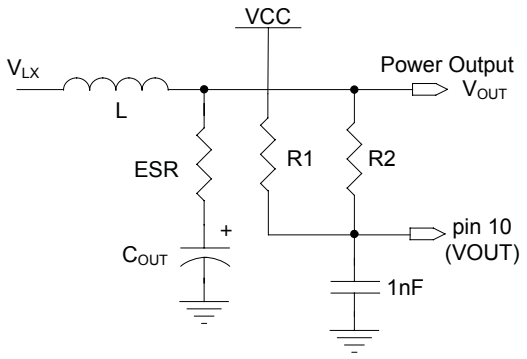


Figure 3

VOUT Voltage Selection

Output voltage is regulated by comparing VOUT as seen through a resistor divider to the internal 0.75V reference, see Figure 1. With D0 in the open state, the output voltage is at the lowest value and is set by the equation:

$$V_{OUT} = 0.75 \bullet (1 + R1/R2)$$

Voltage Transition Control

The SC475A provides a G0 control input to allow selecting between two output voltages. The output voltage is regulated by comparing the FB pin (connected to VOUT via an external resistor divider) to the internal 0.75V reference. The G0 input controls the gate of an internal MOSFET whose source is connected to D0. Using G0 the user controls whether D0 is grounded or open, which then controls the resistor divider ratio for VOUT. A logic low signal on G0 will connect D0 to ground.

When the G0 input changes state, this change quickly causes three actions:

1. D0 changes state.
2. The power good PGD output is temporarily latched into its present state. This prevents chattering or false tripping while VOUT moves to the new level.
3. The output over-voltage OVP point is raised to 50% above nominal, or 1.125V at FB. When going from a higher to lower voltage, the G0 change causes rapid change of D0, which in turns cause a rapid change at FB. The temporary increase in OVP allows the output to slew down to the new level without tripping the OVP function.

Applications Information *(continued)*

VOUT Voltage Selection

VOUT voltage is regulated through the FB pin via resistors R1 through R3 as shown in Figure 4.

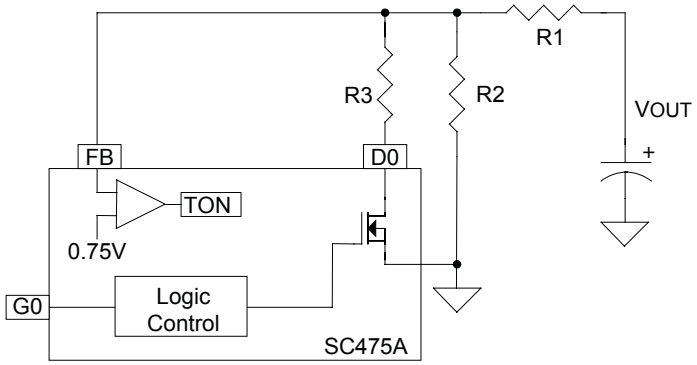


Figure 4

The following table shows the equations for VOUT as a function of control input G0:

VOUT Equation	G0
0.75 • (1 + R1/R2)	1
0.75 • (1 + R1/R2 + R1/R3)	0

Note that the RDSON of the internal D0 mosfet is in series with R3, which adds typically 15 ohms in series.

Voltage Transitioning

The G0 pin allows VOUT to transition to both higher and lower values. The two directions have differing responses.

When doing a down transition, the sudden release of R3 will cause FB to go above the 0.75V threshold. Depending on the level of VOUT change and the load, the IC responds in different ways.

At light load conditions when power-save is active, and when the downward change is 8% or greater, the rapid change of D0 is large enough to cause FB to rise up to the Smart Power Save threshold (810mV). DL will then drive high to turn on the low-side MOSFET and draw current from the output capacitor via the inductor. DL will remain on until FB falls to 0.75V, at which point a normal DH switching cycle begins, see Figure 5. This causes the output to transition to the new voltage level quickly, typically 10~20 usec. Refer to the Smart Power Save Protection section for a full description.

A rapid downward change in VOUT also occurs for downward changes less than 8%, provided the load is high enough such that power-save is not active. In this case, after D0 opens and FB rises above the 0.75V trip point, DL will drive high and stay high until FB drops to the trip point.

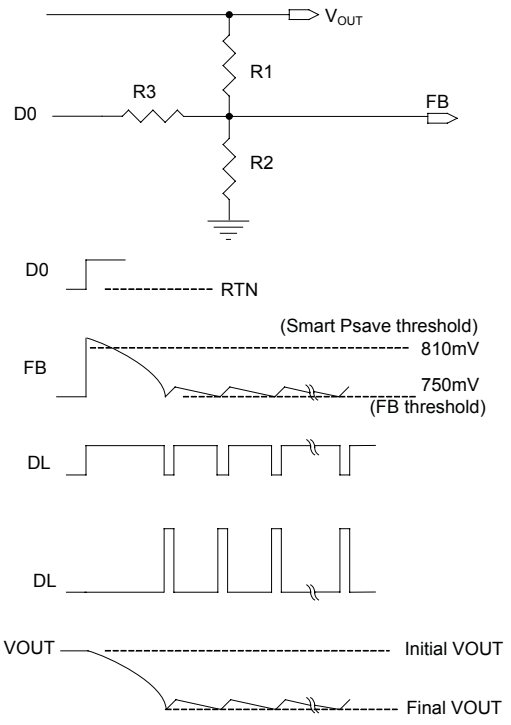


Figure 5

For the case where the down transition is less than 8%, and the load is light such that power-save is active, the Smart Power Save detector will not activate. In this case, with FB already above the 0.75V reference there is no switching activity. DL and DH will remain off, and the output voltage will slowly fall as the output capacitors discharge into the load, see Figure 6.

Applications Information *(continued)*

Note that at light loads it can take many msec for the output to fall to the new value. This should have no adverse effect. Many loads such as graphics chipsets can have a minimum load of several hundred mA, which will naturally pull VOUT down to the next level.

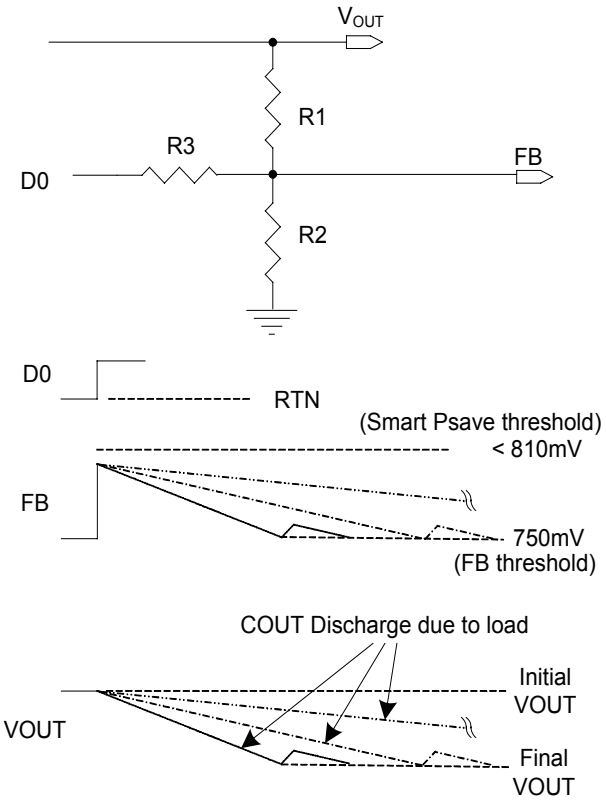


Figure 6

For the case in Figure 6 the time needed to reach the final voltage is found from the following equation, where COUT is in µF, and LOAD is in Amps:

$$\text{Time (µsec)} = \text{COUT} * (V_{INITIAL} - V_{FINAL})/\text{LOAD}$$

Note that the above equation only applies to the condition where the VOUT downward change is less that the 8% limit for Smart Psave, and also the load is light such that Psave is active.

When doing an up transition (from lower to higher VOUT), the G0 change affects D0 and causes FB to drop below the 0.75V trip point. This quickly trips the FB comparator regardless of whether psave is active or not, generating a DH on-time and a subsequent DL high time. At the end of the minimum off-time (350nsec), if FB is still below 0.75V then another DH on-time is started. This sequence continues until the FB pin exceeds 0.75V see Figure 7.

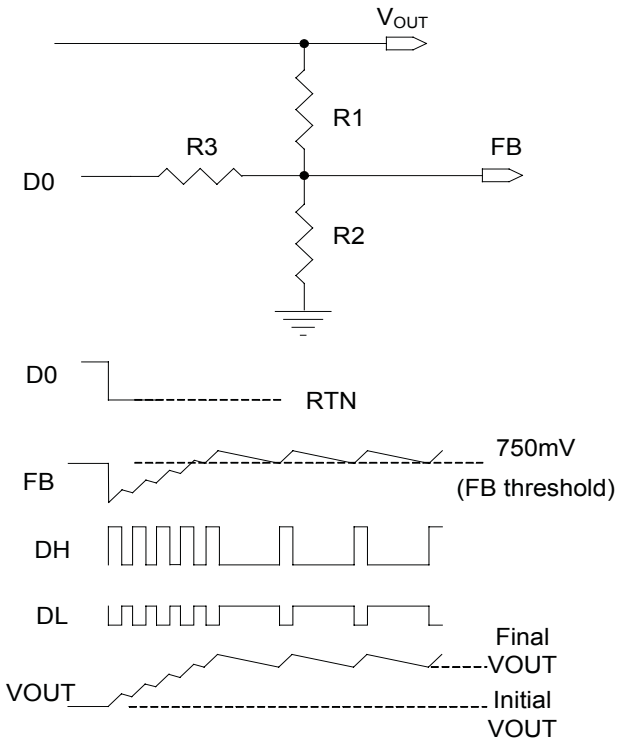


Figure 7

If the VOUT change is significant, there can be several consecutive cycles of DH on-time followed by minimum DL time. This can cause a rapid increase in inductor current: typically it only takes a few switching cycles for the inductor current to rise up to the Current Limit. At some point the FB voltage will rise up to the 0.75V reference and the DH pulses will cease, but the inductor's LI^2 energy must then flow into the output cap. This can create a significant overshoot as shown in Figure 8.

Applications Information *(continued)*

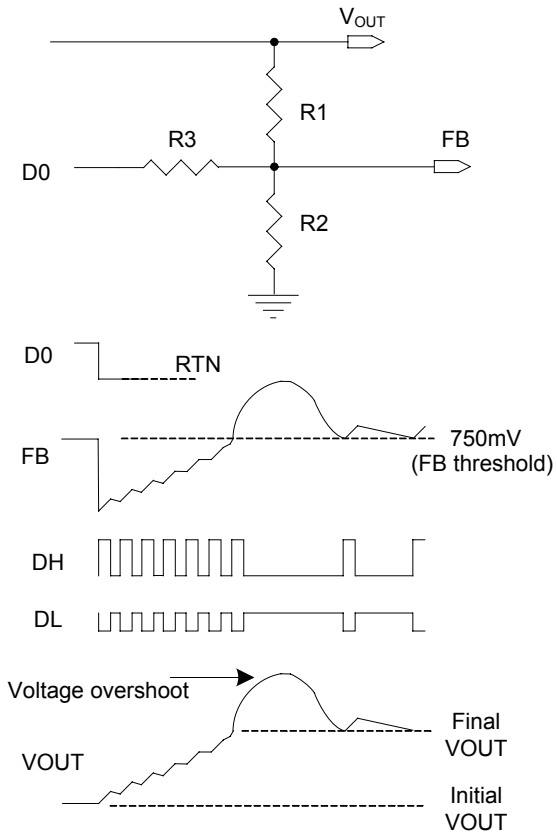


Figure 8

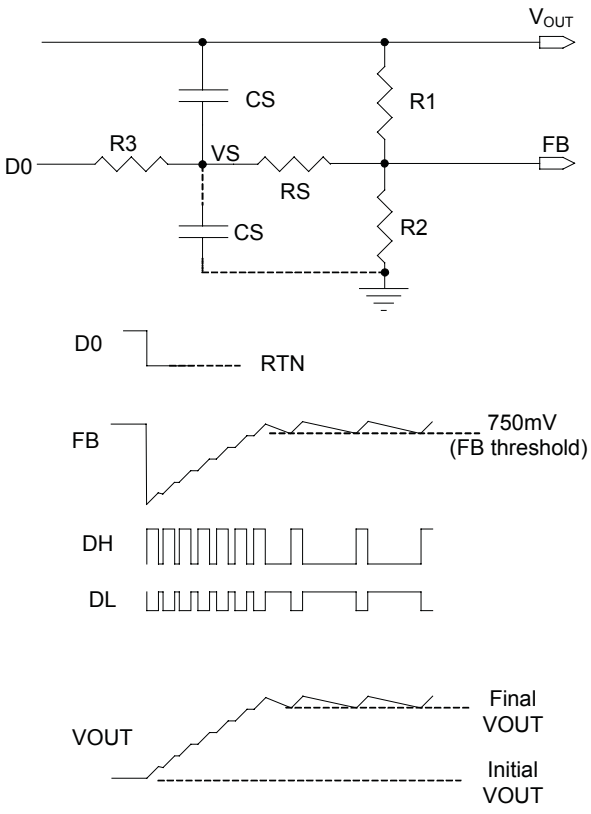


Figure 9

The overshoot can be approximated by the following equation, where ICL is the current limit, V_{FINAL} is the desired setpoint for the final voltage, L is in µH and COUT is in µF.

$$VMAX = \sqrt{(ICL^2 * L/COUT + V_{FINAL}^2)}$$

This overshoot can be eliminated by using a small RC circuit to smooth the voltage seen at FB, see Figure 9. The presence of Rs/Cs will prevent the rapid changes at D0 from moving FB too quickly. The result is a gradual change from $VOUT_{INITIAL}$ to $VOUT_{FINAL}$, to prevent the build-up of high inductor current and reducing overshoot. Note that Cs can be connected to either VOUT or GND. VOUT is preferred because this results in higher ripple seen at the FB pin, which improves stability.

Note that Rs/Cs are part of the FB resistor divider and therefore affect the output voltage sensing. To minimize the effect of this, select Rs and Cs according to the following guidelines:

The total of Rs + R3 should be chosen to give the correct total resistance needed to adjust VOUT. Set Rs and R3 to the same value.

Cs should be chosen to give a time constant equal to approximately 18µsec for 325 kHz operation. Note that Cs is charging through a resistive network composed of Rs/R1/R2/R3. The effective resistance seen by Cs is roughly equal to the parallel combination of Rs and R3. For example, if the values for R1/R2/R3/Rs are 10k/50k/15k/15k, then the effective resistance would be (10k + 15k) paralleled with 15k, which is 9.4k. To set a time constant of 18µsec, CS should be approximately 18µsec/9.4k or 2000pF.

Applications Information *(continued)*

Note that the presence of Rs/Cs will affect the effective resistance at the FB pin, and therefore modifies the VOUT setpoints. If Rs is used, the following table shows the calculated values for VOUT.

VOUT Equation	G0
0.75 • (1 + R1/R2)	1
0.75 • (1 + R1/R2 + R1/(R3+Rs))	0

Enable Input

The EN is used to disable or enable the SC475A. When EN is low (grounded), the SC475A is off and in its lowest-power state. When EN is high the controller is enabled and switching will begin.

PSAVE Operation

The SC475A provides automatic power save operation at light loads. The internal Zero-Cross comparator looks for inductor current (via the voltage across the lower MOSFET) to fall to zero on eight consecutive switching cycles. Once observed, the controller enters power save and turns off the low-side MOSFET on each cycle when the current crosses zero. To add hysteresis, the on-time is increased by 25% in power save. The efficiency improvement at light loads more than offsets the disadvantage of slightly higher output ripple. If the inductor current does not cross zero on any switching cycle, the controller immediately exits power save. Since the controller counts zero crossings, the converter can sink current as long as the current does not cross zero on eight consecutive cycles. This allows the output voltage to recover quickly in response to negative load steps, or to voltage transitions from a higher to a lower voltage where the change exceeds 8%.

Smart Power Save Protection

In some applications, active loads on VOUT can leak current from a higher voltage and thereby cause VOUT to slowly rise and reach the OVP threshold, causing a hard shutdown; the SC475A uses Smart Power Save to prevent this. When FB exceeds 8% above nominal (810mV), the IC exits power save (if already active) and DL drives high to turn on the low-side MOSFET, which starts to draw current from VOUT via the inductor. When FB drops to the 0.75V trip point, a normal TON switching cycle begins. This cycles energy from VOUT back to VBAT and prevents a hard OVP shutdown, and also minimizes operating power by avoiding continuous conduction-mode operation. If a light load is present, the switching continues for 8 consecutive clock cycles and then the IC will re-enter power save to reduce operating power.

Current Limit Circuit

Current limiting can be accomplished in two ways. The RDSON of the lower MOSFET can be used as a current sensing element, or a sense resistor at the lower MOSFET source can be used if greater accuracy is needed. RDSON sensing is more efficient and less expensive. In both cases, the R_{ILIM} resistor sets the over-current threshold. The R_{ILIM} connects from the ILIM pin to either the lower MOSFET drain (for RDSON sensing) or the high side of the current-sense resistor. R_{ILIM} connects to a 10µA current source from the ILIM pin which turns on when the low-side MOSFET turns on, after the on-time DH pulse has completed. If the voltage drop across the sense resistor or low-side MOSFET exceeds the voltage across the R_{ILIM} resistor, current limit will activate. The high-side MOSFET is held off until the voltage drop across the sense element (resistor or MOSFET) falls below the voltage across the R_{ILIM} resistor.

This current sensing scheme actually regulates the inductor valley current, (see Figure 10). This means that if the current limit is set to 10A, the peak current through the inductor would be 10A plus the peak ripple current, and the average current through the inductor would be 10A plus 1/2 the peak-to-peak ripple current.

Applications Information *(continued)*

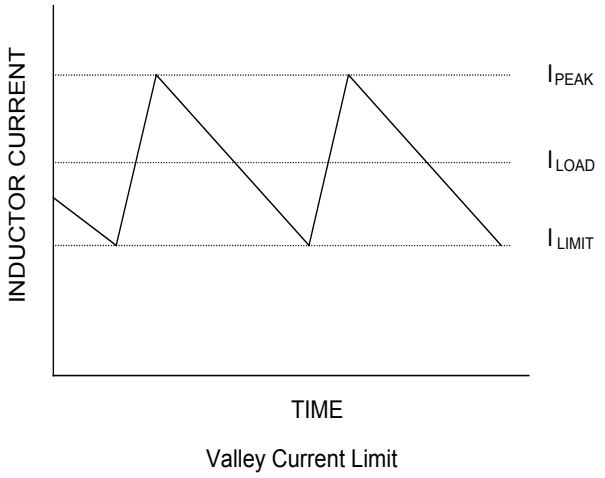


Figure 10

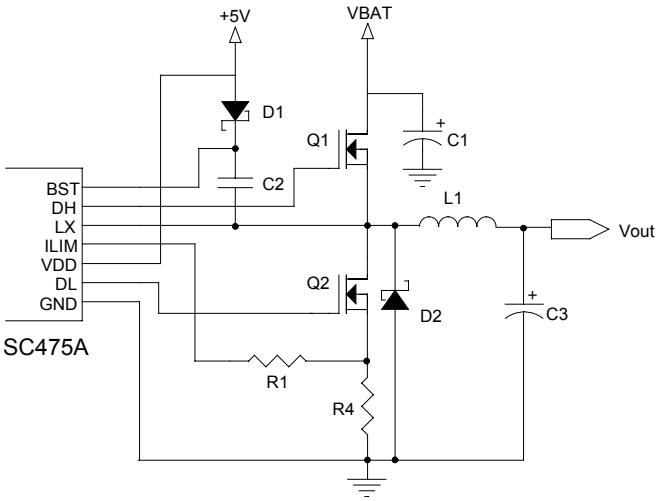


Figure 12

The RDSON sensing circuit is shown in Figure 11 with RILIM = R1 and RDSON of Q2.

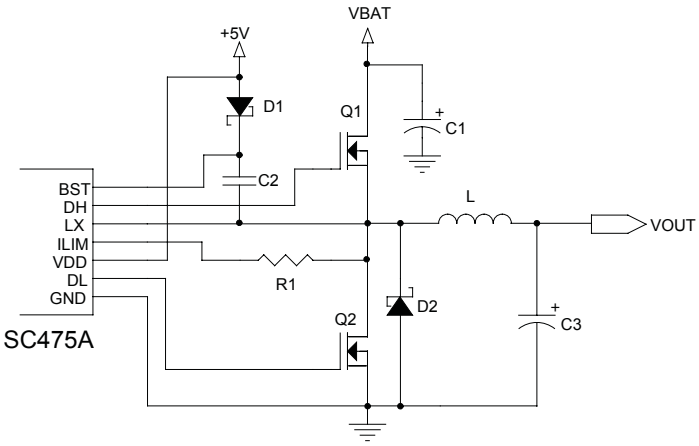


Figure 11

The resistor sensing circuit is shown in Figure 12 with RILIM = R1 and RSENSE = R4

For resistor sensing, the current through the lower MOSFET and the source sense resistor develops a voltage that opposes the voltage developed across RILIM. When the voltage developed across the RSENSE resistor reaches voltage drop across RILIM, an over-current exists and the high-side MOSFET will not be allowed to turn on.

The following over-current equation can be used for both RDSON or resistive sensing. For RDSON sensing, the MOSFET RDSON rating is used for the value of RSENSE.

$$IL_{OC}(Valley) = 10\mu A \bullet \frac{R_{ILIM}}{R_{SENSE}}$$

Power Good Output

The power good (PGD) output is an open-drain output which requires a pull-up resistor. When the output voltage as sensed at FB is -20% from the 0.75V reference (600mV), PGD is pulled low. It is held low until the output voltage returns above -20% of nominal. PGD is held low during start-up and will not be allowed to transition high until soft-start is completed when FB reaches 0.75V. There is a 5µs delay built into the PGD circuit to prevent false transitions.

Applications Information *(continued)*

PGD also transitions low if the FB pin exceeds +20% of nominal, which is also the over-voltage shutdown point.

When G0 changes state, PGD is immediately latched into its present state for 32 clock cycles while VOUT and FB change to the new level, after which the latch is disabled.

Output Over-Voltage Protection

In steady state operation, when FB exceeds 20% of nominal (900mV), DL latches high and the low-side MOSFET is turned on. DL stays high and the SMPS stays off until the EN/PSV input is toggled or VCC is recycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGD is also held low after an OVP.

During G0 transitions, the OVP threshold is temporarily increased to 50% above nominal (1.125V) for 32 clock cycles. This is for cases where the output voltage is slewing from a higher to a lower voltage: the change in G0 affects the D0 pin immediately, which in turn affects the FB voltage immediately. The increase in OVP from 20% to 50% is to prevent nuisance OVP tripping caused by the immediate change at FB. It also protects against the case of output overshoot for a lower to higher VOUT transition.

Note: since the temporary OVP is +50%, it is not possible to have a VOUT change which causes an immediate FB change of +50% or more. To transition VOUT under this condition, use the RC smoothing circuit to slow the FB transition edges and prevent +50% OVP.

Output Under-Voltage Protection

When FB falls 30% below nominal (525mV) for eight consecutive clock cycles, the output is shut off; the DL/DH drives are pulled low to tristate the MOSFETS, and the SMPS stays off until the Enable input is toggled or VCC is recycled.

POR and UVLO

Under-voltage lockout circuitry (UVLO) inhibits switching and tristates the DH/DL drivers until VCC rises above 4.4V. An internal power-on reset (POR) occurs when VCC exceeds 4.4V, which resets the fault latch and the soft-start counter, to prepare the PWM for switching. At this time the SC475A will come out of UVLO and begin the soft-start cycle.

Soft-Start

The soft-start is accomplished by ramping the FB comparator's internal reference from zero to 0.75V in 30mV increments. Each 30mV step typically lasts for eight clock cycles.

During the soft-start period, the Zero Cross Detector is active to monitor the voltage across the lower MOSFET while DL is high. If the inductor current reaches zero, the FB comparator's internal ramp reference is immediately overridden to match the voltage at the FB pin. This soon causes the FB comparator to trip which forces DL to turn off and the next DH on-time will begin. This prevents the inductor current from going too negative which would cause droop in the VOUT startup waveform. The next 30mV step on the internal reference ramp occurs from the new point at the FB pin. Since any of the internal 30mV steps can be overridden by the FB waveform, the startup time is dependent upon operating conditions. This override feature will stop when the FB pin reaches approximately 600mV, at which point the ramp resume 30mV steps up to 750mV.

At start-up, during the first 32 switching cycles, the over-current threshold is reduced by 50%, to reduce overshoot caused by the first set of switching pulses.

MOSFET Gate Drivers

The DH and DL drivers are optimized for moderate, high-side, and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off, and conversely, monitors the DH output and prevents the low-side MOSFET from turning on until DH is fully off.

Note: be sure there is low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.

Design Procedure

Prior to designing a switch mode supply, the input voltage, load current, switching frequency and inductor ripple current must be specified. For notebook systems the maximum input voltage (VIN_{MAX}) is determined by the highest AC adaptor voltage, and the minimum input voltage (VIN_{MIN}) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches.

Applications Information *(continued)*

In general, four parameters are needed to define the design:

1) Nominal output voltages (V_{OUT})
2) Static or DC output tolerance
3) Transient response
4) Maximum load current (I_{OUT})

There are two values of load current to consider: continuous load current and peak load current. Continuous load current is concerned with thermal stresses which drive the selection of input capacitors, MOSFETs and diodes. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors and design of the current limit circuit.

Design example:

- VBAT = 10V min, 20V max
- VOUT1 = 0.9V +/- 4%
- VOUT2 = 1.15V +/-4%
- Load = 20A maximum

Inductor Selection

Low inductor values result in smaller size but create higher ripple current. Higher inductor values will reduce the ripple current but are larger and more costly. Because wire resistance varies widely for different inductors and because magnetic core losses vary widely with operating conditions, it is often difficult to choose which inductor will optimize efficiency. The general rule is that higher inductor values have better efficiency at light loads due to lower core losses and lower peak currents, but at high load the smaller inductors are better because of lower resistance. The inductor selection is generally based on the ripple current which is typically set between 20% to 50% of the maximum load current. Cost, size, output ripple and efficiency all play a part in the selection process.
The switching frequency is optimized for 325kHz.
The equation for on-time is:

$$TON\ (nsec) = 2560 \bullet (VOUT/VBAT) + 35$$

During the DH on-time, voltage across the inductor is (VBAT - VOUT). To determine the inductance, the ripple current must be defined. Smaller ripple current will give smaller output ripple and but will lead to larger inductors. The ripple current will also set the boundary for PSAVE operation. The switcher will typically enter PSAVE operation when the load current decreases to 1/2 of the ripple current; (i.e. if ripple current is 4A then PSAVE operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then PSAVE will commence for loads less than 20% of maximum current).

The equation for determining inductance is:

$$L = (VBAT - VOUT) \bullet TON / I_{RIPPLE}$$

Use the maximum value for VBAT, and for TON use the value associated with maximum VBAT. For selecting the inductor, we start with the highest VOUT setting and a maximum ripple current of 5A.

$$TON = 182\ nsec\ at\ 20VBAT,\ 1.15VOUT$$

$$L = (20 - 1.15) \bullet 182\ nsec / 5A = 0.69\mu H$$

We will select a slightly larger value of 0.7µH, which will decrease the maximum I_{RIPPLE} to 4.91A.

Note: the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The minimum ripple current under is also checked .This occurs when VBAT and VOUT are set to their minimum values of 10V and 0.9V.

$$TON_{VBATMIN} = 2560 \bullet (0.9/10) + 35 = 265\ nsec$$

$$I_{RIPPLE} = (VBAT - VOUT) \bullet TON / L$$
$$I_{RIPPLE\_VBATMIN} = (10 - 0.9) \bullet 265\ nsec / 0.7\mu H = 3.45A$$

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The ESR requirement is driven by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple, plus 1/2 of the peak-to-peak ripple.

Applications Information *(continued)*

Change in the ripple voltage will lead to a change in DC voltage at the output.

The design goal is +/-4% output regulation. The internal 0.75V reference tolerance is 1%, assuming 1% tolerance for the FB resistor divider, this allows 2% tolerance due to VOUT ripple. Since this 2% error comes from 1/2 of the ripple voltage, the allowable ripple is 4%, or 46mV for a 1.15V output.

The maximum ripple current of 4.05A creates a ripple voltage across the ESR. The maximum ESR value allowed would create 46mV ripple:

$$ESR_{MAX} = V_{RIPPLE}/I_{RIPPLEMAX} = 46mV / 4.91A$$
$$ESR_{MAX} = 9.4\ m\Omega$$

The output capacitance is typically chosen based on transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, defines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in a very small time), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the equation:

$$COUT_{MIN} = L \bullet (I_{OUT} + 1/2 \bullet I_{RIPPLEMAX})^2 \ / \ (V_{PEAK}^2 - V_{OUT}^2)$$

With a peak voltage VPEAK of 1.230 (80mV rise above 1.15 upon load release), the required capacitance is:

$$COUT_{MIN} = 0.7\mu H \bullet (10 + 1/2 \bullet 4.91)^2/(1.24^2 - 1.15^2)$$

$$COUT_{MIN} = 570\mu F$$

The above requirements (570µF, 9.4mΩ) will be met using two capacitors, 330µF 6mΩ.

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 0.75V reference, the DL output is high and the low-side mosfet is on. During this time, the voltage across the inductor is approximately -VOUT. This causes a downslope or falling di/dt in the inductor. If the load di/dt is not much faster than the di/dt in the inductor, then the inductor current can track change in load current, and there will be relatively less overshoot from a load release. The following can used to calculate the needed capacitance for a given dILOAD/dt.

Peak inductor current,

$$ILPEAK = I_{LOADMAX} + 1/2 \bullet I_{RIPPLEMAX}$$

$$ILPEAK = 10 + 1/2 \bullet 4.91 = 12.45A$$

Rate of change of Load current = dILOAD/dt

IMAX = maximum DC load current = 10A

$$COUT = \frac{ILPEAK \bullet (L \bullet ILPEAK / VOUT - IMAX/dILOAD/dt)}{2 \bullet (VPEAK - VOUT)}$$

Example: Load dI/dt = 2.5A/µsec

This would cause the output current to move from 10A to zero in 4µsec.

$$COUT = \frac{12.45 \bullet (0.7\mu H \bullet 12.45/1.15 - 10/(2.5/1\mu sec)}{2 \bullet (1.23 - 1.15)}$$

$$COUT = 278\ \mu F$$

Stability Considerations

Unstable operation shows up in two related but distinctly different ways: double-pulsing and fast-feedback loop instability. double-pulsing occurs due to switching noise seen at the FB input or because the ESR is too low, causing insufficient voltage ramp in the FB signal. This causes the error amplifier to trigger prematurely after the 350ns minimum off-time has expired. Double-pulsing will result in higher ripple voltage at the output but in most cases is harmless. In some cases, however, double-pulsing can indicate the presence of loop instability, which is caused by insufficient ESR.

One simple way to solve this problem is to add some trace resistance between the VOUT/FB sense point and the output capacitor in the high current output path. A side effect of doing this is output voltage droop with load. Another way to eliminate doubling-pulsing is to add a small (e.g. 10pF) capacitor across the upper feedback resistor

Applications Information *(continued)*

divider network, as shown in Figure 13. This capacitance should be left out until confirmation that double-pulsing exists. Adding this capacitance will add a zero in the transfer function and should eliminate the problem. It is best to leave a spot on the PCB in case it is needed.

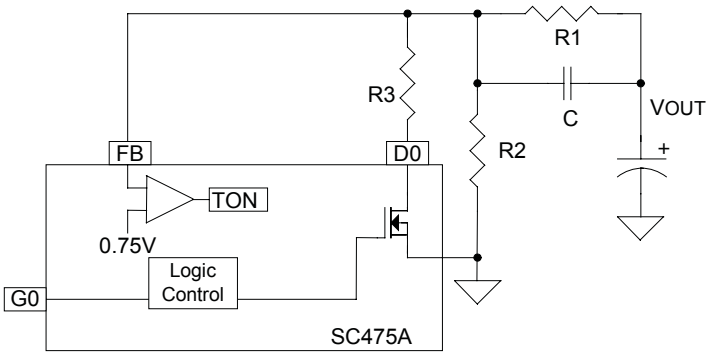


Figure 13

Loop instability can cause oscillations at the output as a response to line or load transients. These oscillations can trip the over-voltage protection latch or cause the output voltage to fall below the tolerance limit.

The best way for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Over one cycle of ringing after the initial step is a sign that the ESR should be increased.

SC475A ESR Requirements

The constant on-time control used in the SC475A regulates the valley of the output ripple voltage. This signal consists of a term generated by the output ESR of the capacitor and a term based on the increase in voltage across the capacitor due to charging and discharging during the switching cycle. The minimum ESR is set to generate the required ripple voltage for regulation. For most applications the minimum ESR ripple voltage is dominated by PCB layout and the properties of SP or POSCAP type output capacitors. For applications using ceramic output capacitors, the absolute minimum ESR must be considered. If the ESR is low enough the ripple voltage is dominated by the charging of the output capacitor. This ripple voltage lags the on-time due to the LC poles and can cause double pulsing if the phase delay exceeds the off-time of the converter. To prevent double pulsing, the ripple voltage present at the FB pin should be 10-15mV minimum over the on-time interval.

Dropout Performance

The VOUT adjust range for continuous-conduction operation is limited by the fixed 350nsec (typical) Minimum Off-time One-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The IC duty-factor limitation is given by:

$$DUTY = TONMIN/(TONMIN + TOFFMAX)$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case dropout duty-factor calculations.

SC475A System DC Accuracy (VOUT Controller)

Three factors affect VOUT accuracy: the trip point of the FB error comparator, the switching frequency variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed to trip when the feedback pin is 0.75V, +/-1%.

The on-time pulse in the SC475A is calculated to give a pseudo-fixed frequency of 325kHz. Nevertheless, some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because constant on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, If the output ripple is 50mV with VIN = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with VIN = 25 volts, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation it is often desirable to use passive droop. Take the feedback directly from the output side of the inductor, placing a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit.

Applications Information *(continued)*

Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced.

The use of 1% feedback resistors contributes typically 1% error. If tighter DC accuracy is required use 0.1% resistors.

The output inductor value may change with current. This will change the output ripple and thus the DC output voltage. The output ESR also affects the ripple and thus the DC output voltage.

Switching Frequency Variations

The switching frequency will vary somewhat due to line and load conditions. The line variations are a result of a fixed offset in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As VBAT increases, these factors make the actual DH on-time slightly longer than the idealized on-time. The net effect is that frequency tends to fall slightly with increasing input voltage.

The load variations are due to losses in the power train from IR drop and switching losses. For a conventional PWM constant-frequency topology, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A constant on-time topology must also overcome the same losses by increasing the duty cycle (more time is spent drawing energy from VBAT as losses increase). Since the on-time is constant for a given VOUT/VBAT combination, the way to increase duty cycle is to gradually shorten the off-time. The net effect is that switching frequency increases slightly with increasing load.

Layout Guidelines

One or more ground planes are recommended to minimize the effect of switching noise and copper losses and to maximize heat removal. The analog ground reference, RTN, should connect directly to the thermal pad, which in turn connects to the ground plane through preferably one large via. There should be a RTN plane or copper are near the chip; all components that are referenced to RTN should connect to this plane directly, not through the ground plane, and located on the chip side of the PCB if possible.

GND should be a separate plane which is not used for routing analog traces. The VCC input provides power to the internal analog circuits and the upper and lower gate drivers.

The VCC supply decoupling capacitor should be tied between VCC and GND with short traces. All power GND connections should connect directly to this plane with special attention given to avoiding indirect connections between RTN and GND which will create ground loops. As mentioned above, the RTN plane must be connected to the GND plane at the chip near the RTN/GND pins.

The switcher power section should connect directly to the ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses. Make all the power connections on one side of the PCB using wide copper filled areas if possible. Do not use “minimum” land patterns for power components. Minimize trace lengths and maximize trace widths between the gate drivers and the gates of the MOSFETs to reduce parasitic impedances (and MOSFET switching losses); the low-side MOSFET is most critical. Maintain a length to width ratio of <20:1 for gate drive signals. Use multiple vias as required by current handling requirement (and to reduce parasitic) if routed on more than one layer.

For an accurate ILIM current sense connection, connect the ILIM trace to the current sense element (MOSFET or resistor) directly at the pin of the element, and route that trace over to the ILIM resistor on another layer if needed. The layout can be generally considered in two parts; the analog control section referenced to RTN, and the switcher power section referenced to GND.

Applications Information *(continued)*

Looking at the control section first, locate all components referenced to RTN on the schematic and place these components near the chip and on the same side if possible. Connect RTN using a wide trace. Very little current flows in the RTN path and therefore large areas of copper are not needed. Connect the RTN pin directly to the thermal pad under the device as the only connection between RTN and GND.

The chip supply decoupling capacitor (VCC/GND) should be located near to the pins. Since the DL pin is directly between VCC and GND, and the DL trace must be a wide, direct trace, the VCC decoupling capacitor is best placed on the opposite side of the PCB, routed with traces as short as possible and using at least two vias when connecting through the PCB.

There are two sensitive, feedback-related pins at the chip: VOUT and FB. Proper routing is needed to keep noise away from these signals. All components connected to FB should be located directly at the chip, and the copper area of the FB node minimized. The VOUT trace that feeds into the VOUT pin, which also feeds the FB resistor divider, must be kept far away from noise sources such as switching nodes, inductors and gate drives. Route the VOUT trace in a quiet layer if possible, from the output capacitor back to the chip.

For the switcher power section, there are a few key guidelines to follow:

1) There should be a very small input loop between the input capacitors, MOSFETs, inductor, and output capacitors. Locate the input decoupling capacitors directly at the MOSFETs.

2) The phase node should be a large copper pour, but still compact since this is the noisiest node.

3) The power GND connection between the input capacitors, low-side MOSFET, and output capacitors should be as small as is practical, with wide traces or planes.

4) The impedance of the power GND connection between the low-side MOSFET and the GND pin should be minimized. This connection must carry the DL drive current, which has high peaks at both rising and falling edges. Use mulitple layers and multiple vias to minimize impedance, and keep the distance as short as practical. Finally, connecting the control and switcher power sections should be accomplished as follows:

1) Route the VOUT/FB feedback traces in a “quiet” layer, away from noise sources.

2) Route DL, DH and LX (low side FET gate drive, high side FET gate drive and phase node) to the chip using wide traces, with multiple vias if using more than one layer. These connections are to be as short as possible for loop minimization, with a length to width ratio less than 20:1 to minimize impedance. DL is the most critical gate drive, with power GND as its return path. LX is the noisiest node in the circuit, switching between VBAT and ground at high frequencies, thus should be kept as short as practical. DH has LX as its return path. DL, DH, LX, and BST are high-noise signals and should be kept well away from sensitive signals, particularly FB and VOUT.

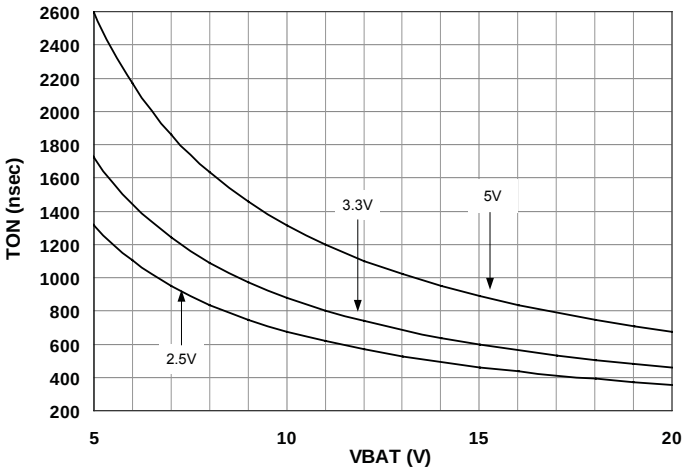
3) BST is also a noisy node and should be kept as short as possible. The high-side DH driver is relies on the boost capacitor to provide the DH drive current, so the boost capacitor must be placed near the IC and connect to the BST and LX pins using short, wide traces to minimize impedance.

4) Connect the GND pin on the chip to the VCC decoupling capacitor and then drop vias directly to the ground plane.

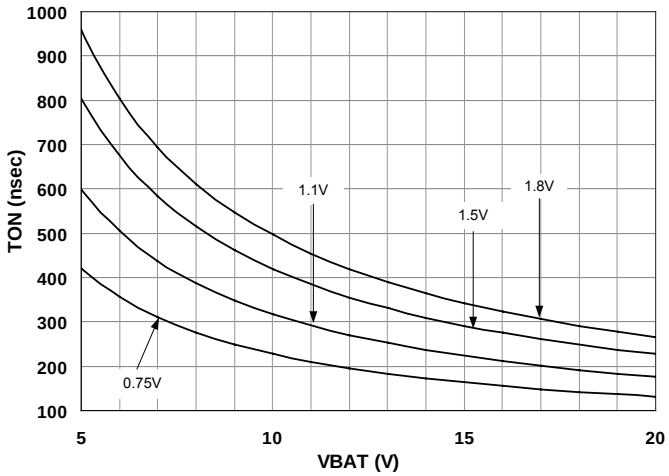
Locate the current limit resistor RLIM at the chip with a kelvin connection to the drain of the lower MOSFET at the phase node, and minimize the copper area of the ILIM trace.

Typical Characteristics

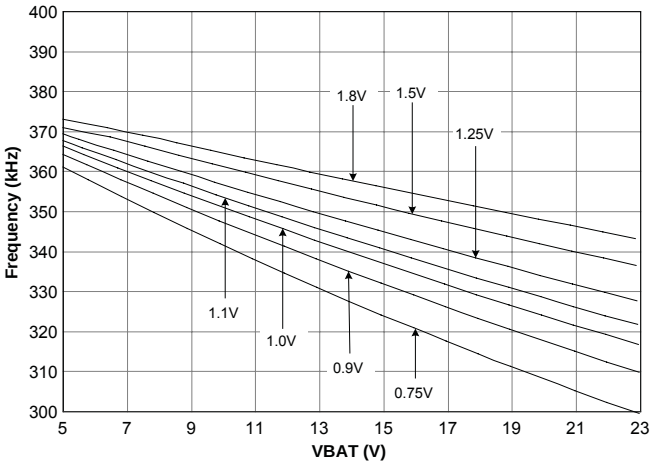
TON vs. VBAT - VOUT ≥ 2.5V



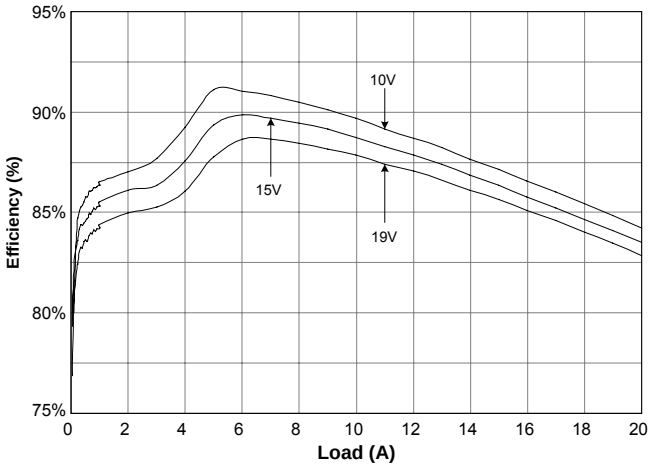
TON vs. VBAT - VOUT ≤ 1.8V



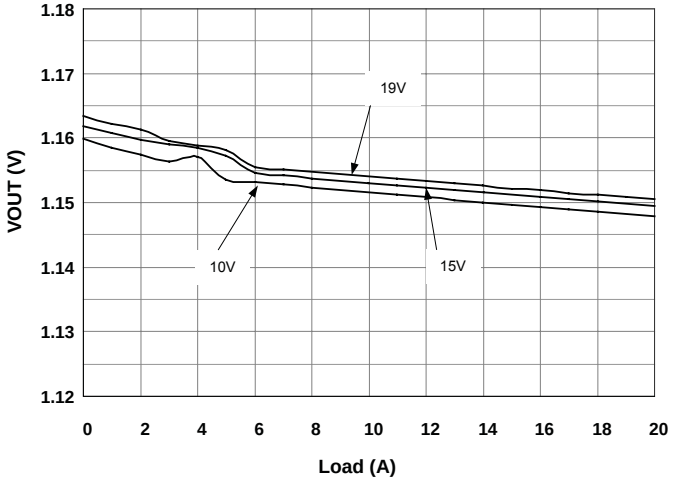
Frequency vs. BAT



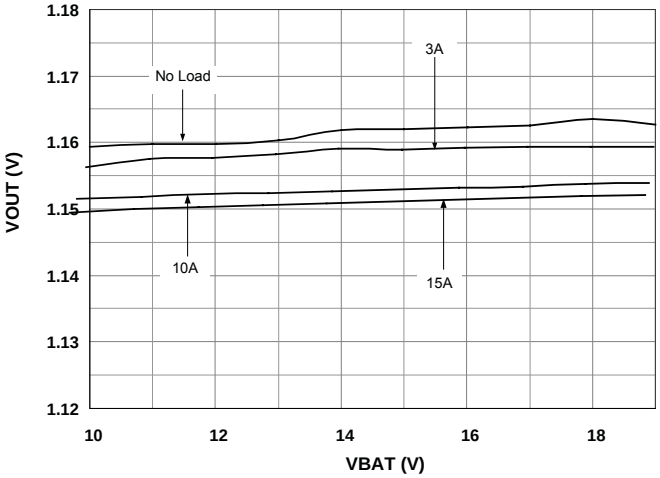
Efficiency vs. Load - VOUT = 1.15V



Load Regulation

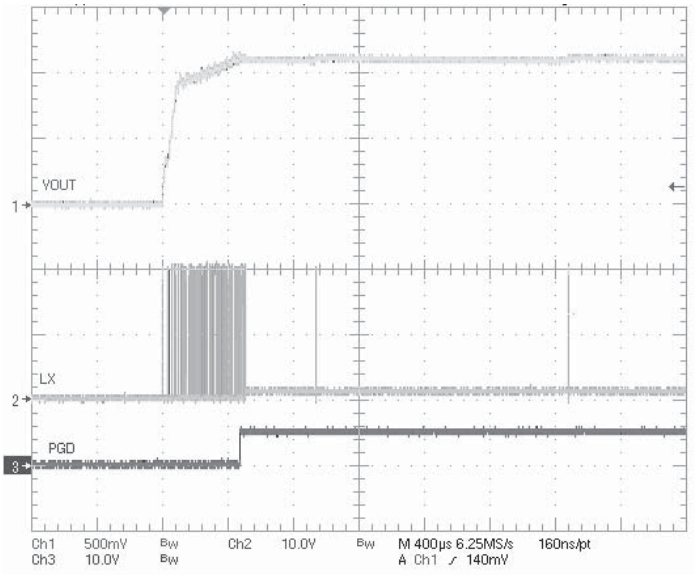


Line Regulation

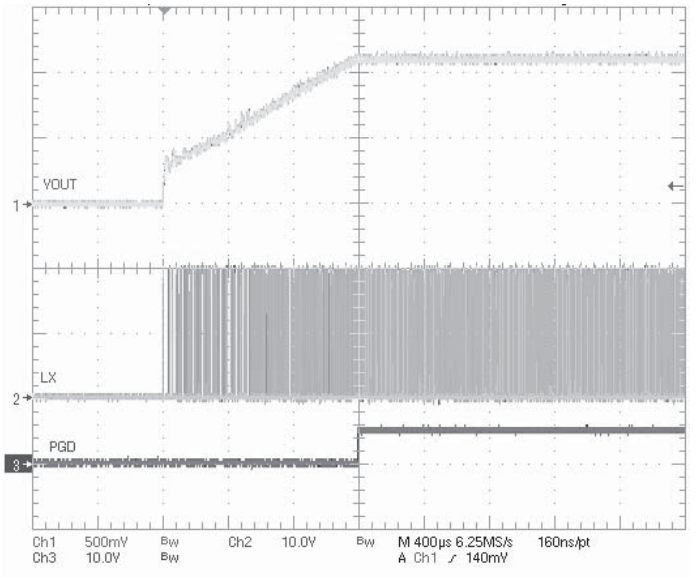


Typical Characteristics *(continued)*

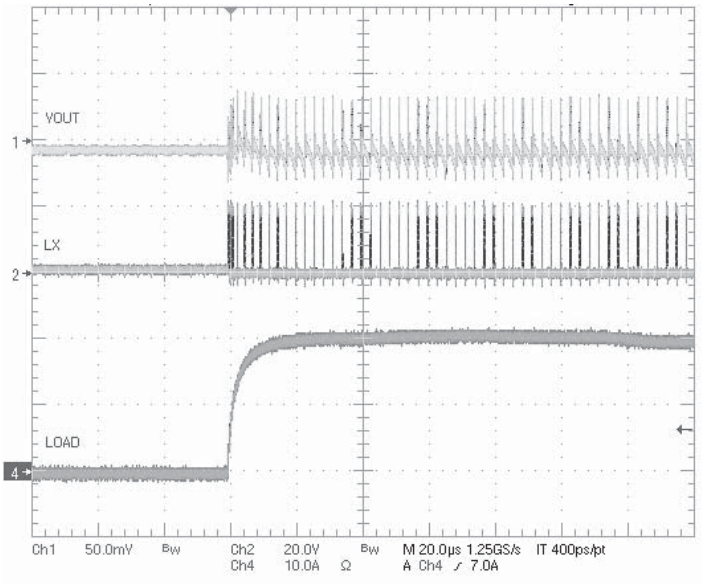
Startup 1.15V 19VBAT No load



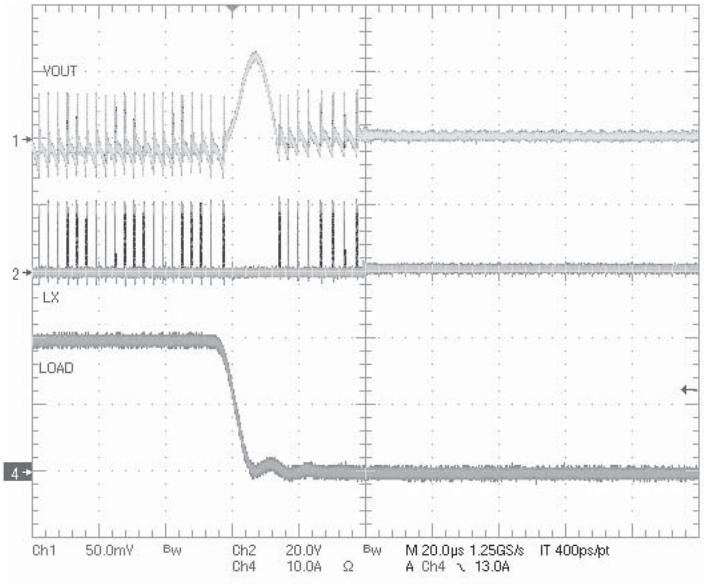
Startup 1.15V 19VBAT 20A load



Load Transient Response 0A to 20A

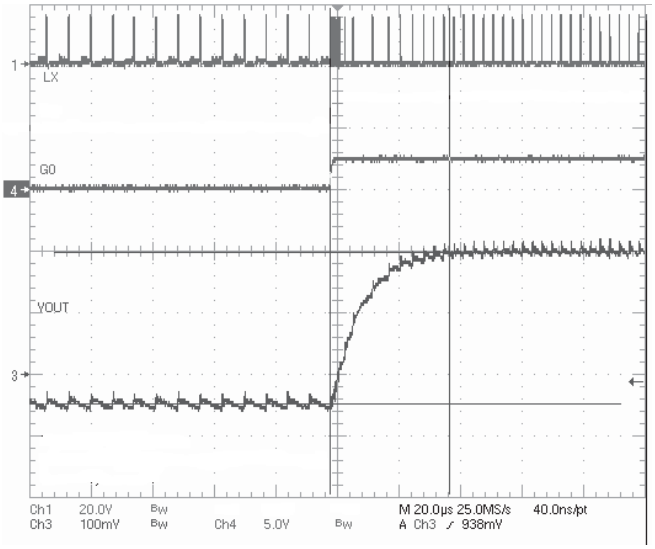


Load Transient Response 20A to 0A

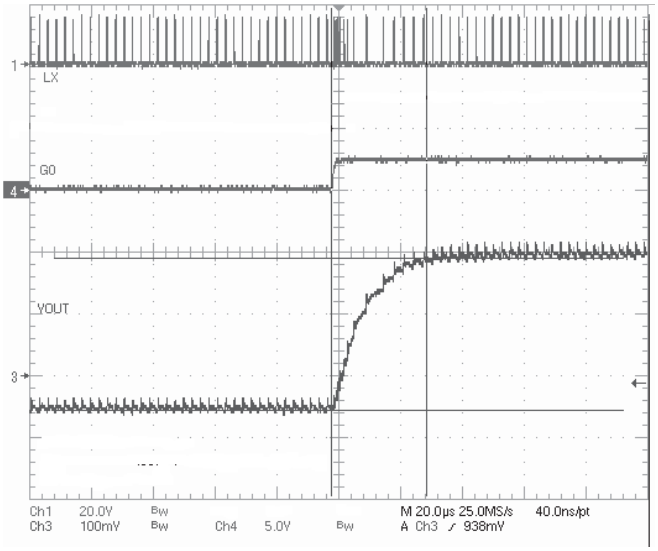


Typical Characteristics *(continued)*

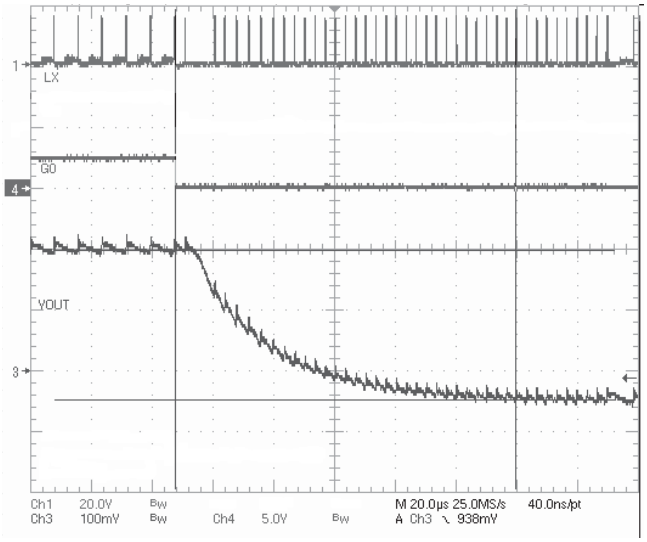
VOUT Up Transition
VOUT = 0.9 to 1.15V, VBAT = 15V 1A Load



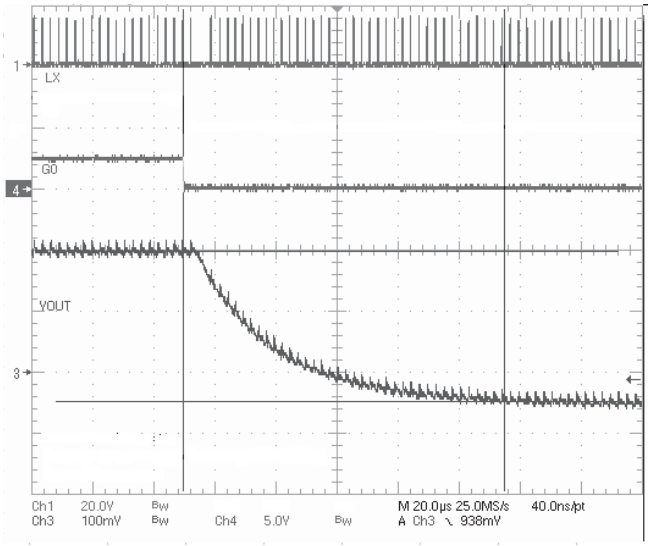
VOUT Up Transition
VOUT = 0.9 to 1.15V, VBAT = 15V 15A Load



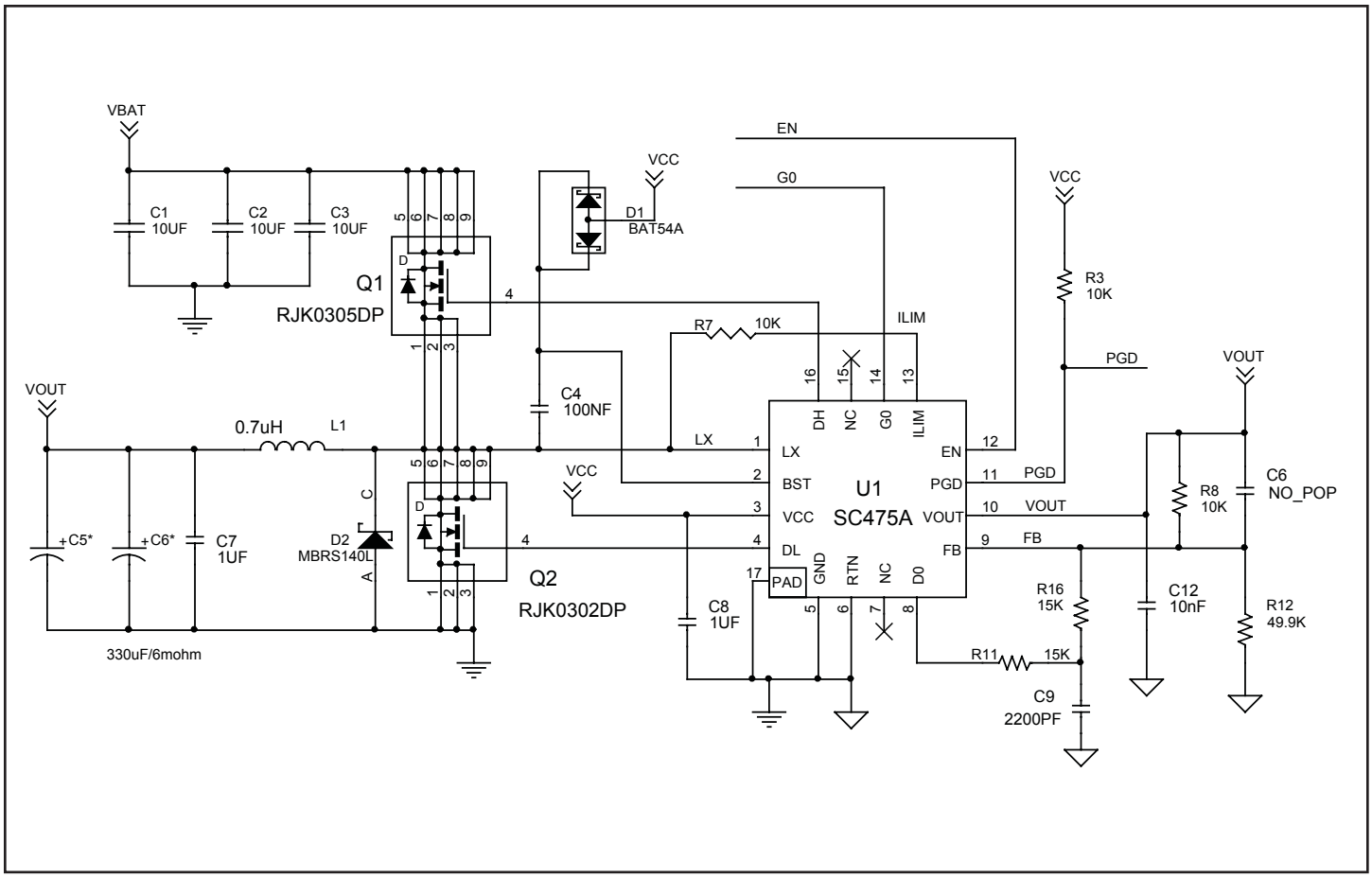
VOUT Down Transition
VOUT = 1.15 to 0.9V, VBAT = 15V 1A Load



VOUT Down Transition
VOUT = 1.15 to 0.9V, VBAT = 15V 15A Load



Reference Design

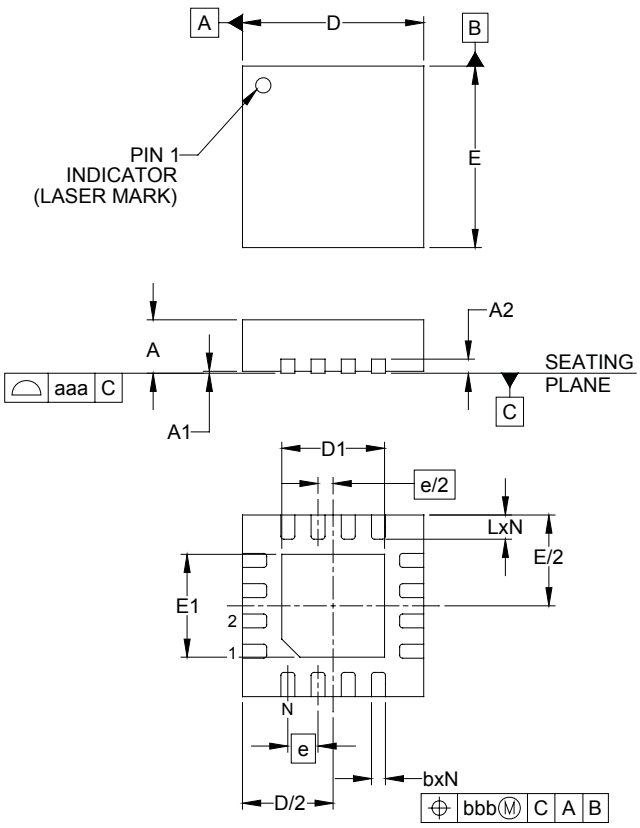


Reference Design — 0.90V/1.15V 20A

Bill of Materials

Component	Value	Manufacturer	Part Number	Web
C1, C2, C3	10uF, 25V	Murata	GRM32DR71E106KA12L	www.murata.com
C5, C5	330uF/6mohm/2V	Panasonic	EEFSX0D331XR	www.panasonic.com
L1	0.7uH, 24A	NEC Tokin	C-PI-1350-0R7S	http://www.nec-tokin.com
Q1	10mohm/30V	Renesas	RJK0305DBP	www.renesas.com
Q2	3.5mohm/30V	Renesas	RJK0302DBP	www.renesas.com
D1	200mA/30V	OnSemi	BAT54C	www.onsemi.com
D2	1A/40V	OnSemi	MBSR140LT3	www.onsemi.com

Outline Drawing - MLPQ-16 3 x 3

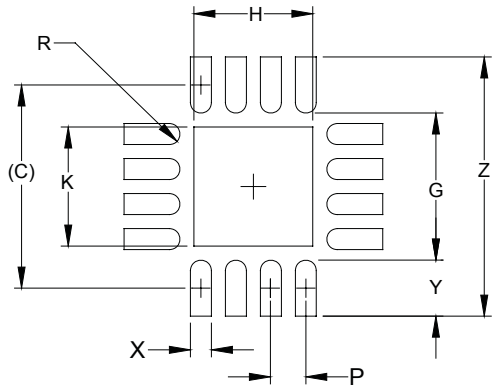


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.040	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.009	.012	0.18	0.23	0.30
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	16			16		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern - MLPQ-16 3 x 3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.020	0.50
R	.006	0.15
X	.012	0.30
Y	.031	0.80
Z	.146	3.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com