

CYPRESS
SEMICONDUCTOR7-46-23-10 CY7C164A
CY7C166A

16,384 x 4 Static R/W RAM

Features

- Automatic power-down when deselected
- Output Enable ($\overline{OE}$) feature (7C166A)
- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 15$ ns
- Low active power
 - 550 mW
- Low standby power
 - 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C164A and CY7C166A are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C166A has an active low output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 60% when deselected.

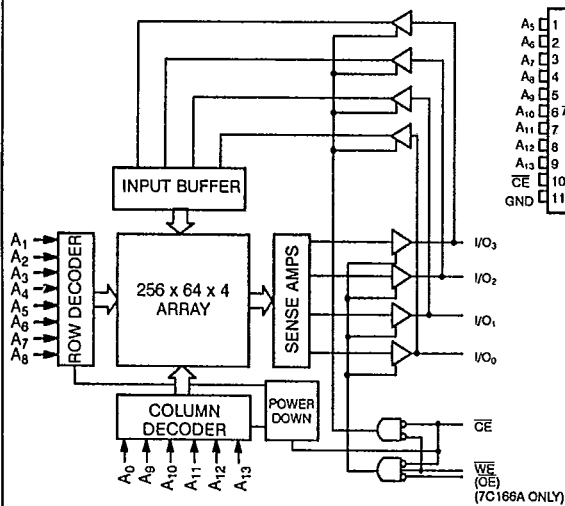
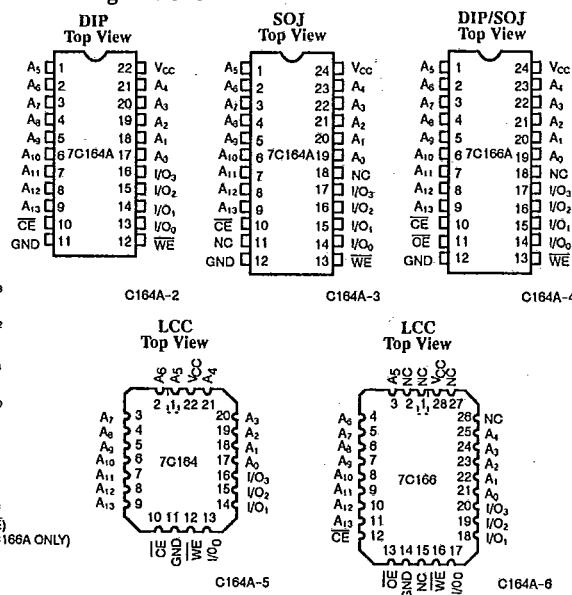
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW (and the output enable ($\overline{OE}$) is LOW for the 7C166A). Data on the four input/output pins (I/O_0 through

I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7C166A), while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{OE}$) is HIGH for 7C166A).

A die coat is used to insure alpha immunity.

Logic Block Diagram**Pin Configurations****Selection Guide**

		7C164A-15 7C166A-15	7C164A-20 7C166A-20	7C164A-25 7C166A-25	7C164A-35 7C166A-35	7C164A-45 7C166A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	100	100	100	100
	Military		100	100	100	100
Maximum Standby Current (mA)	Commercial	40/20	40/20	30	30	30
	Military		40/20	40/20	30	30



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to + 150°C

Ambient Temperature with

Power Applied - 55°C to + 125°C

Supply Voltage to Ground Potential - 0.5V to + 7.0V

DC Voltage Applied to Outputs

in High Z State - 0.5V to + 7.0V

DC Input Voltage - 3.0V to + 7.0V

Output Current into Outputs (Low) 20 mA

Static Discharge Voltage >2001V

(per MIL-STD-883, Method 3015)

Latch-up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military ⁽¹⁾	- 55°C to + 125°C	5V ± 10%

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Electrical Characteristics Over the Operating Range⁽²⁾

Parameters	Description	Test Conditions	7C164A-15 7C166A-15		7C164A-20 7C166A-20		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ⁽³⁾		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+ 10	-10	+ 10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+ 10	-10	+ 10	μA
I _{OS}	Output Short Circuit Current ⁽⁴⁾	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max. I _{OUT} = 0 mA	Com'l	115		100	mA
			Mil			100	
I _{SB1}	Automatic $\overline{CE}$ ⁽⁵⁾ Power Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%	Com'l	40		40	mA
			Mil			40	
I _{SB2}	Automatic $\overline{CE}$ ⁽⁵⁾ Power Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH} - 0.3V$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V	Com'l	20		20	mA
			Mil			20	

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = -3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
6. Tested initially and after any design or process changes that may affect these parameters.



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Electrical Characteristics Over the Operating Range ^[2] (continued)

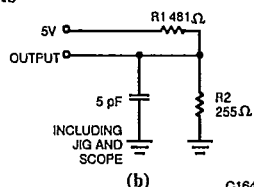
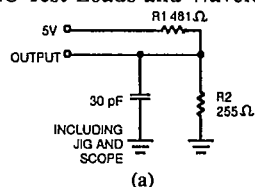
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Parameters	Description	Test Conditions	7C164A-25 7C166A-25		7C164A-35,45 7C166A-35,45		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[3]		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max. I _{OUT} = 0 mA	Com'l	100		100	mA
			Mil	100		100	
I _{SB1}	Automatic $\overline{CE}$ ^[5] Power Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%	Com'l	30		30	mA
			Mil	40		30	
I _{SB2}	Automatic $\overline{CE}$ ^[5] Power Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH} - 0.3V$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V	Com'l	20		20	mA
			Mil	20		20	

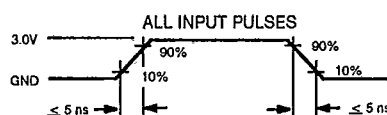
Capacitance^[6]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



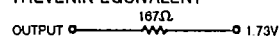
C164A-7



C164A-8

Equivalent to:

THEVENIN EQUIVALENT





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Switching Characteristics Over the Operating Range^[2,7]

			7C164A-15 7C166A-15		7C164A-20 7C166A-20		7C164A-25 7C166A-25		7C164A-35 7C166A-35		7C164A-45 7C166A-45		
Parameters	Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
READ CYCLE													
t _{RC}	Read Cycle Time		15		20		25		35		45		ns
t _{AA}	Address to Data Valid			15		20		25		35		45	ns
t _{OHA}	Output Hold from Address Change		3		3		3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid			15		20		25		35		45	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid	7C166A		10		10		12		15		20	ns
t _{LHZOE}	$\overline{OE}$ LOW to LOW Z	7C166A	3		3		3		3		3		ns
t _{LZOE}	$\overline{OE}$ HIGH to HIGH Z	7C166A		8		8		10		12		15	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[8]		3		5		5		5		5		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[8,9]			8		8		10		15		15	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down			15		20		20		20		25	ns
WRITE CYCLE ^[10]													
t _{WC}	Write Cycle Time		15		20		20		25		40		ns
t _{SCE}	$\overline{CE}$ LOW to Write End		12		15		20		25		30		ns
t _{AW}	Address Set-Up to Write End		12		15		20		25		30		ns
t _{HA}	Address Hold from Write End		0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start		0		0		0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width		12		15		15		20		20		ns
t _{SD}	Data Set-Up to Write End		10		10		10		15		15		ns
t _{HD}	Data Hold from Write End		0		0		0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[8]		5		5		5		5		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[8,9]			7		7		7		10		15	ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
- t_{HZCE} and t_{LZWE} are specified with $C_L = 5$ pF as in part (b) in AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and

either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

- $\overline{WE}$ is HIGH for read cycle.
- Device is continuously selected, $\overline{CE} = V_{IL}$ (7C166: $\overline{OE} = V_{IL}$ also).
- Address valid prior to or coincident with $\overline{CE}$ transition low.
- 7C166 only: Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
- If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

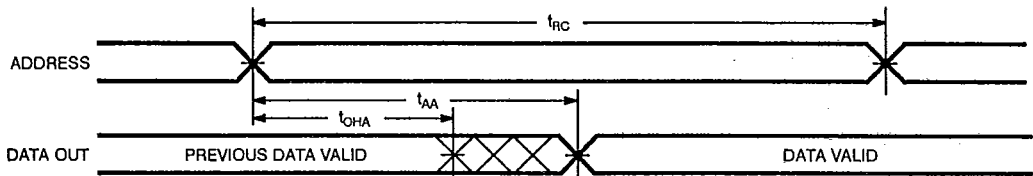


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Switching Waveforms

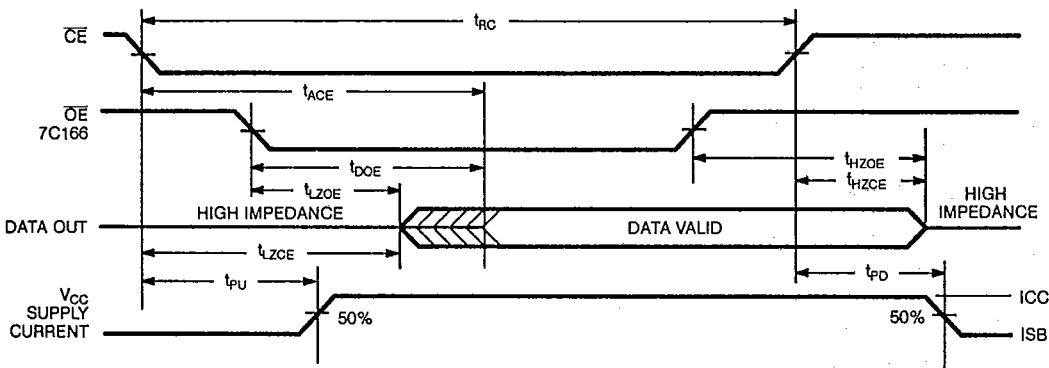
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Read Cycle No. 1^[11, 12]



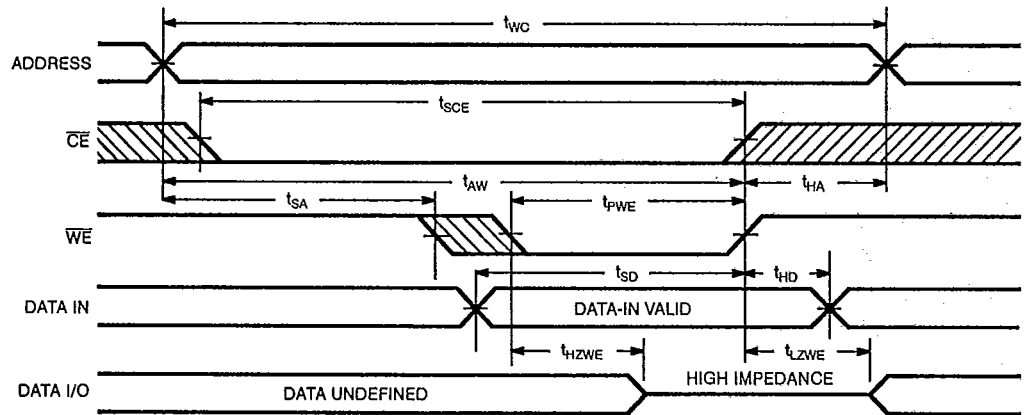
C164A-9

Read Cycle No. 2^[11, 13]



C164A-10

Write Cycle No. 1 (WE Controlled)^[10, 14]



C164A-11

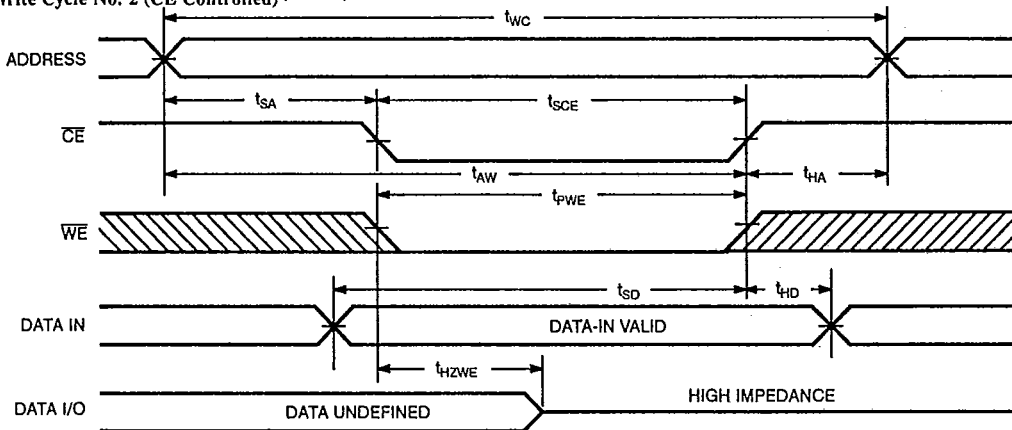


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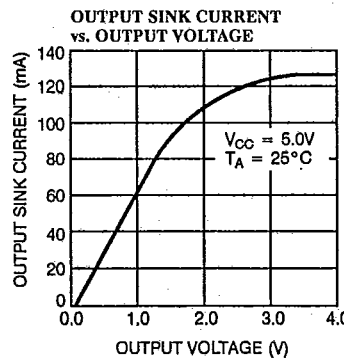
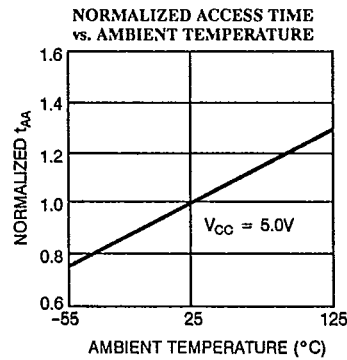
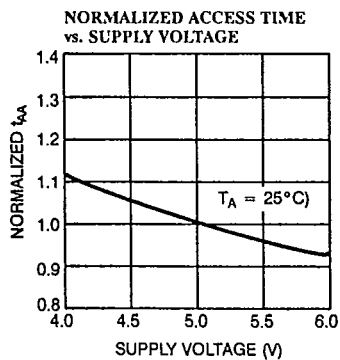
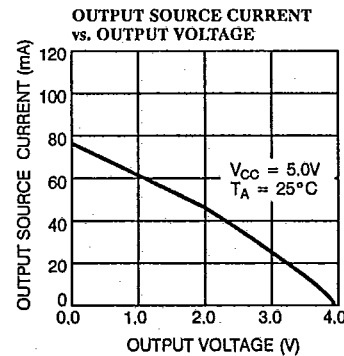
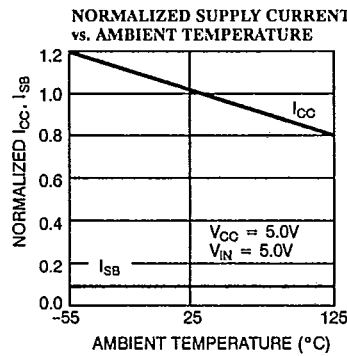
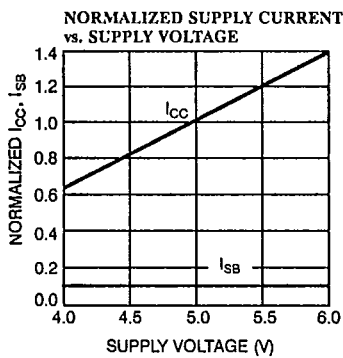
Switching Waveforms (continued)

Write Cycle No. 2 (CE Controlled) [10, 14, 15]



C164A-12

Typical DC and AC Characteristics



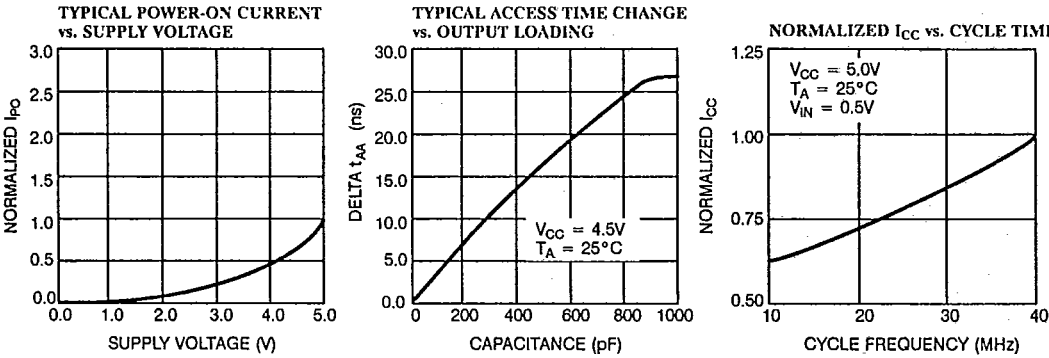


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Typical DC and AC Characteristics (continued)

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7C164A Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

7C166A Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect



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Ordering Information

T-46-23-10

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C164A-15PC	P9	Commercial
	CY7C164A-15VC	V13	
	CY7C164A-15DC	D10	
	CY7C164A-15LC	L52	
20	CY7C164A-20PC	P9	Commercial
	CY7C164A-20VC	V13	
	CY7C164A-20DC	D10	
	CY7C164A-20LC	L52	
	CY7C164A-20DMB	D10	Military
	CY7C164A-20LMB	L52	
	CY7C164A-20KMB	K73	
25	CY7C164A-25PC	P9	Commercial
	CY7C164A-25VC	V13	
	CY7C164A-25DC	D10	
	CY7C164A-25LC	L52	
	CY7C164A-25DMB	D10	Military
	CY7C164A-25LMB	L52	
	CY7C164A-25KMB	K73	
35	CY7C164A-35PC	P9	Commercial
	CY7C164A-35VC	V13	
	CY7C164A-35DC	D10	
	CY7C164A-35LC	L52	
	CY7C164A-35DMB	D10	Military
	CY7C164A-35LMB	L52	
	CY7C164A-35KMB	K73	
45	CY7C164A-45PC	P9	Commercial
	CY7C164A-45VC	V13	
	CY7C164A-45DC	D10	
	CY7C164A-45LC	L52	
	CY7C164A-45DMB	D10	Military
	CY7C164A-45LMB	L52	
	CY7C164A-45KMB	K73	

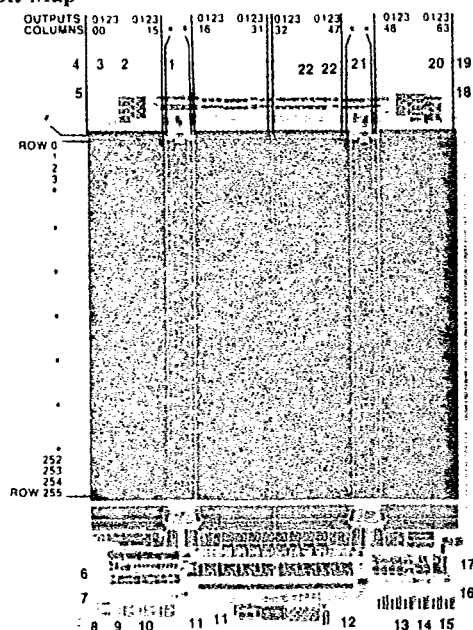
Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C166A-15PC	P13	Commercial
	CY7C166A-15VC	V13	
	CY7C166A-15DC	D10	
	CY7C166A-15LC	L52	
20	CY7C166A-20PC	P13	Commercial
	CY7C166A-20VC	V13	
	CY7C166A-20DC	D14	
	CY7C166A-20LC	L54	
	CY7C166A-20DMB	D14	Military
	CY7C166A-20LMB	L54	
	CY7C166A-20KMB	K73	
25	CY7C166A-25PC	P13	Commercial
	CY7C166A-25VC	V13	
	CY7C166A-25DC	D14	
	CY7C166A-25LC	L54	
	CY7C166A-25DMB	D14	Military
	CY7C166A-25LMB	L54	
	CY7C166A-25KMB	K73	
35	CY7C166A-35PC	P13	Commercial
	CY7C166A-35VC	V13	
	CY7C166A-35DC	D14	
	CY7C166A-35LC	L54	
	CY7C166A-35DMB	D14	Military
	CY7C166A-35LMB	L54	
	CY7C166A-35KMB	K73	
45	CY7C166A-45PC	P13	Commercial
	CY7C166A-45VC	V13	
	CY7C166A-45DC	D14	
	CY7C166A-45LC	L54	
	CY7C166A-45DMB	D14	Military
	CY7C166A-45LMB	L54	
	CY7C166A-45KMB	K73	

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Bit Map



Address Designators

T-46-23-10

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y5	6
A11	Y4	7
A12	Y0	8
A13	Y1	9
A0	Y2	17
A1	Y3	18
A2	X0	19
A3	X1	20
A4	X2	21

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{OS}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB1}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE} ⁽¹⁶⁾	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Note:
16. 7C166A only.