

ADC1005/ADC1025 10-Bit μ P Compatible A/D Converters

General Description

The ADC1005 and ADC1025 are CMOS 10-bit successive approximation A/D converters. The 20-pin ADC1005 outputs 10-bit data in a two-byte format for interface with 8-bit microprocessors.

The 24-pin ADC1025 outputs 10 bits in parallel and is intended for 16-bit data buses or stand-alone applications.

Both A-to-Ds have differential inputs to permit rejection of common-mode signals, allow the analog input range to be offset, and also to permit the conversion of signals not referred to ground. In addition, the reference voltage can be adjusted, allowing smaller voltage spans to be measured with 10-bit resolution.

Features

- Easy interface to all microprocessors
- Differential analog voltage inputs

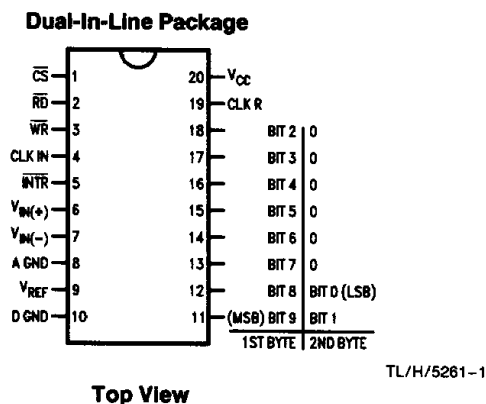
- Operates ratiometrically or with 5 V_{DC} voltage reference or analog span adjusted voltage reference
- 0V to 5V analog input voltage range with single 5V supply
- On-chip clock generator
- TLL/MOS input/output compatible
- 0.3" standard width 20-pin DIP or 24-pin DIP with 10-bit parallel output
- Available in 20-pin or 28-pin molded chip carrier package

Key Specifications

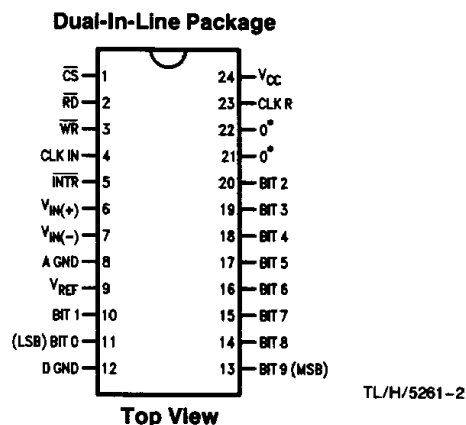
- Resolution 10 bits
- Linearity Error $\pm \frac{1}{2}$ LSB and ± 1 LSB
- Conversion Time 50 μ s

Connection Diagrams

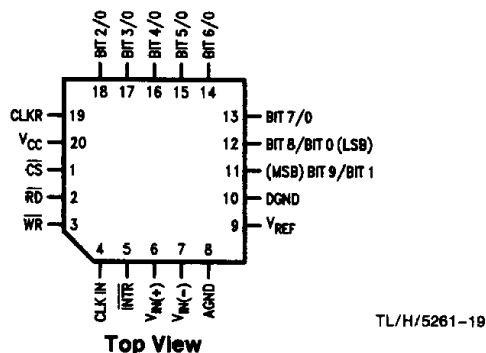
ADC1005 (for an 8-bit data bus)



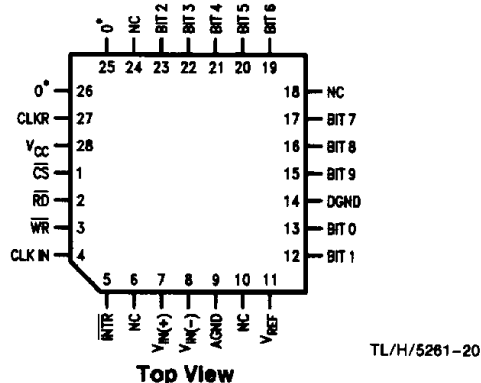
ADC1025 (10-bit parallel outputs)



ADC1005 Molded Chip Carrier Package



ADC1025 Molded Chip Carrier Package



TRI-STATE output buffers which output 0 during $\overline{RD}$

See Ordering Information

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Logic Control Inputs	-0.3V to +15V
Voltage at Other Inputs and Outputs	-0.3V to $V_{CC} + 0.3V$
Input Current Per Pin	± 5 mA
Input Current Per Package	± 20 mA
Storage Temperature Range	-65°C to +150°C
Package Dissipation at $T_A = 25^\circ\text{C}$	875 mW
Lead Temperature (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	800V

Operating Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5V to 6.0V
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC1005BJ, ADC1005CJ	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$
ADC1025BJ, ADC1025CJ	
ADC1005BCJ, ADC1005CCJ	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
ADC1025BCJ, ADC1025CCJ	
ADC1005BCJ-1, ADC1005CCJ-1	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$
ADC1025BCJ-1, ADC1025CCJ-1	
ADC1005BCN, ADC1005CCN	
ADC1025BCN, ADC1025CCN	
ADC1005BCV, ADC1005CCV	
ADC1025BCV, ADC1025CCV	

Electrical Characteristics The following specifications apply for $V_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.8$ MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}** ; All other limits $T_A = T_j = 25^\circ\text{C}$.

Parameter	Conditions	ADC10X5BJ, ADC10X5BCJ ADC10X5CJ, ADC10X5CCJ			ADC10X5BCJ-1, ADC10X5CCJ-1 ADC10X5BCN, ADC10X5CCN ADC10X5BCV, ADC10X5CCV			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
Converter Characteristics								
Linearity Error (Note 3) ADC10X5BJ, ADC10X5BCJ ADC10X5BCJ-1, BCN, BCV ADC10X5CJ, ADC10X5CCJ ADC10X5CCJ-1, CCN, CCV			± 0.5 ± 1			± 0.5 ± 1	± 0.5 ± 1	LSB LSB LSB LSB
Zero Error ADC10X5BJ, ADC10X5BCJ ADC10X5BCJ-1, BCN, BCV ADC10X5CJ, ADC10X5CCJ ADC10X5CCJ-1, CCN, CCV			± 0.5 ± 1			± 0.5 ± 1	± 0.5 ± 1	LSB LSB LSB LSB
Fullscale Error ADC10X5BJ, ADC10X5BCJ ADC10X5BCJ-1, BCN, BCV ADC10X5CJ, ADC10X5CCJ ADC10X5CCJ-1, CCN, CCV			± 0.5 ± 1			± 0.5 ± 1	± 0.5 ± 1	LSB LSB LSB LSB
Reference Input Resistance	MIN MAX	4.8 4.8	2.2 8.3		4.8 4.8	2.4 7.6	2.2 8.3	k Ω k Ω
Common-Mode Input (Note 4)	MIN MAX	$V_{IN}(+)$ or $V_{IN}(-)$	$V_{CC} + 0.05$ $GND - 0.05$			$V_{CC} + 0.05$ $GND - 0.05$	$V_{CC} + 0.05$ $GND - 0.05$	V V
DC Common-Mode Error	Over Common-Mode Input Range	$\pm 1/8$	$\pm 1/4$		$\pm 1/8$	$\pm 1/4$	$\pm 1/4$	LSB
Power Supply Sensitivity	$V_{CC} = 5 V_{DC} \pm 5\%$ $V_{REF} = 4.75V$	$\pm 1/8$	$\pm 1/4$		$\pm 1/8$	$\pm 1/4$	$\pm 1/4$	LSB

Electrical Characteristics

(Continued) The following specifications apply for $V_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.8\text{ MHz}$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}** ; All other limits $T_A = T_j = 25^\circ\text{C}$.

Parameter	Conditions	ADC10X5BJ, ADC10X5BCJ ADC10X5CJ, ADC10X5CCJ			ADC10X5BCJ-1, ADC10X5CCJ-1 ADC10X5BCN, ADC10X5CCN ADC10X5BCV, ADC10X5CCV			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
DC Characteristics								
V _{IN(1)} Logical "1" Input Voltage MIN	V _{CC} = 5.25V (except CLK _{IN})		2.0			2.0	2.0	V
V _{IN(0)} Logical "0" Input Voltage MAX	V _{CC} = 4.75V (Except CLK _{IN})		0.8			0.8	0.8	V
I _{IN} Logical "1" Input Current MAX	V _{IN} = 5.0V	0.005	1		0.005	1	1	μA
I _{IN} Logical "0" Input Current MAX	V _{IN} = 0V	−0.005	−1		−0.005	−1	−1	μA
V _{T+(MIN)} Minimum CLK _{IN} Positive going Threshold Voltage		3.1	2.7		3.1	2.7	2.7	V
V _{T(MAX)} Maximum CLK _{IN} Positive going Threshold Voltage		3.1	3.5		3.1	3.5	3.5	V
V _{T−(MIN)} Minimum CLK _{IN} Negative going Threshold Voltage		1.8	1.5		1.8	1.5	1.5	V
V _{T−(MAX)} Maximum CLK _{IN} Negative going Threshold Voltage		1.8	2.1		1.8	2.1	2.1	V
V _{H(MIN)} Minimum CLK _{IN} Hysteresis (V _{T+} -V _{T−})		1.3	0.6		1.3	0.6	0.6	V
V _{H(MAX)} Maximum CLK _{IN} Hysteresis (V _{T+} -V _{T−})		1.3	2.0		1.3	2.0	2.0	V
V _{OUT(1)} Logical "1" Output Voltage	V _{CC} = 4.75V I _{OUT} = −360 μA I _{OUT} = −10 μA		2.4 4.5			2.8 4.6	2.4 4.5	V V
V _{OUT(0)} Logical "0" Output Voltage	V _{CC} = 4.75V I _{OUT} = 1.6 mA		0.4			0.34	0.4	V
I _{OUT} TRI-STATE Output Current	V _{OUT} = 0V V _{OUT} = 5V	−0.01 0.01	−3 3		−0.01 0.01	−0.3 0.3	−3 3	μA μA
I _{SOURCE} Output Source Current	V _{OUT} = 0V	−14	−6.5		−14	−7.5	−6.5	mA
I _{SINK} Output Sink Current	V _{OUT} = 5V	16	8.0		16	9.0	8.0	mA
I _{CC} Supply Current	f _{CLK} = 1.8 MHz CS = "1"	1.5	3		1.5	2.5	3	mA

AC Electrical Characteristics

The following specifications apply for $V_{CC} = 5V$, $V_{REF} = 5V$, $t_r = t_f = 20\text{ ns}$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}** ; All other limits $T_A = T_j = 25^\circ\text{C}$.

Parameter	Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Limit Units
f_{CLK} Clock Frequency MIN MAX			0.2 2.6	0.2 2.6	MHz MHz
Clock Duty Cycle MIN MAX			40 60	40 60	% %

AC Electrical Characteristics The following specifications apply for $V_{CC} = 5V$, $V_{REF} = 5V$, $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}** ; All other limits $T_A = T_j = 25^\circ C$. (Continued)

Parameter	Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Limit Units
t_C , Conversion Time	MIN		80	80	$1/f_{CLK}$
	MAX		90	90	$1/f_{CLK}$
	MIN	$f_{CLK} = 1.8$ MHz	45	45	μs
	MAX	$f_{CLK} = 1.8$ MHz	50	50	μs
$t_{W(\overline{WR})L}$, Minimum $\overline{WR}$ Pulse Width	$\overline{CS} = 0$	100	150	150	ns
t_{ACC} , Access Time (Delay from falling edge of $\overline{RD}$ to Output Data Valid)	$\overline{CS} = 0$ $C_L = 100$ pF, $R_L = 2k$	170	300	300	ns
t_{1H} , t_{0H} , TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L = 10k$, $C_L = 10$ pF	125		200	ns
	$R_L = 2k$, $C_L = 100$ pF	145	230	230	ns
t_{W1} , t_{R1} , Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$		300	450	450	ns
t_{RS} , $\overline{INTR}$ to 1st Read Set-up Time		400	550	550	ns
C_{IN} , Capacitance of Logic Inputs		5		7.5	pF
C_{OUT} , Capacitance of Logic Outputs		5		7.5	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line which passes through the end points of the transfer characteristic.

Note 4: For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 00 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

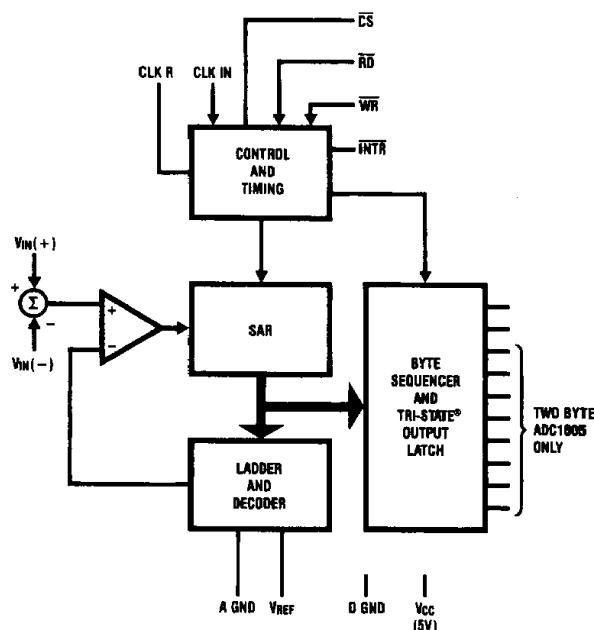
Note 5: Typicals are at $25^\circ C$ and represent most likely parametric norm.

Note 6: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 8: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

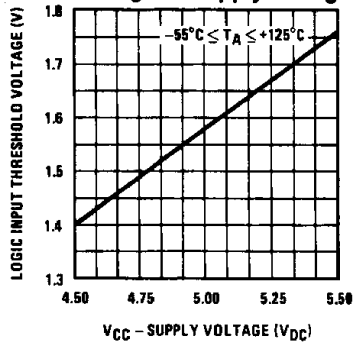
Functional Diagram



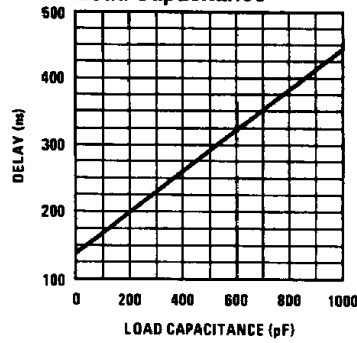
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Typical Performance Characteristics

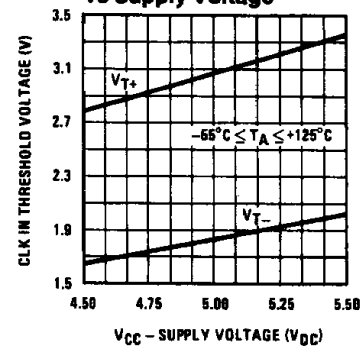
Logic Input Threshold Voltage vs Supply Voltage



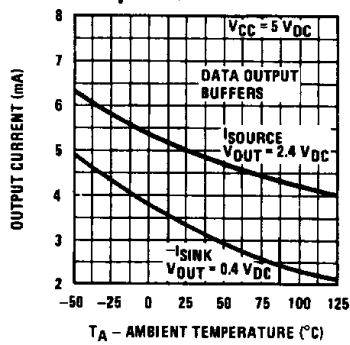
Delay from Falling Edge of RD to Output Data Valid vs Load Capacitance



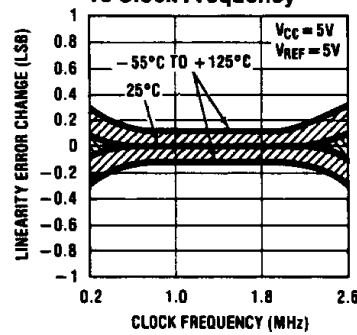
CLK IN Schmitt Trip Levels vs Supply Voltage



Output Current vs Temperature

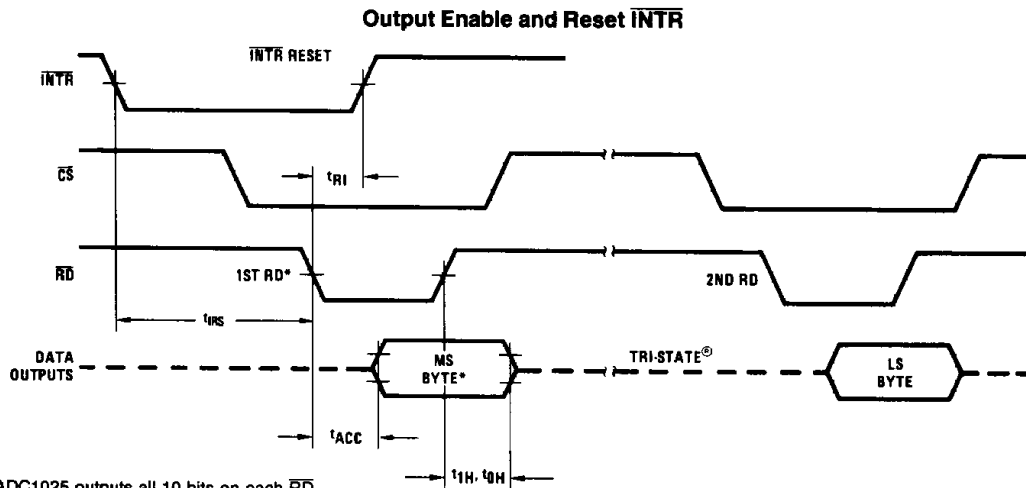
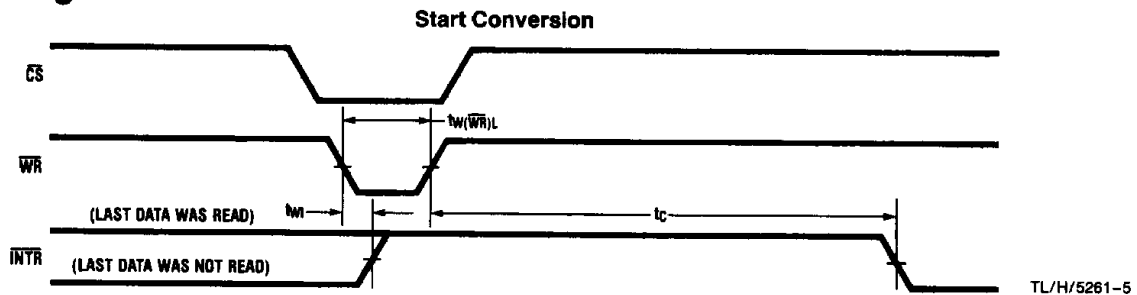


Typical Linearity Error vs Clock Frequency



TL/H/5261-4

Timing Diagrams



*The 24-pin ADC1025 outputs all 10 bits on each $\overline{RD}$

Note: All timing is measured from the 50% voltage points.

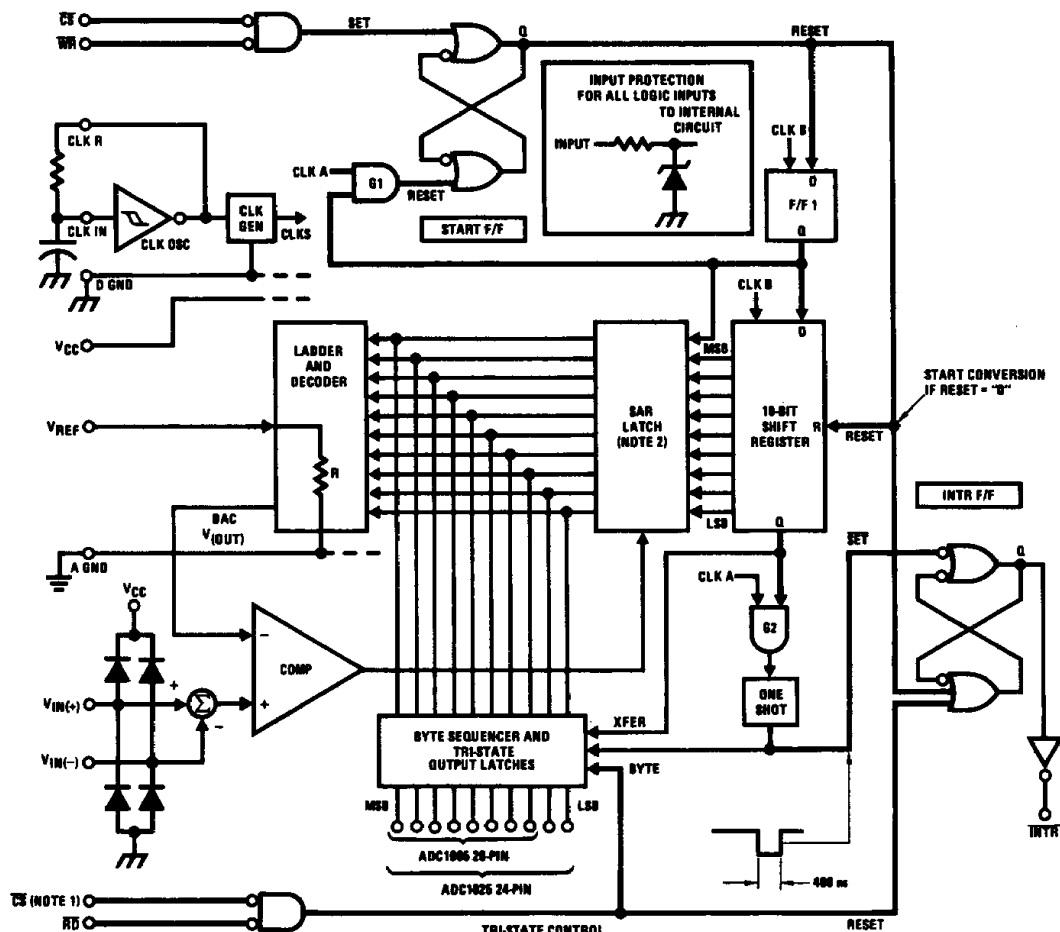
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Timing Diagrams (Continued)

Byte Sequencing for the 20-Pin ADC1005

Byte Order	8-Bit Data Bus Connection							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1st	MSB Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
2nd	Bit 1	LSB Bit 0	0	0	0	0	0	0

Block Diagram



Note 1: CS shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

TRI-STATE CONTROL
"1" = OUTPUT ENABLE

FIGURE 1.

TL/H/5261-11

Functional Description

1.0 GENERAL OPERATION

A block diagram of the A/D converter is shown in *Figure 1*. All of the inputs and outputs are shown and the major logic control paths are drawn in heavier weight lines.

1.1 Converter Operation

The ADC1005, ADC1025 use an advanced potentiometric resistive ladder network. The analog inputs, as well as the taps of this ladder network are switched into a weighted capacitor array. The output of this capacitor array is the input to a sampled data comparator. This comparator allows the successive approximation logic to match the analog input voltage $[V_{IN}(+) - V_{IN}(-)]$ to taps on the R network. The most significant bit is tested first and after 10 comparisons (80 clock cycles) a digital 10-bit binary code (all "1"s = full-scale) is transferred to an output latch.

1.2 Starting a Conversion

The conversion is initialized by taking $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 10-bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 10-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 10-bit shift register then can have the "1" clocked in, allowing the conversion process to continue. If the set signal were still present, this reset pulse would have no effect and the 10-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals. The converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

To summarize, on the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start after at least one of these inputs makes a low-to-high transition.*

1.3 Output Control

After the "1" is clocked through the 10-bit shift register (which completes the SAR search) it causes the new digital word to transfer to the TRI-STATE output latches. When the XFER signal makes a high-to-low transition the one shot fires, setting the INTR F/F. An inverting buffer then supplies the INTR output signal.

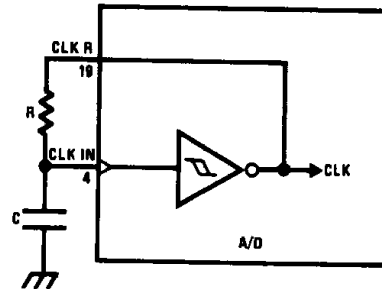
Note that this $\overline{SET}$ control of the INTR F/F remains low for approximately 400 ns. If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low) the INTR output will still signal the end of the conversion (by a high-to-low transition). This is because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level. This INTR output will therefore stay low for the duration of the $\overline{SET}$ signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled.

1.4 Free-Running and Self-Clocking Modes

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the INTR output. This $\overline{WR}$ and INTR node should be momentarily forced to logic low following a power-up cycle to ensure start up.

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN makes use of a Schmitt trigger as shown in *Figure 2*.



TL/H/5261-12

$$f_{CLK} \approx \frac{1}{1.1 RC}$$

FIGURE 2. Self-Clocking the A/D

2.0 REFERENCE VOLTAGE

The voltage applied to the reference input of these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 1024 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 4.8 k Ω . This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 3a*) the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC} . This technique relaxes the stability requirements of the system references as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 3b*), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be small to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout, and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/1024$).

Functional Description (Continued)

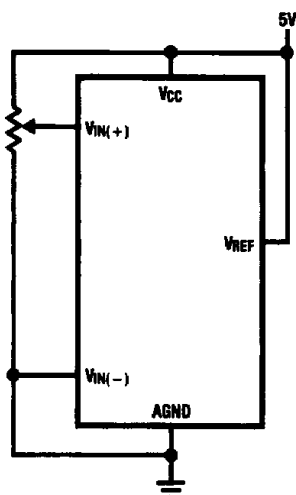


FIGURE 3a. Ratiometric

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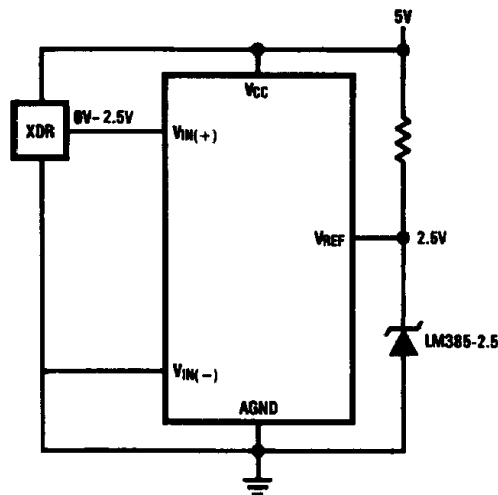


FIGURE 3b. Absolute with a Reduced Span

TL/H/5261-18

3.0 THE ANALOG INPUTS

3.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential inputs of these converters reduce the effects of common-mode input noise, which is defined as noise common to both selected "+" and "-" inputs (60 Hz is most typical). The time interval between sampling the "+" input and the "-" input is half of an internal clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal, this error is:

$$V_{\text{ERROR(MAX)}} = V_{\text{PEAK}} (2\pi f_{\text{CM}}) \times \frac{4}{f_{\text{CLK}}}$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value and f_{CLK} is the clock frequency at the CLK IN pin.

For a 60 Hz common-mode signal to generate a 1/4 LSB error (1.2 mV) with the converter running at 1.8 MHz, its peak value would have to be 1.46V. A common-mode signal this large is much greater than that generally found in data acquisition systems.

3.2 Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "-" input at the clock rising edges during the conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period.

3.3 Input Bypass Capacitors

Bypass capacitors at the inputs will average the current spikes noted in 3.2 and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{\text{IN}(+)}$ input voltage at full scale. For continuous conversions with a 1.8 MHz clock frequency with the $V_{\text{IN}(+)}$

input at 5V, this DC current is at a maximum of approximately 5 μA . Therefore, *bypass capacitors should not be used at the analog inputs or the V_{REF} pin* for high resistance sources ($>1 \text{ k}\Omega$). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a linear function of the differential input voltage.

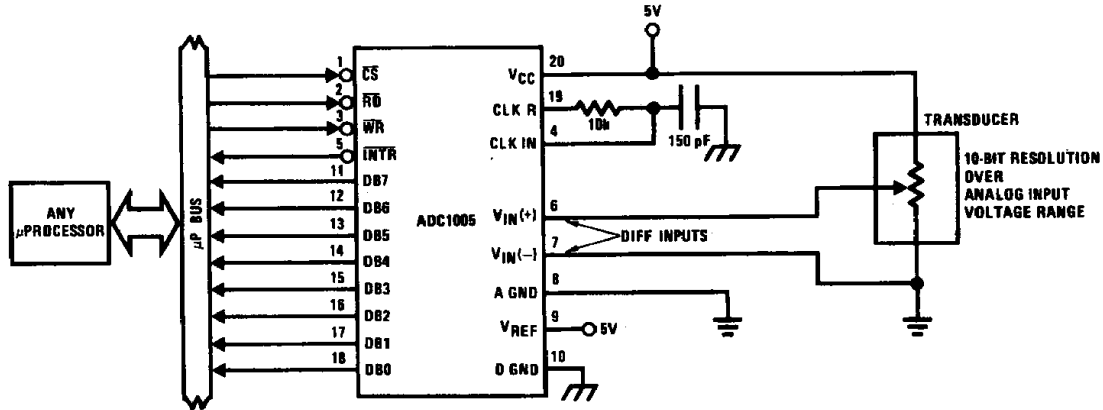
3.4 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* if the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($\leq 1 \text{ k}\Omega$) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications ($\leq 0.1 \text{ k}\Omega$) a 4700 pF bypass capacitor at the inputs will prevent pickup due to series lead inductance of a long wire. A 100 Ω series resistor can be used to isolate this capacitor – both the R and the C are placed outside the feedback loop – from the output of an op amp, if used.

3.5 Noise

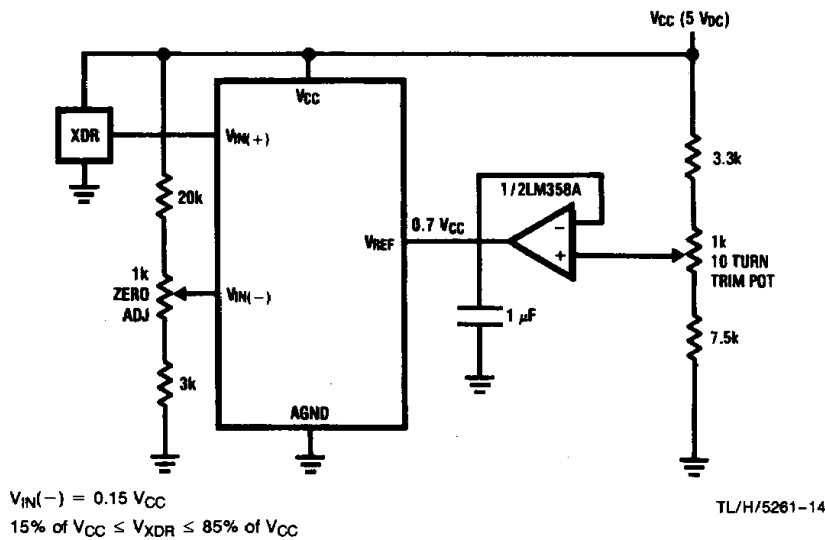
The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 1 k Ω . Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, can reduce system noise pickup but can create analog scale errors. See section 3.2, 3.3, and 3.4 if input filtering is to be used.

Typical Applications



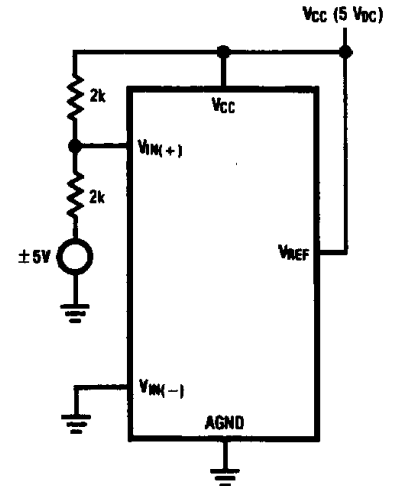
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Operating with Ratimetric Transducers



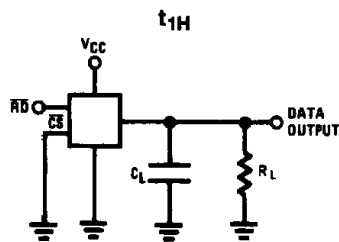
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Handling $\pm 5V$ Analog Inputs



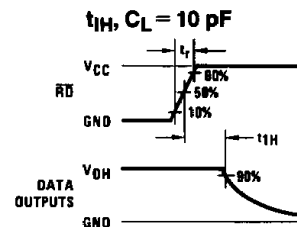
TL/H/5261-15

TRI-STATE Test Circuits and Waveforms

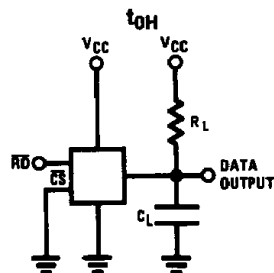


TL/H/5261-7

$t_r = 20 \text{ ns}$

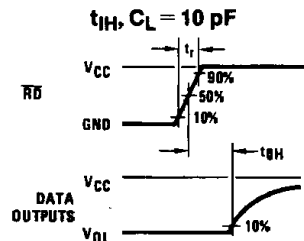


TL/H/5261-9



TL/H/5261-8

$t_r = 20 \text{ ns}$



TL/H/5261-10

Ordering Information

Part Number	Package Outline	Temperature Range	Linearity Error
ADC1005BCN	N20A	0°C to +70°C	± ½ LSB
ADC1025BCN	N24C		
ADC1005BCV	V20A		
ADC1025BCV	V28A		
ADC1005BCJ-1	J20A		
ADC1025BCJ-1	J24F		
ADC1005BCJ	J20A	-40°C to +85°C	
ADC1025BCJ	J24F		
ADC1005BJ	J20A	-55°C to +125°C	
ADC1025BJ	J24F		

Part Number	Package Outline	Temperature Range	Linearity Error
ADC1005CCN	N20A	0°C to +70°C	±1 LSB
ADC1025CCN	N24C		
ADC1005CCV	V20A		
ADC1025CCV	V28A		
ADC1005CCJ-1	J20A		
ADC1025CCJ-1	J24F		
ADC1005CCJ	J20A	−40°C to +85°C	
ADC1025CCJ	J24F		
ADC1005CJ	J20A	−55°C to +125°C	
ADC1025CJ	J24F		