

74HC574-Q100; 74HCT574-Q100

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 6 — 5 August 2024

Product data sheet

1. General description

The 74HC574-Q100; 74HCT574-Q100 is an 8-bit positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable (\overline{OE}) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC574-Q100: CMOS level
 - For 74HCT574-Q100: TTL level
- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- DHVQFN package with Side-Wettable Flanks enabling Automated Optical Inspection (AOI) of solder joints

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC574D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT574D-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HC574BQ-Q100	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

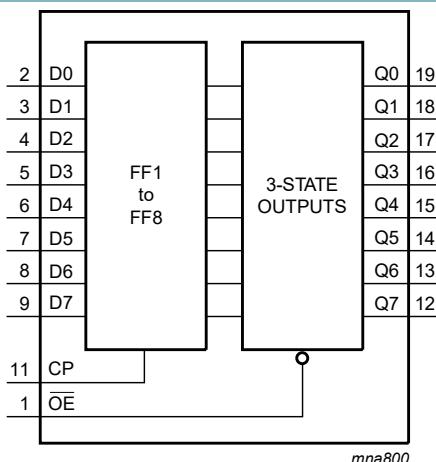


Fig. 1. Functional diagram

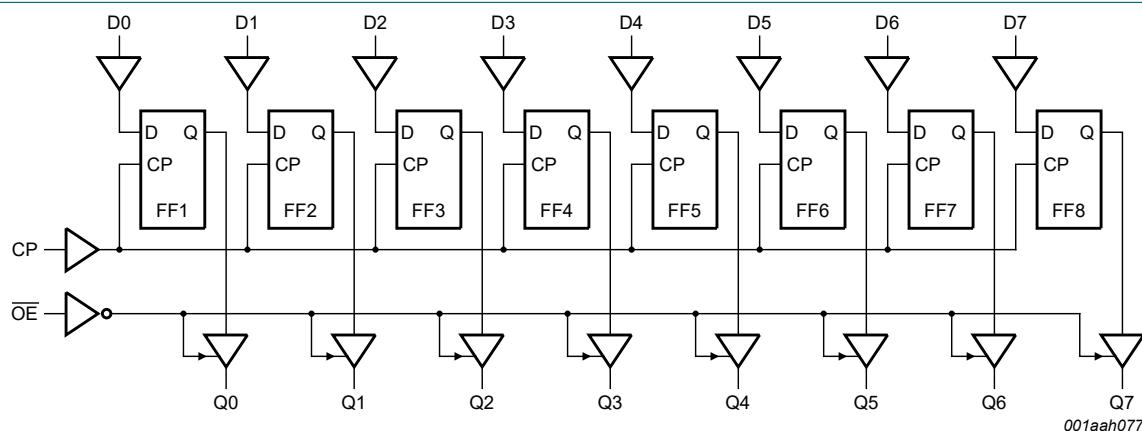


Fig. 2. Logic diagram

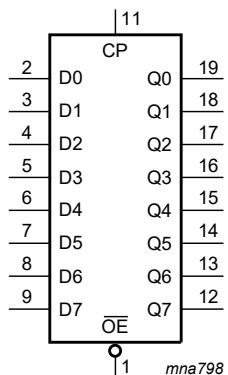


Fig. 3. Logic symbol

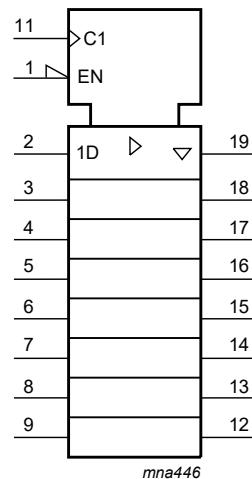
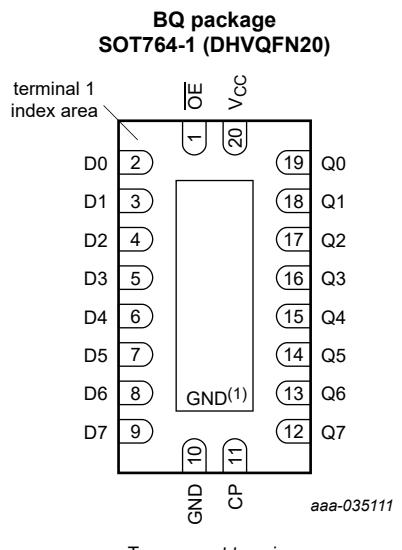
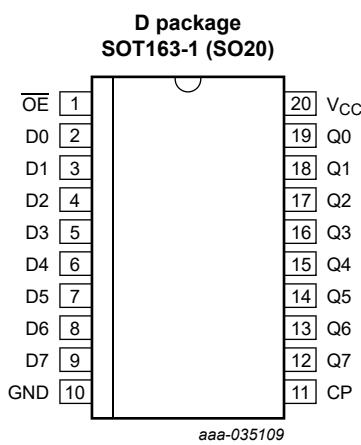


Fig. 4. IEC logic symbol

5. Pinning information

5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
OE	1	3-state output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data inputs
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	3-state flip-flop outputs
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one setup time prior to the HIGH-to-LOW CP transition;

L = LOW voltage level; l = LOW voltage level one setup time prior to the HIGH-to-LOW CP transition;

Z = high-impedance OFF-state; ↑ = LOW-to-HIGH clock transition.

Operating mode	Input			Internal flip-flop	Output
	OE	CP	Dn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable output	H	↑	l	L	Z
	H	↑	h	H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±35	mA
I _{CC}	supply current		-	+70	mA
I _{GND}	ground current		-	-70	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation		[1]	-	500 mW

[1] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.

For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC574-Q100			74HCT574-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC574-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 6.0 V; V _O = V _{CC} or GND	-	-	±0.5	-	±5.0	-	±10.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT574-Q100										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = -20 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -6 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = 20 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6.0 \text{ mA}$	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC} \text{ or GND}; V_{CC} = 5.5 \text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 5.5 \text{ V}; V_O = V_{CC} \text{ or GND}$	-	-	± 0.5	-	± 5.0	-	± 10	μA
I_{CC}	supply current	$V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 2.1 \text{ V}; \text{other inputs at } V_{CC} \text{ or GND}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; I_O = 0 \text{ A}$								
		per input pin; D _n inputs	-	50	180	-	225	-	245	μA
		per input pin; \overline{OE} input	-	125	450	-	563	-	613	μA
		per input pin; CP input	-	150	540	-	675	-	735	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Fig. 8](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC574-Q100										
t_{pd}	propagation delay	CP to Qn; see Fig. 5 [1]								
		$V_{CC} = 2.0 \text{ V}$	-	47	150	-	190	-	225	ns
		$V_{CC} = 4.5 \text{ V}$	-	17	30	-	35	-	45	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	14	26	-	33	-	38	ns
t_{en}	enable time	OE to Qn; see Fig. 7 [2]								
		$V_{CC} = 2.0 \text{ V}$	-	44	140	-	175	-	210	ns
		$V_{CC} = 4.5 \text{ V}$	-	16	28	-	35	-	42	ns
		$V_{CC} = 6.0 \text{ V}$	-	13	24	-	30	-	36	ns
t_{dis}	disable time	OE to Qn; see Fig. 7 [3]								
		$V_{CC} = 2.0 \text{ V}$	-	39	125	-	155	-	190	ns
		$V_{CC} = 4.5 \text{ V}$	-	14	25	-	31	-	38	ns
		$V_{CC} = 6.0 \text{ V}$	-	11	21	-	26	-	32	ns
t_t	transition time	Qn; see Fig. 5 [4]								
		$V_{CC} = 2.0 \text{ V}$	-	14	60	-	75	-	90	ns
		$V_{CC} = 4.5 \text{ V}$	-	5	12	-	15	-	18	ns
		$V_{CC} = 6.0 \text{ V}$	-	4	10	-	13	-	15	ns
t_w	pulse width	CP HIGH or LOW; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	4	-	17	-	20	-	ns
t_{su}	set-up time	Dn to CP; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	60	6	-	75	-	90	-	ns
		$V_{CC} = 4.5 \text{ V}$	12	2	-	15	-	18	-	ns
		$V_{CC} = 6.0 \text{ V}$	10	2	-	13	-	15	-	ns
t_h	hold time	Dn to CP; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	5	0	-	5	-	5	-	ns
		$V_{CC} = 4.5 \text{ V}$	5	0	-	5	-	5	-	ns
		$V_{CC} = 6.0 \text{ V}$	5	0	-	5	-	5	-	ns
f_{max}	maximum frequency	CP; see Fig. 5								
		$V_{CC} = 2.0 \text{ V}$	6.0	37	-	4.8	-	4.0	-	MHz
		$V_{CC} = 4.5 \text{ V}$	30	112	-	24	-	20	-	MHz
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	123	-	-	-	-	-	MHz
		$V_{CC} = 6.0 \text{ V}$	35	133	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ [5]	-	22	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT574-Q100										
t_{pd}	propagation delay	CP to Qn; see Fig. 5 [1]								
		$V_{CC} = 4.5 \text{ V}$	-	18	33	-	41	-	50	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	15	-	-	-	-	-	ns
t_{en}	enable time	OE to Qn; see Fig. 7 [2]								
		$V_{CC} = 4.5 \text{ V}$	-	19	33	-	41	-	50	ns
t_{dis}	disable time	OE to Qn; see Fig. 7 [3]								
		$V_{CC} = 4.5 \text{ V}$	-	16	28	-	35	-	42	ns
t_t	transition time	Qn; see Fig. 5 [4]								
		$V_{CC} = 4.5 \text{ V}$	-	5	12	-	15	-	18	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 6								
		$V_{CC} = 4.5 \text{ V}$	16	7	-	20	-	24	-	ns
t_{su}	set-up time	Dn to CP; see Fig. 6								
		$V_{CC} = 4.5 \text{ V}$	12	3	-	15	-	18	-	ns
t_h	hold time	Dn to CP; see Fig. 6								
		$V_{CC} = 4.5 \text{ V}$	5	-1	-	5	-	5	-	ns
f_{max}	maximum frequency	CP; see Fig. 5								
		$V_{CC} = 4.5 \text{ V}$	30	69	-	24	-	20	-	MHz
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	76	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz};$ [5] $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$	-	25	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_{en} is the same as t_{PZH} and t_{PZL} .

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[4] t_t is the same as t_{THL} and t_{TLH} .

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

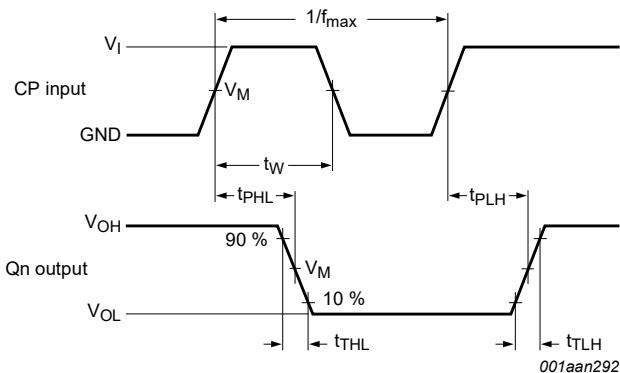
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

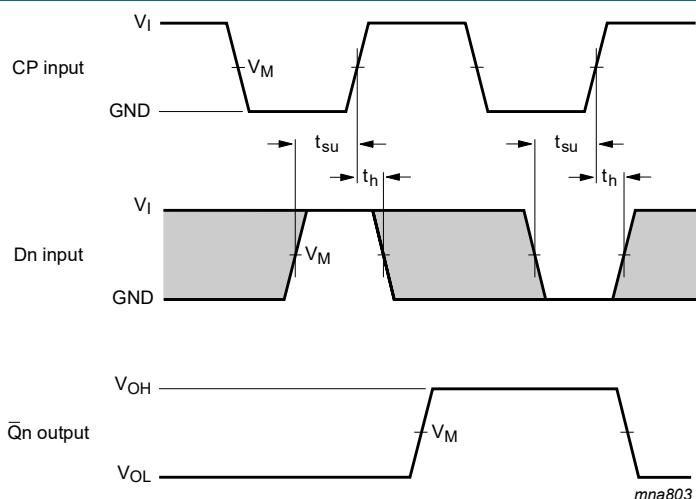
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

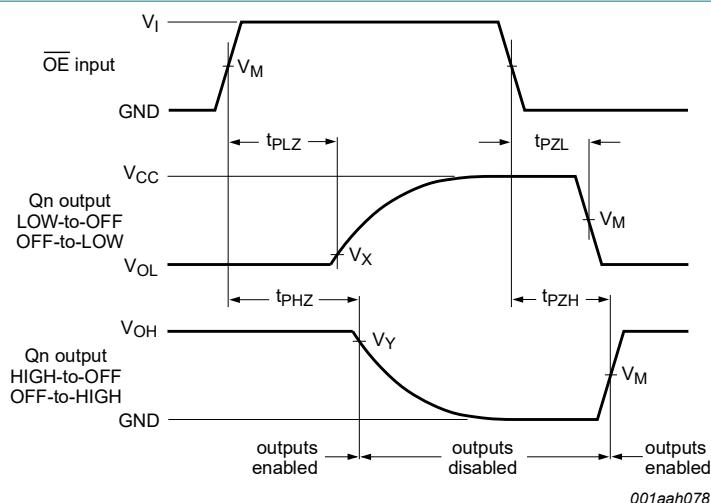
Fig. 5. Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times



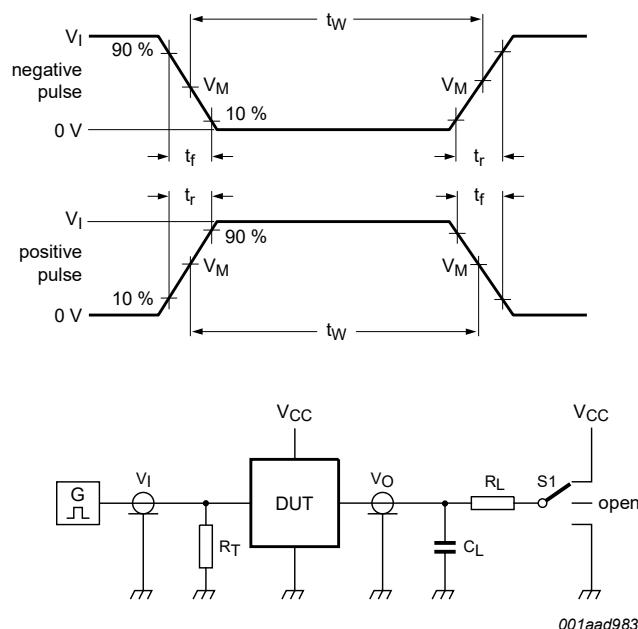
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Enable and disable times

Table 8. Measurement points

Type	Input	Output		
		V_M	V_X	V_Y
74HC574-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$
74HCT574-Q100	1.3 V	1.3 V	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

$S1$ = Test selection switch.

Fig. 8. Test circuit for measuring switching times

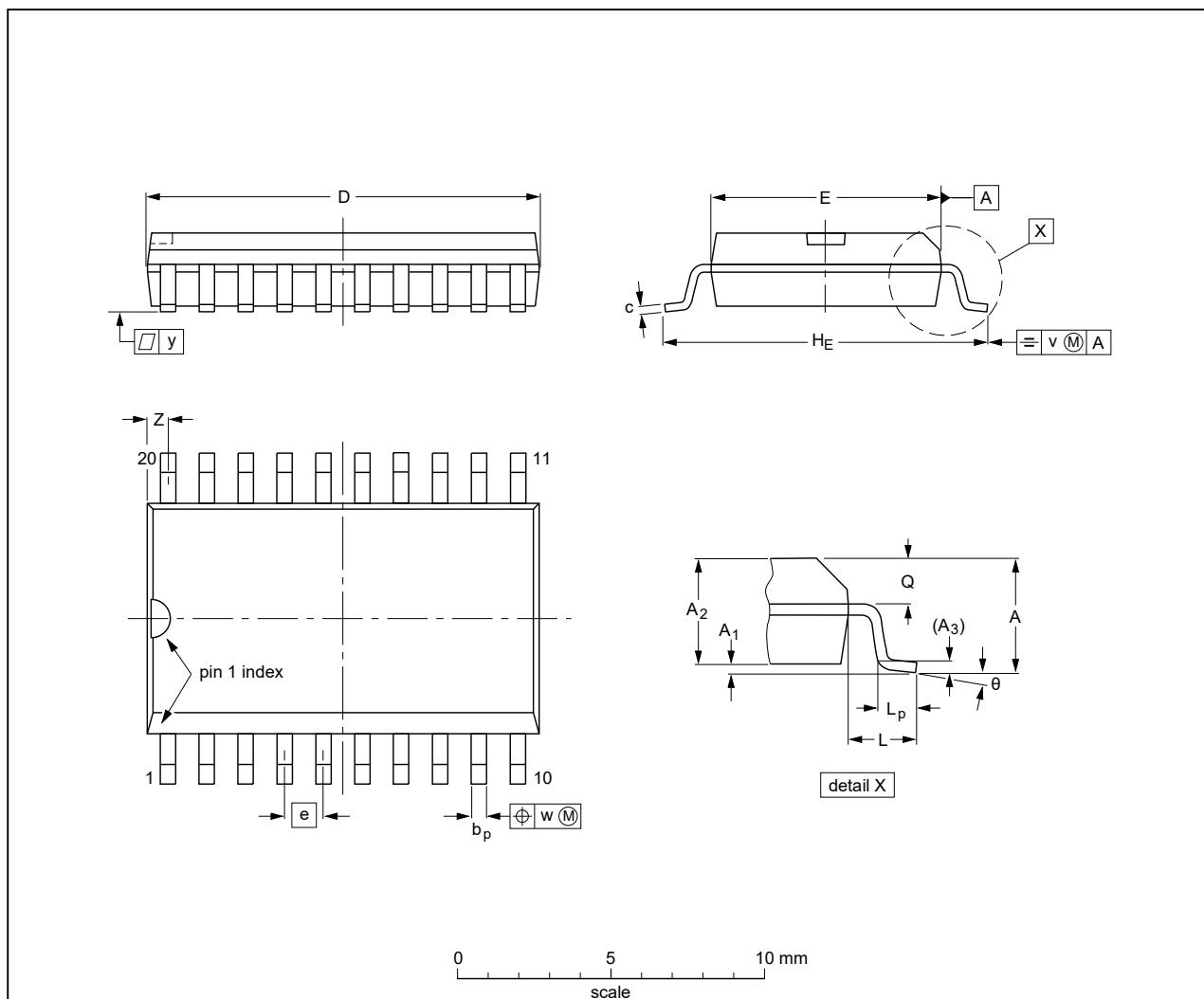
Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC574-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT574-Q100	3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ	
mm	2.65	0.3	2.45	0.25	0.49	0.32	13.0	7.6	1.27	10.65	1.4	1.1	1.1	0.25	0.25	0.1	0.9	8°	
inches	0.1	0.012	0.096	0.01	0.019	0.013	0.51	0.30	0.05	10.00	0.055	0.043	1.0	0.016	0.039	0.004	0.035	0.016	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Fig. 9. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

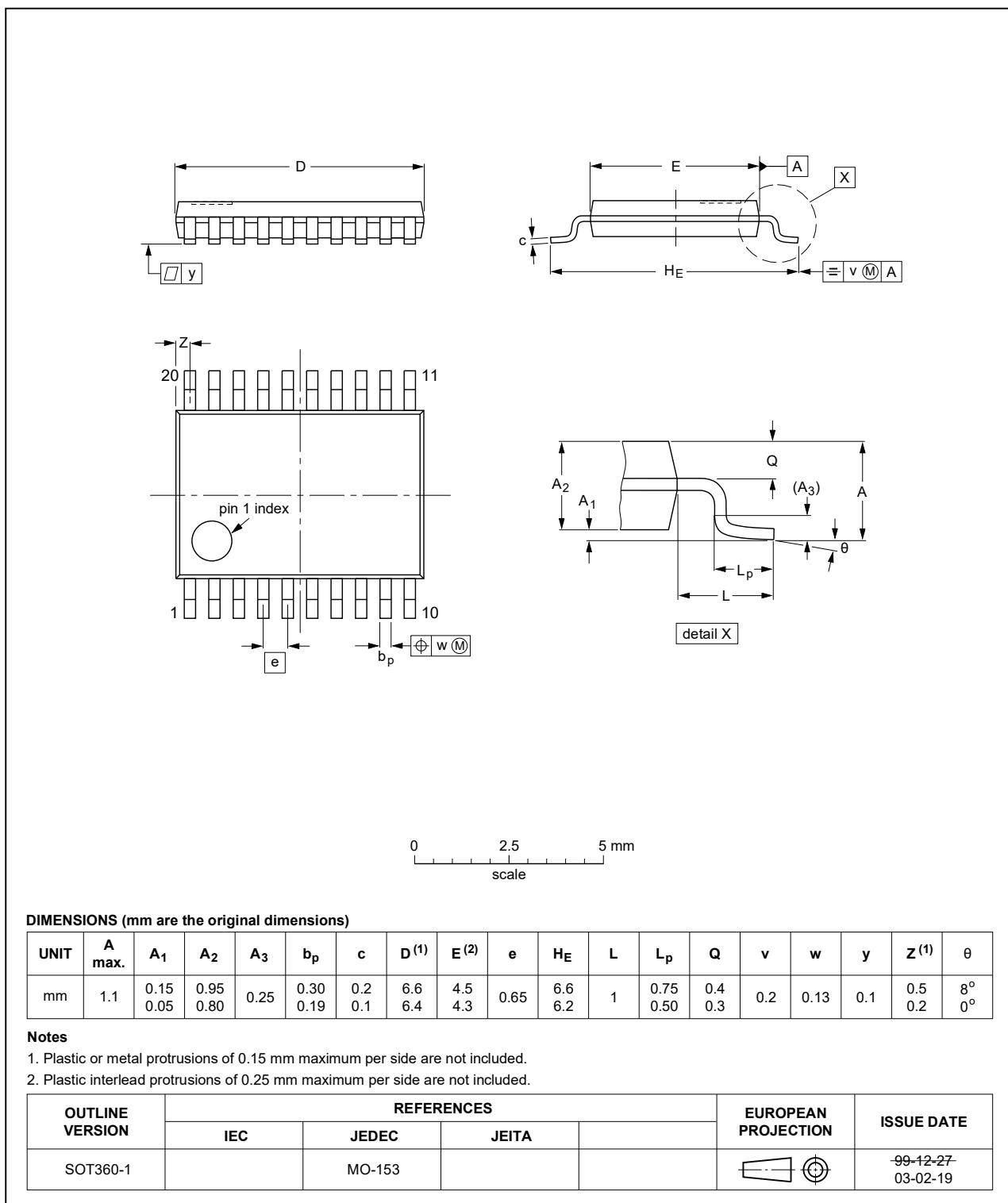


Fig. 10. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

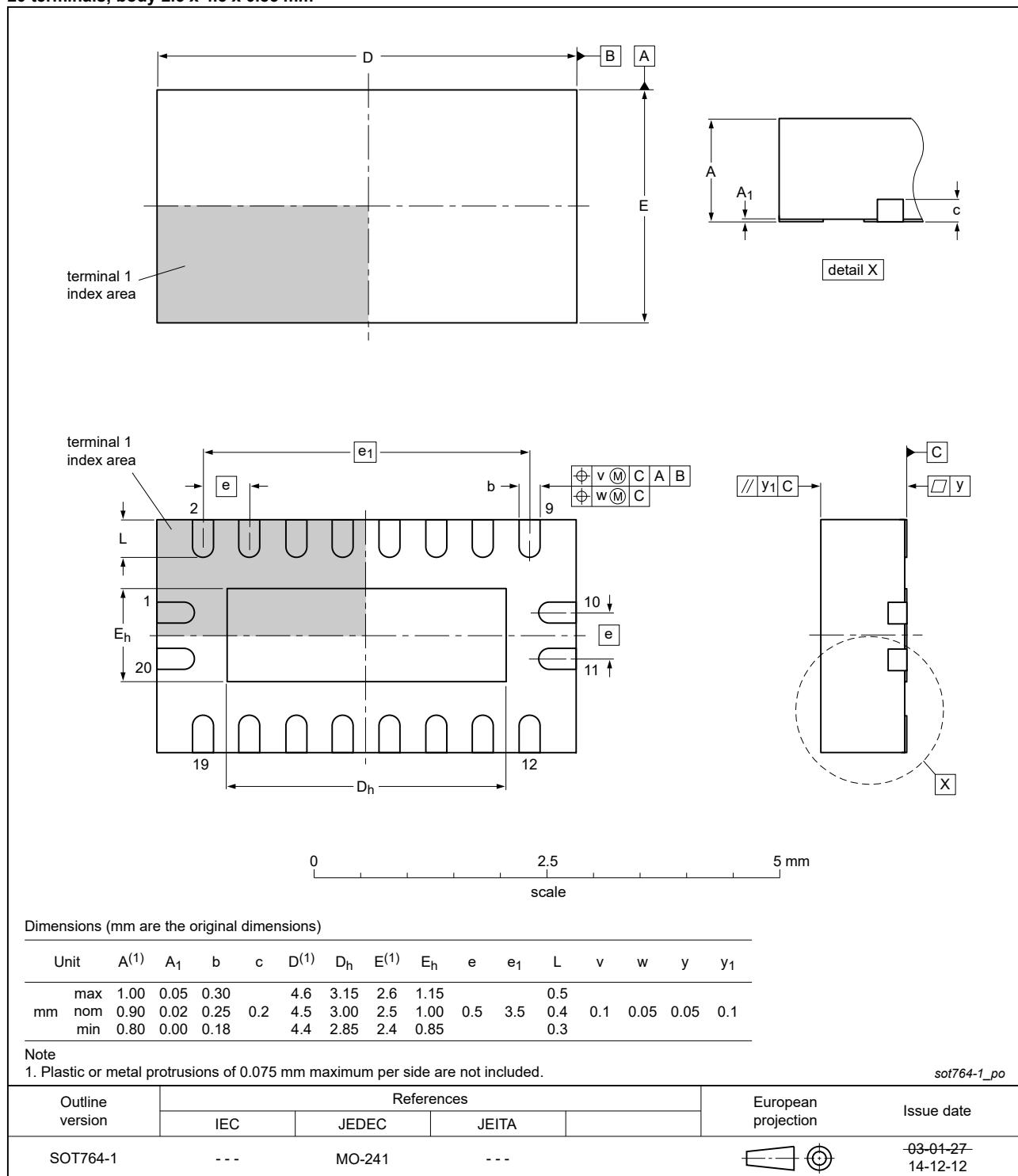


Fig. 11. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT574_Q100 v.6	20240805	Product data sheet	-	74HC_HCT574_Q100 v.5
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74HC_HCT574_Q100 v.5	20221020	Product data sheet	-	74HC_HCT574_Q100 v.4
Modifications:	<ul style="list-style-type: none"> Section 5.1 updated. 			
74HC_HCT574_Q100 v.4	20220713	Product data sheet	-	74HC_HCT574_Q100 v.3
Modifications:	<ul style="list-style-type: none"> Type number 74HC574BQ-Q100 (SOT764-1/DHVQFN20) added. 			
74HC_HCT574_Q100 v.3	20210730	Product data sheet	-	74HC_HCT574_Q100 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation updated. 			
74HC_HCT574_Q100 v.2	20150126	Product data sheet	-	74HC_HCT574_Q100 v.1
Modifications:	<ul style="list-style-type: none"> Table 7: Power dissipation capacitance condition for 74HCT574-Q100 is corrected. 			
74HC_HCT574_Q100 v.1	20120802	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This Nexperia product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or

equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

1. General description.....	1
2. Features and benefits.....	1
3. Ordering information.....	2
4. Functional diagram.....	2
5. Pinning information.....	4
5.1. Pinning.....	4
5.2. Pin description.....	4
6. Functional description.....	5
7. Limiting values.....	5
8. Recommended operating conditions.....	5
9. Static characteristics.....	6
10. Dynamic characteristics.....	8
10.1. Waveforms and test circuit.....	10
11. Package outline.....	13
12. Abbreviations.....	16
13. Revision history.....	16
14. Legal information.....	17

© Nexperia B.V. 2024. All rights reserved

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

Date of release: 5 August 2024