DEMO MANUAL DC1751A

LTM9011-14, LTM9010-14, LTM9009-14, LTM9008-14, LTM9007-14, LTM9006-14: 14-Bit, 125/105/80/65/40/25Msps Octal ADC Family

DESCRIPTION

DC1751 supports the LTM®9011 high speed, octal ADC family.

The versions of the 1751A demo board are listed in Table 1. Depending on the required resolution and sample rate, the DC1751 is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from DC to 70MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo

Table 1. DC1751 Variants

DC1751 Variants	ADC Part Number	Resolution	Maximum Sample Rate	Input Frequency
1751A-A	LTM9011-14	14-Bit	125Msps	DC-70MHz
1751A-B	LTM9010-14	14-Bit	105Msps	DC-70MHz
1751A-C	LTM9009-14	14-Bit	80Msps	DC-70MHz
1751A-D	LTM9008-14	14-Bit	65Msps	DC-70MHz
1751A-E	LTM9007-14	14-Bit	40Msps	DC-70MHz
1751A-F	LTM9006-14	14-Bit	25Msps	DC-70MHz

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage – DC1751A	Depending on Sampling Rate and the A/D Converter Provided, This Supply Must Provide Up to 700mA	Optimized for 3.5V [3.0V to 6V Minimum/Maximum]
Analog Input Range	Depending on SENSE Pin Voltage	$1V_{P-P}$ to $2V_{P-P}$
Logic Input Voltages	Minimum Logic High	1.3V
	Maximum Logic Low	0.6V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode)	350mV/1.25V Common Mode
	Minimum Logic Levels (100Ω Load, 3.5mA Mode)	247mV/1.25V Common Mode
Sampling Frequency (Convert Clock Frequency)		See Table 1
Encode Clock Level	Single-Ended Encode Mode (ENC^- Tied to GND)	0V to 3.6V
Encode Clock Level	Differential Encode Mode (ENC^- Not Tied to GND)	0.2V to 3.6V
Resolution		See Table 1
Input Frequency Range		See Table 1
SFDR		See Applicable Data Sheet
SNR		See Applicable Data Sheet

QUICK START PROCEDURE

DC1751 is easy to set up to evaluate the performance of the LTM9011 A/D converters. For proper measurement equipment setup, refer to Figure 1 and follow the procedure explained in the following sections. Figure 2 shows the pinout of the analog input header.

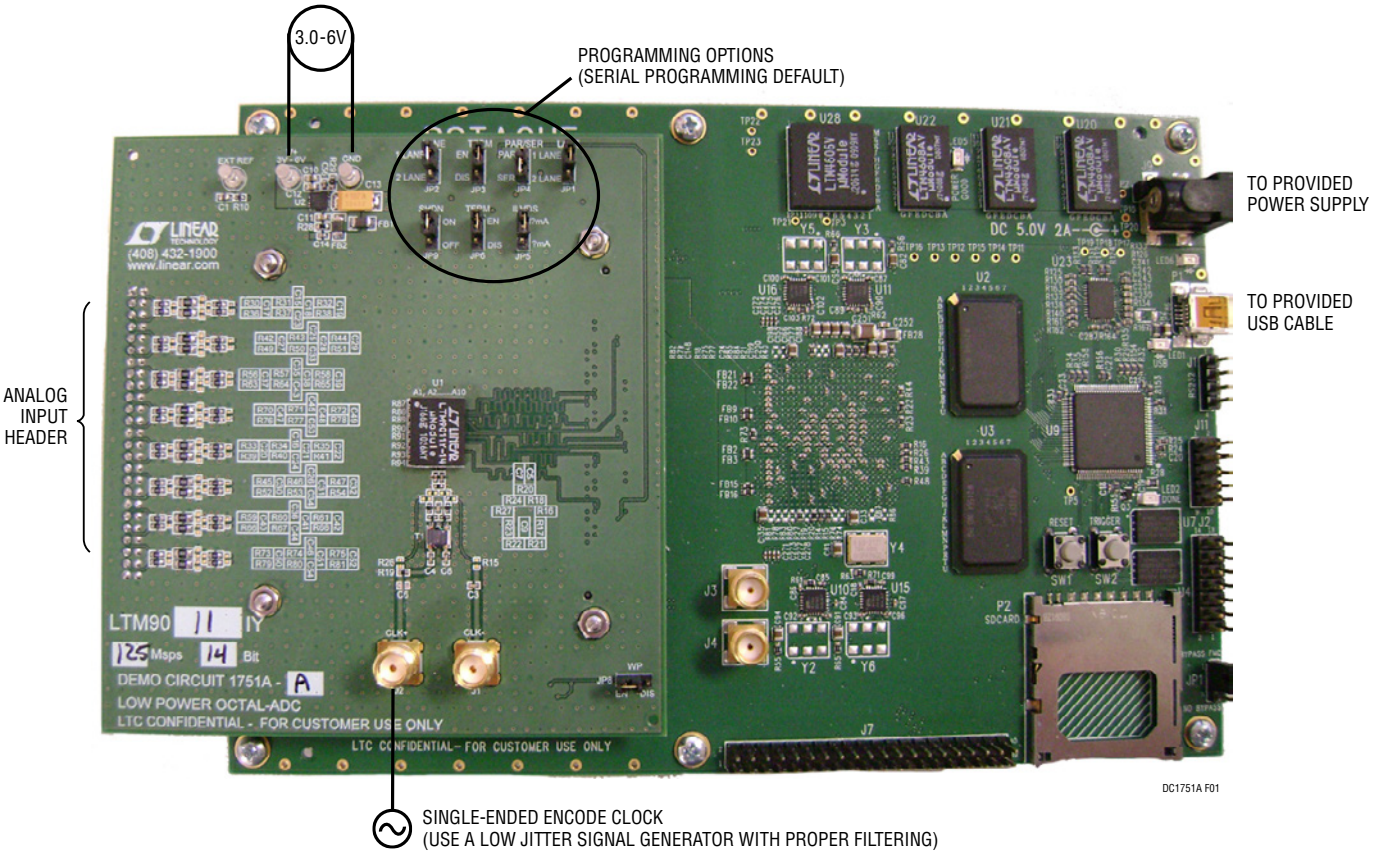


Figure 1. Test Setup of DC1751

QUICK START PROCEDURE

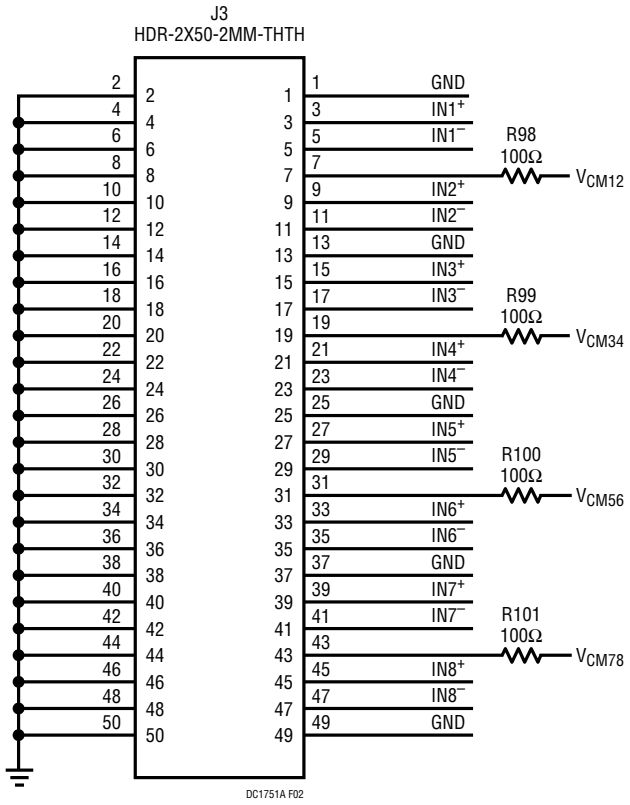


Figure 2. Pinout for Analog Input Header (J3)

QUICK START PROCEDURE

Setup

If a DC1371 data acquisition and collection system was supplied with the DC1751, follow the DC1371 Quick Start Guide to install the required software and to connect the DC1371 to the DC1751 and to a PC.

DC1751 Board Jumpers

The DC1751 board should have the following jumper settings as default positions (as per Figure 1):

JP4: PAR/SER: Selects Parallel or Serial Programming Mode. (Default: Serial)

Optional Jumpers JP3 and JP6: Term: Enables/Disable Optional Output Termination. (Default: Removed)

JP5: I_{LVDS}: Selects Either 1.75mA or 3.5mA of Output Current for the LVDS Drivers. (Default: Removed)

JP1 and JP2: Lane: Selects Either 1-Lane or 2-Lane Output Modes (Default: Removed)

Note: The DC1371 does not support 1-Lane operation.

JP9: SHDN: Enables and Disables the LTM9011. (Default: Removed)

JP8: WP: Enable/Disables Write Protect for the EEPROM. (Default: Removed)

Note: Optional jumper should be left open to ensure proper serial configuration.

Applying Power and Signals to the DC1751

The DC1371 is used to acquire data from the DC1751. The DC1371 must first be connected to a powered USB port and have 5V applied power before applying 3.5V across the pins marked V^+ and GND on the DC1751. DC1751 requires 3.5V for proper operation.

The DC1751 demonstration circuit requires up to 700mA depending on the sampling rate and the A/D converter supplied.

The DC1751 should not be removed or connected to the DC1371 while power is applied.

Analog Input Network

For optimal distortion and noise performance, the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 70MHz, refer to the LTM9011 data sheet for a proper input network.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a gallium arsenide gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and high IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demonstration circuit.

Apply the analog input signals of interest to the header on the DC1751 board marked “JP7.” There is access to the eight analog inputs, as well as the four common mode voltages. For a pinout of this header, see Figure 2 or the Schematic Diagrams.

QUICK START PROCEDURE

Encode Clock

Note: Apply an encode clock to the SMA connector on the DC1751 demonstration circuit board marked "J2 CLK^+." As a default, the DC1751 is populated to have a single-ended input.

For the best noise performance, the ENCODE input must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator, a squaring circuit can be used. Linear Technology also provides demo board DC1075A that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTM9011.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1751 a bandpass filter used for the clock should be used prior to the DC1075A. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used for both the clock input and the analog input.

Digital Outputs

Data outputs, data clock, and frame clock signals are available on J3 of the DC1751. This connector follows the VITA-57/FMC standard, but all signals should be verified when using an FMC carrier card other than the DC1371.

Software

The DC1371 is controlled by the PScope system software that can be downloaded from the Linear Technology website at http://www.linear.com/software/.

To start the data collection software, "PScope.exe," which is installed by default to \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu, and browse to the PScope directory and select "PScope."

If the DC1751 is properly connected to the DC1371, PScope should automatically detect the DC1751 and configure itself accordingly.

If everything is hooked up properly and a powered and suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371 Quick Start Guide, and in the online help feature within the PScope program itself.

QUICK START PROCEDURE

Serial Programming

PScope has the ability to program the DC1751 serially through the DC1371. There are several options available in the LTM9011 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the "Set Demo Bd Options" icon on the PScope toolbar (Figure 3).

This will bring up the menu shown in Figure 4.

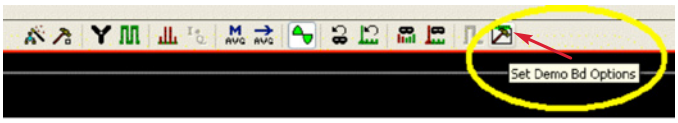


Figure 3. PScope Toolbar

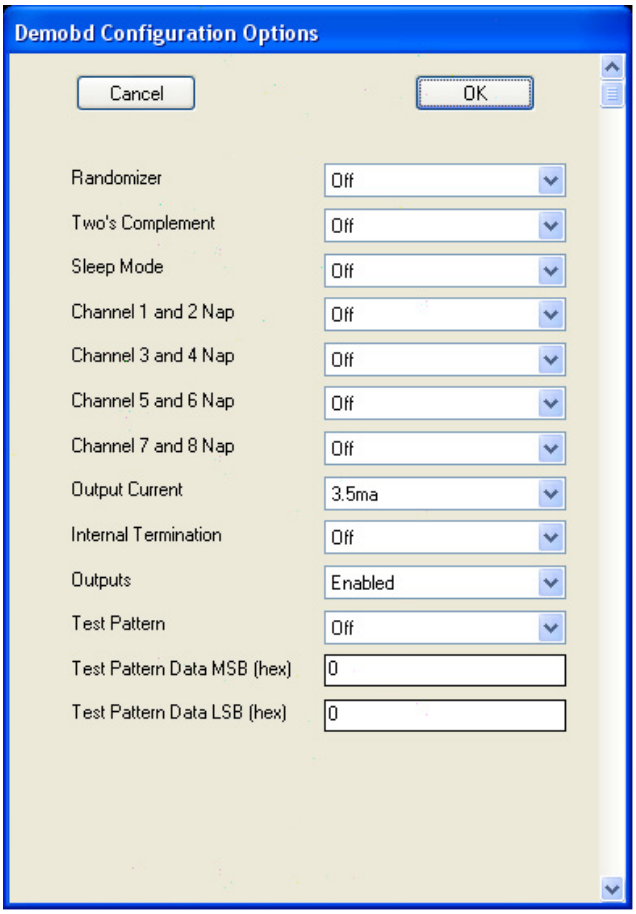


Figure 4. Demo Board Configuration Options

This menu allows any of the options available for the LTM9011 family to be programmed serially. The LTM9011 family has the following options:

Randomizer: Enables Data Output Randomizer.

- Off (Default): Disables data output randomizer.
- On: Enables data output randomizer.

Two's Complement: Enables Two's Complement Mode.

- Off (Default): Selects offset binary mode.
- On: Selects two's complement mode.

Sleep Mode: Selects Between Normal Operation and Sleep Mode.

- Off (Default): Entire ADC is powered and active.
- On: The entire ADC is powered down.

Channels 1 and 2 Nap: Selects Between Normal Operation and Putting Channels 1 and 2 in Nap Mode.

- Off (Default): Channels 1 and 2 is active.
- On: Channels 1 and 2 is in nap mode.

Channels 3 and 4 Nap: Selects Between Normal Operation and Putting Channels 3 and 4 in Nap Mode.

- Off (Default): Channels 3 and 4 is active.
- On: Channels 3 and 4 is in nap mode.

Channels 5 and 6 Nap: Selects Between Normal Operation and Putting Channels 5 and 6 in Nap Mode.

- Off (Default): Channels 5 and 6 is active.
- On: Channels 5 and 6 is in nap mode.

Channels 7 and 8 Nap: Selects Between Normal Operation and Putting Channels 7 and 8 in Nap Mode.

- Off (Default): Channels 7 and 8 is active.
- On: Channels 7 and 8 is in nap mode.

QUICK START PROCEDURE

Output Current: Selects the LVDS Output Drive Current.

- 1.75mA: LVDS output driver current.
- 2.1mA: LVDS output driver current.
- 2.5mA: LVDS output driver current.
- 3.0mA: LVDS output driver current.
- 3.5mA (Default): LVDS output driver current.
- 4.0mA: LVDS output driver current.
- 4.5mA: LVDS output driver current.

Internal Termination: Enables LVDS Internal Termination.

- Off (Default): Disables internal termination.
- On: Enables internal termination.

Outputs: Enables Digital Outputs.

- Enabled (Default): Enables digital outputs.
- Disabled: Disables digital outputs.

Test Pattern: Selects Digital Output Test Patterns. The desired test pattern can be entered into the text boxes provided.

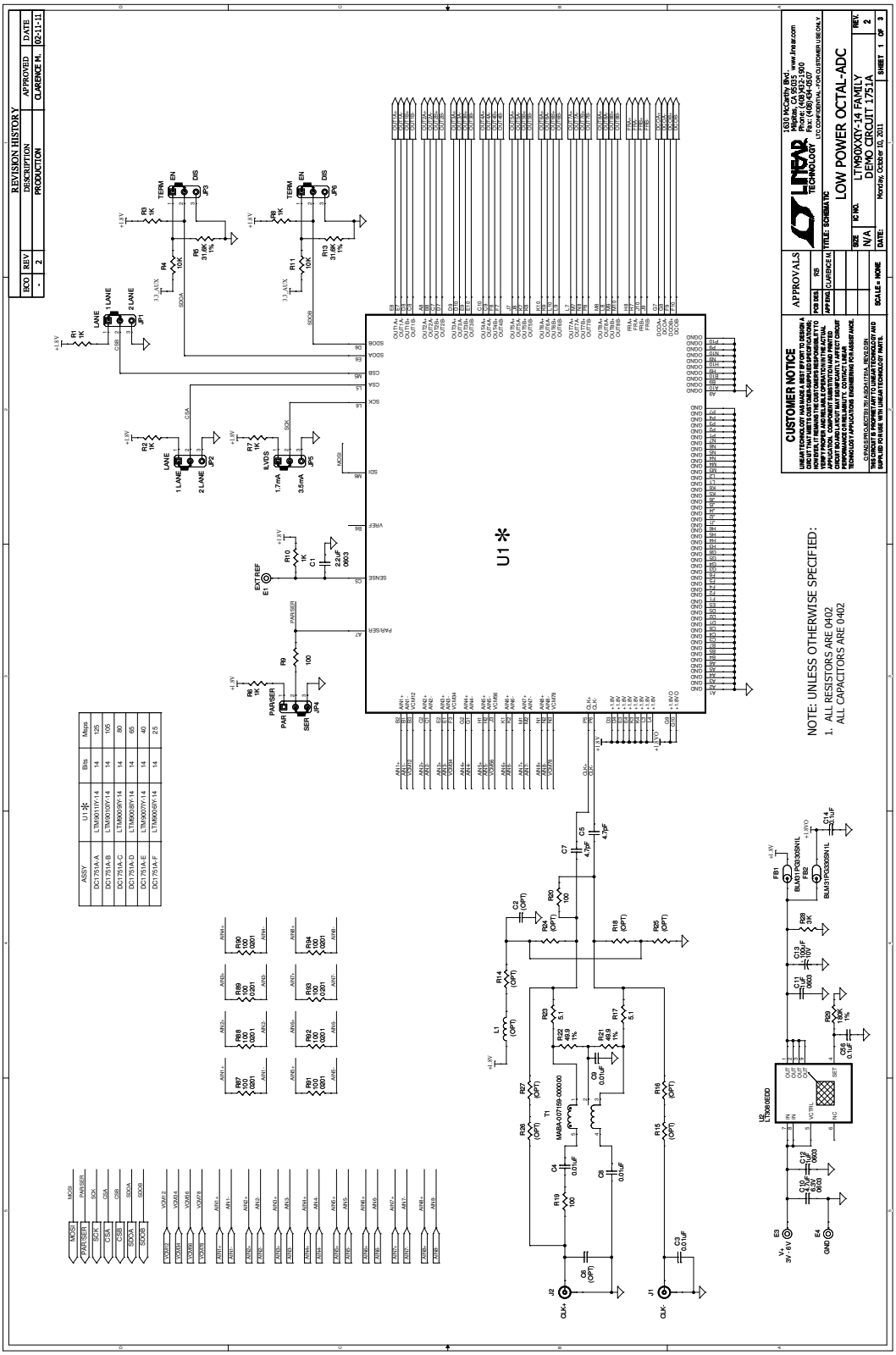
- Off (Default): ADC input data is displayed.
- On: Test pattern is displayed.

Once the desired settings are selected, click “OK” and PScope will automatically update the register of the device on the DC1751 demo board.

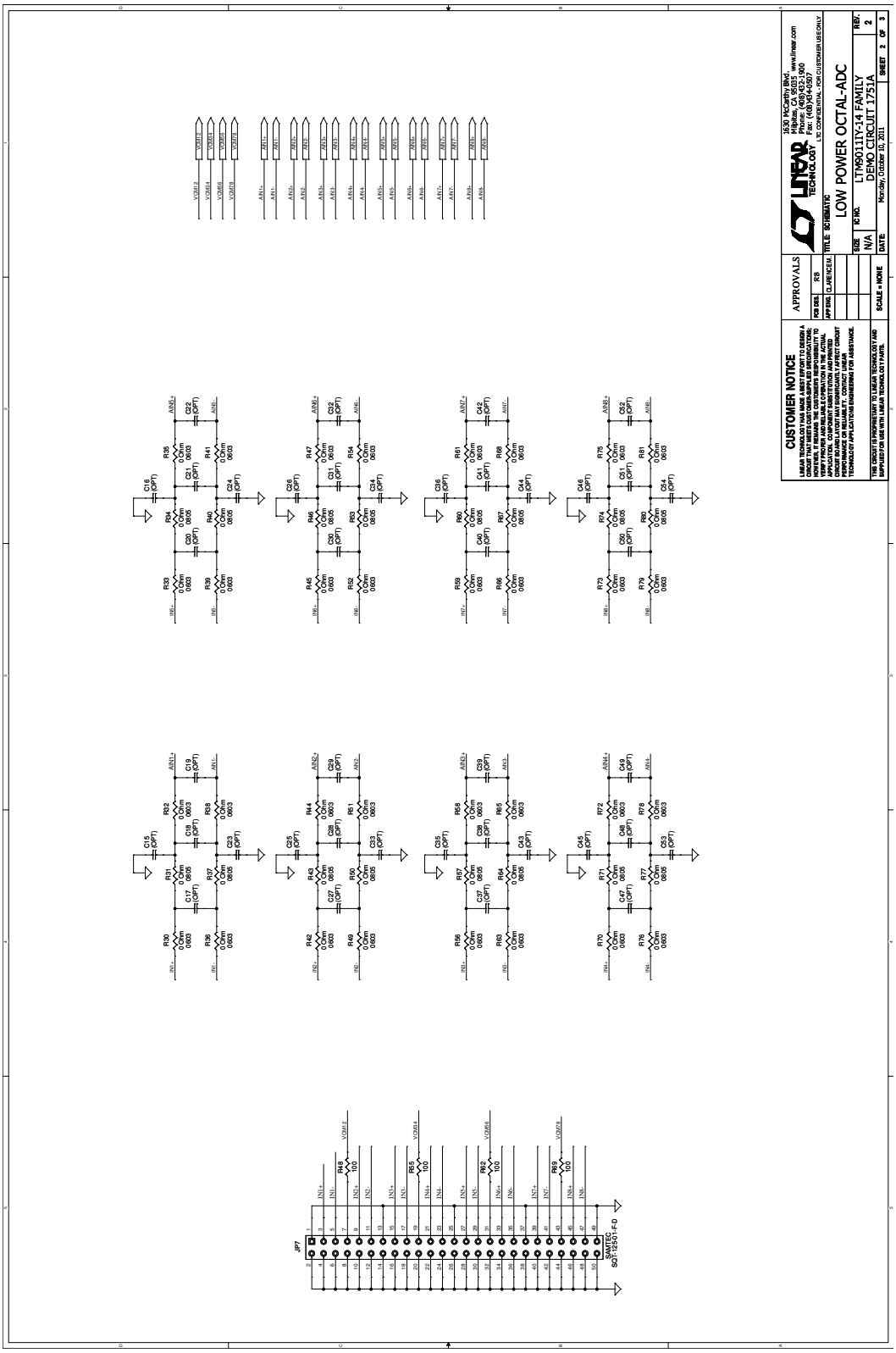
PARTS LIST

ITEM	QUANTITY	REFERENCE-DESCRIPTION	DESCRIPTION	MANUFACTURER'S PART NUMBER
Required Circuit Components:				
1	1	C1	Capacitor, X5R 2.2µF 16V 20% 0603	Taiyo Yuden EMK107BJ225MA
2	3	C2, C14, C55	Capacitor, X5R 0.1µF 10V 10% 0402	AVX 0402ZD104KAT2A
3	5	C3, C4, C6, C8, C9	Capacitor, X7R 0.01µF 16V 10% 0402	AVX 0402YC103KAT2A
4	2	C5, C7	Capacitor, NPO 4.7pF 25V 10% 0402	AVX 04023A4R7KAT2A
5	1	C10	Capacitor, X5R 4.7µF 6.3V 20% 0603	Taiyo Yuden JMK107BJ475MA-T
6	2	C11, C12	Capacitor, X7R 1µF 10V 20% 0603	AVX 0603ZC105MAT1A
7	1	C13	Capacitor, Tant. 100µF 10V 20% 6032	AVX TAJW107M010R
8	0	C15, C16, C17, C18, C19, C20, (Optional), C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37,C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54	Capacitor, 0402	
9	3	E1, E3, E4	Turret, Testpoint. 0.062 Thick Board 0.094"	Mill Max 2501-2-00-80-00-00-07-0
10	2	FB1, FB2	Ferrite Bead, ?A 1206	Murata BLM31PG330SN1L
11	8	JP1, JP2, JP3, JP4, JP5, JP6, JP8, JP9	Headers, Single Row 3 Pins 2mm Ctrs.	Samtec TMM-103-02-L-S
12	1	JP7	Conn, SQT Series, 2mm Ctr 50 Pin	SAMTEC SQT-125-01-F-D
13	2	J1, J2	SMA, Straight Jack	Amphenol Connex 132134
14	1	J3	BGA Conn., 10 × 40 Pin	Samtec Seam-40-02.0-S-10-2-A
15	1	L1 (Optional)	Inductor, 0603	
16	8	R1, R2, R3, R6, R7, R8, R10, R85	Resistor, Chip 1k 0.06W 5% 0402	Vishay CRCW04021K00JNED
17	5	R4, R11, R82, R83, R84	Resistor, Chip 10k 0.06W 5% 0402	Vishay CRCW040210K0JNED
18	2	R5, R13	Resistor, Chip 31.6k 0.06W 1% 0402	Vishay CRCW040231K6FKED
19	16	R9, R14, R15, R16, R18, R19, R20, R24, R25, R26, R27,R48, R55, R62, R69, R86	Resistor, Chip 100k 0.06W 5% 0402	Vishay CRCW0402100RJNED
20	2	R17, R23	Resistor, Chip 5.1k 0.06W 5% 0402	Vishay CRCW04025R10JNED
21	2	R21, R22	Resistor, Chip 49.9k 0.06W 1% 0402	Vishay CRCW040249R9FKED
22	1	R28	Resistor, Chip 3k 0.06W 5% 0603	Vishay CRCW06033K00JNEA
23	1	R29	Resistor, Chip 180k 0.06W 1% 0603	Vishay CRCW0603180KFKEA
24	32	R30, R32, R33, R35, R36, R38, R39, R41, R42, R44, R45, R47, R49, R51, R52, R54, R56,R58, R59, R61, R63, R65, R66, R68, R70, R72, R73, R75, R76, R78, R79, R81	Resistor/Jumper, Chip 0Ω 1/16W 1A 0603	Vishay CRCW06030000Z0EA
25	16	R31, R34, R37, R40, R43, R46, R50, R53, R57, R60, R64, R67, R71, R74, R77, R80	Resistor/Jumper, Chip 0Ω 1/8W 1A 0805	Vishay CRCW08050000ZOEA
26	8	R87, R88, R89, R90, R91, R92, R93, R94	Resistor, Chip 100k 0.05W 5% 0201	Vishay CRCW0201100RJNED
27	1	T1	Transformer MABA-007159-000000	M/A-COM MABA-007159-000000
28	1	U1	I.C., AD Converter Module BGA (140) 11.25mm × 9.00mm × 2.72mm	Linear Technology Corporation LTM9011-14
29	1	U2	I.C., Adustable LDO, DFN(08)(DD) 3mm × 3mm	Linear Techology Corporation LT3080EDD
30	1	U3	I.C., Serial EEPROM, TSSOP-8	Microchip 24LC32A-I/ST
31	8	XJP1, XJP2, XJP3, XJP4, XJP5, XJP6, XJP7, XJP8	Shunt, 2mm Ctrs.	Samtec 2SN-BK-G

SCHEMATIC DIAGRAMS



SCHEMATIC DIAGRAMS



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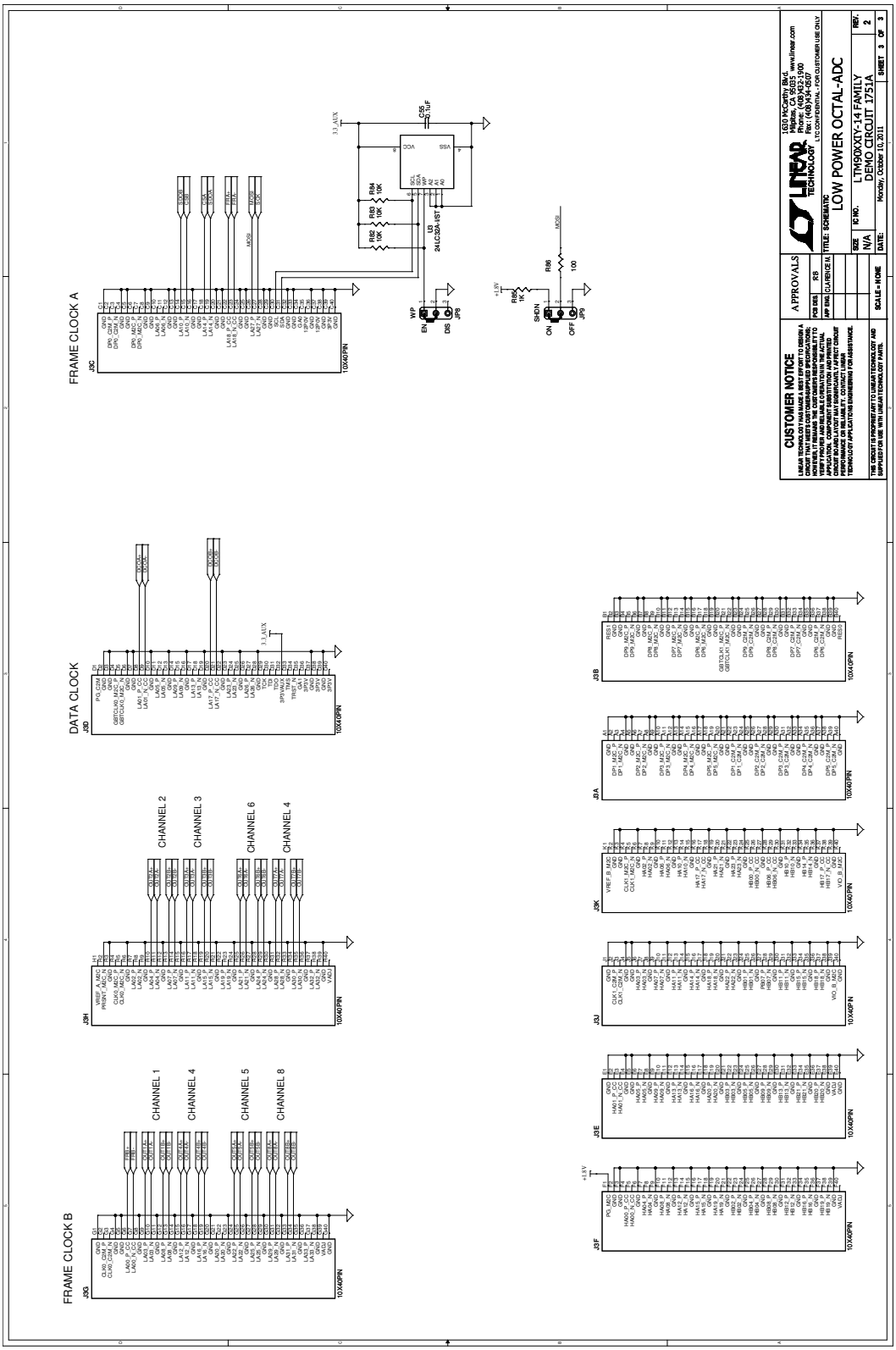

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